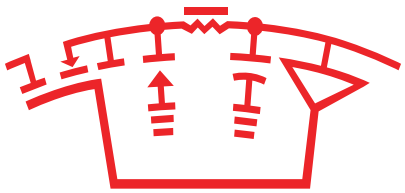

Power Supply Design Seminar

Low-Noise and Low-Ripple Techniques for a Supply Without an LDO

TEXAS INSTRUMENTS

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Many noise-sensitive systems use low-dropout regulators (LDOs) to provide low-noise and low-ripple power to sensitive analog circuits. But with growing current demands for these rails, designers are struggling to include LDOs because of their size, power loss, thermal rise and cost.

Introduction

This document reviews three specific challenges that designers encounter when designing a power supply for a high-speed analog-to-digital converter (ADC) and approaches to solve them.

DC/DC Converters are Noisy

DC/DC switching converters are well known for high efficiency and a relatively small solution size. They are also well known for their larger output voltage ripple and high-frequency noise, which is caused by DC/DC converter switching cycles.

Figure 1 shows an example of the output voltage for a standard DC/DC buck converter. The output voltage ripple shows high-frequency switching noise, output capacitor voltage ripple and general low-frequency noise. Applying this waveform to a noise-sensitive system will reduce signal quality.

Looking at high-speed ADCs, the spurious-free dynamic range (SFDR) and signal-to-noise ratio (SNR) are reduced when using a typical DC/DC buck converter, as shown in **Figure 3**. Frequency synthesizers and phase-locked loops (PLLs) show degradation in phase noise, having larger jitter when powered by a supply rail, as seen in **Figure 3**.

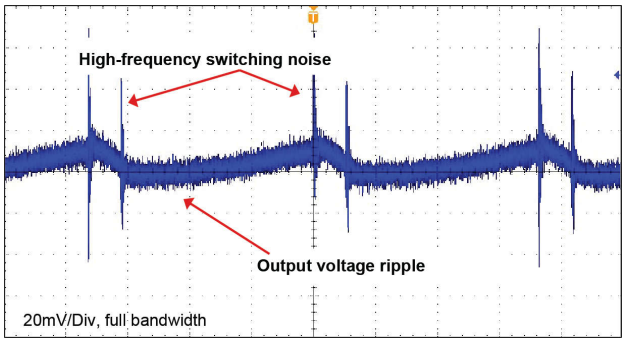


Figure 1. *Typical output voltage ripple of a DC/DC buck converter.*

There are several ways to minimize power-supply output ripple and low- and high-frequency noise. **Figure 2** shows the traditional approach, using an LDO as a post-filter and a ferrite bead as a high-frequency filter.

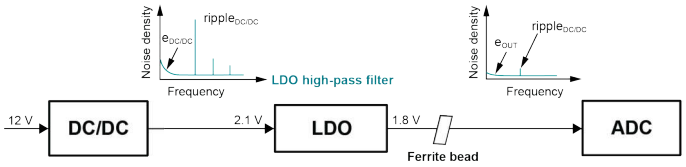


Figure 2. *Traditional LDO post-filtering is large in size, with high power loss at load currents >2A.*

The LDO is simple to use and a popular approach for moderate load currents. For load currents beyond 2A, however, the power loss in the LDO increases to 600mW or more. Compensating for this power loss requires the selection of larger LDO packages, making the solution more expensive and generating excessive system heat – a problem for 5G telecom systems that require several analog front ends (AFEs).

In test and measurement applications, high-speed ADCs require power-supply load currents ≥2A. In order to reduce the power dissipation and solution size for these types of applications, it is advantageous to power the rails directly from the DC/DC converter without LDO post-filtering, but then the DC/DC converter needs to achieve a similar output voltage quality in terms of noise and ripple compared to the LDO.

The LDO filters the output voltage ripple of the DC/DC converter at the converter switching frequency (f_{SW}), which is typically in a range from 100kHz to 2MHz. The power-supply rejection ratio (PSRR) expresses the effectiveness of the LDO to filter noise – it is the attenuation of the input voltage ripple and noise. Most LDOs are optimized for low noise at a frequency range below 100kHz and will not filter high-frequency

components, therefore necessitating a ferrite bead and bypass capacitor after the LDO for additional high-frequency filtering. With these considerations, it becomes possible to derive a target specification for a DC/DC converter to power noise-sensitive systems. For example, a system with a high-speed ADC may require noise levels below 20μV_{RMS}, a maximum output voltage ripple of 200μVpp and a PSRR >30 dB at frequencies of 1 MHz and beyond.

Power-Supply Output Voltage Ripple and Noise Degrade ADC Performance

It is difficult to estimate the acceptable output voltage ripple and noise for a power-supply rail without a deeper understanding of the ADC and its performance. **Figure 3** shows the output frequency spectrum of an ADC.

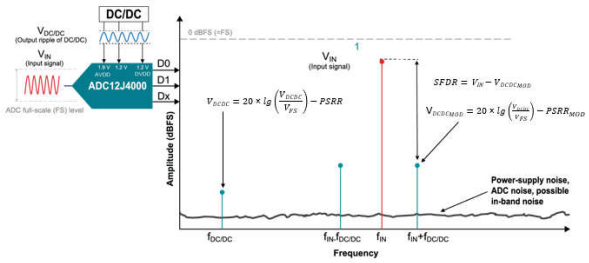


Figure 3. *Power-supply spur modulation, with an ADC input signal decreasing the SFDR.*

In the best case, the output voltage spectrum should show a single line at the input frequency of the ADC. When a power supply connects to an ADC, the frequency of the output voltage ripple modulates with the ADC frequency, generating sidebands above and below the ADC input signal frequency. The larger these sidebands are in amplitude, the lower the SFDR. **Equation 1** calculates the amplitude of the modulated spur:

$$V_{DCDC\_MOD} = 20 \times lg\left(\frac{V_{DCDC}}{V_{FS}}\right) - PSRR_{MOD}[dBFS] \quad (1)$$

where V_{FS} is the full-scale level of the ADC, V_{DCDC} is the peak-to-peak output voltage ripple of the DC/DC converter and $PSRR_{MOD}$ is the power-supply rejection of the ADC.

The spur needs to be lower than the SFDR of the ADC. $PSRR_{MOD}$ is the attenuation of the power-supply ripple to the amplitude of the modulated spur in the ADC output spectrum. $PSRR_{MOD}$ is not usually specified in ADC data sheets, but is possible to characterize. If characterization is not possible, then you can conservatively estimate $PSRR_{MOD}$ by taking 20 dB for the $PSRR_{MOD}$ of the ADC, plus 10 dB for additional printed circuit board (PCB) power-supply bypass capacitor attenuation, for a total system board attenuation of 30 dB. **Equation 2** calculates the acceptable DC/DC converter output voltage ripple:

$$V_{DCDC} = 10^{\frac{V_{DCDC_{MOD}} + PSRR_{MOD}}{20}} \times V_{FS} \quad (2)$$
$$= 10^{\frac{-100\ dB + 30\ dB}{20}} \times 725\ mV_{pp} = 229\ \mu V_{pp}$$

With **Equation 2** setting an SFDR of –100 dB as a target, V_{DCDC_MOD} needs to be –100 dB as well. The typical high-speed ADC full-scale level specified in the ADC data sheet is 725 mV. Having a target output voltage ripple of <200 μVpp for the DC/DC converter proves to be a good value and does not degrade the ADC's SFDR.

Minimizing Low-Frequency Noise Requires Dedicated Low-Noise IC Technologies

Low-frequency noise is not a significant concern for high-speed ADCs, but the noise becomes dominant when powering frequency synthesizers and PLLs where phase noise increases clock jitter. Duty-cycle jitter is very critical, especially at higher clock frequencies, and must be minimized.

To estimate the required low-frequency noise for a DC/DC converter, **Figure 4** shows the low-frequency noise of a typical low-noise LDO vs. a DC/DC converter.

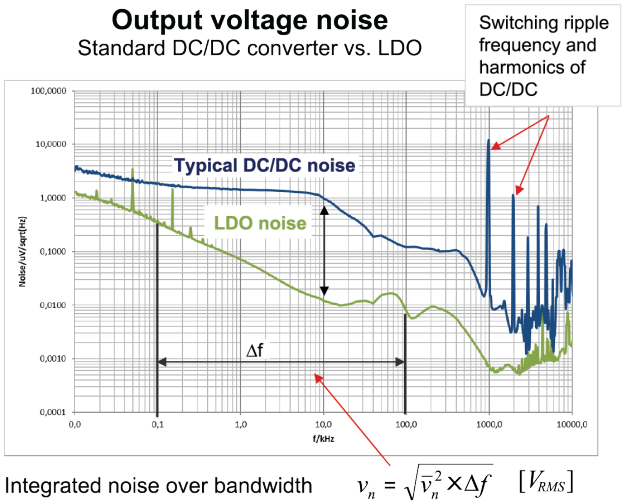


Figure 4. *A DC/DC converter generates three to 10 times more low-frequency noise than a low-noise LDO.*

Low noise is typically a concern in the range of 100 Hz to 100 kHz; interference with the PLL loop is the most sensitive over this frequency range. **Equation 3** expresses the integration of low-frequency noise over a bandwidth from 100 Hz to 100 kHz:

$$v_n = \sqrt{\bar{v}_n^2 \times \Delta f} \quad (3)$$

It is also important to look at the spectral noise density, as shown in **Figure 4** and expressed as microvolts per square-root hertz, because the root-mean-square noise level of an LDO can be very low, while the spectral noise density can still be high at a single frequency, causing distortions. Reducing the low-frequency noise of a DC/DC converter requires an internal integrated circuit (IC) design. Filtering the output voltage at such low frequencies requires large external passive filter components with an inductance of approximately 5 mH and a capacitance of approximately 10,000 µF for a filter cutoff frequency <20 Hz. Using IC techniques and filtering the internal DC/DC converter reference can achieve DC/DC converter frequency noise as low as 20 μV_{RMS}.

Using low-noise circuit techniques for the internal IC error amplifier, current-sense circuit and oscillator make further improvements possible. A low-noise target of 20 μV_{RMS} showed no degradation in phase noise by characterizing TI's **LMX2592** and **LMX2594** frequency synthesizers and **LMK04616** jitter cleaner, which are popular in high-speed systems. Low-noise and low ripple design is described in the last section of this document, but first, how to better understand the complexity of achieving a low-output voltage ripple in a DC/DC converter will be discussed in the next section.

Traditional Approaches to Reducing Ripple

Traditional approaches to reducing output ripple include adjusting the standard inductor-capacitor (LC) output filter and adding more filtering after it. To compare approaches, take measurements using TI's **TPS543620** buck converter evaluation module (EVM). **Figure 5** shows the simplified schematic for the EVM.

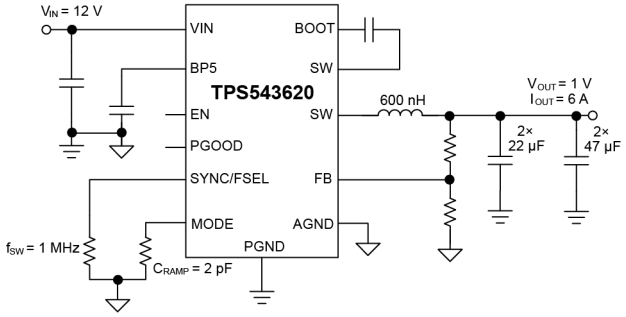


Figure 5. *TPS543620 EVM simplified schematic.*

The low output voltage ripple target of 200µVpp that we described earlier necessitates a low-noise test setup to accurately measure the ripple. A 1-to-1 probe using a coaxial cable provides the best resolution in the measurement. Avoid using a 10-to-1 probe with high-impedance termination at the oscilloscope for low-ripple measurements, as the probe can limit the minimum voltage scale of the oscilloscope and add noise to the measurement, pushing the noise floor near the amplitude of the ripple you are trying to measure. Use SMA or SMB connectors to connect the coax cable to the measurement point.

Taking the measurement with full bandwidth requires proper termination to prevent noise pickup and block reflections on the coax cable.

There are two ways to terminate the measurement:

- Use a DC blocker to enable oscilloscope use with a 50-Ω termination and DC coupling. For many scopes, AC coupling is not possible with a 50-Ω termination.
- Add a series 50-Ω resistor between the coax cable and the point at which you are measuring the output voltage. This configuration makes it possible to configure the scope for high-impedance termination and AC coupling.

The steady-state ripple is taken at full 6-A load, with a high bandwidth limit (BWL) of 250MHz to include the high-frequency switching noise in the measurement. A typical target for an application not requiring low output ripple is 1% peak-to-peak, or 10mV for a 1-V output. Measuring the fast Fourier transform (FFT) of the output voltage at a full 6-A load but with a 1-GHz BWL offers even better insight into the frequency components of the output ripple. In the time domain, the ripple is the addition of all of the different frequency components, making it very difficult to determine the contribution from any particular frequency.

Taking the transient response measurement with a 20-MHz BWL removes high-frequency switching noise and serves two purposes. First, you can use the transient response to judge the control stability, as some filtering techniques can reduce the gain and phase margin. Second, you can monitor the transient response to see if it is worse after adding filtering. Some applications, such as digital power rails for high-speed AFEs in wireless infrastructure applications, require power supplies with low ripple and a fast transient response. A typical target is ±3%, or 60-mV peak-to-peak for a 1-V output with a 25% to 75% step, or 1.5A to 4.5A for a 6-A maximum load.

Figure 6, Figure 7 and Figure 8 show the results of these three measurements on the unmodified TPS543620 EVM. As Figure 6 illustrates, the 250-MHz BWL exceeds the 10-mV target because of the high-frequency switching noise above 100MHz, as shown in the FFT of Figure 8. Output ripple measurements and requirements necessitate only a 20-MHz BWL, which would result in a measured ripple below the 10-mV requirement.

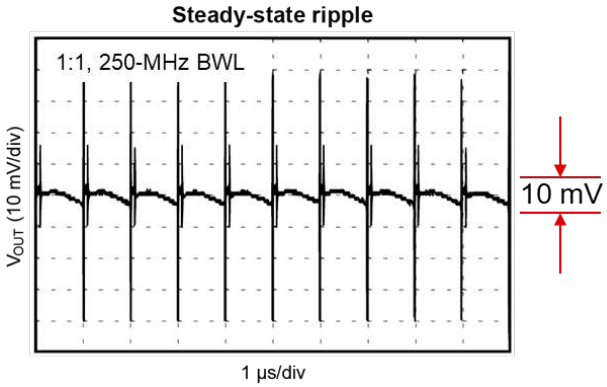


Figure 6. *Unmodified TPS543620 EVM output ripple.*

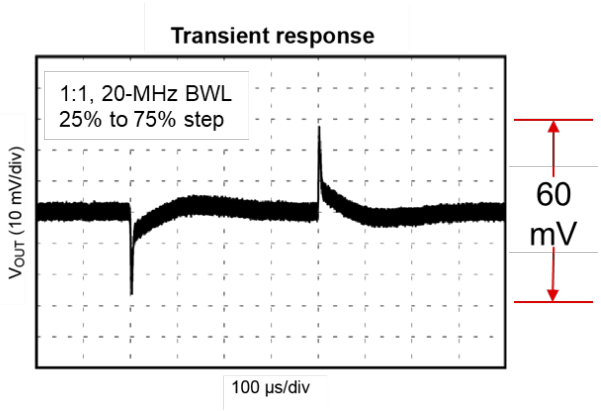


Figure 7. *Unmodified TPS543620 EVM transient response.*

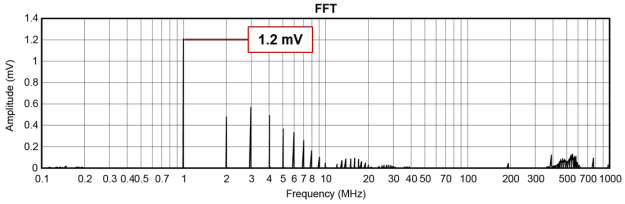


Figure 8. *Unmodified TPS543620 EVM output FFT.*

Using Smaller Capacitors in Parallel

Instead of using a single larger ceramic capacitor, another method uses multiple ceramic capacitors in parallel that are physically smaller and have a lower capacitance on the output and lower parasitic inductance. This lower capacitance and parasitic inductance increase the self-resonant frequency of

the capacitor. Above the self-resonant frequency, the capacitor's parasitic inductance limits its impedance.

A lower parasitic inductance and a higher self-resonant frequency decrease the total impedance of the output capacitors.

To illustrate this concept, **Figure 9** shows the impedance of two 0805 22-µF capacitors in parallel vs. a single 1210 47-µF capacitor. Below 100kHz, the capacitance sets the impedance, so there is no significant difference between the two impedances. The single 47-µF capacitor has a lower self-resonant frequency of approximately 800kHz, while the 22-µF capacitors have a self-resonant frequency greater than 1 MHz. As a result, the 22-µF capacitors have a minimum impedance of less than 2mΩ, while the 47-µF capacitor has a minimum impedance greater than 2mΩ. The minimum impedance occurs at the self-resonant frequency, so selecting a capacitor with a self-resonant frequency near the switching frequency will provide the most filtering at the switching frequency. Above the self-resonant frequencies, the impedance of the 22-µF capacitors is approximately one-third the impedance of the 47-µF capacitor.

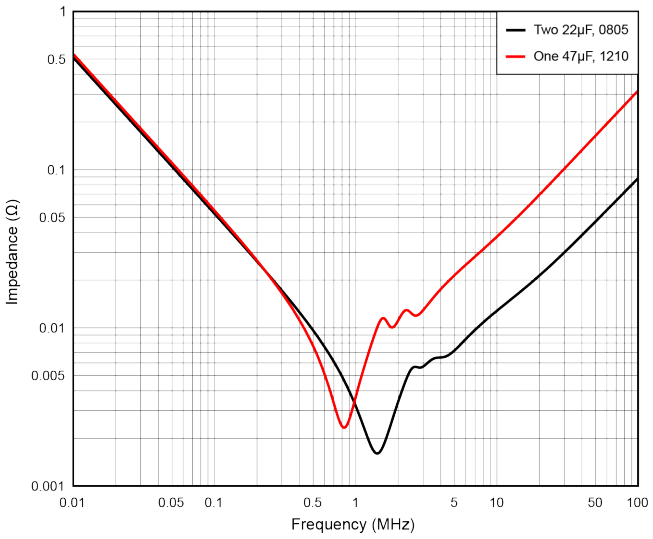


Figure 9. *Impedance of two 0805 22-µF ceramic capacitors vs. one 1210 47-µF ceramic capacitor.*

Figure 10 shows what happens when you replace the one 47-µF capacitor in the schematic shown in **Figure 5** with two 22-µF capacitors. In the output ripple graph shown in **Figure 10**, the black curve on the left is the original output ripple and the red curve on the right is ripple with the modified output capacitors. This waveform shows reduced high-frequency content in the output ripple.

In the transient response graph shown in **Figure 11**, the performance is about the same, but lower high-frequency ripple is visible. And in **Figure 12**, the effect of the reduced impedance across the entire frequency range is more clear. The red curve in **Figure 12** shows a reduction of the fundamental peak at the 1-MHz f_{SW} and its harmonics to about two-thirds their original values.

Figure 9 shows that the impedance of a single 47-µF capacitor is the same as two 22-µF capacitors at the 1-MHz switching frequency. This apparent conflict likely occurs because the impedance curves in **Figure 9** do not include the effects of PCB parasitics on the filter's impedance.

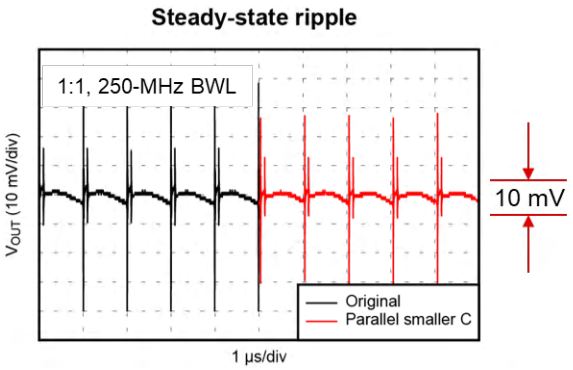


Figure 10. *Smaller capacitor output ripple.*

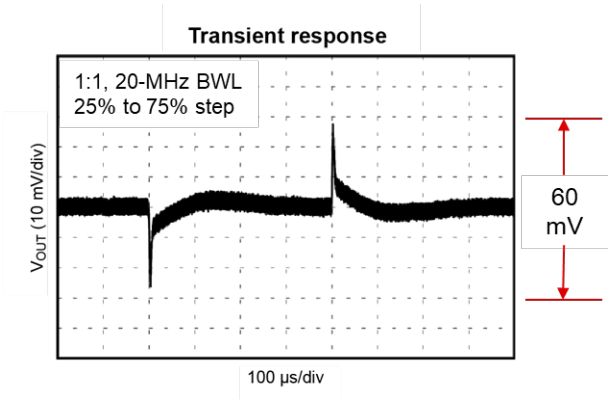


Figure 11. *Smaller capacitor transient response.*

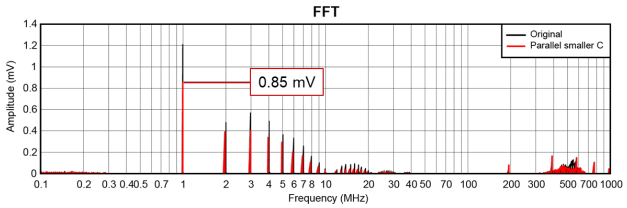


Figure 12. *Smaller capacitor output FFT.*

Although paralleling smaller capacitors can provide higher-frequency broadband filtering, consider the effect of increased impedance caused by inter-capacitance resonance peaks when adding a new capacitor size and value to the output capacitor network. Spacing capacitors in a 10-to-1 ratio can increase the likelihood of this effect.

Figure 13 compares the impedance of capacitor networks with different parallel combinations of 47-µF, 4.7-µF, 0.47-µF, 0.047-µF, 4,700-pF and 470-pF capacitors. The red arrows in the figure point to the increased impedance at the intercapacitance resonant peaks. The effect is more pronounced as the self-resonant frequency of the capacitor increases, such as with the 4,700-pF and 470-pF capacitors. If the output contains ripple or noise at the frequency of the peaks, that ripple or noise would increase as a result of adding the capacitor.

Spacing capacitor values in a 2-to-1 to 3-to-1 ratio can help reduce the peaks caused by intercapacitance resonance. Additionally, when paralleling multiple capacitors, it is important to be aware of the frequency of the noise that needs filtering. We recommend adding a capacitor with a self-resonant frequency as close as possible to the frequency of the noise, and testing multiple adjacent values to find the best value. Measuring an FFT of the output ripple can be useful when selecting the most effective capacitor.

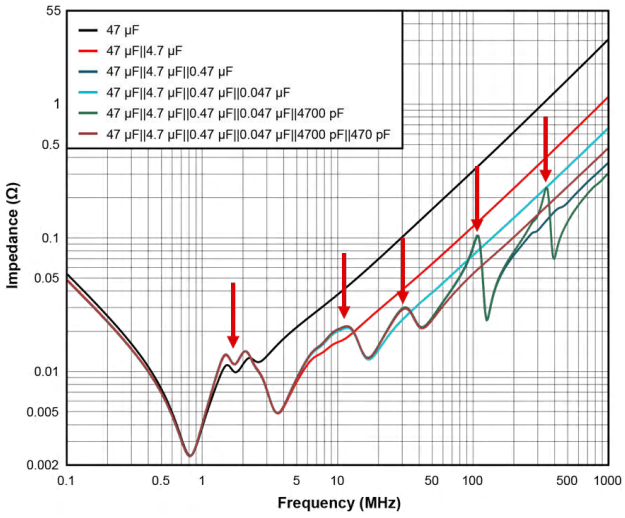


Figure 13. *Intercapacitance resonance peaks when paralleling capacitors in 10-to-1 ratio.*

Paralleling smaller capacitors offers a relatively small reduction in output ripple, and this approach alone is likely not sufficient to meet ripple requirements of 1mV or lower. It is a simple schematic change, however, and uses standard ceramic capacitors. Additionally, given the higher f_{SW} trend, it's a good idea to consider smaller capacitors with a higher self-resonant frequency for all designs. A trade-off when adding smaller capacitors to a design is that it can result in increased costs, because of the increased number of new components in the bill of materials.

Larger Inductance

Another filtering technique to reduce the output ripple is to increase the inductance. Increasing the inductance reduces the amount of ripple current that the output capacitors need to filter. Additionally, the inductor and the parasitic inductance in the output capacitor network form a voltage divider from the switch node to the output. Increasing the inductance increases the inductive

voltage divider ratio, resulting in less output ripple divided down from the switch node.

This approach was tested with the TPS543620 by increasing the inductance of the schematic in **Figure 5** from 600nH to 2.2µH, which reduces the transient currents (di/dt) in the inductor by a factor of 3.7.

As a result of this increase in inductance, we increased the compensation setting for the TPS543620 (CRAMP) to the 4-pF ramp in order to increase the loop gain by 6 dB. **Figure 14**, **Figure 15** and **Figure 16** show the measurements as a result of this change.

Figure 14 shows the reduced ripple at the f_{SW}, but the high-frequency content is about the same as before. In **Figure 15**, however, the reduced di/dt has degraded the transient performance. The peak-to-peak transient response is nearly two times larger with the same step, necessitating an increase in the voltage scale in the waveform to 20mV per division in order to fit the full peak-to-peak voltage on the graph. **Figure 16** shows a reduction of the fundamental peak at the 1-MHz f_{SW} and its harmonics to one-sixth the original.

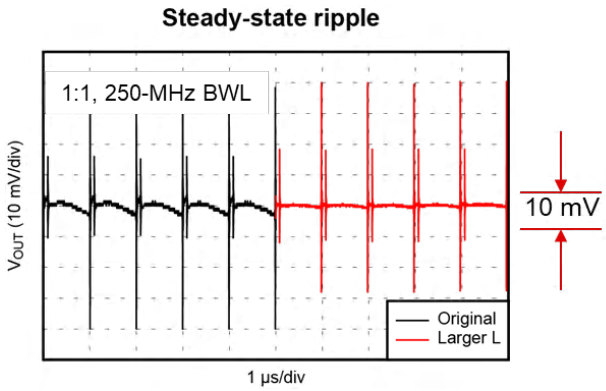


Figure 14. *Larger inductor output ripple.*

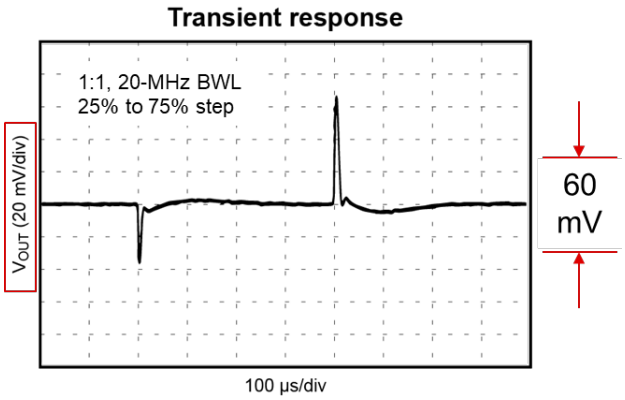


Figure 15. *Larger inductor transient response.*

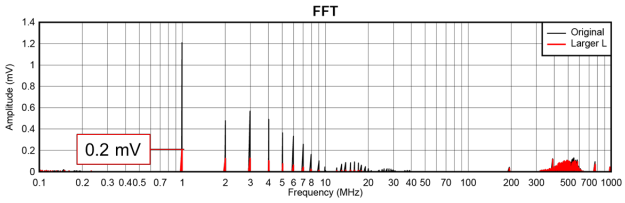


Figure 16. *Larger inductor output FFT.*

Increasing the inductance is a simple and effective change for reducing the output voltage ripple, but that approach comes with some trade-offs that could be significant. A higher inductance typically means a larger inductor with higher direct current resistance (DCR), which results in a larger PCB footprint, increased cost and more conduction losses. The lower di/dt slows down the transient response. And finally, increasing the inductance provides little to no added filtering at frequencies greater than 100 MHz because of the parasitic capacitance of the inductor.

Adding a Feedthrough Capacitor

The next set of modifications inserts another stage of output filtering. Our first example creates a second-stage filter with a feedthrough capacitor. **Figure 17** shows the modified schematic, with a red box indicating the location of the feedthrough capacitor. This modification includes moving one of the 22-µF ceramic capacitors (originally placed near the inductor) after the feedthrough capacitor to maximize capacitance at the load. Connecting the feedback for the TPS543620

control loop after the feedthrough capacitor offers the best output regulation.

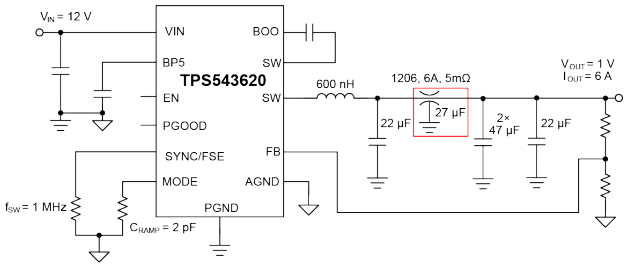


Figure 17. *The TPS543620 EVM with a feedthrough capacitor.*

A feedthrough capacitor is a three-terminal ceramic capacitor designed to give low equivalent series inductance (ESL). Reducing the ESL results in low impedance across a wider range of frequencies than a conventional ceramic capacitor.

Figure 18 shows what feedthrough capacitors look like. There is an input terminal, an output terminal and a ground terminal in the middle. This terminal configuration results in low ESL.

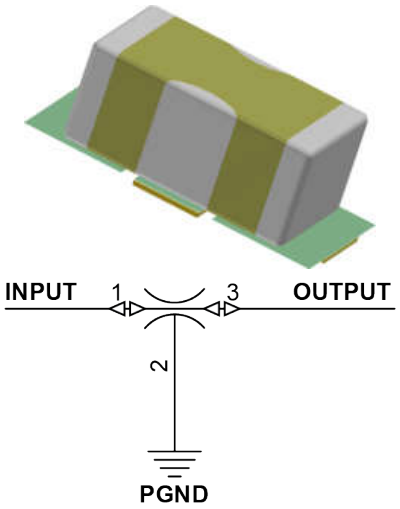


Figure 18. *Feedthrough capacitor.*

Figure 19 shows the impedance of a 27-µF feedthrough capacitor compared to a conventional 22-µF capacitor. This comparison offers three important observations:

- The feedthrough capacitor has a higher self-resonant frequency as a result of the reduced ESL.
- The minimum impedance is lower than the standard capacitor.
- The impedance stays low across a frequency range from approximately 3MHz to almost 20MHz.

These three effects combined result in less than one-tenth the impedance of the conventional ceramic capacitor above 2MHz.

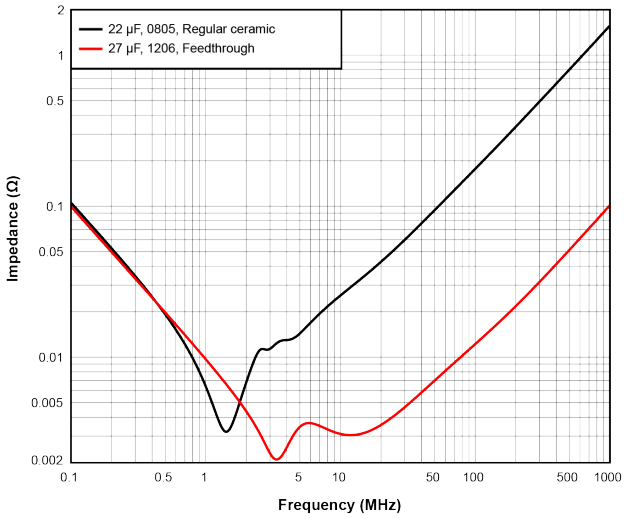


Figure 19. *Impedance of a feedthrough capacitor vs. a standard ceramic capacitor.*

Figure 20, **Figure 21** and **Figure 22** show the results of adding the feedthrough capacitor. The improved filtering across the entire frequency range is clearly visible in the output ripple. The total ripple, including the high-frequency switching noise, is less than 10mVp-p. Adding the feedthrough capacitor slightly improves the transient response because there is more capacitance on the output.

Figure 22 clearly shows significant reductions in the peaks at each frequency. The reduction of ripple at the 1-MHz fundamental, however, is only approximately one-half, because as **Figure 19** shows, the feedthrough capacitors have about the same impedance as the conventional capacitor at 1MHz. Even though the impedance to ground is about the same, the feedthrough capacitor does still provide some additional attenuation at 1MHz because it is inserted in series with the output.

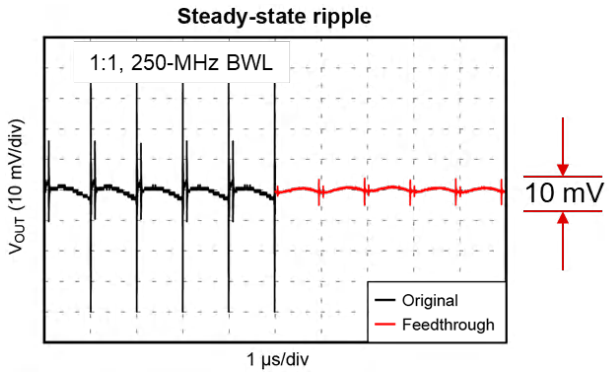


Figure 20. *Feedthrough capacitor output ripple.*

Figure 21. *Feedthrough capacitor transient response.*

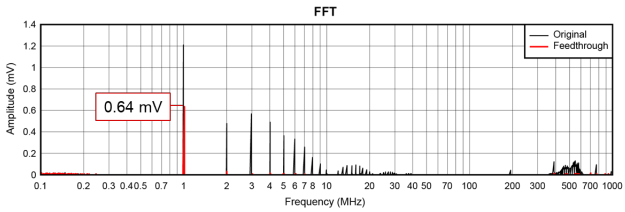


Figure 22. *Feedthrough capacitor output FFT.*

Feedthrough capacitors are an effective and simple way to achieve very low ripple, but they have potentially significant trade-offs:

- A feedthrough capacitor is not a standard component, so there are a limited number of vendors and options for different values.
- The device used in our measurements was rated for only an 85°C junction temperature. Higher-ambient-temperature applications require a capacitor with a higher junction temperature rating, but at the time of this writing, the only feedthrough capacitors available with higher ratings have lower capacitance.
- Adding a feedthrough capacitor will add losses caused by conduction losses in its DCR.
- The ripple at the fundamental frequency only dropped approximately in half, so more filtering at the f_{SW} may be required to achieve ripple below 1mV. More filtering at the f_{SW} typically requires a feedthrough capacitor with more capacitance and a self-resonant frequency near the f_{SW}, but again, there are not any such capacitors available at this time.

Adding a Ferrite Bead

A more popular filtering technique is to use a ferrite bead to add a second-stage LC filter, as shown in **Figure 23**. A ferrite bead works well in a second-stage filter for several reasons. Ferrite beads are available with high enough inductance at frequencies less than 10MHz, so they can filter the output voltage ripple at the f_{SW} and its harmonics. A ferrite bead's increasing impedance from 100MHz to 1GHz enables the filtering of high-frequency switching noise from the rising and falling edges at the switching node.

Ferrite beads are available in small-sized standard packages, such as a 0603 package, and high-current ferrite beads have low DCR to minimize power loss. They are also relatively low cost, which is why designers use them often in systems to provide filtering.

When selecting a ferrite bead for power filtering, pay attention to the inductance saturation, which can reduce the inductance and filtering provided. To minimize the effect of saturation, choose a ferrite bead rated for two times the load current. If the power rail goes to multiple loads, you can use multiple ferrite beads, placing one before each load.

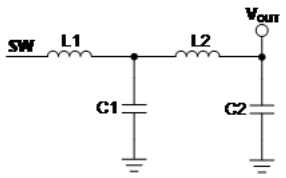


Figure 23. *Two-stage LC filter.*

When adding a second-stage LC filter to the output, one important goal is to keep the second stage's resonance frequency (f_{LC2}) well above the loop bandwidth of the regulator in order to minimize the impact of f_{LC2} on loop stability. A general recommendation is to keep f_{LC2} at least three times above the loop bandwidth. This consideration becomes especially important when using a regulator such as the TPS543620, which is designed for fast transient response – and as a result can have a relatively high loop bandwidth between one-tenth and one-fifth the switching frequency. With a 1-MHz switching frequency, the loop bandwidth is often greater than 100kHz.

There are two ways to design a second-stage filter to have a high resonance frequency:

- Select a ferrite bead with low inductance. Luckily, most high-current ferrite beads with low DCR also have low inductance.
- Keep the capacitance before the ferrite bead small. Minimizing this capacitance increases the second-stage resonance frequency because the f_{LC2} is set by the series combination of C1 and C2, as shown in :

$$C/S = \frac{C1 \times C2}{C1 + C2} \quad (4)$$

When placing capacitors in series, if one capacitor is much smaller than the other, the combined series capacitance is closer to the smaller capacitance. Making C1 much smaller than C2 reduces the combined series capacitance and increases the second-stage resonance frequency. **Equation 5** calculates the f_{LC2}:

$$F_{LC2} = \frac{1}{2\pi \times \sqrt{L2 \times C/S}} \quad (5)$$

Adding a second-stage LC filter often requires damping in order to reduce the quality factor (Q). With too much Q, there will be peaking in the loop gain at f_{LC2}, which can cause the loop gain to go above 0 dB and result in oscillations on the output voltage at f_{LC2}. You can add a damping resistor to the circuit in two places:

- In parallel with the second-stage inductance.
- In series, with a capacitor added before the second-stage inductance.

The parallel damping method is simpler to implement but reduces the filtering provided, which is a significant trade-off. At higher frequencies, the parallel resistor will have a lower impedance than L2, causing high-frequency noise to pass through the resistor and bypass the inductor entirely. So in this example, we used series RC damping. **Figure 24** shows the simplified circuit for this method.

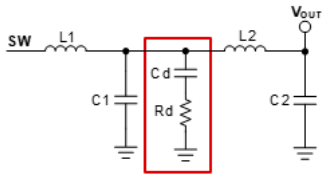


Figure 24. *RC damping of the second-stage filter.*

Let's go through the design methodology for selecting the resistor and capacitor values in the damping circuit. First, select capacitor value Cd to be ≥ C1. Next, select resistor value Rd so that the RC frequency is one-half f_{LC2}, calculated with **Equation 6**:

$$R_d = \frac{1}{\pi \times f_{LC2} \times C1} \quad (6)$$

Equation 6 only considers C1 because, as long as the first condition is met to select Cd ≥ C1, Rd will determine the impedance of the series combination of R_d and C_d at f_{LC2}.

Figure 25 shows the schematic tested with the TPS543620 and a ferrite bead second-stage filter. The resonance frequency of the second-stage filter is approximately 300kHz. In addition to adding the second-stage filter, we changed the ramp to the 1-pF setting to reduce the loop gain by 6dB.

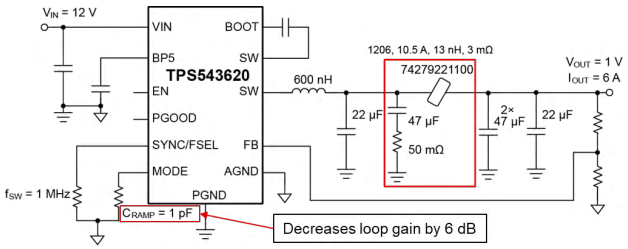


Figure 25. *The TPS543620 EVM with a ferrite bead second-stage filter.*

Figure 26, **Figure 27** and **Figure 28** show the measurements as a result of adding the ferrite bead. In **Figure 26**, the ferrite bead clearly reduces the output ripple – both the ripple at the f_{SW} and the high-frequency switching noise – to less than 10mVp-p. The ripple at the f_{SW} is barely visible with the 10-mV-per-division voltage scale used in **Figure 27**. The FFT in **Figure 28** clearly shows significant reductions in the peaks at each frequency, including reducing the peak at the 1-MHz f_{SW} to almost one-tenth the original.

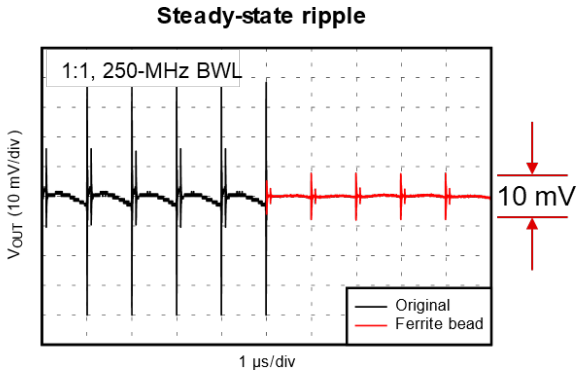


Figure 26. *Ferrite bead output ripple.*

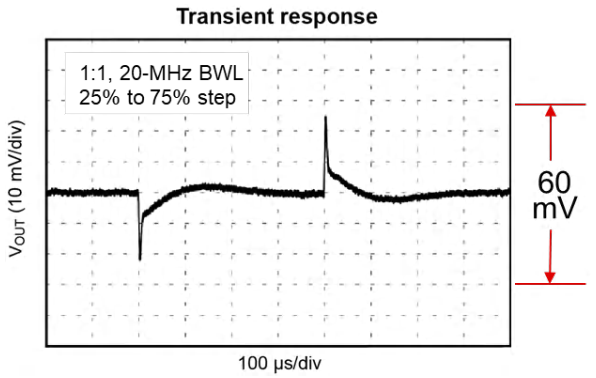


Figure 27. *Ferrite bead transient response.*

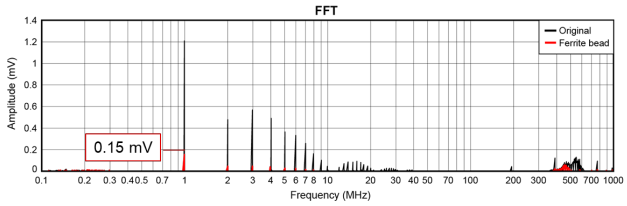


Figure 28. *Ferrite bead output FFT.*

The transient response is about the same, however, so the loop stability requires a closer look. **Figure 29** shows the Bode plot with the ferrite bead added. There is a steep rolloff in the gain and phase from the second-stage filter at approximately 300kHz. The loop bandwidth is also very high at approximately 140kHz, which does not meet the requirement to have the second-stage filter resonance be three times the loop bandwidth. As a result, the gain margin is lower than the 10-dB typical design requirement, and the phase margin is lower as well. A low gain margin introduces a risk that circuit variations could result in oscillations on the output.

To improve the gain margin, you must either increase the second-stage resonance frequency or decrease the loop bandwidth. Increasing the second-stage resonance frequency will reduce the filtering, and in this case the ripple is already higher than the 200-µVp-p target. To avoid increasing the ripple, it's better to decrease the loop bandwidth, but doing so will come with the trade-off of requiring more output capacitance to provide the same transient response performance. And with an internally compensated regulator such as the TPS543620, there is less flexibility in tuning the loop bandwidth, and the lowest loop gain setting is already set. Thus, in this case, reducing the loop bandwidth requires a modification of the output filter.

The second curve in **Figure 29** shows the effect on loop stability with the first-stage inductance increased to 1.5µH. The loop bandwidth decreases to 60kHz and the gain margin improves to 13dB.

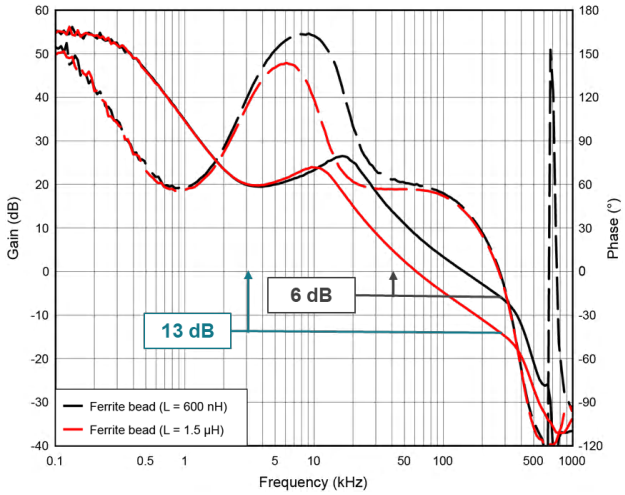


Figure 29. *Bode plot with a ferrite bead filter.*

A sub-1-mV ripple at the f_{SW} and its harmonics is possible when using a ferrite bead to filter the output because a ferrite bead effectively filters the ripple at the f_{sw} and higher. The trade-off is that using a ferrite bead can result in more components (such as damping components) and design time to compensate the loop. Adding in a ferrite bead can also limit the maximum loop bandwidth (which degrades transient response performance) and results in some conduction losses in its DCR.

Layout Techniques

Layout may be the most important part of the design when using a switching DC/DC regulator for many reasons, including the impact to output voltage ripple. A poorly constructed PCB layout can result in increased output ripple. The most important goal when creating a PCB layout for low ripple is to minimize the parasitic inductance. Adding inductance in series with the output capacitors will increase the ESL portion of the output ripple from the voltage divider from the switch node to the output. When designing for low output ripple, the ESL portion can often dominate the output ripple.

Figure 30 shows a simplified layout of the TPS543620. The TPS543620 has a “butterfly”-style pinout, with the input bypass capacitors placed on both sides of the device. The red arrows indicate the switching loops that require minimized parasitic inductance.

The green arrows indicate the output loops that require low ripple and noise.

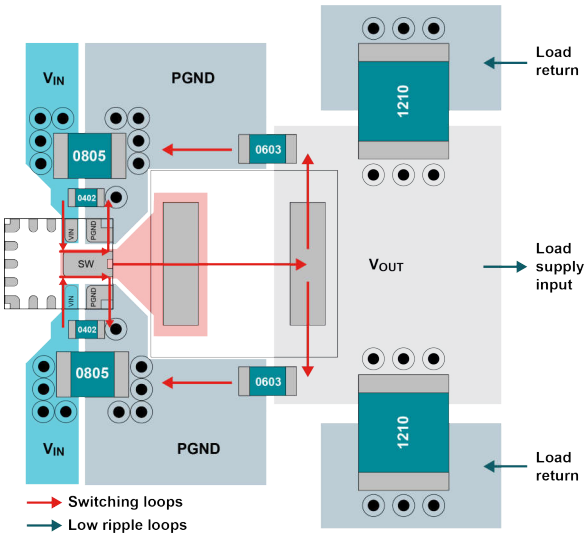


Figure 30. *TPS543620 simplified layout.*

To minimize the layout inductance (and as a result, the output ripple), use wide traces or planes for the input voltage (V_{IN}), the power ground and the output voltage (V_{OUT}). Avoid vias when routing these power signals, if possible. If other design constraints require vias, use multiple vias to minimize the parasitic inductance. To minimize the high-frequency noise caused by the rising and falling edges of the switching node, you’ll also need to minimize the input switching loop inductance, which will in turn minimize voltage stress on the power metal-oxide semiconductor field-effect transistors and reduce radiated noise. Avoid routing power rails that require low noise near high transient voltage (dv/dt) nets such as the switching node or the input switching loop of the regulator because noise can couple from the noisy nodes to low-noise power rails. For example, in **Figure 30**, the 1210 capacitors bypass the loop from the output of the regulator to the load return and connect to ground through an internal plane, away from the input switching loop.

Figure 31 shows layout techniques to minimize parasitic inductance in the output capacitor layout between the regulator and the load. First, if possible, route V_{OUT} between the output capacitor banks and ground.

Placing vias between the output capacitors' terminals can reduce the loop area bypassed by the output capacitors, thus reducing the inductance. **Figure 31** also shows also two sets of ground vias near each capacitor, with one set placed between the capacitor's terminals.

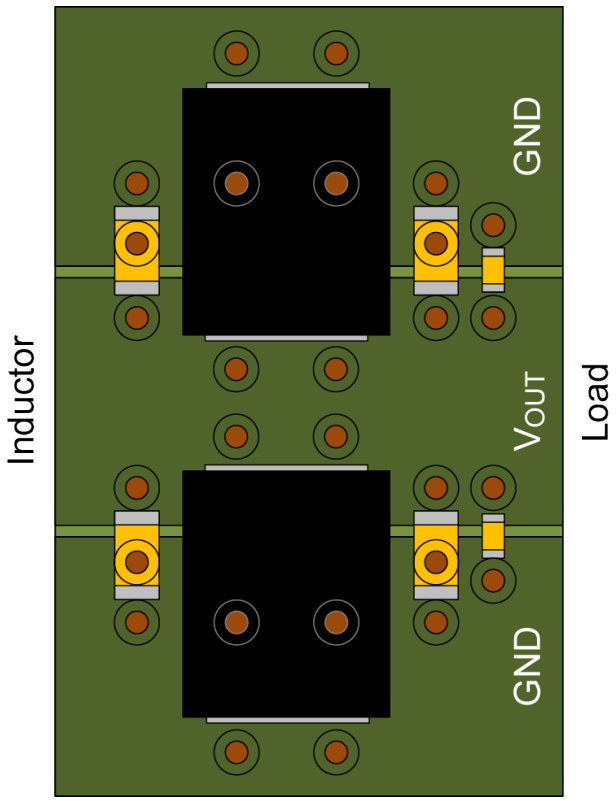


Figure 31. *Output capacitor placement and vias.*

When using multiple vias, space the vias to allow planes to fill between them, as shown in **Figure 32**. Placing vias close together creates a break in the other power planes they pass through on other layers. Spacing the vias further apart minimizes the inductance added by the other power planes.

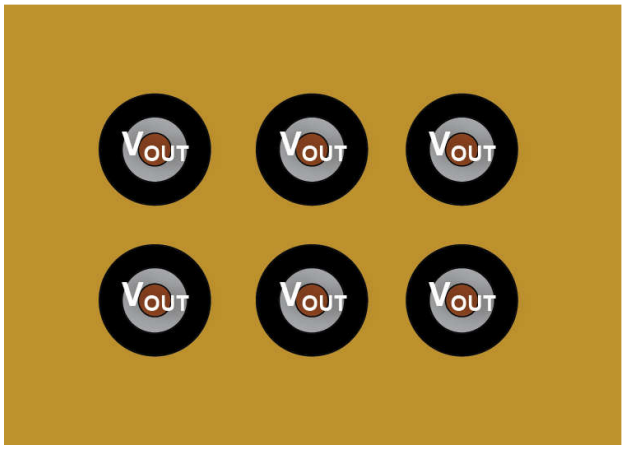


Figure 32. *Vias spaced to allow planes to fill between them.*

Silicon Solutions

The **TPS62913** and **TPS62916** are low-ripple and low-noise buck converters that use the techniques we've previously described as well as low-noise techniques borrowed from low-noise LDOs. These devices support-input voltages from 3V to 17V and output voltages from 0.8V to 5.5V. This product family contains five device variants that can support output currents from 2A to 8A."

The TPS62913 and TPS62916 also have module versions: the **TPSM82913** and **TPSM82916**, which feature integrated inductors for smaller solution sizes while offering the same low-noise performance.

While the efficiency of the TPS62913 and **TPS62916** by itself is quite high, it is possible to further improve system-level efficiency if you consider removing the LDO for many applications. Until now, how to reduce ripple through external design techniques has been discussed. Now, the integration of features into a buck converter like the TPS62913 to reduce noise and ripple will be discussed. **Figure 33** and **Figure 34** show a typical schematic for generating a low-noise 3.3-V supply using the TPS62913 and TPS62916, respectively.

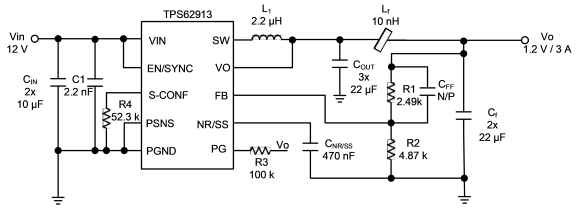


Figure 33. *TPS62913 typical schematic.*

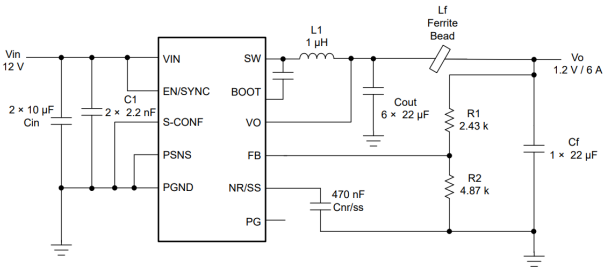


Figure 34. *TPS62916 typical schematic.*

The first technique integrated into the TPS62913 uses a 2.2-MHz switching frequency in conjunction with a larger-than-normal inductance for the first LC filter. The combined result of this high switching frequency with a 2.2-µH inductor is a reduction in the di/dt ripple.

This reduction in di/dt also affects the transient response, though, so using a large inductance is best suited for applications where the load is fairly steady, such as clocks and PLLs. The larger inductance and higher switching frequency may also work for 1.8-V noise-sensitive ADCs, digital to analog converters and AFE rails. For core power, it will depend on the load transient requirements.

The second feature used in both devices is an integrated ferrite bead filter compensation. The first LC filter loop uses the VO pin to sense the first LC output, with a crossover frequency of approximately 130 kHz for the example shown. The device uses the feedback pin to sense the output voltage after the ferrite bead filter through a resistor divider. Using this feedback pin with internal ferrite bead filter compensation (which is much slower than the first LC compensation) enables stable operation of the circuit and eliminates the ferrite bead filter problems discussed earlier.

SMA connectors can measure the output voltage ripple before and after the second LC filter. **Figure 35** highlights the ripple at the first LC filter in red and highlights the ripple after the ferrite bead filter in blue.

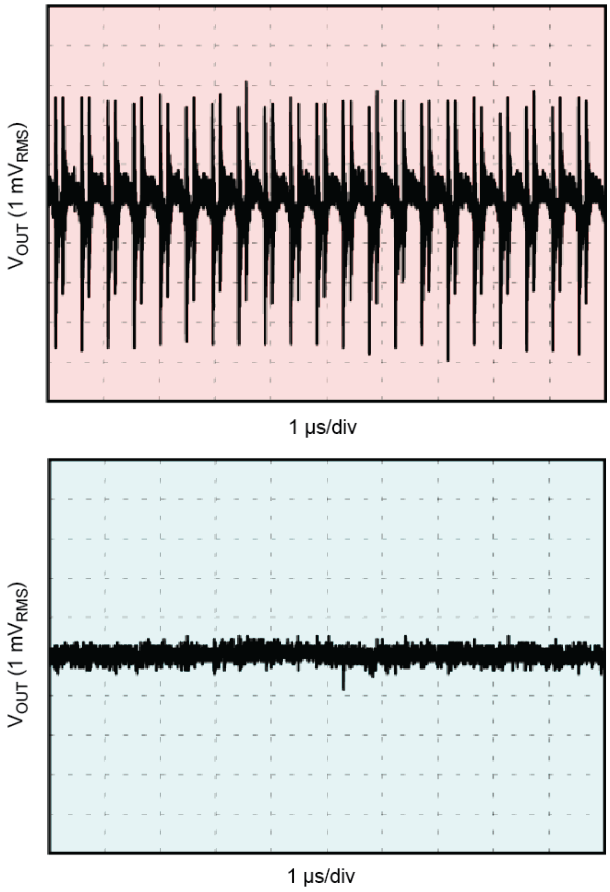


Figure 35. *Output voltage ripple in the time domain before and after the ferrite bead filter.*

In addition to the time-domain measurements, it is useful to use a spectrum analyzer to generate an FFT plot, as shown in **Figure 36**.

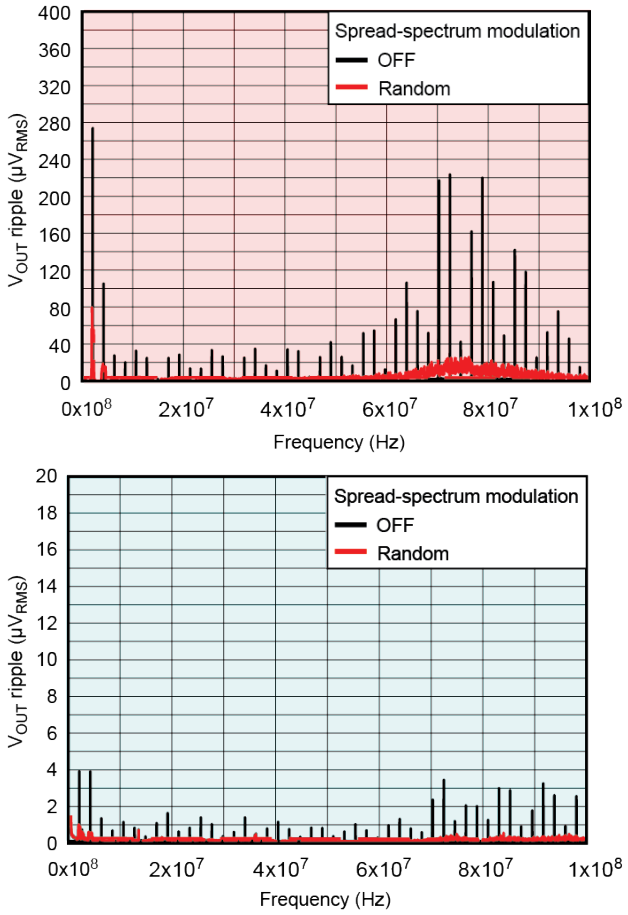


Figure 36. *Output voltage ripple in the frequency domain before and after the ferrite bead filter.*

We generated these plots using a 10-kHz bandwidth from 500 kHz to 100 MHz to show the frequency components of the ripple that you cannot distinguish when looking at the time-domain ripple measurement on an oscilloscope.

As discussed previously, a ferrite bead filter effectively filters the fundamental f_{SW} and the higher-frequency components. Both the TPS62913 and TPS62916 have an integrated ferrite bead filter compensation that works for a wide variety of ferrite beads up to a 50-nH inductance. Note that the output voltage is sensed by the feedback pin resistor divider after the ferrite bead filter, which helps with DC regulation if there is an output voltage drop caused by the ferrite bead resistance. The VO pin feedback achieves loop stability for the primary LC filter. These two separate feedback loops (VO and FB) ensure stability and regulation. The TPS62913 also includes spread-spectrum options that, when enabled, can further reduce the ripple.

There are many potential sources of noise (100Hz to 100kHz), including the bandgap, error amplifier, feedback divider, current-sense amplifier and oscillator. By far, the biggest contributor to noise is the bandgap, so filtering the voltage reference with an external capacitor yields significantly lower integrated noise. The TPS62913 and TPS62913 integrate a noise-reduction capacitor with a soft-start function, similar to many low-noise LDOs. After completing soft start, the soft-start capacitor becomes a noise-reduction capacitor. A 470-nF soft-start noise-reduction capacitor results in a 5-ms soft-start time and a 16.7-μV_{RMS} integrated noise figure from 100Hz to 100kHz. The integrated error amplifier and current-sense amplifier in the TPS62913 and TPS62916 are optimized for low-noise behavior as well.

Keeping the external feedback resistors fairly low in value helps to reduce the impedance on the feedback pin and minimize any noise contribution. Using lower-value resistors will burn slightly more power, but this is usually an acceptable trade-off, since the loads are fairly constant and low quiescent current is not necessary for standby modes. The power savings gained by eliminating the LDO more than make up for the higher light-load current.

A high-performance ADC used in test and measurement applications demonstrates the effectiveness of these silicon techniques. The ***Powering Sensitive Noise ADC Designs with the TPS62913 Low-Noise Buck Converter*** reference design, shown in **Figure 37**, uses four low electromagnetic interference switching converters, using the LMS3635M step converter with three low-noise LDOs and ferrite beads.

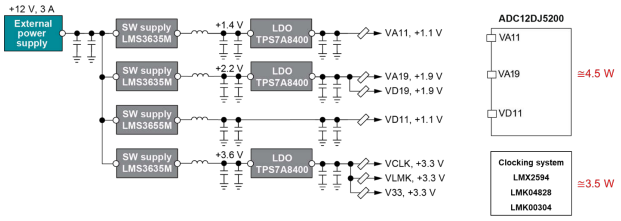


Figure 37. *Original ADC design with switching converters and LDOs.*

Figure 38 shows how the TPS62913 simplifies this design by eliminating the LDOs.

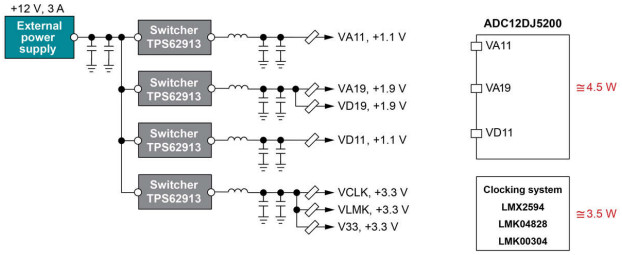
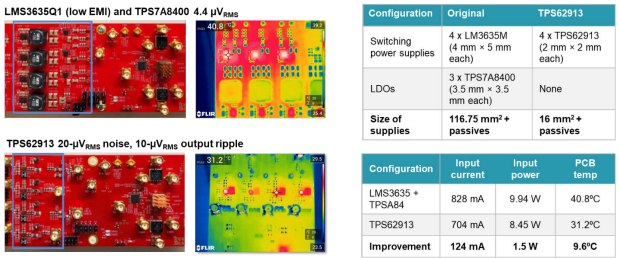


Figure 38. *ADC design using the TPS62913 converter without LDOs.*

In the designs discussed in **Figure 37** and **Figure 38**, the VA11 and VD11 rails are the most noise sensitive, so we used separate switchers for each rail. The clocking circuit implements individual ferrite bead filters on all three 3.3-V rails for clocking power, with the feedback sense point connected to the highest current rail. This approach enables a single device to supply multiple rails with low noise and low ripple while maintaining the best load regulation.

Figure 39 shows how the TPS62913 provides a much smaller solution size by eliminating the LDOs. In addition to the size reduction, eliminating the thermal loss of the LDOs results in a 1.5-W power reduction, which reduces total system power by 15%. Thermal management also becomes easier, since the hottest parts on the original board were the LDOs.



Configuration	Original	TPS62913
Switching power supplies	4 x LM3635M (4 mm × 5 mm each)	4 x TPS62913 (2 mm × 2 mm each)
LDOs	3 x TPS7A8400 (3.5 mm × 3.5 mm each)	None
Size of supplies	**116.75 mm² + passives**	**16 mm² + passives**

Configuration	Input current	Input power	PCB temp
LMS3635 + TPSA84	828 mA	9.94 W	40.8°C
TPS62913	704 mA	8.45 W	31.2°C
Improvement	**124 mA**	**1.5 W**	**9.6°C**

Figure 39. *Size and power savings comparison.*

Figure 40 compares the traditional approach with LDOs and a clock vs. The TPS62913 approach with no LDOs powering the ADC and clock for SNR, SFDR, noise spectral density and PSRRMOD. The low-noise features of the TPS62913 enable the powering of noise-sensitive rails of the clock and ADC without an LDO while closely meeting the performance specifications listed on the ***ADC12DJ5200RF 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC) Data Sheet***.

The SNR achieves results within half a decibel of the LDO implementation and close to the performance listed on the data sheet.

The SFDR also achieves results within half a decibel of the LDO implementation.

The noise spectral density shows performance within 1 dB of the LDO implementation.

And finally, the PSRRMOD shows no in-band noise vs. the LDO implementation. Since the TPS62913 solution switches at 1 MHz, even the spur at 600 kHz from the previous DC/DC converter is eliminated.

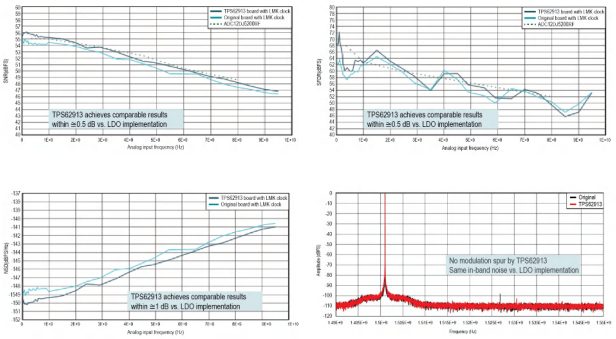


Figure 40. *Performance comparisons for SNR, SFDR, noise spectral density and PSMR.*

Conclusions

This paper explored how to power noise-sensitive systems without LDO post-filtering, resulting in reduced power dissipation and system cooling costs. The total solution size decreases, and with a derived target for output voltage ripple and noise, it is possible to power high-speed, noise-sensitive systems for telecommunication and test-and-measurement applications.

It is also possible to optimize a DC/DC converter LC filter to lower the output voltage ripple in several ways. But only integrated low-noise circuit techniques can achieve truly low-frequency noise (<100kHz) on the output voltage of a DC/DC converter. A ferrite bead provides the most effective and affordable way to filter high-frequency noise >10MHz.

The TPS62913, TPS62916, TPSM82913, and TPSM82916 address of DC/DC f_{SW}, low-noise and high-frequency filtering. These buck converters can power noise-sensitive loads without the need for LDO post-filtering, providing a tested and specified solution for today's precision systems.

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