BQ21062 具有电源路径、负载开关、10nA 运输模式和稳压系统 (PMID) 电压的 I^2C 控制型单节电池 500mA 线性电池充电器

1 特性

- 具有 1.25mA 至 500mA 快速充电电流范围的线性电池充电器
    - 0.5% 精度 I^2C 可编程电池稳压电压，范围为 3.6V 至 4.6V 且阶跃为 10mV
    - 可配置的终止电流，支持低至 0.5mA
    - 可耐受 20V 的输入，具有 3.4V 至 5.5V 的典型输入电压工作范围
    - 可编程热负荷曲线，完全可配置的热、温、凉、冷阈值
- 电源路径管理，用于系统供电和电池充电
    - I^2C 可编程稳定系统电压 (PMID) 范围为 4.4V 至 4.9V，此外还具有电池电压跟踪功能和输入直通选项
    - 动态电源路径管理可以对通过弱适配器充电进行优化
    - 利用高级 I^2C 控制，主机可以根据需要断开电池或适配器
- I^2C 可配置负载开关或高达 150mA LDO 输出
    - 可编程范围为 0.6V 至 3.7V，阶跃为 100mV
- 超低 Iddq，可延长电池寿命
    - 10nA 运输模式电池 Iq
    - 在为系统供电时具有 400nA 的 Iq（PMID 和 VDD 打开）
- 通过可调节计时器实现单按钮唤醒和重置输入
    - 支持系统循环通电和硬件重置
- 20 引脚 2mm x 1.6mm CSP 封装
- 总解决方案尺寸为 $11mm^2$

2 应用

- 耳麦、耳塞和助听器
- 智能手表和智能追踪器
- 可穿戴健身和活动监测仪
- 血糖监测仪

3 说明

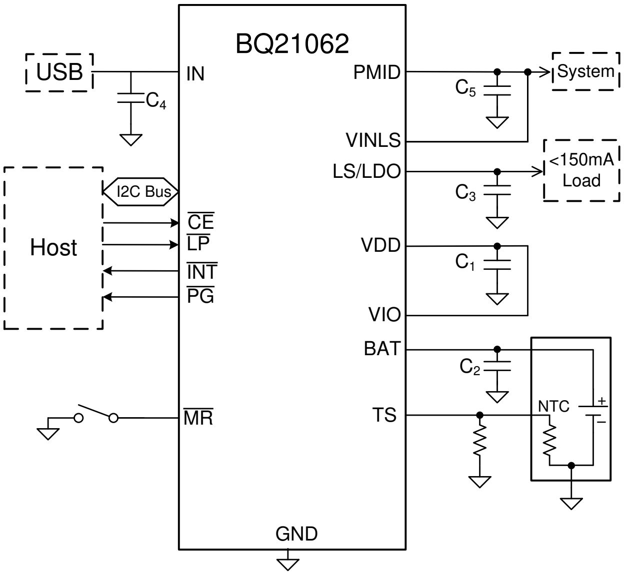
BQ21062 是一款高度集成的电池充电管理 IC，其集成了适用于可穿戴设备、便携式设备和小型医疗设备的常用功能，即充电器、用于系统电源的稳定输出电压轨、负载开关/LDO 以及按钮控制器。

BQ21062 IC 集成了具有电源路径的线性充电器，可实现对小型电池进行快速准确的充电，同时为系统提供稳定电压。根据下游 IC 和系统负载的建议运行条件，稳定系统电压 (PMID) 输出可通过 I^2C 进行配置，从而实现最佳的系统运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
BQ21062	DSBGA (20)	2.00mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2020) to Revision A (April 2023)	**Page**
• Changed $t_{HW\_RESET\_WD}$ Test Conditions and MAX value	10
• Changed t_{RESET_WARN}	10
• Changed t_{HW_RESET}	10
• Changed 图 9-3	20
• Changed $t_{HW\_RESET\_WARN}$ to t_{RESET_WARN} in 节 9.3.7.2	21
• Changed VIN presence to valid VIN presence in 节 9.3.7.2	21
• Changed text in 节 9.4.1	29

5 说明（续）

该器件支持高达 500mA 的充电电流，并且支持低至 0.5mA 的终止电流，以实现最充分的充电。该器件采用标准锂离子充电曲线分三个阶段对电池进行充电：预充电、恒流和恒压调节。

该器件集成了高级电源路径管理和控制，使该器件可以为系统提供电源，同时甚至能够使用很差的适配器为电池充电。主机还可以通过 I^2C 控制电源路径，允许它断开输入适配器和/或电池，而无需实际移除它们。单按钮输入无需单独的按钮控制器 IC，从而减少了整体解决方案占用空间。按钮输入可用于唤醒功能或重置系统。运行和关断期间的低静态电流有助于延长电池寿命。可通过 I^2C 接口对输入电流限制、充电电流、LDO 输出电压和其他参数进行编程，从而使 BQ21062 成为非常灵活的充电解决方案。该器件包含一个基于电压的 JEITA 兼容（或标准热/冷）电池组热敏电阻监控输入 (TS)，可监控电池温度并自动更改充电参数，从而防止电池在超出其安全温度范围的温度下充电。还可以通过 I^2C 对温度阈值进行编程，从而使主机能够自定义热负荷曲线。该充电器针对 5V USB 输入进行了优化，具有 20V 的绝对最大容差，可承受线路瞬变。该器件还集成了一个用于为无线电或处理器提供静态轨的线性稳压器，可以通过 I^2C 独立地为其提供电源并对其进行控制。

6 Device Comparison Table

表 6-1. Device Comparison

PARAMETER	BQ21061	BQ21062
ICHARGE (default)	10mA	67.5mA
IPRECHARGE (default)	2.5mA	8.75mA
INLIM (default)	500mA	100mA
WATCHDOG TIMER (default)	Enabled	Disabled
VINDPM (default)	Disabled	Enabled
DPPM	Enabled	Disabled
LS/LDO (default)	Enabled	Disabled
LDO CONFIG (default)	LDO	Load Switch
BATUVLO (default)	3V	2.8V
MR HW RESET (default)	8s	14s
AUTOWAKE TIME (default)	1.2s	2.4s
TS THRESHOLD (default)	TWARM = 45°C; THOT = 60°C	TWARM = THOT = 45°C

7 Pin Configuration and Functions

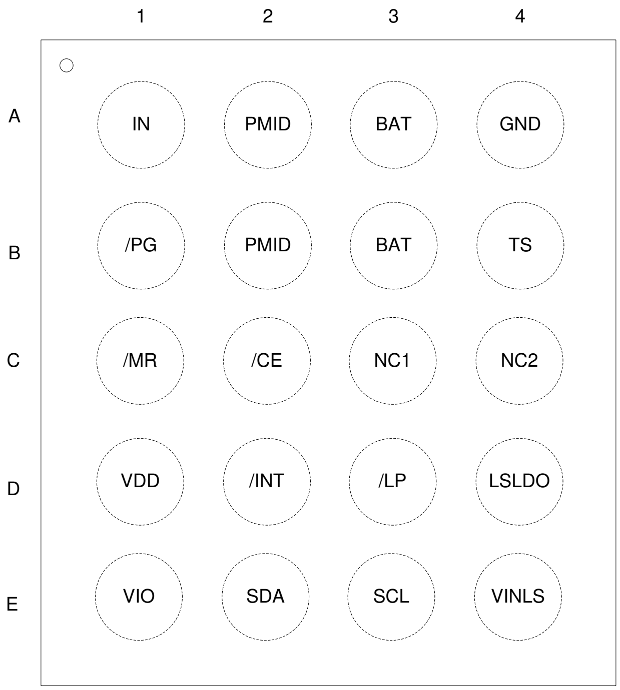


图 7-1. YFP Package 20-Pin DSBGA Top View

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	A1	I	DC Input Power Supply. IN is connected to the external DC supply. Bypass IN to GND with at least 1-μF of capacitance using a ceramic capacitor.
PMID	A2, B2	I/O	Regulated System Output. Connect 22-μF capacitor from PMID to GND as close to the PMID and GND pins as possible. If operating in VIN Pass-Through Mode (PMID_REG = 111) a lower capacitor value may be used (at least 3-μF of ceramic capacitance with DC bias de-rating).
GND	A4	PWR	Ground connection. Connect to the ground plane of the circuit.
VDD	D1	O	Digital supply LDO. Must connect a 2.2-μF from this pin to ground, do not leave floating.
$\overline{\text{CE}}$	C2	I	Charge Enable. Drive $\overline{\text{CE}}$ low or leave disconnected to enable charging when VIN is valid. $\overline{\text{CE}}$ is pulled low internally with 900-kΩ resistor.
SCL	E3	I/O	I^2C Interface Clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	E2	I	I^2C Interface Data. Connect SDA to the logic rail through a 10-kΩ resistor.
$\overline{\text{LP}}$	D3	I	Low Power Mode Enable. Drive this pin low to set the device in low power mode when powered by the battery. This pin must be driven high to allow I^2C communication when VIN is not present. $\overline{\text{LP}}$ is pulled low internally with 900-kΩ resistor. This pin has no effect when VIN is present.
$\overline{\text{INT}}$	D2	O	$\overline{\text{INT}}$ is an open-drain output that signals fault interrupts. When a fault occurs, a 128-μs pulse is sent out as an interrupt for the host.
$\overline{\text{MR}}$	C1	I	Manual Reset Input. $\overline{\text{MR}}$ is a general purpose input used to reset the device or to wake it up from Ship Mode. $\overline{\text{MR}}$ has in internal 125-kΩ pull-up resistor to BAT. The battery voltage V_{BAT} must be above $V_{BATUVLO}$ in order for $\overline{\text{MR}}$ low logic level to be detected.
LS/LDO	D4	O	Load Switch or LDO output. Connect 2.2 μF of ceramic capacitance to this pin to assure stability. Be sure to account for capacitance bias voltage derating when selecting the capacitor. If LDO is not used, short to VINLS
VINLS	E4	I	Input to the Load Switch / LDO output. Connect at least 1 μF of ceramic capacitance from this pin to ground.

表 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
BAT	A3, B3	I/O	Battery Connection. Connect to the positive terminal of the battery. Bypass BAT to GND with at least 1 μF of ceramic capacitance.
TS	B4	I	Battery Pack NTC Monitor. Connect TS to a 10-kΩ NTC thermistor in parallel to a 10-kΩ resistor. If TS function is not to be used connect a 5-kΩ resistor from TS to ground.
$\overline{\text{PG}}$	B1	O	Open-drain Power Good status indication output. The $\overline{\text{PG}}$ pin can also be configured as a general purpose open drain output or level shifter version of $\overline{\text{MR}}$.
VIO	E1	I	System IO supply. Connect to system IO supply to allow level shifting of input signals (SDA, SCL, LP and CE) to the device internal digital domain. Connect to VDD when external IO supply is not available.
NC1	C3	I	No Connect. Connect to ground if possible for better thermal dissipation or leave floating. Do not connect to a any voltage source or signal to avoid higher quiescent current.
NC2	C4	I	No Connect. Connect to ground if possible for better thermal dissipation. May be shorted to /LP for easier routing as long as Absolute Maximum Rating requirements are met..

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	20	V
	TS,VDD, NC	–0.3	1.95	V
	All other pins	–0.3	5.5	V
Current	IN	0	800	mA
	BAT, PMID	–0.5	1.5	A
	INT, $\overline{PG}$	0	10	mA
Junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery voltage range	2.4		4.6	V
V_{IN}	Input voltage range	3.15		5.25(1)	V
V_{INLS}	LDO input voltage range	2.2		5.25(1)	V
V_{IO}	IO supply voltage range	1.2		3.6	V
I_{LDO}	LDO output current	0		100	mA
I_{PMID}	PMID output current	0		1.5	A
T_A	Operating free-air temperature range	–40		85	°C

(1) Based on minimum V_{OVP} value. 5.5V under typical conditions

8.4 Thermal Information

THERMAL METRIC(1)		BQ21062	UNIT
		YFP (DSBGA)	
		20-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	36.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

8.4 Thermal Information (continued)

THERMAL METRIC[1]		BQ21062 YFP (DSBGA) 20-PIN	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	17.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured in BQ21062EVM board.

8.5 Electrical Characteristics

V_{IN} = 5V, V_{BAT} = 3.6V, -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{IN}	Input supply current	PMID_MODE = 01, V_{IN} = 5V, V_{BAT} = 3.6V			500	µA
		V_{IN} = 5V, V_{BAT} = 3.6V Charge Disabled			1.6	mA
I_{BAT_SHIP}	Battery Discharge Current in Ship Mode	V_{IN} = 0V , V_{BAT} = 3.6V		10		nA
I_{BAT_LP}	Battery Quiescent Current in Low-power Mode	V_{IN} = 0V , V_{BAT} = 3.6V, LDO Disabled		0.46	0.9	µA
		V_{IN} = 0V , V_{BAT} = 3.6V, LDO Enabled		1.7	1.9	µA
I_{BAT_ACTIVE}	Battery Quiescent Current in Active Mode	V_{IN} = 0V , V_{BAT} = 3.6V, LDO Disabled		18	23	µA
		V_{IN} = 0V , V_{BAT} = 3.6V, LDO Enabled		21	25	µA
POWER PATH MANAGEMENT AND INPUT CURRENT LIMIT						
V_{PMID_REG}	Default System (PMID) Regulation Voltage			4.5		V
$V_{PMID\_REG\_ACC}$	System Regulation Voltage Accuracy	V_{IN} = 5V, V_{PMID_REG} = 4.5V. I_{PMID} = 100mA, T_J = 25°C	-1		1	%
		V_{IN} = 5V, V_{PMID_REG} = 4.5V. I_{PMID} = 0-500mA	– 3		3	%
$R_{ON(IN-PMID)}$	Input FET ON resistance	I_{ILIM} = 500mA (ILIM = 110), V_{IN} = 5V, I_{IN} = 150mA		280	520	mΩ
V_{BSUP1}	Enter supplements mode threshold	V_{BAT} > $V_{BATUVLO}$, Charge disabled		V_{PMID} < V_{BAT} – 40mV		mV
V_{BSUP2}	Exit supplements mode threshold	V_{BAT} > $V_{BATUVLO}$, Charge disabled		V_{PMID} < V_{BAT} – 20mV		mV
I_{ILIM}	Input Current Limit	Programmable Range	50		600	mA
		I_{ILIM} = 50mA		45	50	mA
		I_{ILIM} = 100mA		90	100	mA
		I_{ILIM} = 150mA		135	150	mA
		I_{ILIM} = 500mA		450	500	mA
V_{IN_DPM}	Input DPM voltage threshold where current in reduced	Programmable Range	4.2		4.9	V
	Accuracy		– 3		3	%
BATTERY CHARGER						
$R_{ON(BAT-PMID)}$	Battery Discharge FET On Resistance	V_{BAT} = 4.35V, I_{BAT} = 100mA		100	175	mΩ
V_{BATREG}	Charge Voltage	Programmable charge voltage range	3.6		4.6	V
	Voltage Regulation Accuracy		0.5		0.5	%

8.5 Electrical Characteristics (continued)

V_{IN} = 5V, V_{BAT} = 3.6V, -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHARGE}	Fast Charge Programmable Current Range	$V_{LOWV} < V_{BAT} < V_{BATREG}$	1.25			mA
	Fast Charge Current Accuracy	I_{CHARGE} > 5mA	–5		5	%
$I_{PRECHARGE}$	Precharge current	Precharge current programmable range	1.25			mA
	Precharge Current Accuracy	-40°C < T_J < 85°C	–10		10	%
I_{TERM}	Termination Charge Current	Termination Current Programmable Range	1		31	%
	Accuracy	I_{TERM} = 10% I_{CHARGE}, I_{CHARGE} = 100mA	–5[1]		5[1]	%
V_{LOWV}	Programmable voltage threshold for pre-charge to fast charge transitions	VBAT rising. Programmable Range	2.8		3	V
V_{SHORT}	Battery voltage threshold for short detection	VBAT falling, VIN = 5V	2.41	2.54	2.67	V
I_{SHORT}	Charge Current in Battery Short Condition	$V_{BAT} < V_{SHORT}$		$I_{PRECHARGE}$		mA
V_{RCH}	Recharge Threshold voltage	V_{BAT} falling, V_{BATREG} = 4.2V, V_{RCH} = 140mV setting		140		mV
		V_{BAT} falling, V_{BATREG} = 4.2V, V_{RCH} = 200mV setting		200		mV
R_{PMID_PD}	PMID pull-down resistance	V_{PMID} = 3.6V		25		Ω
VDD						
V_{DD}	VDD LDO output voltage			1.8		V
LS/LDO						
V_{INLS}	Input voltage range for Load switch Mode		0.8		5.5	V
	Input voltage range for LDO Mode		2.2 or V_{LDO} + 500mV		5.5	V
V_{LDO}	LDO programmable output voltage range		0.6		3.7	V
	LDO output accuracy	T_J = 25°C	–2		2	%
		V_{LDO} = 1.8V, V_{INLS} =3.6V. I_{LOAD} = 1mA	–3		3	%
$\Delta V_{OUT}/\Delta I_{OUT}$	DC Load Regulation	0°C < T_J < 85°C, 1 mA < I_{OUT} < 150mA, V_{LDO} = 1.8V		1.2		%
$\Delta V_{OUT}/\Delta V_{IN}$	DC Line Regulation	0°C < T_J < 85°C, Over V_{INLS} range, I_{OUT} = 100mA, V_{LDO} = 1.8V		0.5		%
R_{DOSN_LDO}	Switch On resistance	V_{INLS} = 3.6V		250	450	mΩ
R_{DSCH_LSLDO}	Discharge FET On-resistance for LS	V_{INLS} = 3.6V		40		Ω
I_{OCL_LDO}	Output Current Limit	$V_{LS/LDO}$ = 0V	200	300		mA
I_{IN_LDO}	LDO VINLS quiescent current in LDO mode	$V_{BAT} = V_{INLS}$=3.6V		0.9		µA
	OFF State Supply Current	$V_{BAT} = V_{INLS}$=3.6V		0.25		µA
BATTERY PACK NTC MONITOR						
V_{HOT}	High temperature threshold	V_{TS} falling, -10°C < T_J < 85°C	0.256[1]	0.265	0.268[1]	V
V_{WARM}	Warm temperature threshold	V_{TS} falling, -10°C < T_J < 85°C	0.256[1]	0.265	0.268[1]	V
V_{COOL}	Cool temperature threshold	V_{TS} rising, -10°C < T_J < 85°C	0.510[1]	0.514	0.523[1]	V
V_{COLD}	Cold temperature threshold	V_{TS} rising, -10°C < T_J < 85°C	0.581[1]	0.585	0.594[1]	V
V_{OPEN}	TS Open threshold	V_{TS} rising, -10°C < T_J < 85°C		0.9		V
V_{HYS}	Threshold hysteresis			4.7		mV

8.5 Electrical Characteristics (continued)

V_{IN} = 5V, V_{BAT} = 3.6V, -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TS_BIAS}	TS bias current	-10°C < T_J < 85°C	78.4	80	81.6	µA
PROTECTION						
V_{UVLO}	IN active threshold voltage	V_{IN} rising		3.4		V
		V_{IN} falling		3.25		V
$V_{BATUVLO}$	Battery undervoltage Lockout Threshold Voltage	Programmable range, 150 mV Hysteresis	2.4		3	V
	Accuracy		–3		3	%
	Battery undervoltage Lockout Threshold Voltage at Power Up	V_{BAT} rising, V_{IN} = 0V, T_J = 25°C		3.15		V
V_{SLP_ENTRY}	Sleep Entry Threshold (V_{IN} - V_{BAT})	2.0V < V_{BAT} < V_{BATREG}, V_{IN} falling		80		mV
V_{SLP_EXIT}	Sleep Exit Threshold (V_{IN} - V_{BAT})	2.0V < V_{BAT} < V_{BATREG}		130		mV
V_{OVP}	Input Supply Over Voltage Threshold	V_{IN} rising	5.35	5.5	5.8	V
		V_{IN} falling (125mV hysteresis)		5.4		V
I_{BAT_OCP}	Battery Over Current Threshold Programmable range	I_{BAT_OCP} increasing	1200		1600	mA
	Current Limit Accuracy		–30		30	%
$T_{SHUTDOWN}$	Thermal shutdown trip point			125		°C
T_{HYS}	Thermal shutdown trip point hysteresis			15		°C
I^2C INTERFACE (SCL and SDA)						
	I^2C Frequency		100		400	kHz
V_{IL}	Input Low threshold level	V_{PULLUP} = V_{IO} = 1.8V			0.25 * V_{IO}	V
V_{IH}	Input High Threshold level	V_{PULLUP} = V_{IO} = 1.8V	0.75 * V_{IO}			V
V_{OL}	Output Low threshold level	V_{PULLUP} = V_{IO} = 1.8V, I_{LOAD} = 5mA			0.25 * V_{IO}	V
I_{LKG}	High-level leakage Current	V_{PULLUP} = V_{IO} = 1.8V			1	µA
/MR INPUT						
R_{PU}	Internal pull up resistance		90	125	170	kΩ
V_{IL}	/MR Input Low threshold level	V_{BAT} > V_{BUVLO}			0.3	V
/INT, /PG OUTPUTS						
V_{OL}	Output Low threshold level	V_{PULLUP} = V_{IO} = 1.8V, I_{LOAD} = 5mA			0.25 * V_{IO}	V
I_{LKG}	/INT Hi level leakage Current	High Impedance, V_{PULLUP} = V_{IO} = 1.8V			1	µA
/CE, /LP INPUTS						
R_{PDOWN}	/CE pull down resistance			900		kΩ
V_{IL}	Input Low threshold level	V_{IO} = 1.8V			0.45	V
V_{IH}	/CE Input High Threshold level	V_{IO} = 1.8V	1.35			V

(1) Based on Characterization Data

8.6 Timing Requirements

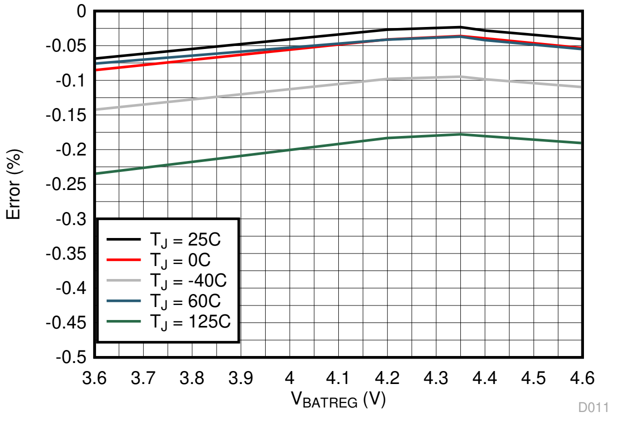
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGE TIMERS						
t_{MAXCHG}	Charge safety timer	Programmable range	180		720	min

8.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PRECHG}	Precharge safety timer		0.25 * t_{MAXCHG}			
WATCHDOG TIMERS						
$t_{WATCHDOG\_SW}$	SW Watchdog timer		25	50		s
$t_{HW\_RESET\_WD}$	HW reset watchdog timer	HWRESET_14S_WD = 1			14	s
LDO						
t_{ON_LDO}	Turn ON time	100mA load, to 90% V_{LDO}		500		µs
t_{OFF_LDO}	Turn OFF time	100mA load, to 10% V_{LDO}		30		µs
$t_{PMID\_LDO\_DELAY}$	Delay between PMID and LDO enable during power up	Startup		20		ms
PUSHBUTTON TIMERS (/MR)						
t_{WAKE1}	WAKE1 Timer. Timer for Ship Mode wake.	MR_WAKE1_TIMER = 0	106	125	144	ms
t_{WAKE2}	WAKE2 Timer. Time from /MR falling edge to INT being asserted.	MR_WAKE2_TIMER = 1	1.7	2	2.3	s
t_{RESET_WARN}	RESET_WARN Timer. Time prior to HW RESET or entering shipmode with MR press	MR_RESET_WARN = 01	0.85	1	1.15	s
t_{HW_RESET}	HW RESET Timer. Time from /MR falling edge to HW Reset or PMID falling for shipmode entry	MR_HW_RESET = 01	6.8	8	9.2	s
$t_{RESTART(AUTOWAKE)}$	RESTART Timer. Time from /MR HW Reset to PMID power up	AUTOWAKE = 01	1.05	1.2	1.35	s
PROTECTION						
t_{DGL_SLP}	Deglitch time for supply rising above V_{SLP} + V_{SLP_HYS}			120		µs
t_{DGL_OVP}	Deglitch time for V_{OVP} Threshold	VIN falling below V_{OVP}		32		ms
t_{DGL_OCP}	Battery OCP deglitch time			30		µs
t_{REC_SC}	Recovery time, BAT Short Circuit during Discharge Mode			250		ms
t_{RETRY_SC}	Retry window for PMID or BAT short circuit recovery			2		s
t_{DGL_SHTDWN}	Deglitch time, Thermal shutdown	T_J rising above $T_{SHUTDOWN}$		10		µs
I2C INTERFACE						
$t_{WATCHDOG}$	I^2C interface reset timer for host	When enabled		50		s
$t_{I2CRESET}$	I^2C interface inactive reset timer			500		ms
INPUT PINS (/CE and /LP)						
$t_{LP\_EXIT\_I2C}$	Time for device to exit Low-power mode and allow I^2C communication	V_{IN} = 0V.			1	ms

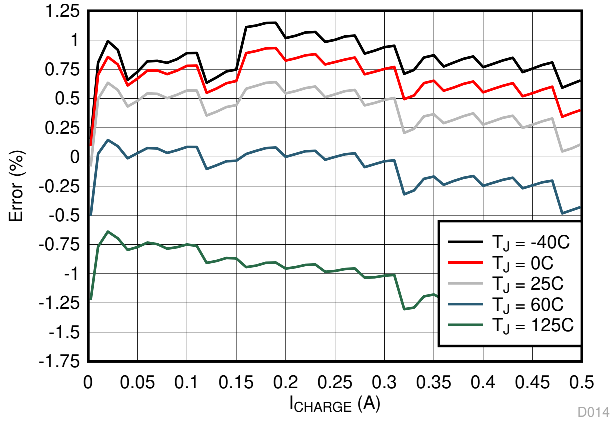
8.7 Typical Characteristics

C_{IN} = 1 µF, C_{PMID}= 10 µF, C_{LSLDO} = 2.2 µF, C_{BAT} = 1 µF (unless otherwise specified)



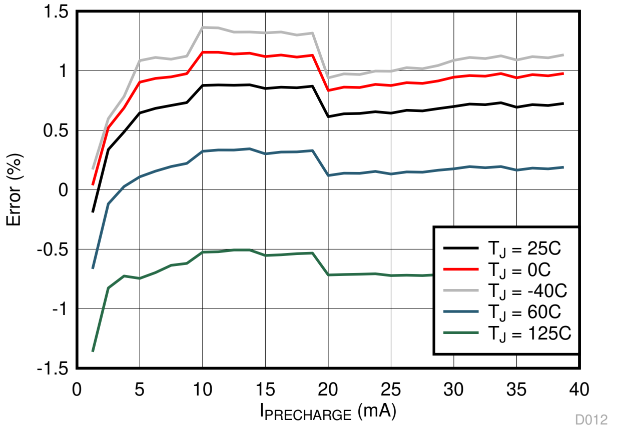
VIN = 5 V PMID_REG_CTRL = 111 (Pass-Through)

图 8-1. Battery Regulation Voltage Accuracy vs. VBATREG Setting



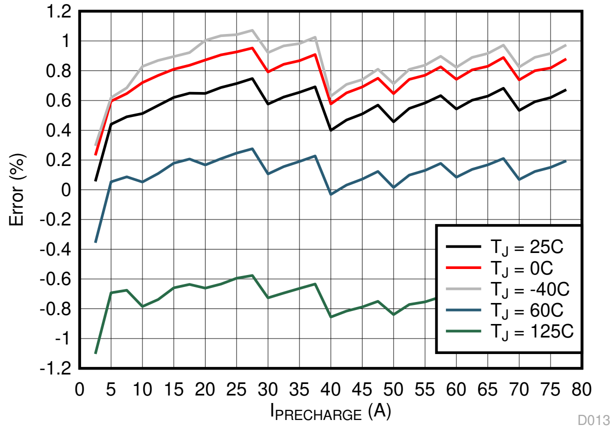
VIN = 5 V VBAT = 3.6 V ICHARGE_RANGE = 1

图 8-2. Charge Current Accuracy vs. ICHARGE Setting



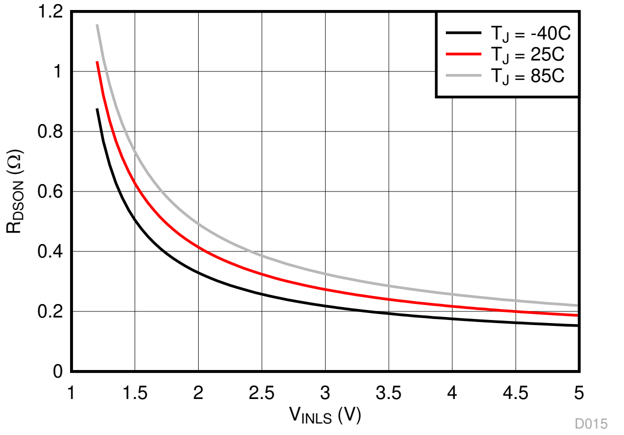
VIN = 5 V VBAT = 2.7 V ICHARGE_RANGE = 0

图 8-3. Pre-Charge Current Accuracy vs. IPRECHARGE setting (ICHARGE_RANGE = 0)



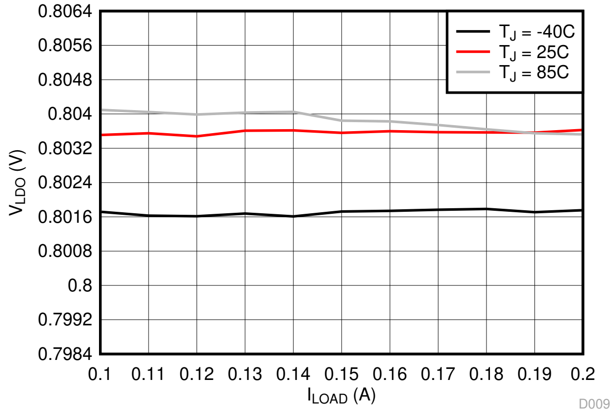
VBUS = 5 V VBAT = 2.7 V ICHARGE_RANGE = 1

图 8-4. Pre-Charge Current Accuracy vs. IPRECHARGE Setting (ICHARGE_RANGE = 1)



VBUS = 5 V

图 8-5. LS/LDO Switch On Resistance vs. VINLS

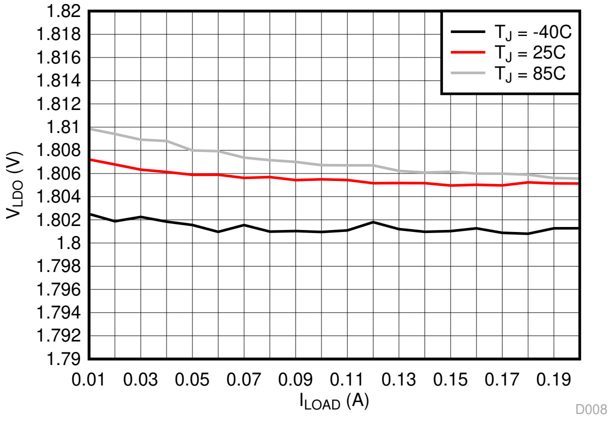


VIN = 0 V VBAT = 3.6 V VINLS = VPMID

图 8-6. LDO Load Regulation (VLDO = 0.8 V)

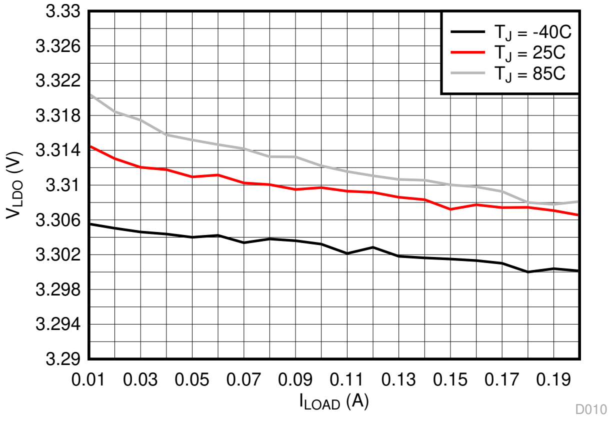
8.7 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{PMID}= 10 µF, C_{LSLDO} = 2.2 µF, C_{BAT} = 1 µF (unless otherwise specified)



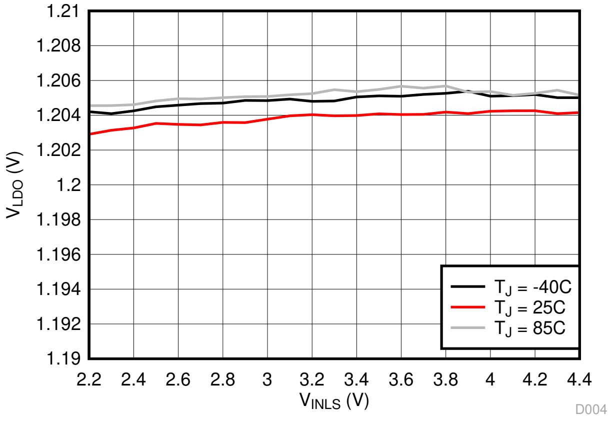
VIN = 0 V VBAT = 3.6 V VINLS = VPMID

图 8-7. LDO Load Regulation (VLDO = 1.8 V)



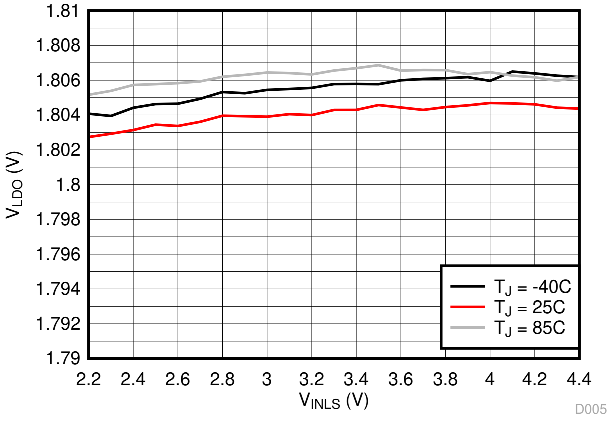
VIN = 0 V VBAT = 3.6 V VINLS= VPMID

图 8-8. LDO Load Regulation (VLDO = 3.3 V)



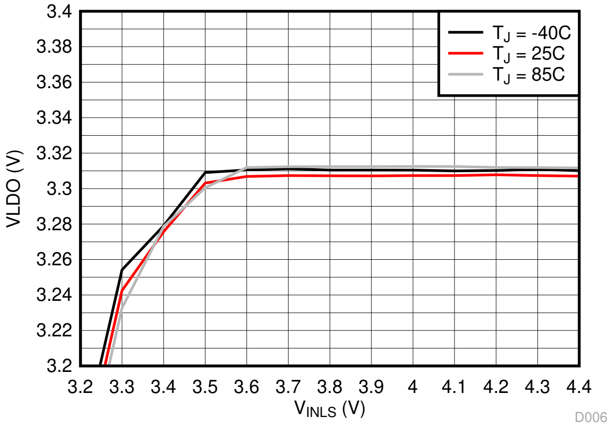
VBAT = 4.4 V ILOAD = 150 mA

图 8-9. LDO Line Regulation (VLDO = 1.2 V)



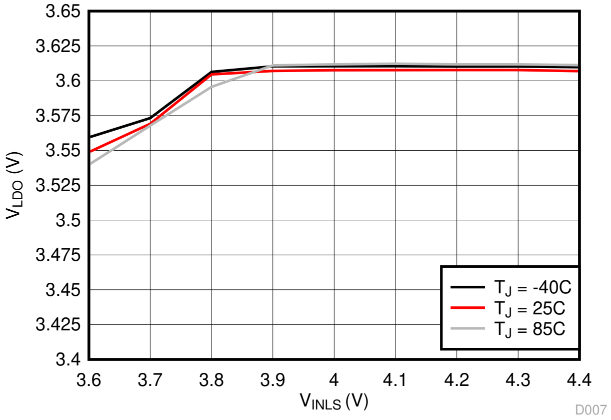
VBAT = 4.4 V ILOAD = 150 mA

图 8-10. LDO Line Regulation (VLDO = 1.8 V)



VBAT = 4.4 V ILOAD = 150 mA

图 8-11. LDO Line Regulation (VLDO = 3.3 V)

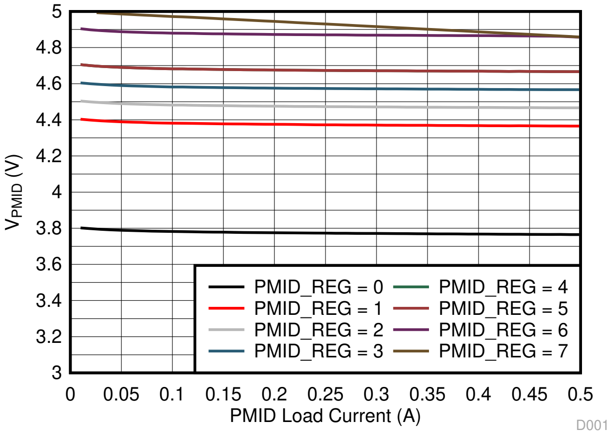


VBAT = 4.4 V ILOAD = 150 mA

图 8-12. LDO Line Regulation (VLDO = 3.6 V)

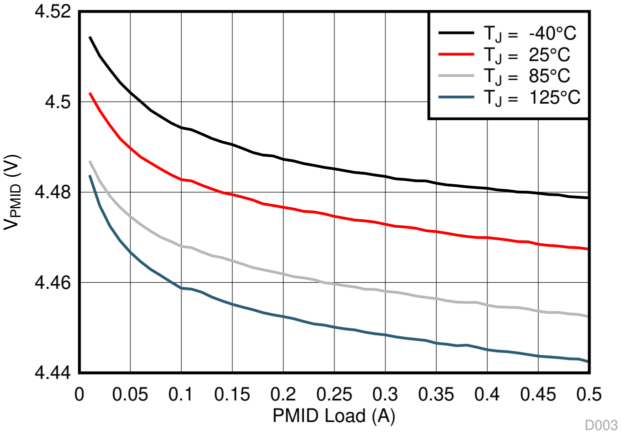
8.7 Typical Characteristics (continued)

C_{IN} = 1 µF, C_{PMID}= 10 µF, C_{LSLDO} = 2.2 µF, C_{BAT} = 1 µF (unless otherwise specified)



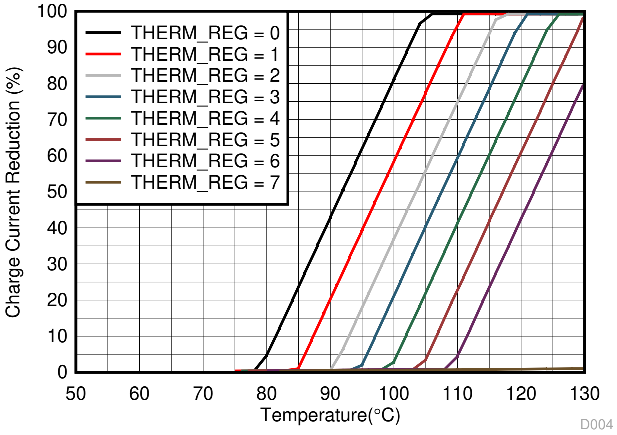
VBAT = 0 V

图 8-13. PMID Load Regulation



VBAT = 3.6 V VIN = 5 V

图 8-14. PMID Load Regulation vs. Temperature



VBAT = 3.6 V VIN = 5 V

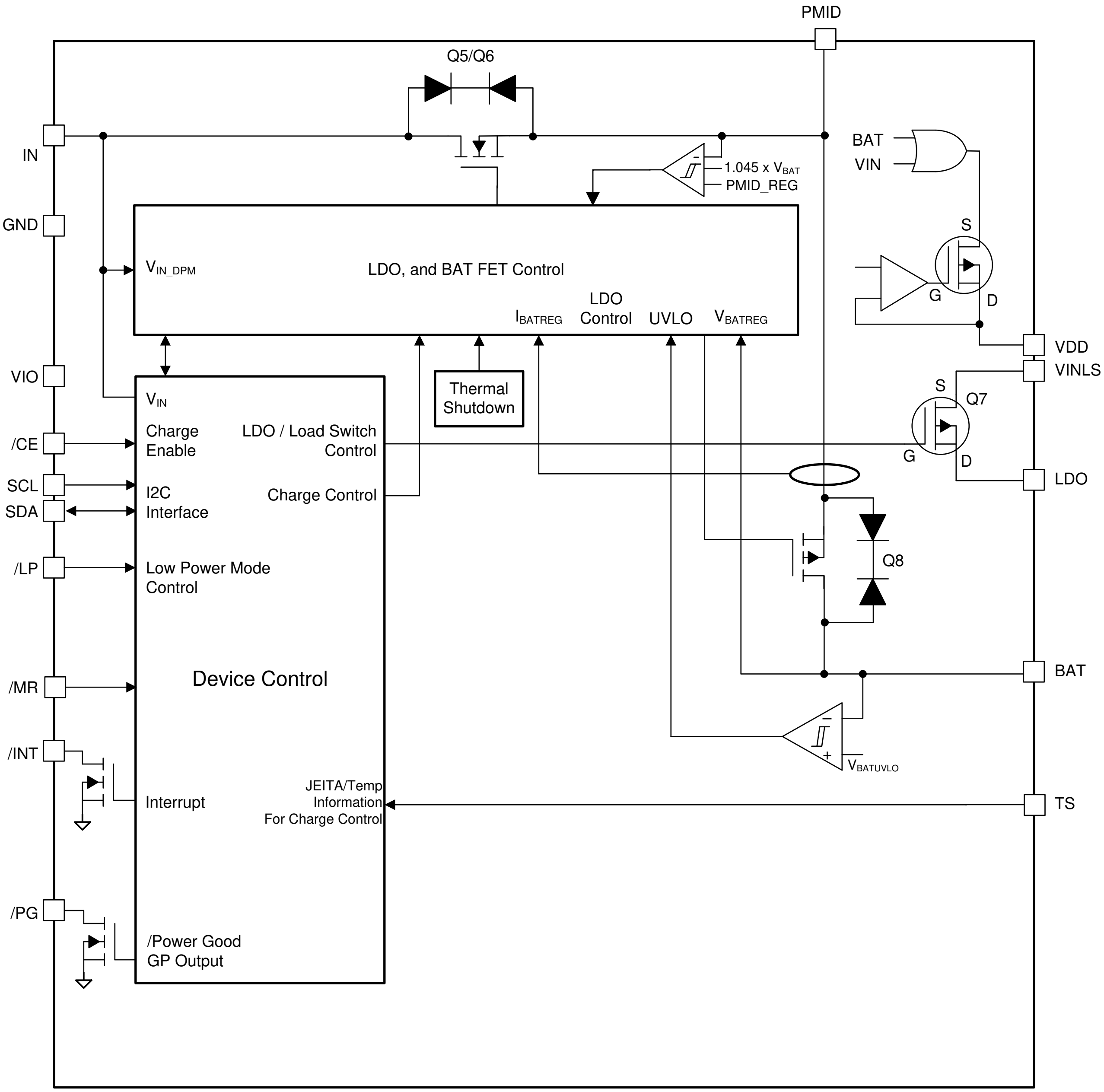
图 8-15. Charge Current Thermal Regulation

9 Detailed Description

9.1 Overview

The IC is a highly programmable battery management device that integrates a 500-mA linear charger for single cell Li-Ion batteries, a general purpose LDO that may be configured as a load switch, and a push-button controller. Through it's I^2C interface the host may change charging parameters such as battery regulation voltage and charge current, and obtain detailed device status and fault information. The push-button controller allows the user to reset the system without any intervention from the host and wake up the device from Ship Mode.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Linear Charger and Power Path

The BQ21062 IC integrates a linear charger that allows the battery to be charged with a programmable charge current of up to 500 mA. In addition to the charge current, other charging parameters can be programmed through I^2C such as the battery regulation voltage, pre-charge current, termination current, and input current limit current.

The power path allows the system to be powered from PMID, even when the battery is dead or charging, by drawing power from IN pin. It also prioritizes the system load connected to PMID, reducing the charging current, if necessary, in order to support the load when input power is limited. If the input supply is removed and the battery voltage level is above $V_{BATUVLO}$, PMID will automatically and seamlessly switch to battery power.

A more detailed description of the charger functionality is presented in the following sections of this document.

9.3.1.1 Battery Charging Process

The following diagram summarizes the charging process of the BQ21062 charger.

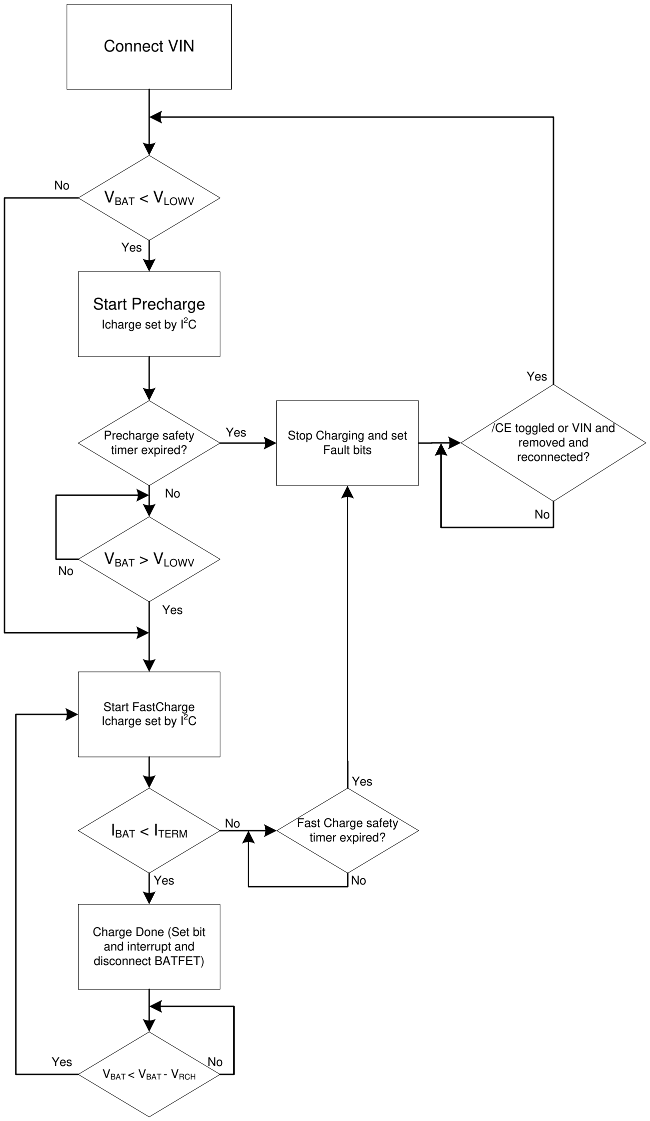


图 9-1. BQ21062 Charger Flow Diagram

When a valid input source is connected (V_{IN} > V_{UVLO} and $V_{BAT}+V_{SLP}$ < V_{IN} < V_{OVP}), the state of the $\overline{CE}$ pin determines whether a charge cycle is initiated. When the $\overline{CE}$ input is high and a valid input source is connected, the battery charge FET is turned off, preventing any kind of charging of the battery. A charge cycle is initiated when the CHARGE_DISABLE bit is written to 0 and $\overline{CE}$ pin in low. 表 9-1 shows the $\overline{CE}$ pin and bit priority to enable/disable charging.

表 9-1. Charge Enable Function Through $\overline{CE}$ Pin and $\overline{CE}$ Bit

$\overline{CE}$ PIN	CHARGE _DISABLE BIT	CHARGING
0	0	Enabled
0	1	Disabled
1	0	Disabled
1	1	Disabled

图 9-2 shows a typical charge cycle.

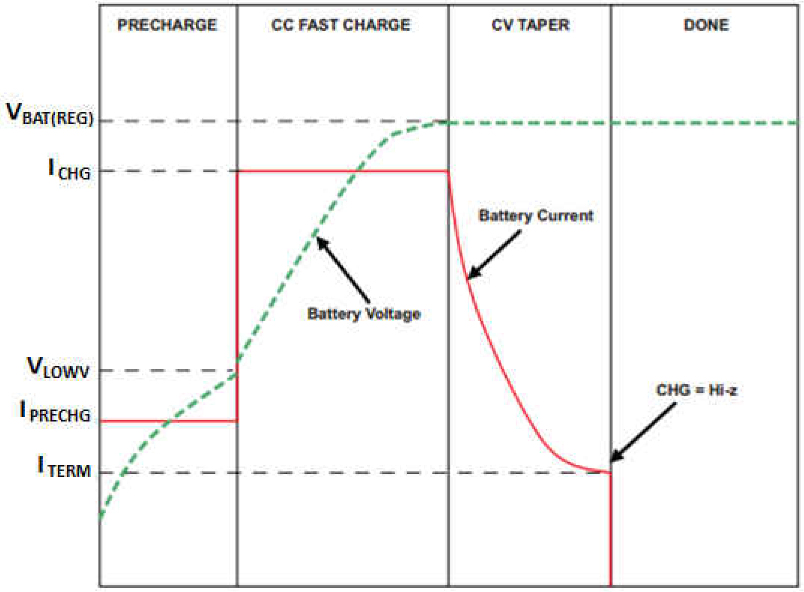


图 9-2. BQ21062 Typical Charge Cycle

During Pre-Charge, where the battery voltage is below the V_{LOWV} level, the battery willl be charge with $I_{PRECHARGE}$ current which can be programmed through I^2C. During pre-charge, the safety timer is set to 25% of the safety timer value during fast charge. Once the battery voltage reaches V_{LOWV}, the charger will then operate in Fast Charge Mode, charging the battery at I_{CHARGE} which may also be programmed through I_2C. Once the battery voltage approaches the V_{BATREG} level, the charging current starts tapering off as shown in 图 9-2. Once the charging current reaches the termination current (I_{TERM}) charging is stopped. Note that to ensure that the battery is charged to V_{BATREG} level, the regulated PMID voltage should be set to at least 200mV above V_{BATREG}. Termination is only enabled when the charger CV loop is active in fast charge operation. No termination will occur if the charge current reaches I_{TERM} while VINDPM is active as well as the thermal regulation loop. Termination is also disabled when operating in the TS WARM region. The charger only goes to termination when the current drops to I_{TERM} due to the battery reaching the target voltage and not due to the charge current limitation imposed by the previously mentioned control loops

Whenever a change in the charge current setting is triggered, whether it occurs due to I^2C programming by the host, Pre-Charge/Fast Charge transition or JEITA TS control, the device will temporarily disable charging (for ~ 1 ms) before updating the charge current value.

9.3.1.2 JEITA and Battery Temperature Dependent Charging

The charger can be configured through I^2C setting to provide JEITA support, automatically reducing the charging current and voltage depending on the battery temperature as monitored by an NTC thermistor connected to the BQ21062 TS pin. See 节 9.3.11 for details.

9.3.1.3 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a point where charging would be interrupted by reducing the current drawn by charger in order to keep V_{IN} from dropping below V_{IN_DPM}. Once the IN voltage drops to V_{IN_DPM}, the VINDPM loops will reduce the input current through the blocking FETs, to prevent the further drop of the supply voltage. The VINDPM function is enabled by default and may be disabled through I^2C command. The V_{IN_DPM} threshold is programmable through the I^2C register from 4.2 V to 4.9 V in 100-mV steps.

DPPM is disabled by default in this device and cannot be re-enabled through I^2C. When the device enters this mode, the charge current may be lower than the set value and the corresponding status bits and flags are set. If the 2X timer is set, the safety timer is extended while the loop is active. Additionally, termination is disabled.

9.3.1.4 Battery Supplement Mode

When the PMID voltage drops below the battery voltage by V_{BSUP1}, the battery supplements the system load. The battery stops supplementing the system load when the voltage on the PMID pin rises above the battery voltage by V_{BSUP2}. During supplement mode, the battery supplement current is not regulated, however, the Battery Over-Current Protection mechanism is active. Battery charge termination is disabled while in supplement mode.

9.3.2 Protection Mechanisms

9.3.2.1 Input Over-Voltage Protection

The input over-voltage protection protects the device and downstream components connected to PMID, and BAT against damage from over-voltage on the input supply. When $V_{IN} > V_{OVP}$ an OVP fault is determined to exist. During the OVP fault, the device turns the input FET off, sends a single 128-µs pulse on $\overline{\text{INT}}$, and the VIN_OVP_FAULT FLAG and STAT bits are updated over I^2C. Once the OVP fault is removed, the STAT bit is cleared and the device returns to normal operation. The FLAG bit is not cleared until it is read through I^2C after the OVP condition no longer exists. The OVP threshold for the device is 5.5 V to allow operation from standard USB sources.

9.3.2.2 Safety Timer and I^2C Watchdog Timer

At the beginning of the charge cycle, the device starts the safety timer. If charging has not terminated before the programmed safety time, t_{MAXCHG}, expires, charging is disabled. The pre-charge safety time, t_{PRECHG}, is 25% of t_{MAXCHG}. When a safety timer fault occurs, a single 128-µs pulse is sent on the $\overline{\text{INT}}$ pin and the SAFETY_TMR_FAULT_FLAG bit in the FLAG3 register is updated over I^2C. The $\overline{\text{CE}}$ pin or input power must be toggled in order to reset the safety timer and exit the fault condition. Note that the flag bit will be reset when the bit is read by the host even if the fault has not been cleared. The safety timer duration is programmable using the SAFETY_TIMER bits. When the safety timer is active, changing the safety timer duration resets the safety timer. The device also contains a 2X_TIMER bit that doubles the timer duration to prevent premature safety timer expiration when the charge current is reduced by VIN DPM, thermal regulation, or a NTC (JEITA) condition. When 2X_TIMER function is enabled, the timer is allowed to run at half speed when any loop is active other than CC or CV.

In addition, the BQ21062 has a 50s watchdog timer which resets after every I^2C transaction. This feature, which is disabled by default, resets all charger parameters registers to their default values when the timer expires.

9.3.2.3 Thermal Protection and Thermal Charge Current Foldback

In order to protect the device from damage due to overheating, the junction temperature of the die, T_J, is monitored. When T_J reaches $T_{SHUTDOWN}$ the device stops operation and is turned off. The device resumes operation when T_J falls below $T_{SHUTDOWN}$ by T_{HYS}.

During the charging process, the device will reduce the charging current at a rate of (0.04 x I_{CHARGE})/°C once T_J exceeds the thermal foldback threshold, T_{REG} to prevent further heating. If the charge current is reduced to 0, the battery supplies the current needed to supply the PMID output. The thermal regulation threshold may be set through I^2C by setting the THERM_REG bits to the desired value.

The die junction temperature, T_J, can be estimated based on the expected board performance using 方程式 1:

$$T_J = T_A + \theta_{JA} \times P_{DISS} \tag{1}$$

Where P_{DISS} is the total power dissipation in the IC. The θ_{JA} is largely driven by the board layout. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*. Under typical conditions, the time spent in this state is very short.

9.3.2.4 Battery Short and Over Current Protection

In order to protect the device from over current and prevent excessive battery discharge current, the BQ21062 detects if the current on the battery FET exceeds I_{BAT_OCP}. If the short circuit limit is reached for the deglitch time (t_{DGL_OCP}), the battery discharge FET is turned off and start operating in hiccup mode, re-enabling the BATFET t_{REC_SC} (250 ms) after being turned off by the over-current condition. If the over-current condition is triggered upon retry for 3 to 7 consecutive times, the BATFET will then remain off until the part is reset or until Vin is connected and valid. If the over-current condition and hiccup operation occurs while in supplement mode where VIN is already present, VIN must be toggled in order for BATFET to be enabled and start another detection cycle.

In the case where the battery is suddenly shorted while charging and VBAT drops below V_{SHORT}, a fast comparator quickly reduces the charge current to $I_{PRECHARGE}$ preventing fast charge current to be momentarily injected to the battery while shorted.

9.3.2.5 PMID Short Circuit

A short on the PMID pin is detected when the PMID voltage drops below 1.6 V (PMID short threshold). PMID short threshold has a 200-mV hysteresis. When this occurs, the input FET temporarily disconnects IN for up to 200 µs to prevent stress on the device if a sudden short condition happens, before allowing a softstart on the PMID output.

9.3.3 VDD LDO

The device integrates a low current always-on LDO that serves as the digital I/O supply to the device. This LDO is supplied by VIN or by BAT. The VDD LDO will remain on through all power states with the exception of Ship Mode.

9.3.4 Load Switch/LDO Output and Control

The device integrates a low Iq load switch which can also be used as a regulated output. The LDO/LS has a dedicated input pin VINLS and can support up to 150 mA of load current.

The LS/LDO may be enabled/disabled through I^2C. The output voltage is programmable using the LS_LDO bits in the registers. To limit voltage drop or voltage transients, a small ceramic capacitor must be placed close to VINLS pin.

表 9-2. LDO Mode Control

I2C EN_LS_LDO	LDO_SWITCH_CONFIG	LS/LDO OUTPUT
0	0	Pulldown
0	1	Pulldown
1	0	LDO
1	1	Load Switch

The current capability of the LDO will depend on the VINLS input voltage and the programmed output voltage. When the LS/LDO output is disabled through the register, an internal pull-down will discharge the output. The LDO has output current limit protection, limiting the output current in the event of a short in the output. When the LDO output current limit trips and is active for at least 1 ms, the device will set a flag and send an interrupt to the host. The host must take action to enable the LDO if desired. The LS/LDO may be set to operate as a LDO by setting the LDO_SWITCH_CONFIG bit to 0. Note that in order to change the configuration, the LS/LDO must be disabled first, then the LDO_SWITCH_CONFIG bit is set for it to take effect. This is not the case when updating the LDO output voltage which can be done on the fly without the need of disabling the LDO first.

9.3.5 PMID Power Control

The BQ21062 offers the option to control PMID through the I^2C PMID_MODE bits. These bits can force PMID to be supplied by BAT instead of IN, even if $V_{IN} > V_{BAT} + V_{SLP}$. They can also disconnect PMID, pulling it down or leaving it floating. See 表 9-30 for details.

9.3.6 System Voltage (PMID) Regulation

The BQ21062 has a regulated system voltage output (PMID) that is programmable through I^2C. PMID regulation is only active when the adapter is connected and $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT}$ _ V_{SLP} and $V_{IN} < V_{OVP}$. In Battery Tracking operation (PMID_REG_CTRL = 000), the PMID voltage will be regulated to about 4.7% over battery level ($V_{PMID} = V_{BAT} \times 1.047$) or 3.8 V, whichever is higher. Note that the PMID regulation target should be set to be at least 200mV higher than V_{BATREG}.

9.3.7 MR Wake and Reset Input

The $\overline{\text{MR}}$ input has three main functions in the BQ21062. First, it serves as a means to wake the device from Ship Mode. Second, it serves as a short button press detector, sending an interrupt to the host when the button driving the $\overline{\text{MR}}$ pin has been pressed for a given period of time. This allows the implementation of different functions in the end application such as menu selection and control. And finally it serves as a means to get the BQ21062 to reset the system by performing a power cycle (shut down PMID and automatically powering it back on) or go to Ship Mode after detecting a long button press. In order for the $\overline{\text{MR}}$ to be functional, the battery voltage V_{BAT} must be above the $V_{BATUVLO}$ level. The timing for the short and long button press duration is programmable through I^2C for added flexibility. Note that if a specific timer duration is changed through I^2C while that timer is active and has not expired, the new programmed value will be ignored until the timer expires and/or is reset by $\overline{\text{MR}}$. The $\overline{\text{MR}}$ input has an internal pull-up to BAT.

9.3.7.1 $\overline{\text{MR}}$ Wake or Short Button Press Functions

There are two programmable wake or short button press timers, WAKE1 and WAKE2. When the $\overline{\text{MR}}$ pin is held low for t_{WAKE1} the device sends an interrupt (128 μs active low pulse in the $\overline{\text{INT}}$ pin) and sets the MRWAKE1_TIMEOUT flag when it expires. If the $\overline{\text{MR}}$ pin continues to be driven low after WAKE1 and the WAKE2 timer expires, the BQ21062 sends a second interrupt and sets the MRWAKE2_TIMOUT flag. WAKE1 is used as the timer to wake the device from ship mode. WAKE2’ s only function is to send the interrupt and has no effect on other BQ21062 functions. These flags are not cleared until they have been read by the host. Note that interrupts are only sent when the flags are set and the flags must be cleared in order for another interrupt to be sent upon $\overline{\text{MR}}$ press. The timer durations can be set through the MR_WAKEx_TIMER bits in the MRCTRL Register section.

One of the main $\overline{\text{MR}}$ functions is to wake the device from Ship Mode when the $\overline{\text{MR}}$ is asserted. The device will exit the Ship Mode when the $\overline{\text{MR}}$ pin is held low for at least t_{WAKE1}. Immediately after the $\overline{\text{MR}}$ is asserted, VDD will be enabled and the digital will start the WAKE counter. If the $\overline{\text{MR}}$ signal remains low until after the WAKE1 timer expires, the device will power up PMID and LDO (If enabled) completing the exit from the ship mode. If the $\overline{\text{MR}}$ signal goes high before the WAKE1 timer expires, the device will go back to the Ship Mode operation, never powering up PMID or the LDO. Note that if the $\overline{\text{MR}}$ pin remains low after exiting Ship Mode the wake interrupts will not be sent and the long button press functions like HW reset will not occur until the $\overline{\text{MR}}$ pin is toggled. In the case where a valid V_{IN} ($V_{IN} > V_{UVLO}$) is connected prior to WAKE2 timer expiring, the device will exit the ship mode immediately regardless of the $\overline{\text{MR}}$ or wake timer state. 图 9-3 and 图 9-4 show these different scenarios.

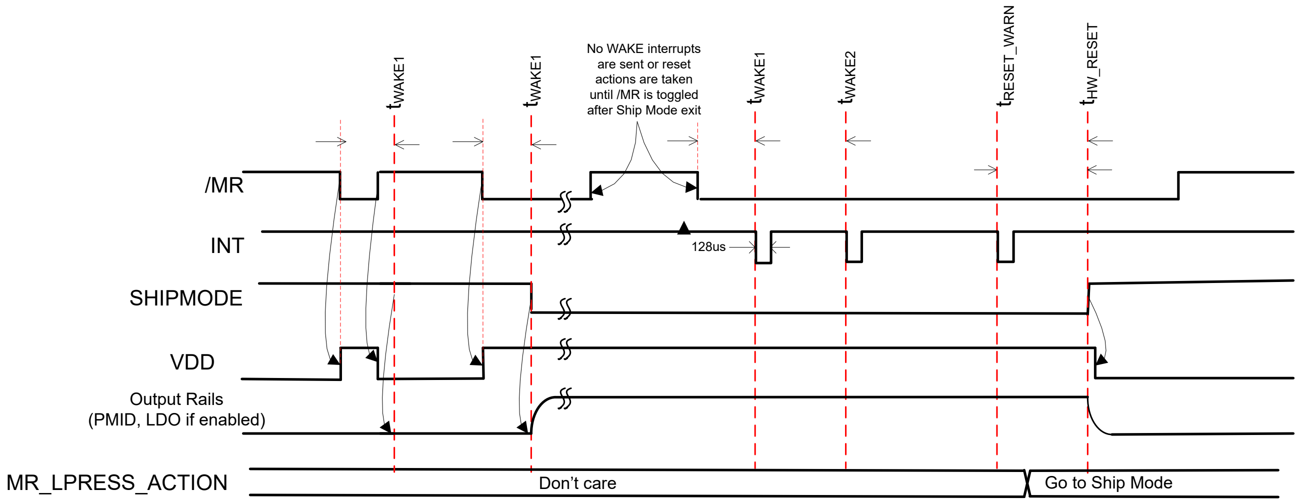


图 9-3. MR Wake from Ship Mode (MR_LPRESS_ACTION = Ship Mode, VIN not valid)

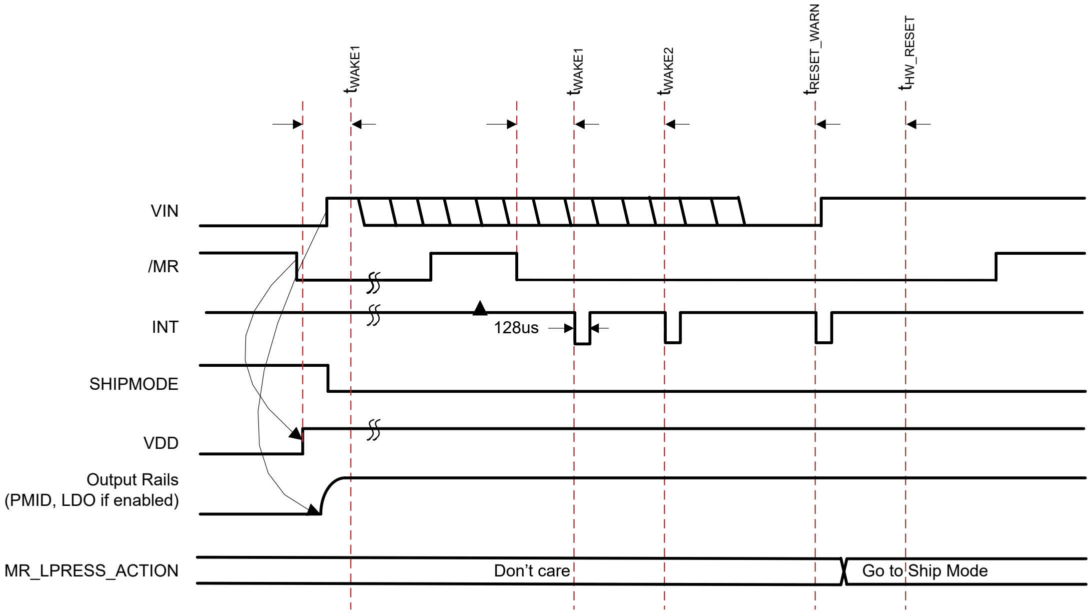


图 9-4. MR Wake from Ship Mode – VIN Dependencies

9.3.7.2 $\overline{\text{MR}}$ Reset or Long Button Press Functions

The BQ21062 device may be configured to perform a system hardware reset (Power Cycle/Autowake), go into Ship Mode, or simply do nothing after a long button press (for example, when the $\overline{\text{MR}}$ pin is driven low until the MR_HW_RESET timer expires).The action taken by the device when the timer expires is configured through the MR_LPRESS_ACTION bits in the ICCTRL1 Register section. Once the MR_HW_RESET timer expires the device immediately performs the operation set by the MR_LPRESS_ACTION bits. The BQ21062 sends an interrupt to the host when the device detects that $\overline{\text{MR}}$ has been pressed for a period that is within t_{RESET_WARN} from reaching t_{HW_RESET}. This may warn the host that the button has been pressed for a period close to t_{HW_RESET} which would trigger a HW Reset or used as another button press timer interrupt like the WAKE1 and WAKE2 timers. This interrupt is sent before the MR_HW_RESET timer expires and sets the MRRESET_WARN flag. The t_{RESET_WARN} may be set through I^{2}C by the MR_RESET_WARN bits in the MRCTRL register. The host may change the reset behavior at any time after $\overline{\text{MR}}$ going low and prior to the MR_HW_RESET timer expiring. It may not change it however from another behavior to a HW reset (Power Cycle/Autowake) since a HW reset can be gated by other condition requirements, such as a valid VIN presence (controlled by MR_RESET_VIN bit), throughout the whole duration of the button press. This flexibility allows the host to abort any reset or power shutdown to the system by overriding a long button press command.

A HW reset may also be started by setting the HW_RESET bit. Note that during a HW reset , VDD remains on.

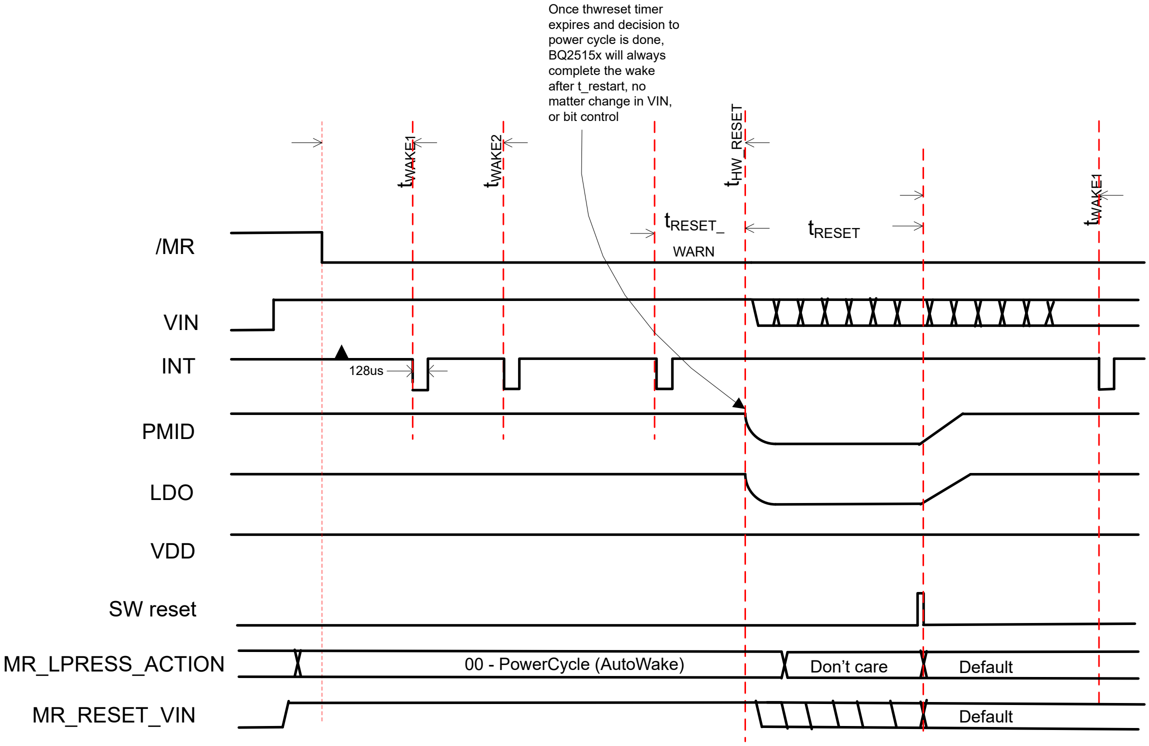


图 9-5. MR Wake and Reset Timing with VIN Present or BAT Active Mode When MR_LPRESS_ACTION = 00

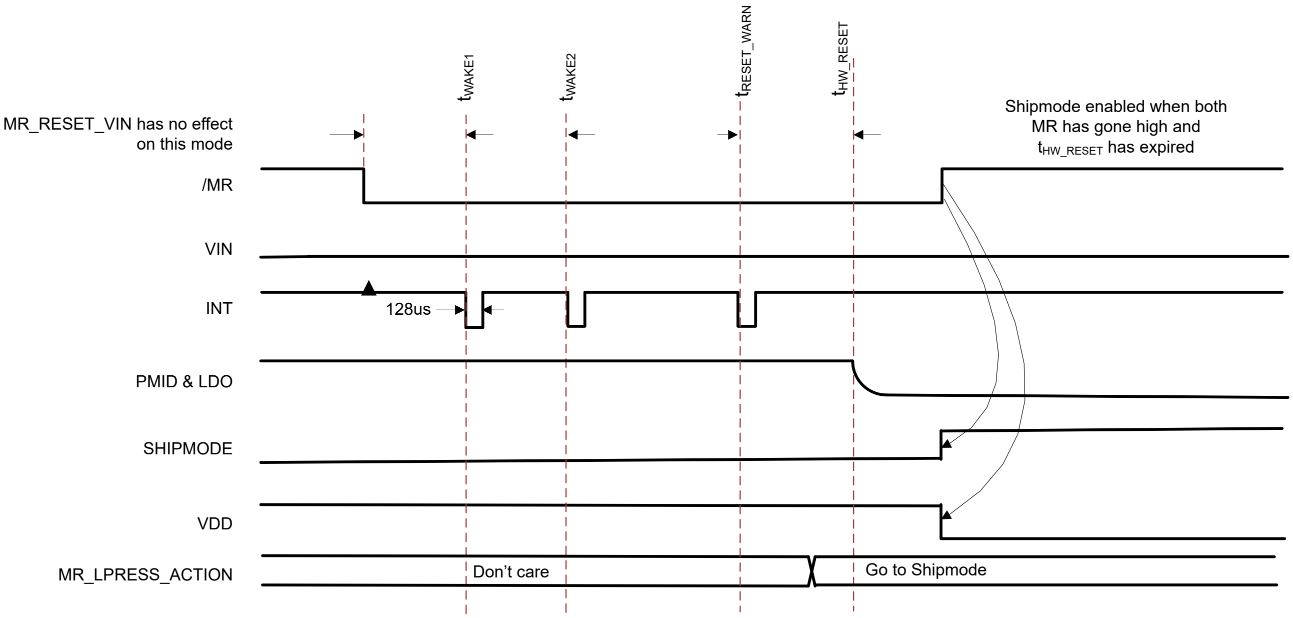


图 9-6. MR Wake and Reset Timing Active Mode When MR_LPRESS_ACTION = 1x (Ship Mode) and Only BAT is Present

9.3.8 14-Second Watchdog for HW Reset

The BQ21062 integrates a 14-second watchdog timer that makes the BQ21062 perform a HW reset/power cycle if no I^2C transaction is detected within 14 seconds of a valid adapter being connected. If the adapter is connected and the host responds with an I^2C transaction before the 14-second watchdog window expires, the part continues in normal operation. The 14-second watchdog is disabled by default and may be enabled through I^2C by setting the HWRESET_14S_WD bit. 图 9-7 shows the basic functionality of this feature.

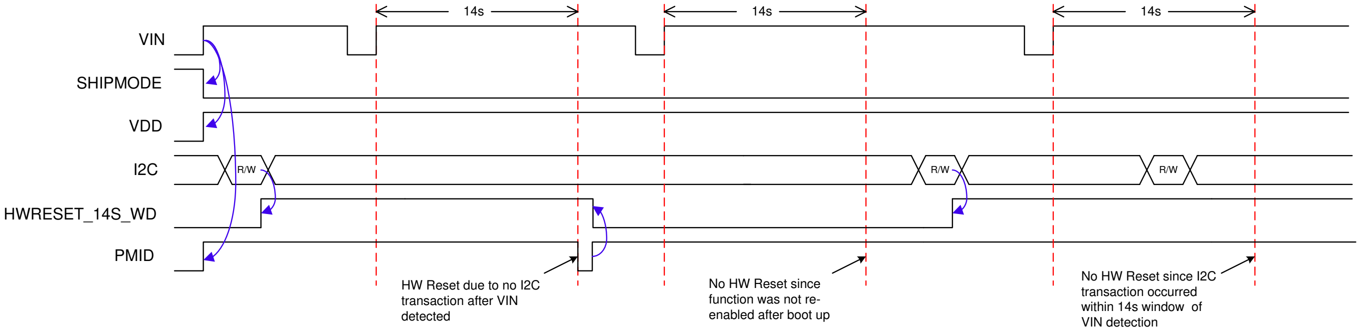


图 9-7. 14-Second Watchdog for HW Reset Behavior

9.3.9 Faults Conditions and Interrupts ($\overline{\text{INT}}$)

The device contains an open-drain output that signals an interrupt and is valid only after the device has completed start-up into a valid state. If the part starts into a fault, interrupts will not be sent. The $\overline{\text{INT}}$ pin is normally in high impedance and is pulled low for 128 μs when an interrupt condition occurs. When a fault or status change occurs or any other condition that generates an interrupt such as CHARGE_DONE, a 128-μs pulse (interrupt) is sent on $\overline{\text{INT}}$ to notify the host. All interrupts may be masked through I^2C. If the interrupt condition occurs while the interrupt is masked an interrupt pulse will not be sent. If the interrupt is unmasked while the fault condition is still present, an interrupt pulse will not be sent until the $\overline{\text{INT}}$ trigger condition occurs while unmasked.

9.3.9.1 Flags and Fault Condition Response

表 9-3 below details the BQ21062 behavior when a fault condition occurs.

表 9-3. Interrupt Triggers and Fault Condition Response

FAULT / FLAG	DESCRIPTION	INTERRUPT TRIGGER BASED ON STATUS BIT CHANGE	CHARGER BEHAVIOR	CHARGER SAFETY TIMER	PMID BEHAVIOR
CHRG_CV_FLAG	Set when charger enters Constant Voltage operation	Rising Edge	Enabled	No effect	IN powered if V_{IN} is valid
CHARGE_DONE_FLAG	Set when charger reaches termination	Rising Edge	Paused- Charging resumes with VIN or $\overline{\text{CE}}$ toggle or when V_{RCH} is reached	Reset	IN powered if V_{IN} is valid
IINLIM_ACTIVE_FLAG	Set when Input Current Limit loop is active	Rising Edge	Enabled. Reduced charge current.	Doubled if option is enabled	IN powered VIN powered unless supplement mode condition is met.
VINDPM_ACTIVE_FLAG	Set when VINDPM loop is active	Rising Edge	Enabled. Reduced charge current.	Doubled if option is enabled	VIN powered unless supplement mode condition is met.

表 9-3. Interrupt Triggers and Fault Condition Response (continued)

FAULT / FLAG	DESCRIPTION	INTERRUPT TRIGGER BASED ON STATUS BIT CHANGE	CHARGER BEHAVIOR	CHARGER SAFETY TIMER	PMID BEHAVIOR
THERMREG_ACTIVE	Set when Thermal Charge Current Foldback (Thermal Regulation) loop is active	Rising Edge	Enabled. Reduced charge current.	Doubled if option is enabled	VIN powered unless supplement mode condition is met.
VIN_PGOOD_FLAG	Set when VIN changes PGOOD status	Rising and Falling Edge	If VIN_PGOOD_STAT is low, charging is disabled.	Reset	VIN powered (if VIN_PGOOD_STAT =1) unless PMID_MODE is not 00.
VIN_OVP_FAULT_FLAG	Set when $V_{IN} > V_{OVP}$	Rising Edge	Charging is paused until condition disappears	Reset	BAT powered
BAT_OCP_FAULT_FLAG	Set when $I_{BAT} > I_{BATOCP}$	Rising Edge	Disabled (BAT only condition)	N/A	Disconnect BAT
BAT_UVLO_FAULT_FLAG	Set when $V_{BAT} < V_{BATUVLO}$	Rising Edge	Enabled	No effect	IN powered of V_{IN} is valid
TS_COLD_FLAG	Set when $V_{TS} > V_{TS\_COLD}$	Rising Edge	Charging paused until condition is cleared	Paused	IN powered of V_{IN} is valid
TS_COOL_FLAG	Set when $V_{TS\_COLD} > V_{TS} > V_{TS\_COOL}$	Rising Edge	Enabled. Reduced charge current.	Doubled if option is enabled	IN powered of V_{IN} is valid
TS_WARM_FLAG	Set when $V_{TS\_HOT} < V_{TS} < V_{TS\_WARM}$	Rising Edge	Enabled. Reduce battery regulation voltage.	No effect	IN powered of V_{IN} is valid
TS_HOT_FLAG	Set when $V_{TS} < V_{HOT}$	Rising Edge	Charging paused until condition is cleared	Paused	IN powered of V_{IN} is valid
TS_OPEN_FLAG	Set when $V_{TS} > V_{TS\_OPEN}$	Rising Edge	Charging is paused until condition disappears	Paused	N/A
WD_FAULT_FLAG	Set when I^2C watchdog timer expires	Rising Edge	Enabled	N/A	N/A
SAFETY_TMR_FAULT_FLAG	Set when safety Timer expires. Cleared after VIN or $\overline{CE}$ toggle	Rising Edge	Disabled until VIN or $\overline{CE}$ toggle	Reset after flag is cleared	IN powered of V_{IN} is valid
LS_LDO_OCP_FAULT_FLAG	Set when LDO output current exceeds OCP condition	Rising Edge	N/A	N/A	N/A
MRWAKE1_TIMEOUT_FLAG	Set when $\overline{MR}$ is low for at least t_{WAKE1}	Rising Edge	N/A	N/A	N/A
MRWAKE2_TIMEOUT_FLAG	Set when $\overline{MR}$ is low for at least t_{WAKE2}	Rising Edge	N/A	N/A	N/A
MRRESET_WARN_FLAG	Set when $\overline{MR}$ is low for at least $t_{RESETWARN}$	Rising Edge	N/A	N/A	N/A
TSHUT	No flag. Die temperature exceeds thermal shutdown threshold is reached	N/A	Disabled	Disabled	Disabled

9.3.10 Power Good ($\overline{PG}$) Pin

The $\overline{PG}$ pin is an open-drain output that by default indicates when a valid IN supply is present. It may also be configured to be a general purpose output (GPO) controlled through I^2C or to be a level shifted version of the

$\overline{\text{MR}}$ input signal. Connect $\overline{\text{PG}}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication. See 表 9-30 for details.

9.3.11 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the device provides a flexible voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The TS pin is not biased continuously, instead it is biased only when the voltage at the pin is being sampled (for about 25ms in 225ms intervals when VIN is present. Note that the TS biasing cannot be disabled when VIN is present.

The part can be configured to meet JEITA requirements or a simpler HOT/COLD function only. Additionally, the TS charger control function can be disabled. To satisfy the JEITA requirements, four temperature thresholds are monitored: the cold battery threshold, the cool battery threshold, the warm battery threshold, and the hot battery threshold. These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{COOL} < V_{TS} < V_{COLD}$, the charging current is reduced to the value programmed in the TS_FASTCHGCTRL register. Note that the current steps for fast charge in the COOL region, just as those in normal fast charge, are multiples of the fast charge LSB value (1.25 mA by default). So in the case where the calculated scaled down current for the COOL region falls in between charge current steps, the device will round down the charge current to the nearest step. For example, if the fast charge current is set for 15 mA (ICHG = 1100) and TS_FASTCHARGE =111 (0.125*ICHG), the charge current in the COOL region will be 1.25 mA instead of the calculated 1.85 mA.

When $V_{HOT} < V_{TS} < V_{WARM}$, the battery regulation voltage is reduced to the value programmed in the TS_FASTCHGCTRL register.

Regardless of whether the part is configured for JEITA, HOT/COLD, or disabled, when a TS fault occurs, a 128-μs pulse is sent on the INT output, and the FAULT bits of the register are updated over I^2C. The FAULT bits are not cleared until they are read over I^2C. This allows the host processor to take action if a different behavior than the pre-set function is needed. Alternately, the TS pin voltage can be read by the host if VIN is present or when BAT is present, so the appropriate action can be taken by the host.

When in Battery only mode, a reading of the TS pin can be triggered to check for any TS faults. This is done by setting the TS_FAULT_MEAS register (0x58) to 0x04 which sets the TS_FAULT_MEAS_ENABLE bit. The interval of the /INT interrupt can be configured in TS_READ Register to either be a manual read or every second in the INTERVAL bit. When configured to manual read, the fault read will have to be iniated by setting the GET_FAULT_ENABLE bit which will automatically enable the I_{TS_BIAS} current on TS.

9.3.11.1 TS Thresholds

The BQ21062 monitors the TS voltage and sends an interrupt to the host whenever it crosses the V_{HOT}, V_{WARM}, V_{COOL} and V_{COLD} thresholds which correspond to different temperature thresholds based on the NTC resistance and biasing. These thresholds may be adjusted through I^2C by the host. The device will also disable charging if TS pin exceeds the V_{TS_OPEN} threshold.

The TS biasing circuit is shown in 图 9-8. Note that the respective V_{TS} for T_{COLD} (0°C), T_{COOL} (10°C), T_{WARM} (45°C) and T_{HOT} (60°C) changes for every NTC, therefore the threshold values may need to be adjusted through I^2C based on the supported NTC type.

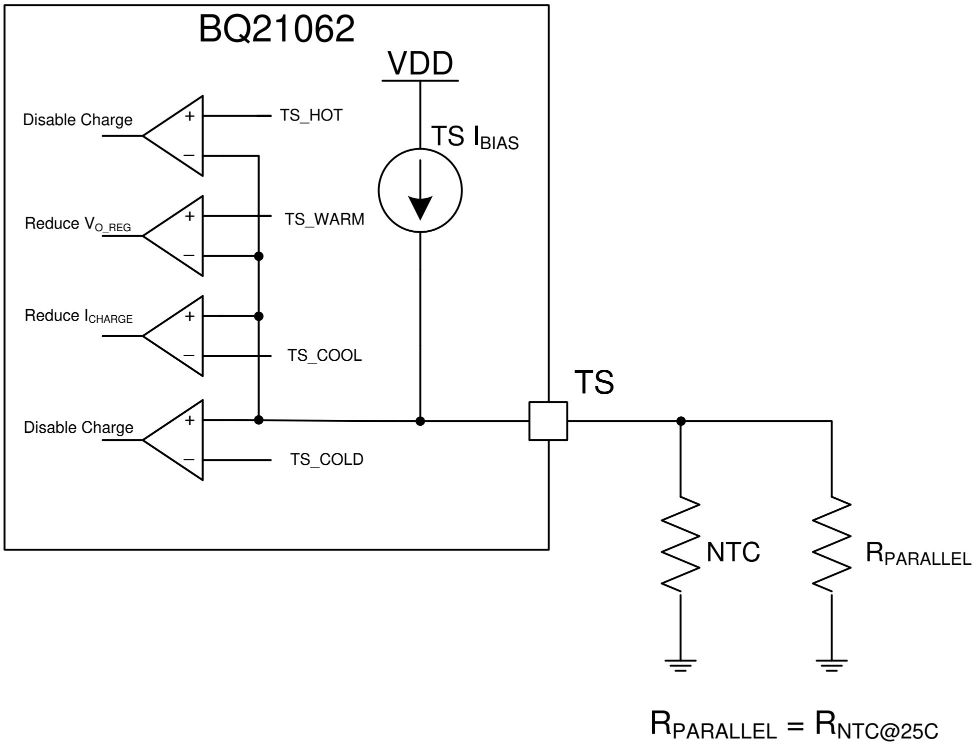


图 9-8. TS Bias Functional Diagram

The BQ21062 supports by default the following thresholds for a 10-KΩ NTC.

表 9-4. TS Thresholds for 10-KΩ Thermistor with 3380 B-Constant

THRESHOLD	TEMPERATURE (°C)	VTS (V)
Open	--	>0.9
Cold	0	0.585
Cool	10	0.514
Warm	45(1)	0.265
Hot	45(1)	0.265

(1) When V_{HOT} is set to the same or higher voltage level as V_{WARM}, the WARM region is overwitten by HOT region functionality (charge is disabled).

9.3.12 I²C Interface

The BQ21062 device uses a fully compliant I²C interface to program and read control parameters, status bits, and so on. I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a micro-controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The BQ21062 works as a slave and supports the following data transfer modes, as defined in the I²C Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charge solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements.

Register contents remain intact as long as VBAT or VIN voltages remains above their respective UVLO levels.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The BQ21062 device 7-bit address is 0×6B (shifted 8-bit address is 0xD6).

9.3.12.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in 图 9-9. All I^{2}C-compatible devices should recognize a start condition.

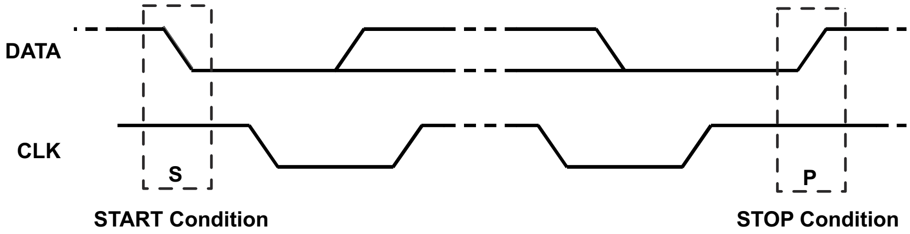


图 9-9. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see 图 9-10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 图 9-11) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

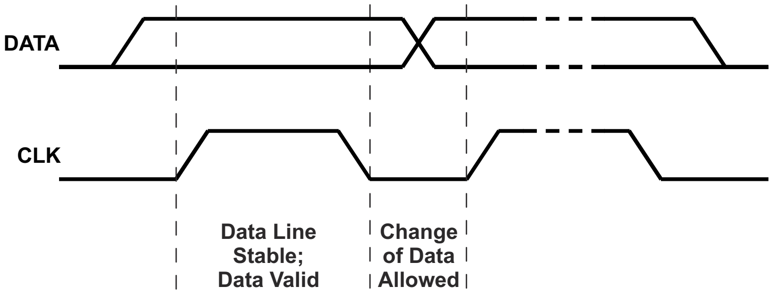


图 9-10. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 图 9-9). This releases the bus and stops the communication link with the addressed slave. All I^{2}C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs to send a STOP condition to prevent the slave I^{2}C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section will result in FFh being read out.

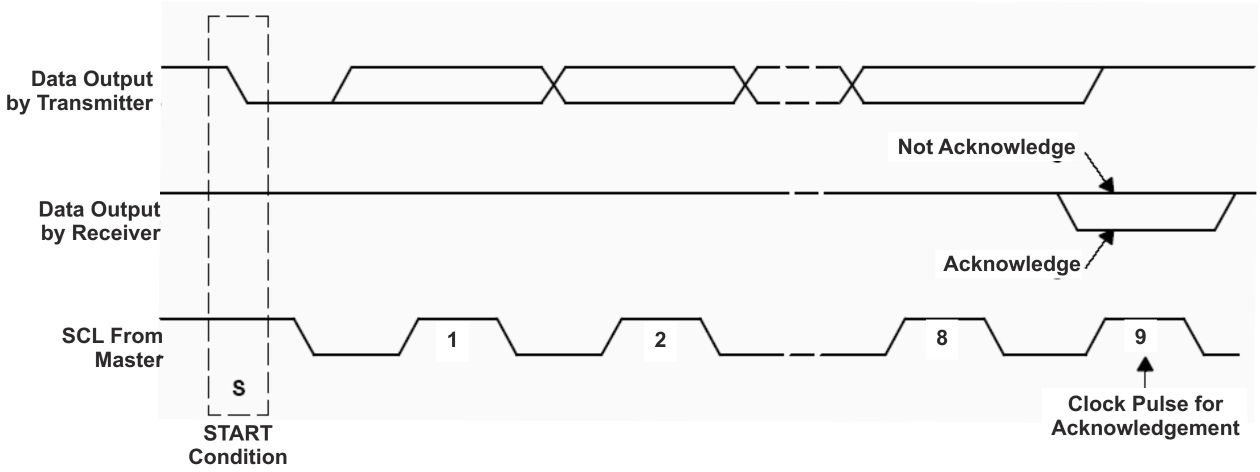


图 9-11. Acknowledge on the I²C Bus

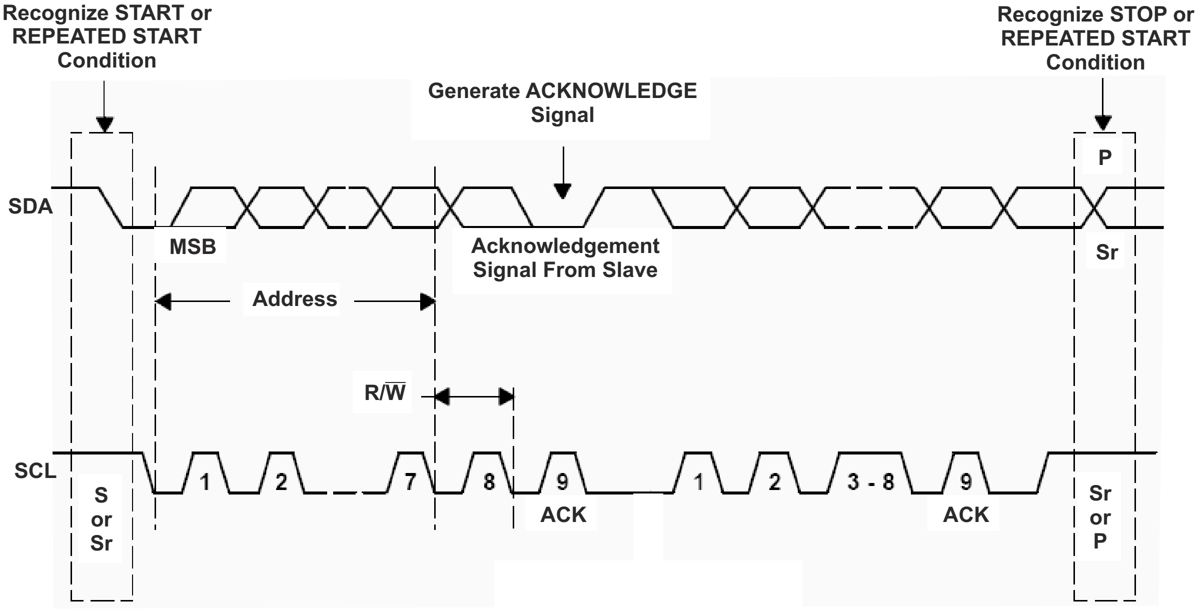


图 9-12. Bus Protocol

9.4 Device Functional Modes

The BQ21062 has four main modes of operation: Active Battery Mode, Low Power Mode and Ship Mode which are battery only modes and Charge/Adapter Mode when a supply is connected to IN. 表 9-5 below summarizes the functions that are active for each operation mode. Each mode is discussed in further detail in the following sections in addition to the device's power-up/down sequences.

表 9-5. Function Availability Based on Primary Mode of Operation

FUNCTION	CHARGE/ ADAPTER MODE	SHIP MODE	LOW POWER MODE	ACTIVE BATTERY MODE
VOVP	Yes	No	Yes	Yes
VUVLO	Yes	Yes	Yes	Yes
BATOCP	Yes	No	No	Yes
BATUVLO	Yes	No	Yes	Yes
VINDPM	If enabled	No	No	No
VDD	Yes	No	Yes	Yes
LS/LDO	Yes	No	If enabled	If enabled
BATFET	Yes	No	Yes	Yes
TS Measurement	Yes	No	No	If enabled
Battery Changing	If enabled	No	No	No
ILIM	Yes (Register Value)	No	No	No
$\overline{\text{MR}}$ input	Yes	Yes	Yes	Yes
$\overline{\text{LP}}$ input	No	No	Yes	Yes
$\overline{\text{INT}}$ output	Yes	No	No	Yes
I^2C	Yes	No	No	Yes
$\overline{\text{CE}}$ input	Yes	No	No	No

9.4.1 Ship Mode

Ship Mode is the lowest quiescent current state for the device. Ship Mode latches off the device and BAT FET until $V_{IN} > V_{UVLO}$ or the $\overline{\text{MR}}$ button is depressed for t_{WAKE1} and released. Ship mode can be entered regardless of the state of $\overline{\text{CE}}$. The device will also enter Ship Mode upon battery insertion when no valid VIN is present. If the EN_SHIPMODE is written to a 1 while a valid input supply is connected, the device will wait until the IN supply is removed to enter ship mode. If the $\overline{\text{MR}}$ pin is held low when the EN_SHIPMODE bit is set, the device will wait until the $\overline{\text{MR}}$ pin goes high before entering Ship Mode. 图 9-13 shows this behavior. The battery voltage must be above the maximum programmable $V_{BATUVLO}$ threshold in order to exit Ship Mode with $\overline{\text{MR}}$ press. The EN_SHIPMODE bit can be cleared using the I^2C interface while the VIN input is valid. The EN_SHIPMODE bit is not cleared upon the I^2C watchdog expiring, this means that if watchdog timer fault occurs while the EN_SHIPMODE bit is set and the device is waiting to go into Ship Mode because V_{IN} is present or $\overline{\text{MR}}$ is low, the device will still proceed to go into Ship Mode once those conditions are cleared.

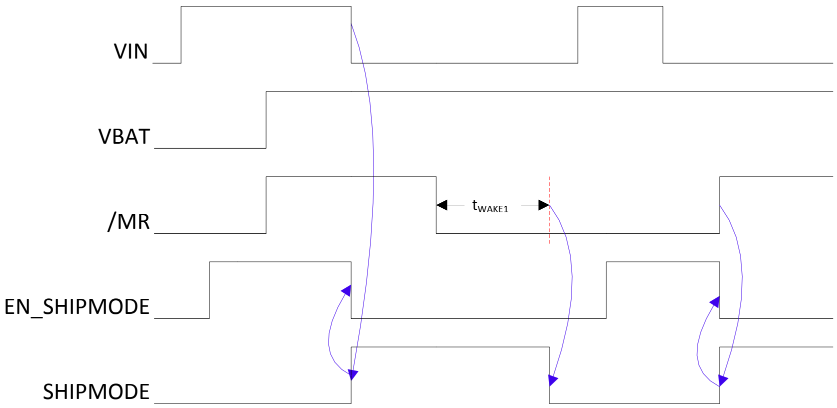


图 9-13. Ship Mode Entry Based On EN_SHIPMODE Bit

9.4.2 Low Power

Low Power mode is a low quiescent current state while operating from the battery. The device will operate in low power mode when the $\overline{\text{LP}}$ pin is set low, $V_{IN} < V_{UVLO}$, $\overline{\text{MR}}$ pin is high and all I^2C transactions and interrupts that started while in the Active Battery or Charging Modes have been completed and sent. During LP mode the VDD output is powered by BAT, the $\overline{\text{MR}}$ inputs are active and the I^2C is disabled. All other circuits, such as oscillators, are in a low power or off state. The LS/LDO outputs will remain in the state set by the EN_LS_LDO bit prior to entering Low Power Mode. The device exits LP Mode when the $\overline{\text{LP}}$ pin is set high or $V_{IN} > V_{UVLO}$.

In the case that a faulty adapter with $V_{IN} > V_{OVP}$ is connected to the device while $\overline{\text{LP}}$ pin is low, the device will be powered from the battery, but will operate in Active battery mode instead of Low Power mode regardless of the $\overline{\text{LP}}$ pin state.

When $\overline{\text{MR}}$ is held low while $\overline{\text{LP}}$ is low, the device will enter Active Battery Mode, this allows for the internal clocks of the device to be running and allow the $\overline{\text{MR}}$ long button press HW reset. I^2C operation is also possible during this condition. Note that as soon as the $\overline{\text{MR}}$ input is released and goes high, the device will go back to LP Mode tuning off all clocks. Note that if a HW reset has occurred while $\overline{\text{LP}}$ is low, $\overline{\text{MR}}$ must remain low until the power cycle has completed (PMID and LDO enable) to allow completion of the power up sequence.

9.4.3 Active Battery

When the device is out of Ship Mode and battery is above $V_{BATUVLO}$ with no valid input source, the battery discharge FET is turned on connecting PMID to the battery. The current flowing from BAT to PMID is not regulated, but it is monitored by the battery over-current protection (OCP) circuitry. If the battery discharge current exceed the OCP threshold, the battery discharge FET will be turned off as detailed in 节 9.3.2.4.

If only battery is connected and the battery voltage goes below $V_{BATUVLO}$, the battery discharge FET is turned off. To provide designers the most flexibility in optimizing their system, an adjustable BATUVLO is provided. Deeper discharge of the battery enables longer times between charging, but may shorten the battery life. The BATUVLO is adjustable with a fixed 150-mV hysteresis.

9.4.4 Charger/Adapter Mode

This mode is active when $V_{IN} > V_{UVLO}$. If the supply at IN is valid and above the V_{IN_DPM} level, PMID will be powered by the supply connected to IN. The device will charge the battery, if charging is enabled, until termination has occurred.

9.4.5 Power-Up/Down Sequencing

The power-up and power-down sequences for the BQ21062 are shown below. Upon V_{IN} insertion, VIN> V_{UVLO}, the device wakes up, powering the VDD rail. If $V_{IN} > V_{BAT} + V_{SLP}$ and $V_{IN} < V_{OVP}$, PMID will be powered by VIN and if $V_{IN} > V_{IN\_DPM}$ charging will start if enabled.

In the case where $V_{IN} < V_{UVLO}$ and the battery is inserted ($V_{BAT} > V_{BATUVLO}$), the device will immediately enter Ship Mode unless $\overline{\text{MR}}$ is held low. Upon battery insertion the VDD rail will come up to allow the device to check the $\overline{MR}$ state and if $\overline{MR}$ is high VDD will immediately be disabled and the device will enter Ship Mode. If $\overline{MR}$ is low, the device will start the WAKE timer and power up PMID and other rails if $\overline{MR}$ is held low for longer than t_{WAKE1}.

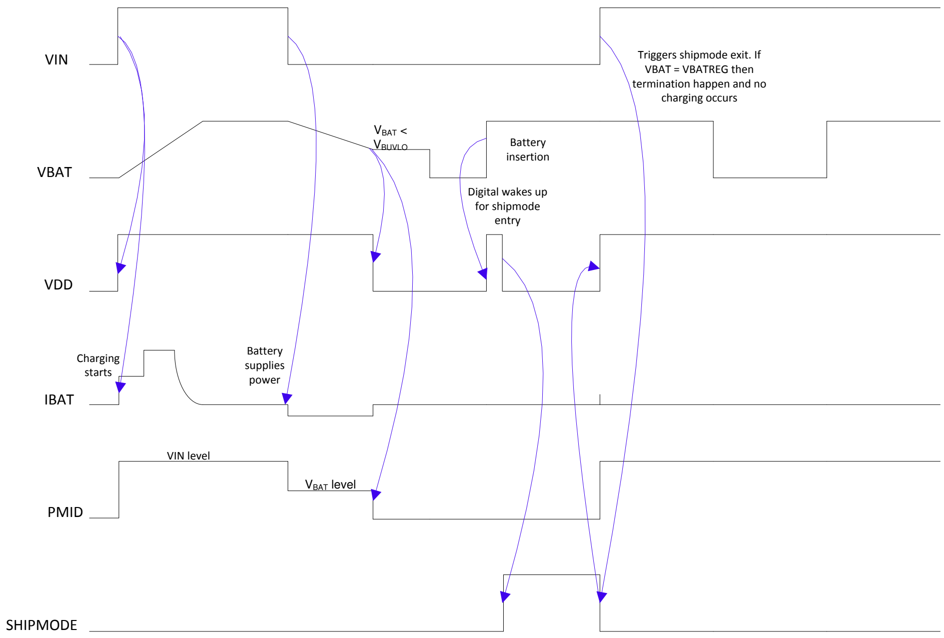


图 9-14. BQ21062 Wake-Up Upon Supply Insertion

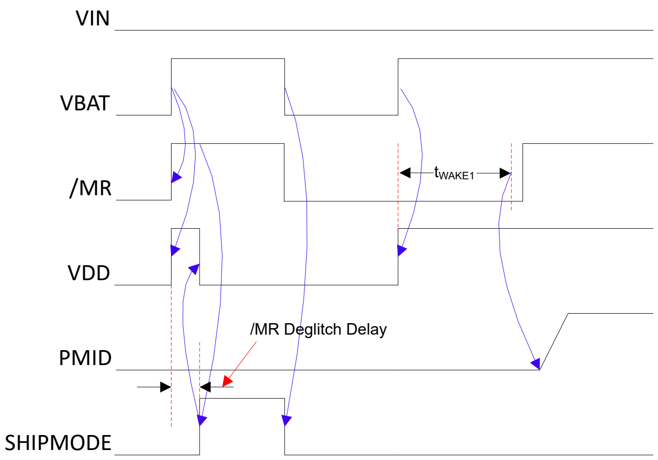


图 9-15. BQ21062 Wake-Up Upon Battery Insertion

9.5 Register Map

The device 7-bit address I^2C is 0x6B (shifted 8-bit address is 0xD6).

9.5.1 I^2C Registers

表 9-6 lists the memory-mapped registers for the I^2C registers. All register offset addresses not listed in 表 9-6 should be considered as reserved locations and the register contents should not be modified.

表 9-6. I^2C Registers

Address	Acronym	Register Name	Section
0x0	STAT0	Charger Status 0	Go
0x1	STAT1	Charger Status 1	Go
0x2	STAT2	Status 2	Go
0x3	FLAG0	Charger Flags 0	Go
0x4	FLAG1	Charger Flags 1	Go
0x5	FLAG2	Flags 2	Go
0x6	FLAG3	Timer Flags	Go
0x7	MASK0	Interrupt Masks 0	Go
0x8	MASK1	Interrupt Masks 1	Go
0x9	MASK2	Interrupt Masks 2	Go
0xA	MASK3	Interrupt Masks 3	Go
0x12	VBAT_CTRL	Battery Voltage Control	Go
0x13	ICHG_CTRL	Fast Charge Current Control	Go
0x14	PCHRGCTRL	Pre-Charge Current Control	Go
0x15	TERMCTRL	Termination Current Control	Go
0x16	BUVLO	Battery UVLO and Current Limit Control	Go
0x17	CHARGERCTRL0	Charger Control 0	Go
0x18	CHARGERCTRL1	Charger Control 1	Go
0x19	ILIMCTRL	Input Corrent Limit Control	Go
0x1D	LDOCTRL	LDO Control	Go
0x30	MRCTRL	MR Control	Go
0x35	ICCTRL0	IC Control 0	Go
0x36	ICCTRL1	IC Control 1	Go
0x37	ICCTRL2	IC Control 2	Go
0x40	TS_READ	TS Read	Go
0x58	TS_FAULT_MEAS	TS Fault Measurement	Go
0x61	TS_FASTCHGCTRL	TS Charge Control	Go
0x62	TS_COLD	TS Cold Threshold	Go
0x63	TS_COOL	TS Cool Threshold	Go
0x64	TS_WARM	TS Warm Threshold	Go
0x65	TS_HOT	TS Hot Threshold	Go
0x6F	DEVICE_ID	Device ID	Go

Complex bit access types are encoded to fit into small table cells. 表 9-7 shows the codes that are used for access types in this section.

表 9-7. I^2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	C R	to Clear Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

9.5.1.1 STAT0 Register (Address = 0x0) [reset = X]

STAT0 is shown in 图 9-16 and described in 表 9-8.

Return to Summary Table.

图 9-16. STAT0 Register

7	6	5	4	3	2	1	0
RESERVED	CHRG_CV_STAT	CHARGE_DONE_STAT	IINLIM_ACTIVE_STAT	RESERVED	VINDPM_ACTIVE_STAT	THERMREG_ACTIVE_STAT	VIN_PGOOD_STAT
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

表 9-8. STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	Reserved
6	CHRG_CV_STAT	R	X	Constant Voltage Charging Mode (Taper Mode) Status 1b0 = Not Active 1b1 = Active
5	CHARGE_DONE_STAT	R	X	Charge Done Status 1b0 = Not Active 1b1 = Active
4	IINLIM_ACTIVE_STAT	R	X	Input Current Limit Status 1b0 = Not Active 1b1 = Active
3	RESERVED	R	X	Reserved
2	VINDPM_ACTIVE_STAT	R	X	VINDPM Status 1b0 = Not Active 1b1 = Active
1	THERMREG_ACTIVE_STAT	R	X	Thermal Regulation Status 1b0 = Not Active 1b1 = Active
0	VIN_PGOOD_STAT	R	X	VIN Power Good Status . 1b0 = Not Good 1b1 = $V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{SLP}$ and $V_{IN} < V_{OVP}$

9.5.1.2 STAT1 Register (Address = 0x1) [reset = X]

STAT1 is shown in 图 9-17 and described in 表 9-9.

Return to Summary Table.

图 9-17. STAT1 Register

7	6	5	4	3	2	1	0
VIN_OVP_FAULT_STAT	RESERVED	BAT_OCP_FAULT_STAT	BAT_UVLO_FAULT_STAT	TS_COLD_STAT	TS_COOL_STAT	TS_WARM_STAT	TS_HOT_STAT
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

表 9-9. STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVP_FAULT_STAT	R	X	VIN Overvoltage Status 1b0 = Not Active 1b1 = Active
6	RESERVED	R	X	Reserved
5	BAT_OCP_FAULT_STAT	R	X	Battery Over-Current Protection Status 1b0 = Not Active 1b1 = Active
4	BAT_UVLO_FAULT_STAT	R	X	Battery voltage below BATUVLO Level Status 1b0 = $V_{BAT} > V_{BATUVLO}$ 1b1 = $V_{BAT} < V_{BATUVLO}$
3	TS_COLD_STAT	R	X	TS Cold Status - $V_{TS} > V_{COLD}$ (charging suspended) 1b0 = Not Active 1b1 = Active
2	TS_COOL_STAT	R	X	TS Cool Status - $V_{COOL} < V_{TS} < V_{COLD}$ (charging current reduced by value set by TS_Registers) 1b0 = Not Active 1b1 = Active
1	TS_WARM_STAT	R	X	TS Warm - $V_{WARM} > V_{TS} > V_{HOT}$ (charging voltage reduced by value set by TS_Registers) 1b0 = Not Active 1b1 = Active
0	TS_HOT_STAT	R	X	TS Hot Status - $V_{TS} < V_{HOT}$ (charging suspended) 1b0 = Not Active 1b1 = Active

9.5.1.3 STAT2 Register (Address = 0x2) [reset = X]

STAT2 is shown in 图 9-18 and described in 表 9-10.

Return to Summary Table.

图 9-18. STAT2 Register

7	6	5	4	3	2	1	0
RESERVED							TS_OPEN_STAT
R-X	R-X	R-X	R-X		R-X		R-X

表 9-10. STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	Reserved
3-1	RESERVED	R	X	Reserved

表 9-10. STAT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_OPEN_STAT	R	X	TS Open Status 1b0 = $V_{TS} < V_{OPEN}$ 1b1 = $V_{TS} > V_{OPEN}$

9.5.1.4 FLAG0 Register (Address = 0x3) [reset = 0x0]

FLAG0 is shown in 图 9-19 and described in 表 9-11.

Return to Summary Table.

Clear on Read

图 9-19. FLAG0 Register

7	6	5	4	3	2	1	0
RESERVED	CHRG_CV_FLAG	CHARGE_DONE_FLAG	IINLIM_ACTIVE_FLAG	RESERVED	VINDPM_ACTIVE_FLAG	THERMREG_ACTIVE_FLAG	VIN_PGOOD_FLAG
RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0

表 9-11. FLAG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	1b0	Reserved
6	CHRG_CV_FLAG	RC	1b0	Constant Voltage Charging Mode (Taper Mode) Flag 1b0 = CV Mode Entry not detected 1b1 = CV Mode Entry detected
5	CHARGE_DONE_FLAG	RC	1b0	Charge Done Flag 1b0 = Charge Done (Termination) not detected 1b1 = Charge Done (Termination) detected
4	IINLIM_ACTIVE_FLAG	RC	1b0	Input Current Limit Flag 1b0 = Input Current Limit not detected 1b1 = Input Current Limit detected
3	RESERVED	RC	1b0	Reserved
2	VINDPM_ACTIVE_FLAG	RC	1b0	VINDPM Flag 1b0 = VINDPM operation not detected 1b1 = VIINDPM operation detected
1	THERMREG_ACTIVE_FLAG	RC	1b0	Thermal Regulation Flag 1b0 = Thermal Regulation not detected 1b1 = Thermal Regulation detected
0	VIN_PGOOD_FLAG	RC	1b0	VIN Power Good Flag . Interrupt will not be sent if device powers up with VIN_PGOOD condition and $V_{BAT} < V_{BATUVLO}$ 1b0 = No change in VIN Power Good Status 1b1 = Change in VIN Power Good Status detected.

9.5.1.5 FLAG1 Register (Address = 0x4) [reset = 0x0]

FLAG1 is shown in 图 9-20 and described in 表 9-12.

Return to Summary Table.

Clear on Read

图 9-20. FLAG1 Register

7	6	5	4	3	2	1	0

图 9-20. FLAG1 Register (continued)

VIN_OVP_FAULT_FLAG	RESERVED	BAT_OCP_FAULT_FLAG	BAT_UVLO_FAULT_FLAG	TS_COLD_FLAG	TS_COOL_FLAG	TS_WARM_FLAG	TS_HOT_FLAG
RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0

表 9-12. FLAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVP_FAULT_FLAG	RC	1b0	VIN Over Voltage Fault Flag 1b0 = No overvoltage condition detected 1b1 = VIN overvoltage condition detected
6	RESERVED	RC	1b0	Reserved
5	BAT_OCP_FAULT_FLAG	RC	1b0	Battery Over Current Protection Flag 1b0 = No Battery Over Current condition detected 1b1 = Battery Over Current condition detected
4	BAT_UVLO_FAULT_FLAG	RC	1b0	Battery Under Voltage Flag 1b0 = Battery below BATUVLO condition detected 1b1 = No Battery below BATUVLO condition detected
3	TS_COLD_FLAG	RC	1b0	TS Cold Region Entry Flag 1b0 = TS Cold Region Entry not detected 1b1 = TS Cold Region Entry detected
2	TS_COOL_FLAG	RC	1b0	TS Cool Region Entry Flag 1b0 = TS Cool Region Entry not detected 1b1 = TS Co0l Region Entry detected
1	TS_WARM_FLAG	RC	1b0	TS Warm Region Entry Flag 1b0 = TS Warm Region Entry not detected 1b1 = TS Warm Region Entry detected
0	TS_HOT_FLAG	RC	1b0	TS Hot Region Entry Flag 1b0 = TS Hot Region Entry not detected 1b1 = TS Hot Region Entry detected

9.5.1.6 FLAG2 Register (Address = 0x5) [reset = 0x0]

FLAG2 is shown in 图 9-21 and described in 表 9-13.

Return to Summary Table.

Clear on Read

图 9-21. FLAG2 Register

7	6	5	4	3	2	1	0
RESERVED							TS_OPEN_FLAG
RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-3b000			RC-1b0

表 9-13. FLAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	X	Reserved
3-1	RESERVED	RC	3b000	Reserved
0	TS_OPEN_FLAG	RC	1b0	TS Open Flag 1b0 = No TS Open fault detected 1b1 = TS Open fault detected

9.5.1.7 FLAG3 Register (Address = 0x6) [reset = 0x0]

FLAG3 is shown in 图 9-22 and described in 表 9-14.

Return to Summary Table.

Clear on Read

图 9-22. FLAG3 Register

7	6	5	4	3	2	1	0
RESERVED	WD_FAULT_FLAG	SAFETY_TMR_FAULT_FLAG	LDO_OCP_FAULT_FLAG	RESERVED	MRWAKE1_TIMEOUT_FLAG	MRWAKE2_TIMEOUT_FLAG	MRRESET_WARN_FLAG
RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0	RC-1b0

表 9-14. FLAG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	1b0	Reserved
6	WD_FAULT_FLAG	RC	1b0	Watchdog Fault Flag 1b0 = Watchdog Timer not expired 1b1 = Watchdog Timer expired
5	SAFETY_TMR_FAULT_FLAG	RC	1b0	Safety Timer Fault Flag 1b0 = Safety Timer not expired 1b1 = Safety Timer Expired
4	LDO_OCP_FAULT_FLAG	RC	1b0	LDO Over Current Fault 1b0 = LDO Normal 1b1 = LDO Over current fault detected
2	MRWAKE1_TIMEOUT_FLAG	RC	1b0	MR Wake 1 Timer Flag 1b0 = MR Wake 1 timer not expired 1b1 = MR Wake 1 timer expired
1	MRWAKE2_TIMEOUT_FLAG	RC	1b0	MR Wake 2 Timer Flag 1b0 = MR Wake 2 timer not expired 1b1 = MR Wake 2 timer expired
0	MRRESET_WARN_FLAG	RC	1b0	MR Reset Warn Timer Flag 1b0 = MR Reset Warn timer not expired 1b1 = MR Reset Warn timer expired

9.5.1.8 MASK0 Register (Address = 0x7) [reset = 0x0]

MASK0 is shown in 图 9-23 and described in 表 9-15.

Return to Summary Table.

图 9-23. MASK0 Register

7	6	5	4	3	2	1	0
RESERVED	CHRG_CV_MASK	CHARGE_DONE_MASK	IINLIM_ACTIVE_MASK	RESERVED	VINDPM_ACTIVE_MASK	THERMREG_ACTIVE_MASK	VIN_PGOOD_MASK
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

表 9-15. MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

表 9-15. MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CHRG_CV_MASK	R/W	1b0	Mask for CHRG_CV interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
5	CHARGE_DONE_MASK	R/W	1b0	Mask for CHARGE_DONE interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
4	IINLIM_ACTIVE_MASK	R/W	1b0	Mask for IINLIM_ACTIVE interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
3	RESERVED	R/W	1b0	Reserved
2	VINDPM_ACTIVE_MASK	R/W	1b0	Mask for VINDPM_ACTIVE interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
1	THERMREG_ACTIVE_MASK	R/W	1b0	Mask for THERMREG_ACTIVE interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
0	VIN_PGOOD_MASK	R/W	1b0	Mask for VIN_PGOOD interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

9.5.1.9 MASK1 Register (Address = 0x8) [reset = 0x0]

MASK1 is shown in 图 9-24 and described in 表 9-16.

Return to Summary Table.

图 9-24. MASK1 Register

7	6	5	4	3	2	1	0
VIN_OVP_FAULT_MASK	RESERVED	BAT_OCP_FAULT_MASK	BAT_UVLO_FAULT_MASK	TS_COLD_MASK	TS_COOL_MASK	TS_WARM_MASK	TS_HOT_MASK
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

表 9-16. MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVP_FAULT_MASK	R/W	1b0	Mask for VIN_OVP_FAULT interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
6	RESERVED	R/W	1b0	Reserved
5	BAT_OCP_FAULT_MASK	R/W	1b0	Mask for BAT_OCP_FAULT interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
4	BAT_UVLO_FAULT_MASK	R/W	1b0	Mask for BAT_UVLO_FAULT interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
3	TS_COLD_MASK	R/W	1b0	Mask for TS_COLD interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
2	TS_COOL_MASK	R/W	1b0	Mask for TS_COOL interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

表 9-16. MASK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TS_WARM_MASK	R/W	1b0	Mask for TS_WARM interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
0	TS_HOT_MASK	R/W	1b0	Mask for TS_HOT interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

9.5.1.10 MASK2 Register (Address = 0x9) [reset = 0x71]

MASK2 is shown in 图 9-25 and described in 表 9-17.

Return to Summary Table.

图 9-25. MASK2 Register

7	6	5	4	3	2	1	0
RESERVED							TS_OPEN_MASK
R/W-1b0	R/W-1b1	R/W-1b1	R/W-1b1	R/W-3b000			R/W-1b1

表 9-17. MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	X	Reserved
6	RESERVED	R	X	Reserved
5	RESERVED	R	X	Reserved
4	RESERVED	R	X	Reserved
3-1	RESERVED	R/W	3b000	Reserved
0	TS_OPEN_MASK	R/W	1b1	Mask for TS_OPEN Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

9.5.1.11 MASK3 Register (Address = 0xA) [reset = 0x0]

MASK3 is shown in 图 9-26 and described in 表 9-18.

Return to Summary Table.

图 9-26. MASK3 Register

7	6	5	4	3	2	1	0
RESERVED	WD_FAULT_MASK	SAFETY_TMR_FAULT_MASK	LDO_OCP_FAULT_MASK	RESERVED	MRWAKE1_TIMEOUT_MASK	MRWAKE2_TIMEOUT_MASK	MRRESET_WARN_MASK
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

表 9-18. MASK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6	WD_FAULT_MASK	R/W	1b0	Mask for WD_FAULT Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

表 9-18. MASK3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SAFETY_TMR_FAULT_MASK	R/W	1b0	Mask for SAFETY_TIMER_FAULT Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
4	LDO_OCP_FAULT_MASK	R/W	1b0	Mask for LDO_OCP_FAULT Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
3	RESERVED	R/W	1b0	Reserved
2	MRWAKE1_TIMEOUT_MASK	R/W	1b0	Mask for MRWAKE1_TIMEOUT Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
1	MRWAKE2_TIMEOUT_MASK	R/W	1b0	Mask for MRWAKE2_TIMEOUT Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked
0	MRRESET_WARN_MASK	R/W	1b0	Mask for MRRESET_WARN Interrupt 1b0 = Interrupt Not Masked 1b1 = Interrupt Masked

9.5.1.12 VBAT_CTRL Register (Address = 0x12) [reset = 0x3C]

VBAT_CTRL is shown in 图 9-27 and described in 表 9-19.

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图 9-27. VBAT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	VBAT_REG_6:0						
R/W-1b0	R/W-7b0111100						

表 9-19. VBAT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6-0	VBAT_REG_6:0	R/W	7b0111100	Battery Regulation Voltage (4.2 V default) VBATREG = 3.6 V + VBAT_REG code x 10 mV If a value greater than 4.6 V is written, the setting will go to 4.6 V

9.5.1.13 ICHG_CTRL Register (Address = 0x13) [reset = 0x36]

ICHG_CTRL is shown in 图 9-28 and described in 表 9-20.

Return to Summary Table.

图 9-28. ICHG_CTRL Register

7	6	5	4	3	2	1	0
ICHG_7:0							
R/W-8b00110110							

表 9-20. ICHG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ICHG_7:0	R/W	8b00110110	Fast Charge Current (67.5 mA default) Fast Charge Current = 1.25 mA x ICHG code (ICHARGE_RANGE = 0) Fast Charge Current = 2.5 mA x ICHG code (ICHARGE_RANGE = 1)

9.5.1.14 PCHRGCTRL Register (Address = 0x14) [reset = 0x7]

PCHRGCTRL is shown in 图 9-29 and described in 表 9-21.

Return to Summary Table.

图 9-29. PCHRGCTRL Register

7	6	5	4	3	2	1	0
ICHARGE_RANGE	RESERVED		IPRECHG_4:0				
R/W-1b0	R/W-2b00		R/W-5b00111				

表 9-21. PCHRGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ICHARGE_RANGE	R/W	1b0	Charge Current Step 1b0 = 1.25 mA step (318.75 mA max charge current) 1b1 = 2.5 mA step (500 mA max charge current)
6-5	RESERVED	R/W	2b00	Reserved
4-0	IPRECHG_4:0	R/W	5b00111	Pre-Charge Current (8.75 mA default) Pre-Charge Current = 1.25 mA x IPRECHG code (ICHARGE_RANGE = 0) Pre-Charge Current = 2.5 mA x IPRECHG code (ICHARGE_RANGE = 1)

9.5.1.15 TERMCTRL Register (Address = 0x15) [reset = 0x14]

TERMCTRL is shown in 图 9-30 and described in 表 9-22.

Return to Summary Table.

图 9-30. TERMCTRL Register

7	6	5	4	3	2	1	0
RESERVED		ITERM_4:0					TERM_DISABLE
R/W-2b00		R/W-5b01010					R/W-1b0

表 9-22. TERMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	2b00	Reserved

表 9-22. TERMCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-1	ITERM_4:0	R/W	5b01010	Termination Current (10% of ICHRG default) Programmable Range = 1% to 31% of ICHRG 5b00000 = Do not Use 5b00001 = 1% of ICHRG 5b00010 = 2% of ICHRG 5b00100 = 4% of ICHRG 5b01000 = 8% of ICHRG 5b10000 = 16% of ICHRG
0	TERM_DISABLE	R/W	1b0	Termination Disable 1b0 = Termination Enabled 1b1 = Termination Disabled

9.5.1.16 BUVLO Register (Address = 0x16) [reset = 0x3]

BUVLO is shown in 图 9-31 and described in 表 9-23.

Return to Summary Table.

图 9-31. BUVLO Register

7	6	5	4	3	2	1	0
RESERVED		VLOWV_SEL	IBAT_OCP_ILIM_1:0		BUVLO_2:0		
R/W-2b00		R/W-1b0	R/W-2b00		R/W-3b011		

表 9-23. BUVLO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	2b00	Reserved
5	VLOWV_SEL	R/W	1b0	Pre-charge to Fast Charge Threshold 1b0 = 3.0 V 1b1 = 2.8 V
4-3	IBAT_OCP_ILIM_1:0	R/W	2b00	Battery Over-Current Protection Threshold 2b00 = 1200 mA 2b01 = 1500 mA 2b10 = Disabled 2b11 = Disabled
2-0	BUVLO_2:0	R/W	3b011	Battery UVLO Voltage 3b000 = 3.0 V 3b001 = 3.0 V 3b010 = 3.0 V 3b011 = 2.8 V 3b100 = 2.6 V 3b101 = 2.4 V 3b110 = 2.2 V 3b111 = Disabled

9.5.1.17 CHARGERCTRL0 Register (Address = 0x17) [reset = 0x92]

CHARGERCTRL0 is shown in 图 9-32 and described in 表 9-24.

Return to Summary Table.

图 9-32. CHARGERCTRL0 Register

7	6	5	4	3	2	1	0
TS_EN	TS_CONTROL_MODE	VRH_THRESH	WATCHDOG_DISABLE	2XTMR_EN	SAFETY_TIMER_LIMIT_1:0		RESERVED
R/W-1b1	R/W-1b0	R/W-1b0	R/W-1b1	R/W-1b0	R/W-2b01		R/W-1b0

表 9-24. CHARGERCTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TS_EN	R/W	1b1	TS Function Enable 1b0 = TS function disabled (Only charge control is disabled. TS_OPEN detection and TS ADC monitoring remain enabled) 1b1 = TS function enabled
6	TS_CONTROL_MODE	R/W	1b0	TS Function Control Mode 1b0 = Custom (JEITA) 1b1 = Disable charging on HOT/COLD Only
5	VRH_THRESH	R/W	1b0	Recharge Voltage Threshold 1b0 = 140 mV 1b1 = 200 mV
4	WATCHDOG_DISABLE	R/W	1b1	Watchdog Timer Disable 1b0 = Watchdog timer enabled 1b1 = Watchdog timer disabled
3	2XTMR_EN	R/W	1b0	Enable 2X Safety Timer 1b0 = The timer is not slowed at any time 1b1 = The timer is slowed by 2x when in any control other than CC or CV
2-1	SAFETY_TIMER_LIMIT_1:0	R/W	2b01	Charger Safety Timer 2b00 = 3 Hr Fast Charge 2b01 = 6 Hr Fast Charge 2b10 = 12 Hr Fast Charge 2b11 = Disabled
0	RESERVED	R/W	1b0	Reserved

9.5.1.18 CHARGERCTRL1 Register (Address = 0x18) [reset = 0x32]

CHARGERCTRL1 is shown in 图 9-33 and described in 表 9-25.

Return to Summary Table.

图 9-33. CHARGERCTRL1 Register

7	6	5	4	3	2	1	0
VINDPM_DIS	VINPDM_2:0			RESERVED	THERM_REG_2:0		
R/W-1b0	R/W-3b011			R/W-1b1	R/W-3b010		

表 9-25. CHARGERCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VINDPM_DIS	R/W	1b0	Disable VINDPM Function 1b0 = VINDPM Enabled 1b1 = VINDPM Disabled

表 9-25. CHARGERCTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	VINPDM_2:0	R/W	3b011	VINDPM Level Selection 3b000 = 4.2 V 3b001 = 4.3 V 3b010 = 4.4 V 3b011 = 4.5 V 3b100 = 4.6 V 3b101 = 4.7 V 3b110 = 4.8 V 3b111 = 4.9 V
3	RESERVED	R/W	1b1	Reserved
2-0	THERM_REG_2:0	R/W	3b010	Thermal Charge Current Foldback Threshold 3b000 = 80°C 3b001 = 85°C 3b010 = 90°C 3b011 = 95°C 3b100 = 100°C 3b101 = 105°C 3b110 = 110°C 3b111 = Disabled

9.5.1.19 ILIMCTRL Register (Address = 0x19) [reset = 0x1]

ILIMCTRL is shown in 图 9-34 and described in 表 9-26.

Return to Summary Table.

图 9-34. ILIMCTRL Register

7	6	5	4	3	2	1	0
RESERVED					ILIM_2:0		
R/W-5b00000					R/W-3b001		

表 9-26. ILIMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	5b00000	Reserved
2-0	ILIM_2:0	R/W	3b001	Input Current Limit Level Selection 3b000 = 50 mA 3b001 = 100 mA 3b010 = 150 mA 3b011 = 200 mA 3b100 = 300 mA 3b101 = 400 mA 3b110 = 500 mA 3b111 = 600 mA

9.5.1.20 LDOCTRL Register (Address = 0x1D) [reset = 0x32]

LDOCTRL is shown in 图 9-35 and described in 表 9-27.

Return to Summary Table.

图 9-35. LDOCTRL Register

7	6	5	4	3	2	1	0
EN_LS_LDO	VLDO_4:0					LDO_SWITCH_CONFG	RESERVED
R/W-1b0	R/W-5b01100					R/W-1b1	R/W-1b0

表 9-27. LDOCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_LS_LDO	R/W	1b0	LS/LDO Enable 1b0 = Disable LS/LDO 1b1 = Enable LS/LDO
6-2	VLDO_4:0	R/W	5b01100	LDO output voltage setting (1.8 V default) LDO Voltage = 600 mV + VLDO Code x 100 mV
1	LDO_SWITCH_CONFG	R/W	1b1	LDO / Load Switch Configuration Select 1b0 = LDO 1b1 = Load Switch
0	RESERVED	R/W	1b0	Reserved

9.5.1.21 MRCTRL Register (Address = 0x30) [reset = 0x2E]

MRCTRL is shown in 图 9-36 and described in 表 9-28.

Return to Summary Table.

图 9-36. MRCTRL Register

7	6	5	4	3	2	1	0
MR_RESET_VIN	MR_WAKE1_TIMER	MR_WAKE2_TIMER	MR_RESET_WARN_1:0		MR_HW_RESET_1:0		RESERVED
R/W-1b0	R/W-1b0	R/W-1b1	R/W-2b01		R/W-2b11		R/W-1b0

表 9-28. MRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MR_RESET_VIN	R/W	1b0	VIN Power Good gated MR Reset Enable 1b0 = Reset sent when /MR reset time is met regardless of VIN state 1b1 = Reset sent when MR reset is met and Vin is valid
6	MR_WAKE1_TIMER	R/W	1b0	Wake 1 Timer setting 1b0 = 125 ms 1b1 = 500 ms
5	MR_WAKE2_TIMER	R/W	1b1	Wake 2 Timer setting 1b0 = 1 s 1b1 = 2 s
4-3	MR_RESET_WARN_1:0	R/W	2b01	MR Reset Warn Timer setting 2b00 = MR_HW_RESET - 0.5 s 2b01 = MR_HW_RESET - 1.0 s 2b10 = MR_HW_RESET - 1.5 s 2b11 = MR_HW_RESET - 2.0 s
2-1	MR_HW_RESET_1:0	R/W	2b11	MR HW Reset Timer setting 2b00 = 4 s 2b01 = 8 s 2b10 = 10 s 2b11 = 14 s
0	RESERVED	R/W	1b0	Reserved

9.5.1.22 ICCTRL0 Register (Address = 0x35) [reset = 0x20]

ICCTRL0 is shown in 图 9-37 and described in 表 9-29.

Return to Summary Table.

图 9-37. ICCTRL0 Register

7	6	5	4	3	2	1	0
EN_SHIP_MODE	RESERVED	AUTOWAKE_1:0		RESERVED	GLOBAL_INT_MASK	HW_RESET	SW_RESET
R/W-1b0	R/W-1b0	R/W-2b10		R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0

表 9-29. ICCTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_SHIP_MODE	R/W	1b0	Ship Mode Enable 1b0 = Normal operation 1b1 = Enter Ship Mode when VIN is not valid and /MR is high
6	RESERVED	R/W	1b0	Reserved
5-4	AUTOWAKE_1:0	R/W	2b10	Auto-wakeup Timer (TRESTART) for /MR HW Reset 2b00 = 0.6 s 2b01 = 1.2 s 2b10 = 2.4 s 2b11 = 5 s

表 9-29. ICCTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	1b0	Reserved
2	GLOBAL_INT_MASK	R/W	1b0	Global Interrupt Mask 1b0 = Normal Operation 1b1 = Mask all interrupts
1	HW_RESET	R/W	1b0	HW Reset 1b0 = Normal operation 1b1 = HW Reset. Temporarily power down all power rails, except VDD. I^2C Register go to default settings.
0	SW_RESET	R/W	1b0	SW_Reset 1b0 = Normal operation 1b1 = SW Reset. I^2C Registers go to default settings.

9.5.1.23 ICCTRL1 Register (Address = 0x36) [reset = 0x0]

ICCTRL1 is shown in 图 9-38 and described in 表 9-30.

Return to Summary Table.

图 9-38. ICCTRL1 Register

7	6	5	4	3	2	1	0
MR_LPRESS_ACTION_1:0		RESERVED	RESERVED	PG_MODE_1:0		PMID_MODE_1:0	
R/W-2b00		R/W-1b0	R/W-1b0	R/W-2b00		R/W-2b00	

表 9-30. ICCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	MR_LPRESS_ACTION_1:0	R/W	2b00	MR Long Press Action 2b00 = HW Reset (Power Cycle) 2b01 = Do nothing 2b10 = Enter Ship Mode 2b11 = Enter Ship Mode
5	RESERVED	R/W	1b0	Reserved
4	RESERVED	R/W	1b0	Reserved
3-2	PG_MODE_1:0	R/W	2b00	$\overline{\text{PG}}$ Pin Mode of Operation 2b00 = VIN Power Good. $\overline{\text{PG}}$ pulls to GND when $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT}+V_{SLP}$ and $V_{IN} < V_{IN\_OVP}$. 2b01 = Deglitched Level Shifted /MR. $\overline{\text{PG}}$ is high impedance when the $\overline{\text{MR}}$ input is high, and $\overline{\text{PG}}$ pulls to GND when the $\overline{\text{MR}}$ input is low. 2b1x = General Purpose Open Drain Output. The state of the $\overline{\text{PG}}$ pin is then controlled through the GPO_PG bit, where if GPO_PG is 0 , the $\overline{\text{PG}}$ pin is pulled to GND and if it is 1, the $\overline{\text{PG}}$ pin is in high impedance.
1-0	PMID_MODE_1:0	R/W	2b00	PMID Control Sets how PMID is powered in any state, except Ship Mode. 2b00 = PMID powered from BAT or VIN if present 2b01 = PMID powered from BAT only, even if VIN is present 2b10 = PMID disconnected and left floating 2b11 = PMID disconnected and pulled down.

9.5.1.24 ICCTRL2 Register (Address = 0x37) [reset = 0x40]

ICCTRL2 is shown in 图 9-39 and described in 表 9-31.

Return to Summary Table.

图 9-39. ICCTRL2 Register

7	6	5	4	3	2	1	0
PMID_REG_CTRL_2:0			GPO_PG	RESERVED		HWRESET_14S_WD	CHARGER_DISABLE
R/W-3b010			R/W-1b0	R/W-2b00		R/W-1b0	R/W-1b0

表 9-31. ICCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	PMID_REG_CTRL_2:0	R/W	3b010	System (PMID) Regulation Voltage 3b000 = Battery Tracking 3b001 = 4.4 V 3b010 = 4.5 V 3b011 = 4.6 V 3b100 = 4.7 V 3b101 = 4.8 V 3b110 = 4.9 V 3b111 = Pass-Through (V_{IN})
4	GPO_PG	R/W	1b0	/PG General Purpose Output State Control 1b0 = Pulled Down 1b1 = High Z
3-2	RESERVED	R/W	2b00	Reserved
1	HWRESET_14S_WD	R/W	1b0	Enable for 14-second I^2C watchdog timer for HW Reset after VIN connection 1b0 = Timer disabled 1b1 = Device will perform HW reset if no I^2C transaction is done within 14 s after VIN is present
0	CHARGER_DISABLE	R/W	1b0	Charge Disable 1b0 = Charge enabled if /CE pin is low 1b1 = Charge disabled

9.5.1.25 TS_READ Register (Address = 0x40) [reset = 0x2]

TS_Read is shown in 图 9-40 and described in 表 9-32.

Return to Summary Table.

图 9-40. TS_READ Register

7	6	5	4	3	2	1	0
INTERVAL	RESERVED	GET_FAULT_ENABLE	RESERVED		RESERVED		
R/W-1b0	R-1b0	R/W-1b0	R/W-2b00		R/W-3b010		

表 9-32. TS_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INTERVAL	R/W	1b0	Interval rate for TS read in BAT Only operation 1b0 = Manual Read (TS pin checked when GET_FAULT_ENABLE is set) 1b1 = TS pin checked every 1 second

表 9-32. TS_READ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R/W	1b0	Reserved
5	GET_FAULT_ENABLE	R/W	1b0	TS Fault Read Trigger. Bit goes back to 0 when read is complete 1b0 = Normal Operation 1b1 = Initiate TS Fault read
4-3	RESERVED	R/W	2b00	Reserved
2-0	RESERVED	R/W	3b010	Reserved

9.5.1.26 TS_FAULT_MEAS Register (Address = 0x58) [reset = 0x0]

TS_FAULT_MEAS is shown in 图 9-41 and described in 表 9-33.

Return to Summary Table.

图 9-41. TS_FAULT_MEAS Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Fault_Enable	Reserved	Reserved
R/W-1b0	R/W-1b0	R/W-1b0	R/W-1b0	R/W- 1b0	R/W-1b0	R/W-1b0	R/W-1b0

表 9-33. TS_Fault_MEAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6	RESERVED	R/W	1b0	Reserved
5	RESERVED	R/W	1b0	Reserved
4	RESERVED	R/W	1b0	Reserved
3	RESERVED	R/W	1b0	Reserved
2	TS_FAULT_MEAS_ENABLE	R/W	1b0	Enable TS Fault Measurement 1b0 = Measurement disabled 1b1 = Measurement enabled
1	RESERVED	R/W	1b0	Reserved
0	RESERVED	R/W	1b0	Reserved

9.5.1.27 TS_FASTCHGCTRL Register (Address = 0x61) [reset = 0x34]

TS_FASTCHGCTRL is shown in 图 9-42 and described in 表 9-34.

Return to Summary Table.

图 9-42. TS_FASTCHGCTRL Register

7	6	5	4	3	2	1	0
RESERVED	TS_VBAT_REG__2:0			RESERVED	TS_ICHRG_2:0		
R/W-1b0	R/W-3b011			R/W-1b0	R/W-3b100		

表 9-34. TS_FASTCHGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved

表 9-34. TS_FASTCHGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	TS_VBAT_REG__2:0	R/W	3b011	Reduced target battery voltage during Warm 3b000 = No reduction 3b001 = VBAT_REG - 50 mV 3b010 = VBAT_REG - 100 mV 3b011 = VBAT_REG - 150 mV 3b100 = VBAT_REG - 200 mV 3b101 = VBAT_REG - 250 mV 3b110 = VBAT_REG - 300 mV 3b111 = VBAT_REG - 350 mV
3	RESERVED	R/W	1b0	Reserved
2-0	TS_ICHRG_2:0	R/W	3b100	Fast charge current when decreased by TS function 3b000 = No reduction 3b001 = 0.875 x ICHG 3b010 = 0.750 x ICHG 3b011 = 0.625 x ICHG 3b100 = 0.500 x ICHG 3b101 = 0.375 x ICHG 3b110 = 0.250 x ICHG 3b111 = 0.125 x ICHG

9.5.1.28 TS_COLD Register (Address = 0x62) [reset = 0x7C]

TS_COLD is shown in 图 9-43 and described in 表 9-35.

Return to Summary Table.

图 9-43. TS_COLD Register

7	6	5	4	3	2	1	0
TS_COLD_7:0							
R/W-8b01111100							

表 9-35. TS_COLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TS_COLD_7:0	R/W	8b01111100	TS Cold Threshold 1b = 4.688 mV 10b = 9.375 mV 100b = 18.75 mV 1000b = 37.5 mV 10000b = 75 mV 100000b = 150 mV 1000000b = 300 mV 10000000b = 600 mV

9.5.1.29 TS_COOL Register (Address = 0x63) [reset = 0x6D]

TS_COOL is shown in 图 9-44 and described in 表 9-36.

Return to Summary Table.

图 9-44. TS_COOL Register

7	6	5	4	3	2	1	0
TS_COOL_7:0							
R/W-8b01101101							

表 9-36. TS_COOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TS_COOL_7:0	R/W	8b01101101	TS Cool Threshold 1b = 4.688 mV 10b = 9.375 mV 100b = 18.75 mV 1000b = 37.5 mV 10000b = 75 mV 100000b = 150 mV 1000000b = 300 mV 10000000b = 600 mV

9.5.1.30 TS_WARM Register (Address = 0x64) [reset = 0x38]

TS_WARM is shown in 图 9-45 and described in 表 9-37.

Return to Summary Table.

图 9-45. TS_WARM Register

7	6	5	4	3	2	1	0
TS_WARM_7:0							
R/W-8b00111000							

表 9-37. TS_WARM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TS_WARM_7:0	R/W	8b00111000	TS Warm Threshold 1b = 4.688 mV 10b = 9.375 mV 100b = 18.75 mV 1000b = 37.5 mV 10000b = 75 mV 100000b = 150 mV 1000000b = 300 mV 10000000b = 600 mV

9.5.1.31 TS_HOT Register (Address = 0x65) [reset = 0x38]

TS_HOT is shown in 图 9-46 and described in 表 9-38.

Return to Summary Table.

图 9-46. TS_HOT Register

7	6	5	4	3	2	1	0
TS_HOT_7:0							
R/W-8b00111000							

表 9-38. TS_HOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TS_HOT_7:0	R/W	8b00111000	TS Hot Threshold 1b = 4.688 mV 10b = 9.375 mV 100b = 18.75 mV 1000b = 37.5 mV 10000b = 75 mV 100000b = 150 mV 1000000b = 300 mV 10000000b = 600 mV

9.5.1.32 DEVICE_ID Register (Address = 0x6F) [reset = 0x3B]

DEVICE_ID is shown in 图 9-47 and described in 表 9-39.

Return to Summary Table.

图 9-47. DEVICE_ID Register

7	6	5	4	3	2	1	0
DEVICE_ID_7:0							
R-8b00111011							

表 9-39. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID_7:0	R	8b00111011	Device ID 00111011b = BQ21062

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

A typical application of the BQ21062 consists of the device configured as an I^{2}C controlled single cell Li-ion battery charger and power path manager or small battery applications such as smart-watches and wireless headsets. A battery thermistor may be connected to the TS pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the $\overline{\text{MR}}$ input to a push-button to send interrupts to the host as the button is pressed or to allow the application's end user to reset the system. If not used this pin must be left floating or tied to BAT.

10.2 Typical Application

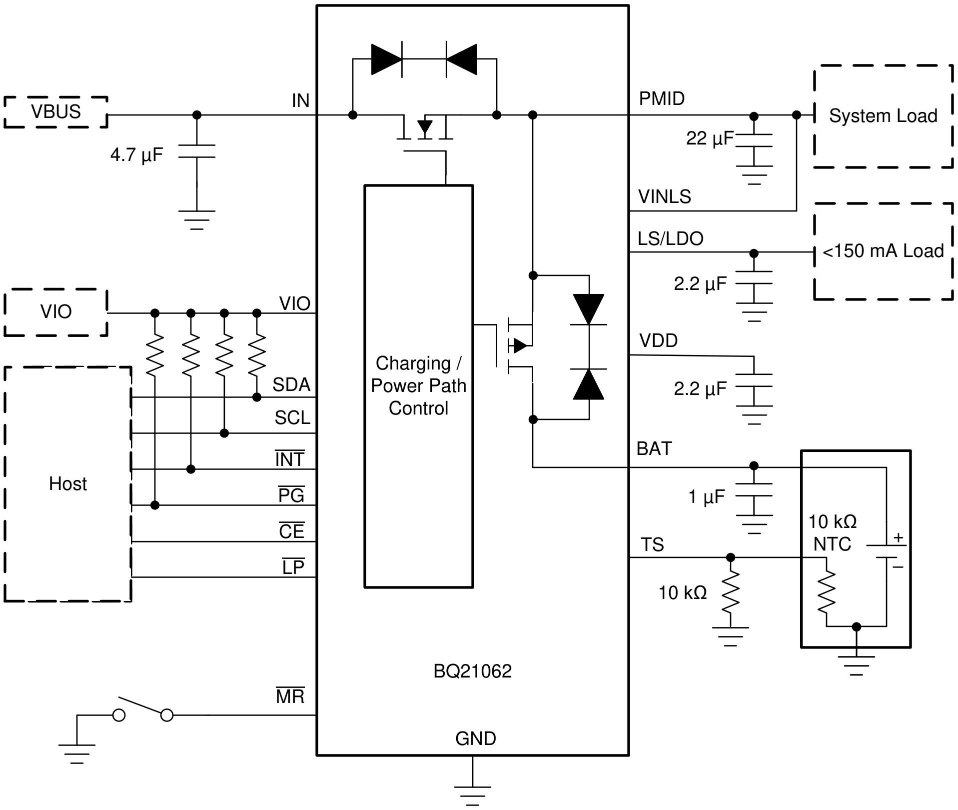


图 10-1. Typical Application Diagram

10.2.1 Design Requirements

The design parameters for the following design example are shown in the table below.

表 10-1. Design Parameters

PARAMETER	VALUE
IN Supply Voltage	5 V
Battery Regulation Voltage	4.35 V
LDO Output Voltage	LDO (1.8 V)

10.2.2 Detailed Design Procedure

10.2.2.1 Input (IN/PMID) Capacitors

Low ESR ceramic capacitors such as X7R or X5R is preferred for input decoupling capacitors and should be places as close as possible to the supply and ground pins fo the IC. Due to the voltage derating of the capacitors it is recommended at 25-V rated capacitors are used for IN and PMID pins which can normally operate at 5 V. After derating the minimum capacitance must be higher than 1 µF.

10.2.2.2 VDD, LDO Input and Output Capacitors

A Low ESR ceramic capacitor such as X7R or X5R is recommended for the LDO decoupling capacitor. A 4.7-µF capacitor is recommended for VDD output. For the LDO output a 2.2-µF capacitor is recommended. The minimum supported capacitance after derating must be higher than 1 µF to ensure stability. The VINLS input bypass capacitor value should match or exceed the LDO output capacitor value.

10.2.2.3 TS

A 10-KΩ NTC should be connected in parallel to a 10-kΩ biasing resistor connected to ground. The ground connection of both the NTC and biasing resistor must be done as close as possible to the GND pin of the device or kelvin connected to it to minimize any error in TS measurement due IR drops on the board ground lines.

If the system designer does not wish to use the TS function for charging control, a 5-kΩ resistor from TS to ground must be connected.

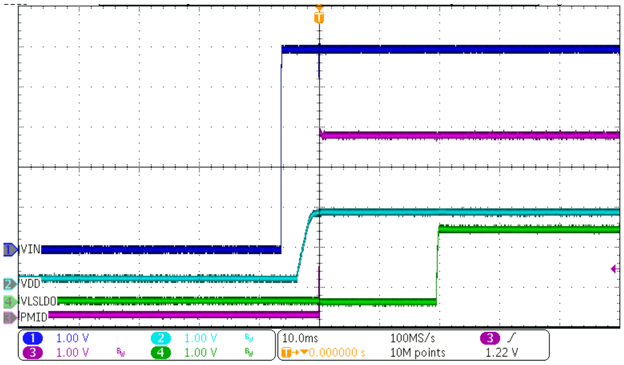
10.2.2.4 Recommended Passive Components

表 10-2. Recommended Passive Components

		MIN	NOM	MAX	UNIT
C_{PMID}	Capacitance in PMID pin	1(1)	22	47	µF
C_{LDO}	LDO output capacitance	1	2.2	4.7	µF
C_{VDD}	VDD output capacitance	1	2.2	4.7	µF
C_{BAT}	BAT pin capacitance	1		–	µF
C_{IN}	IN input bypass capacitance	1	4.7	10	µF
C_{INLS}	VINLS input bypass capacitance	1		–	µF
C_{TS}	Capacitance from TS pin to ground	0	0	1	nF

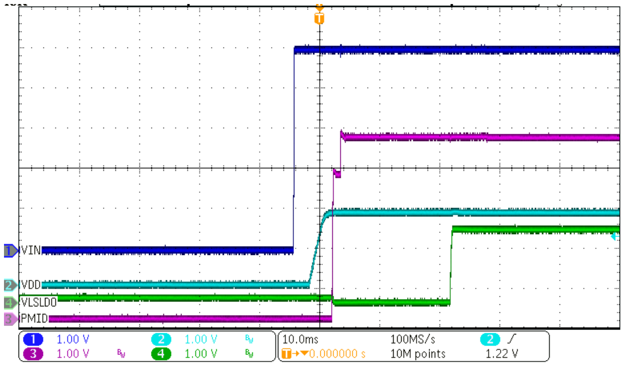
(1) For PMID regulation loop stability, for better transient performance a minimum capacitance (after derating) of 10 µF is recommended.

10.2.3 Application Curves



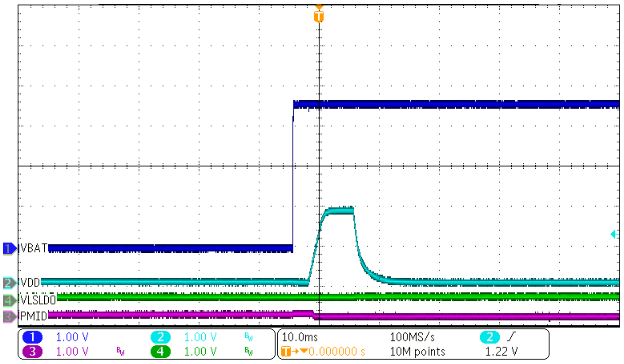
VIN = 5V VBAT = 0V

图 10-2. Power Up from IN Supply Insertion with No Battery



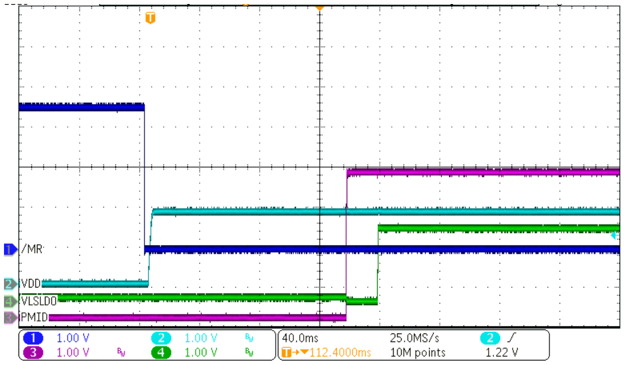
VIN = 5V VBAT = 3.6V

图 10-3. Power Up from Ship Mode with IN Supply Insertion



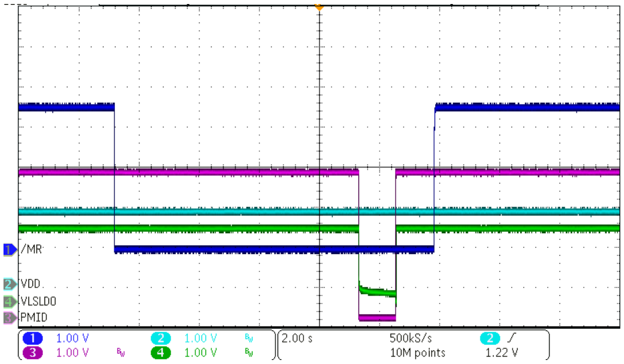
VIN = 0V VBAT = 3.6V

图 10-4. Wake In To Ship Mode on Battery Insertion with No IN Supply



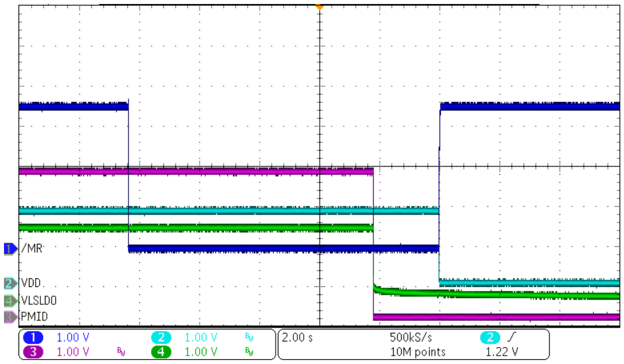
VIN = 0V VBAT = 3.6V

图 10-5. Power Up from Ship Mode with $\overline{MR}$ Press



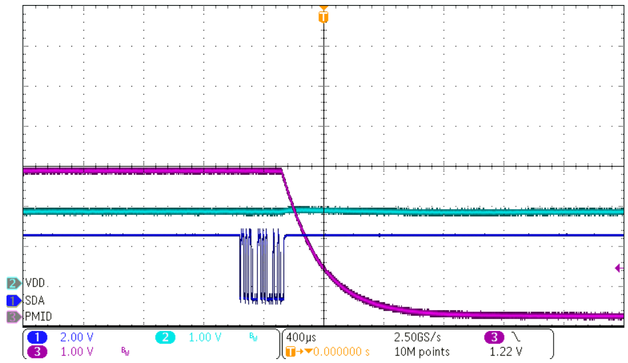
VIN = 0V VBAT = 3.6V

图 10-6. HW Reset on $\overline{MR}$ Long Button Press



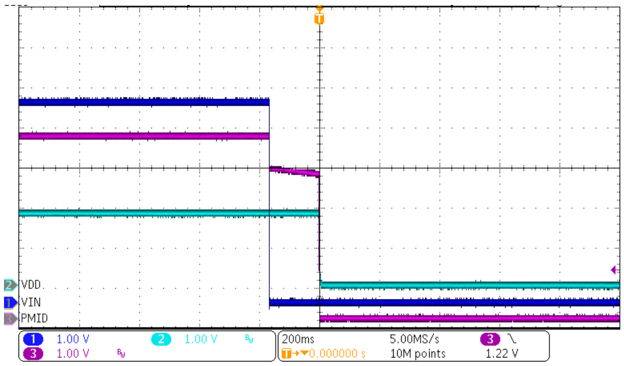
VIN = 0V VBAT = 3.6V LBPRESS_ACTION= 01

图 10-7. Ship Mode Entry with $\overline{MR}$ Long Button Press



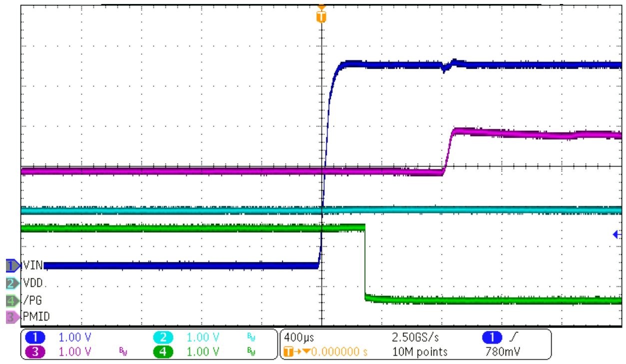
VIN = 0V VBAT = 3.6V

图 10-8. HW Reset Through I^{2}C Command



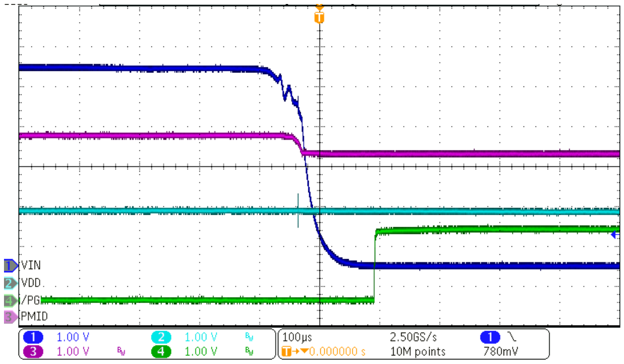
VIN = 5V VBAT = 3.6V SHIPMODE_EN = 1

图 10-9. Ship Mode Entry on IN Supply Removal



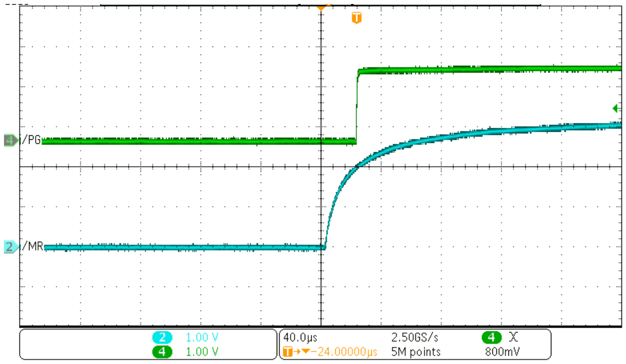
VIN = 5V VBAT = 3.6V

图 10-10. $\overline{\text{PG}}$ Power Good Function - IN Supply Insertion



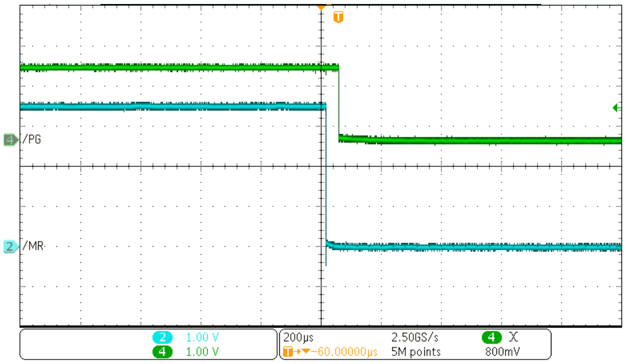
VIN = 5V VBAT = 3.6V

图 10-11. $\overline{\text{PG}}$ Power Good Function - IN Supply Removal



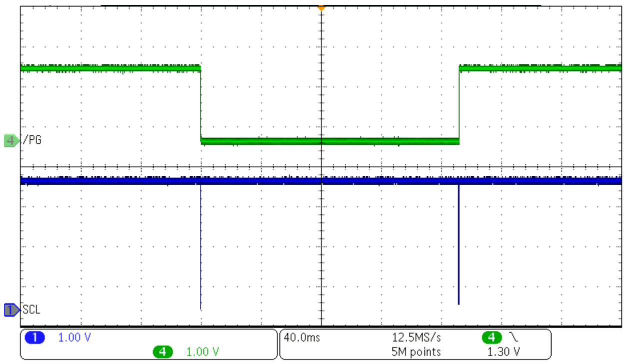
VIN = 5V VBAT = 3.6V

图 10-12. $\overline{\text{PG}}$ $\overline{\text{MR}}$ Level Shift Function - $\overline{\text{MR}}$ Rising



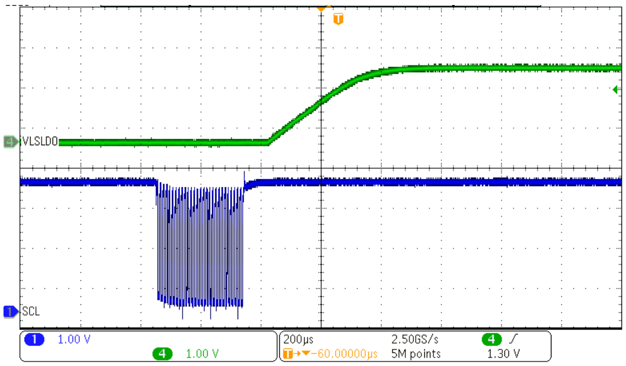
VBAT = 3.6V

图 10-13. $\overline{\text{PG}}$ $\overline{\text{MR}}$ Level Shift Function - $\overline{\text{MR}}$ Falling



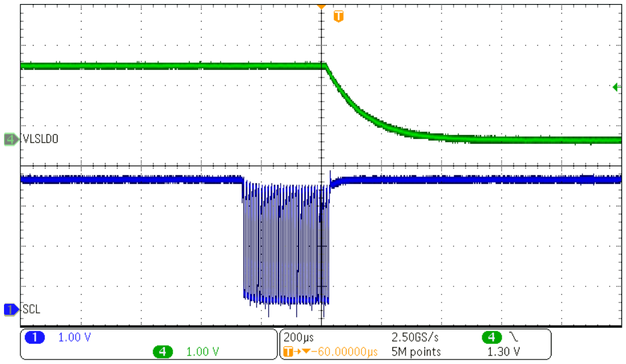
VBAT = 3.6V

图 10-14. PG General Purpose Output Function - GPO_PG Bit Toggle



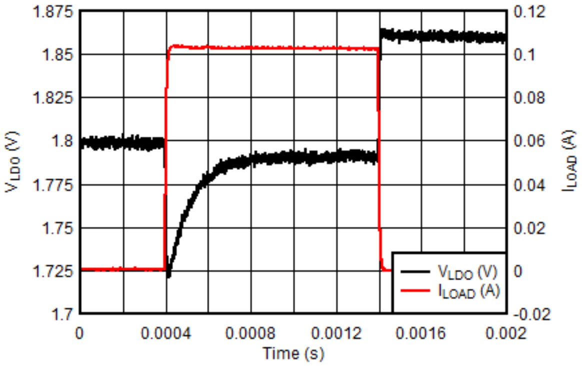
VBAT = 3.6V No load

图 10-15. LDO Enable Through I^2C (EN_LS_LDO)



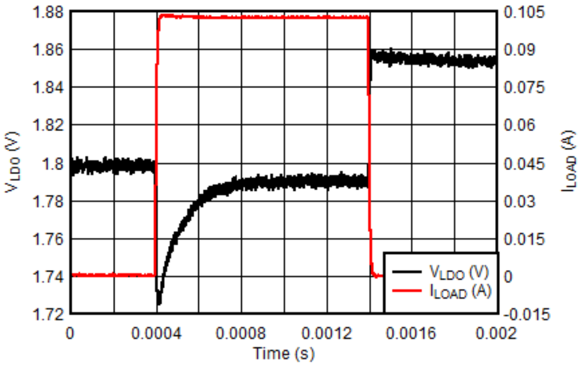
VBAT = 3.6V No load

图 10-16. LDO Disable Through I^2C (EN_LS_LDO)



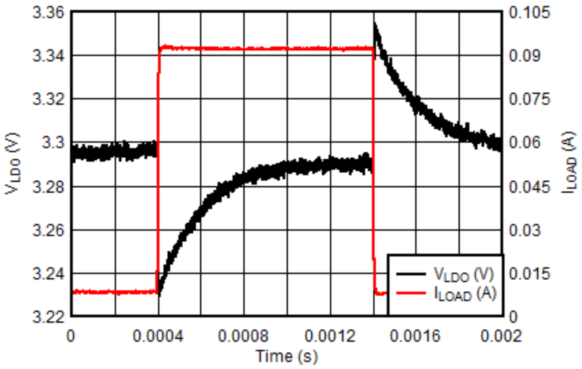
VIN = 0V VBAT = 3.6V VINLS = VPMID

图 10-17. LDO Load Transient - VLDO = 1.8V



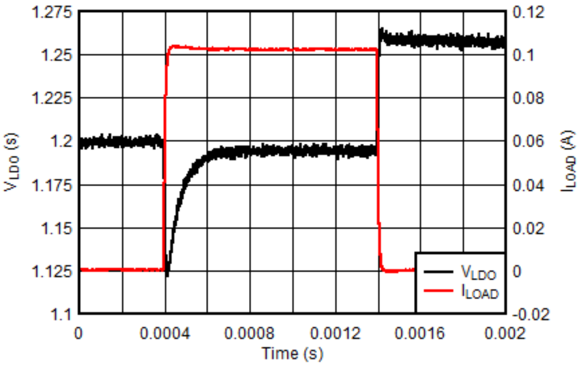
VIN = 0V VBAT = 2.4V VINLS = VPMID

图 10-18. LDO Load Transient - VLDO = 1.8V



VIN = 0V VBAT = 3.8V VINLS = VPMID

图 10-19. LDO Load Transient - VLDO = 3.3V



VIN = 0V VBAT = 3.6V VINLS = VPMID

图 10-20. LDO Load Transient - VLDO = 1.2V

11 Power Supply Recommendations

The BQ21062 requires the adapter or IN supply to be between 3.4 V and 5.5 V with at least 600-mA rating. The battery voltage must be higher than 2.4 V or $V_{BATUVLO}$ to ensure proper operation.

12 Layout

12.1 Layout Guidelines

- Have solid ground plane that is tied to the GND bump
- Place LDO and VDD output capacitors as close as possible to the respective bumps and GND or ground plane with short copper trace connection
- Place PMID capacitor as close to the PMID bump as possible and GND or ground plane.

12.2 Layout Example

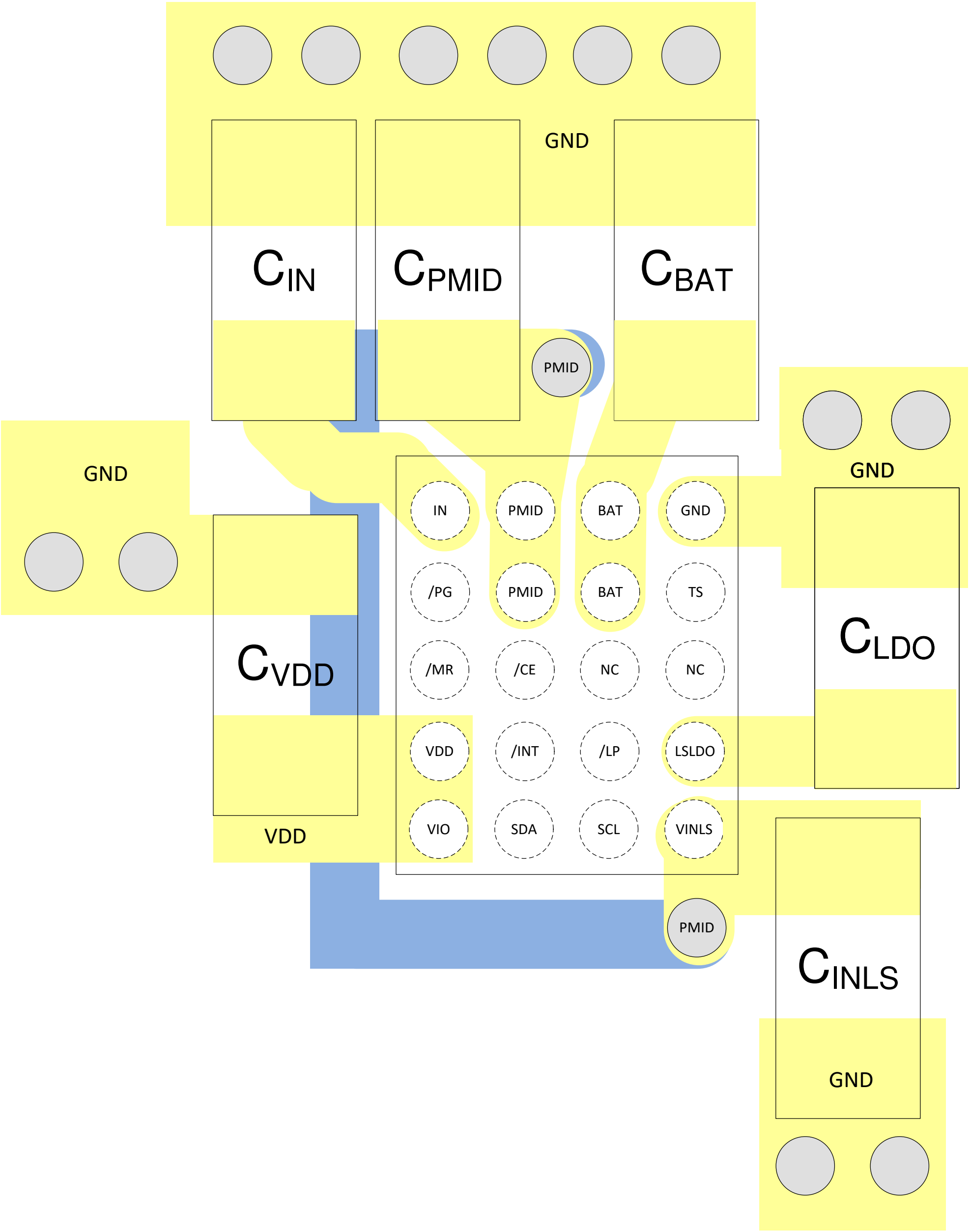


图 12-1. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following: *BQ21061EVM User's Guide* and *BQ21061 Setup Guide Tool*

13.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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13.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

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