CDx4ACT04 六路反相器

1 特性

- 输入兼容 TTL 电压
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- ±24mA 输出驱动电流
  - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV（根据 MIL-STD-883 方法 3015）

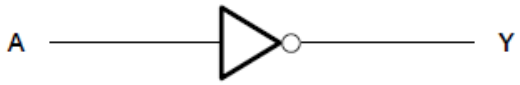
2 说明

'ACT04 器件包含六个独立的反相器。这些器件执行布尔函数 $Y = \overline{A}$。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
CD54ACT04	J（CDIP，14）	19.55mm x 7.9mm	19.55mm x 6.7mm
CD74ACT04	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.9mm
	N（PDIP，14）	19.3mm × 9.4mm	19.3mm × 6.35mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图，每个反相器（正逻辑）

Table of Contents

3 Pin Configuration and Functions

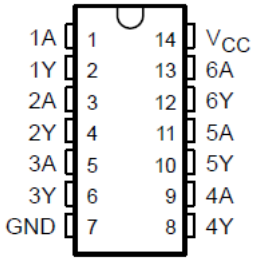


图 3-1. CD54ACT04 J Package, 14-Pin CDIP; CD74ACT04 N or D Package, 14-Pin PDIP or SOIC (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V_{CC}	14	—	Positive Supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6	V
I_{IK}	Input clamp current	(V_I < 0 or V_I > V_{CC})(2)		±20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})(2)		±50	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±50	mA
	Continuous current through V_{CC}or GND			±100	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		T_A = 25°C		− 40°C to 85°C		− 55°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		− 24		− 24		− 24	mA
I_{OL}	Low-level output current		24		24		24	mA
Δt/Δv	Input transition rise or fall rate		10		10		10	ns/V

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC(1)		CD74ACT04		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80	89.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	TA = 25°C		– 40°C to 85°C		– 55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −50 µA	4.5 V	4.4		4.4		4.4		V
		I_{OH} = – 24 mA	4.5 V	3.94		3.8		3.7		
		I_{OH} = – 50 mA(1)	5.5 V					3.85		
		I_{OH} = – 75 mA(1)	5.5 V			3.85				
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 50 µA	4.5 V		0.1		0.1		0.1	V
		I_{OL} = 24 mA	4.5 V		0.36		0.44		0.5	
		I_{OL} = 50 mA(1)	5.5 V						1.65	
		I_{OL} = 75 mA(1)	5.5 V				1.65			
I_I	$V_I = V_{CC}$ or GND		5.5 V		± 0.1		± 0.1		± 0.1	µA
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	5.5 V		4		40		80	µA
ΔI_{CC}	$V_I = V_{CC}$ – 2.1 V		4.5 V to 5.5 V		2.4		2.8		3	mA
C_i					10		10		10	pF

表 4-1. Act Input Load Table

INPUT	UNIT LOAD
A	0.18

(1) Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

4.5 Switching Characteristics

over operating free-air temperature range V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Load Circuit and Voltage Wave Forms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	– 40°C TO 85°C		– 55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.4	8.5	2.3	9.3	ns
t_{PHL}			2.4	8.5	2.3	9.3	

4.6 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	105	pF

5 Parameter Measurement Information

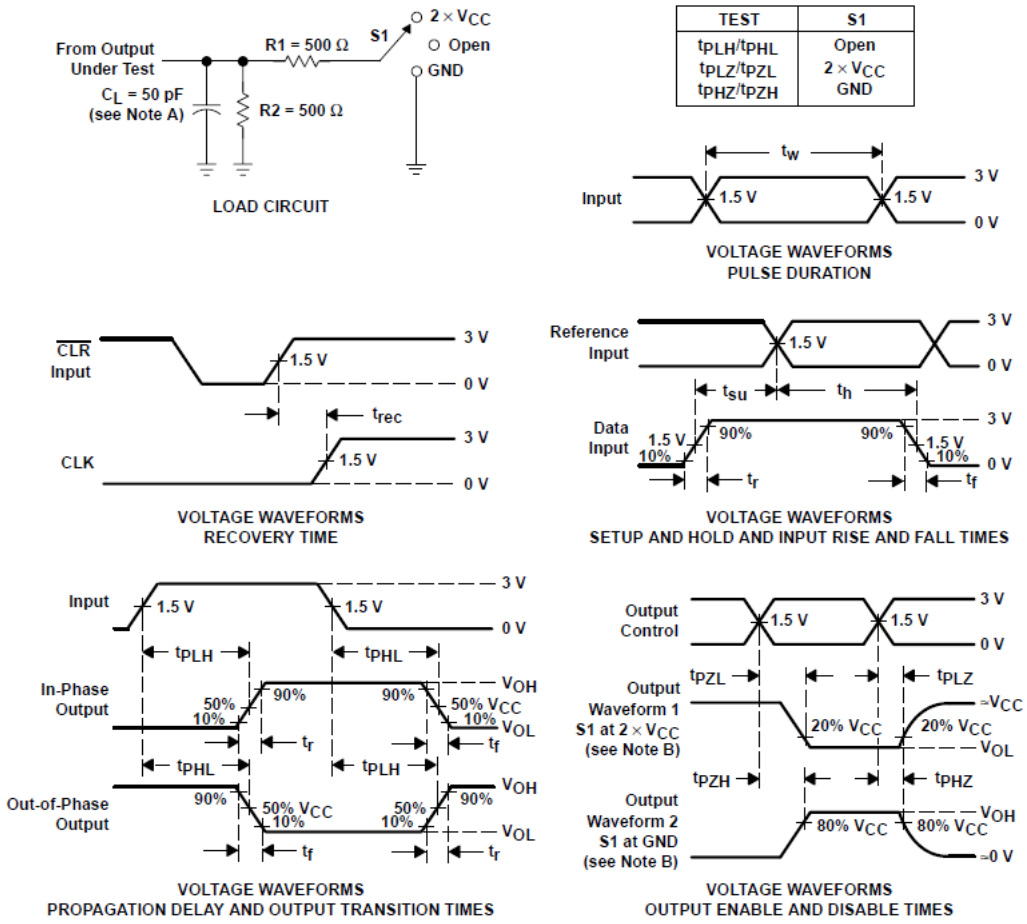


图 5-1.

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r ⩽ 3 ns, t_f ⩽ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

6 Detailed Description

6.1 Functional Block Diagram

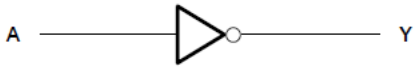


图 6-1. Logic Diagram, Each Inverter (Positive Logic)

6.2 Device Functional Modes

表 6-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *节 4.2* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Example are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

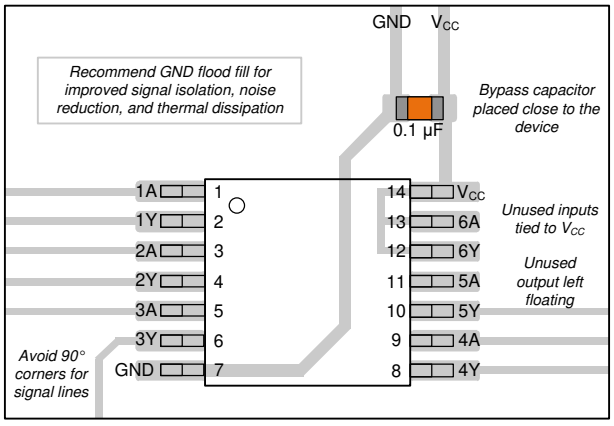


图 7-1. Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54ACT04	Click here	Click here	Click here	Click here	Click here
CD74ACT04	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

Changes from Revision C (May 2023) to Revision D (August 2024) — **Page**

- 向*器件信息* 表中添加了封装尺寸 1
- Updated R θ JA values: D = 86 to 89.9, all values in °C/W 4
- Changed packages from E and M to N and D 4

Changes from Revision B (June 2002) to Revision C (May 2023) — **Page**

- 添加了*封装信息* 表、*引脚功能* 表和*热性能信息* 表 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54ACT04F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT04F3A	Samples
CD74ACT04E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT04E	Samples
CD74ACT04M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	ACT04M	
CD74ACT04M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT04M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54ACT04, CD74ACT04 :

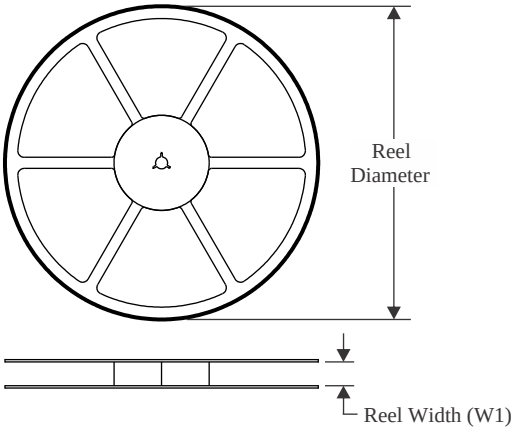
- Catalog : CD74ACT04
- Military : CD54ACT04

NOTE: Qualified Version Definitions:

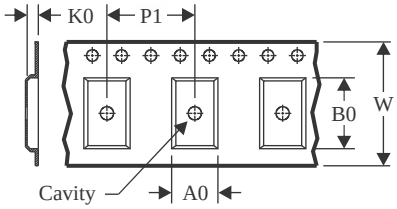
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

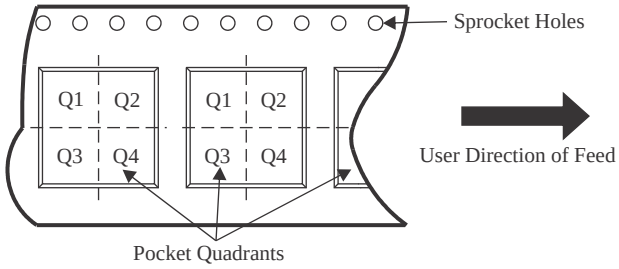


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

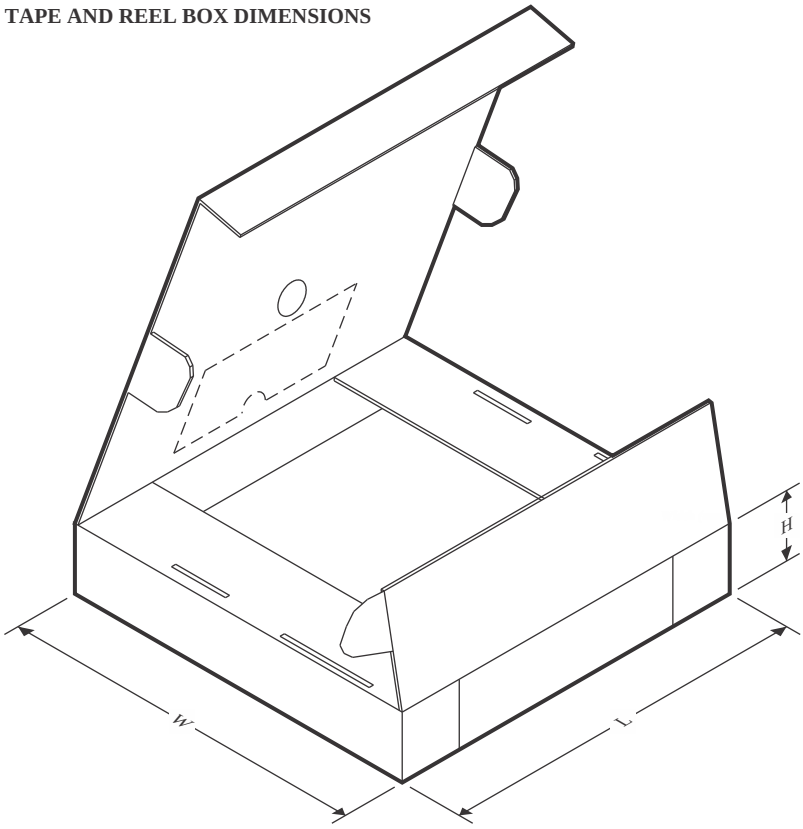
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT04M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74ACT04M96	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74ACT04M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

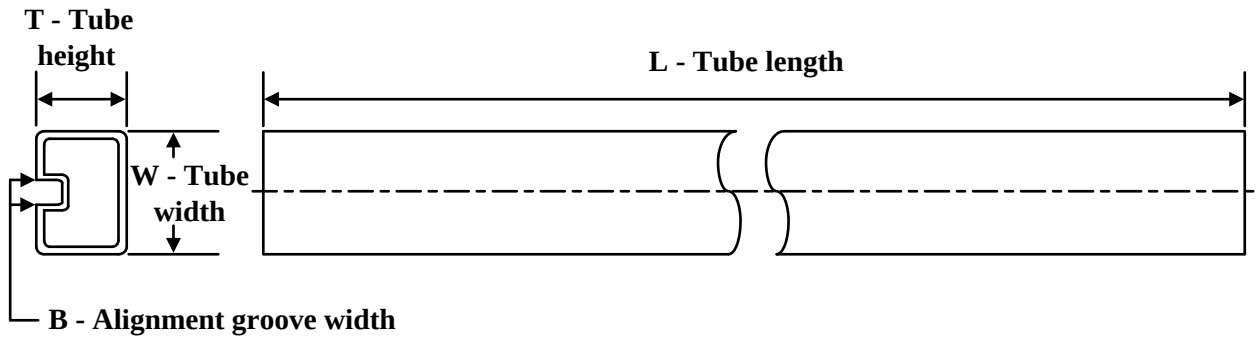
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

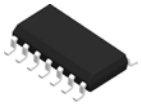
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT04M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74ACT04M96	SOIC	D	14	2500	340.5	336.1	32.0
CD74ACT04M96	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74ACT04E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT04E	N	PDIP	14	25	506	13.97	11230	4.32

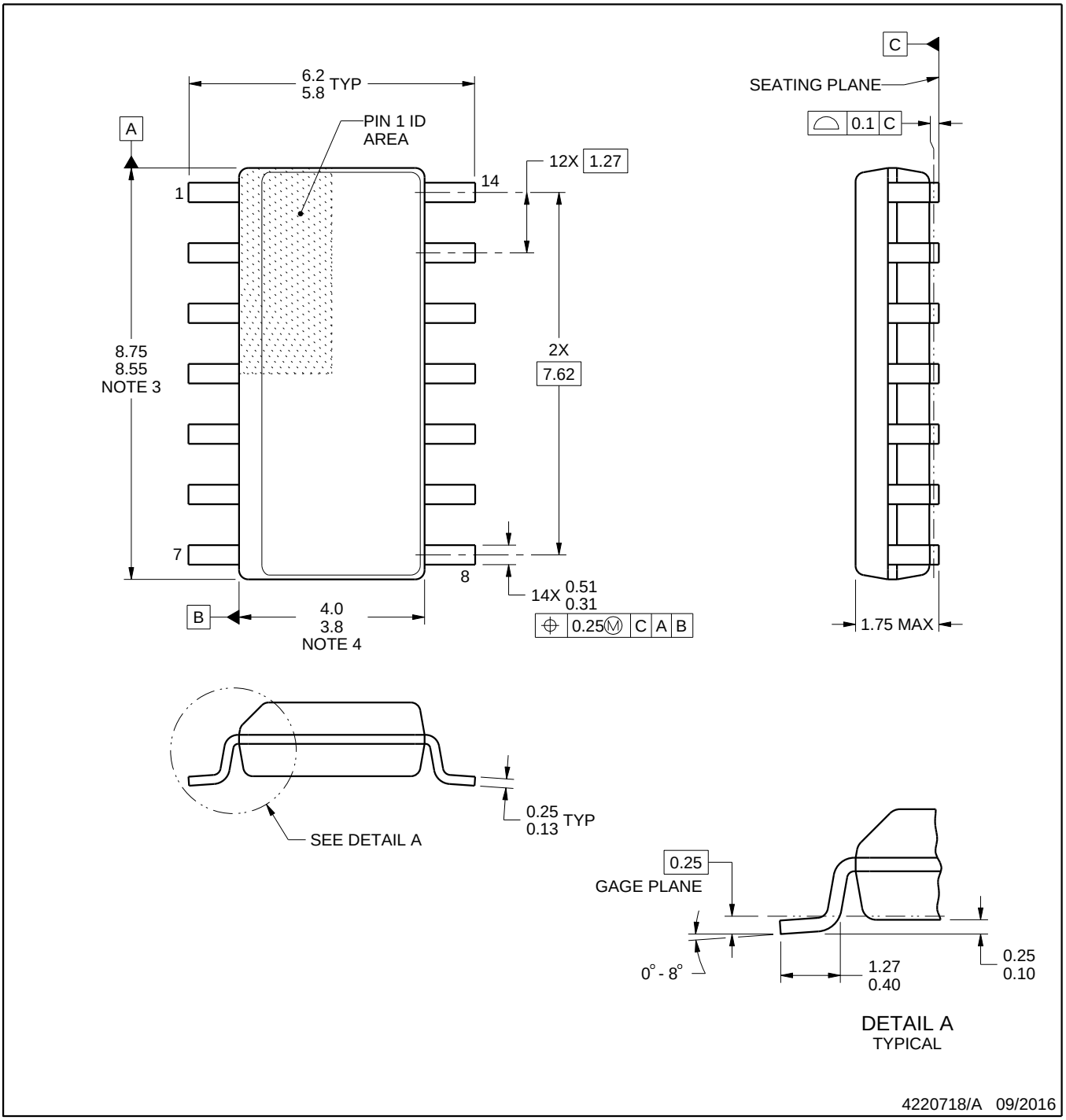


PACKAGE OUTLINE

D0014A

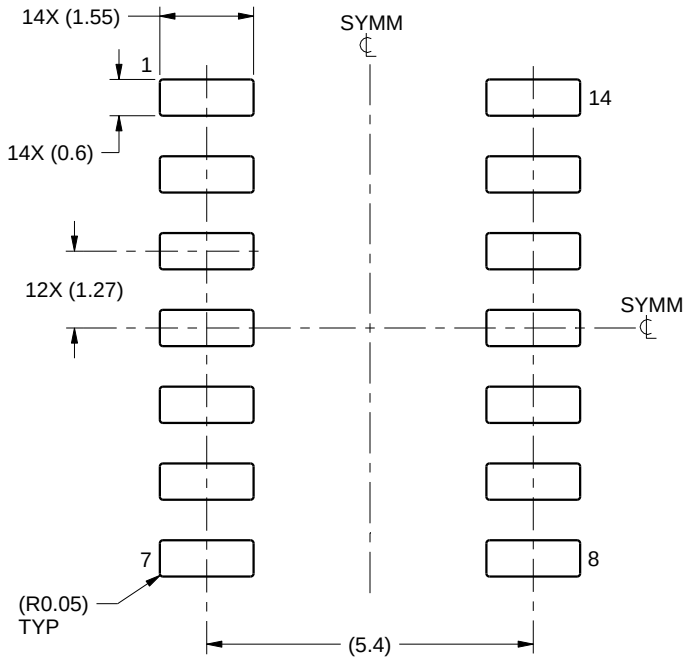
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

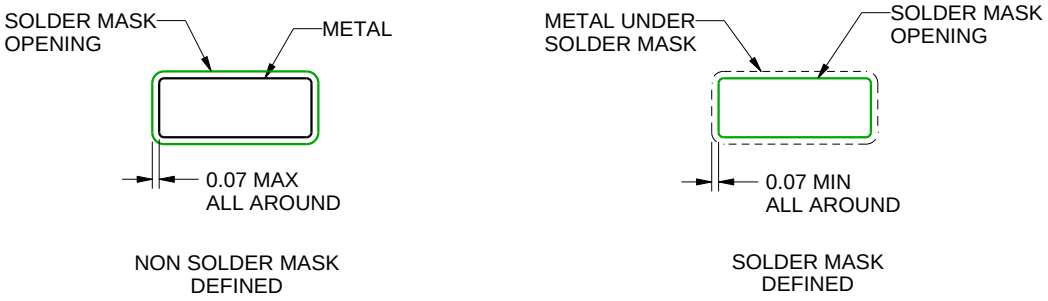


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

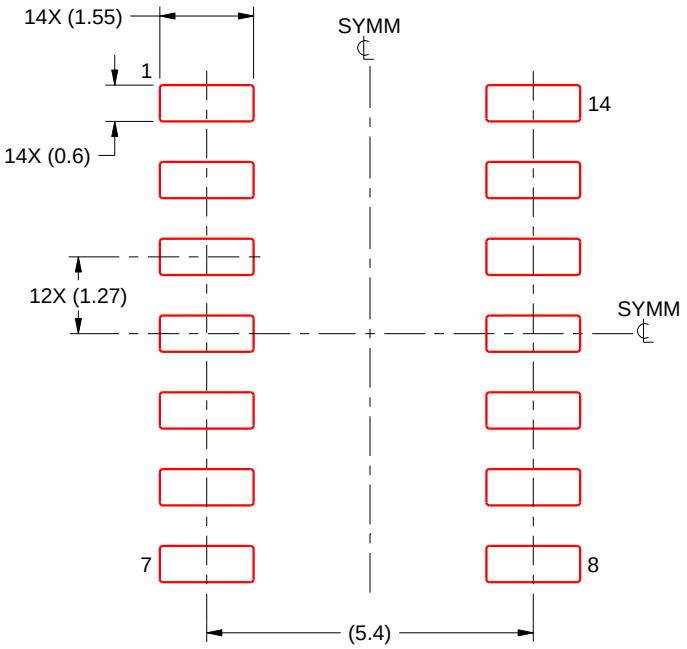
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

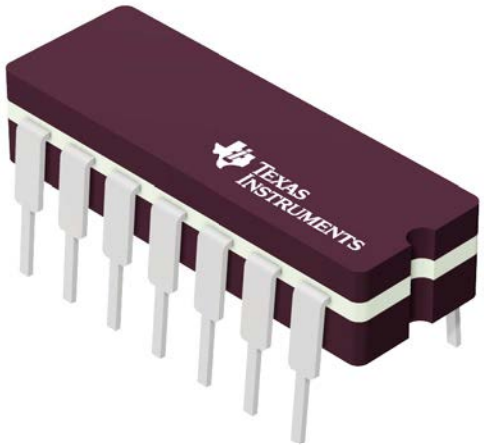
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

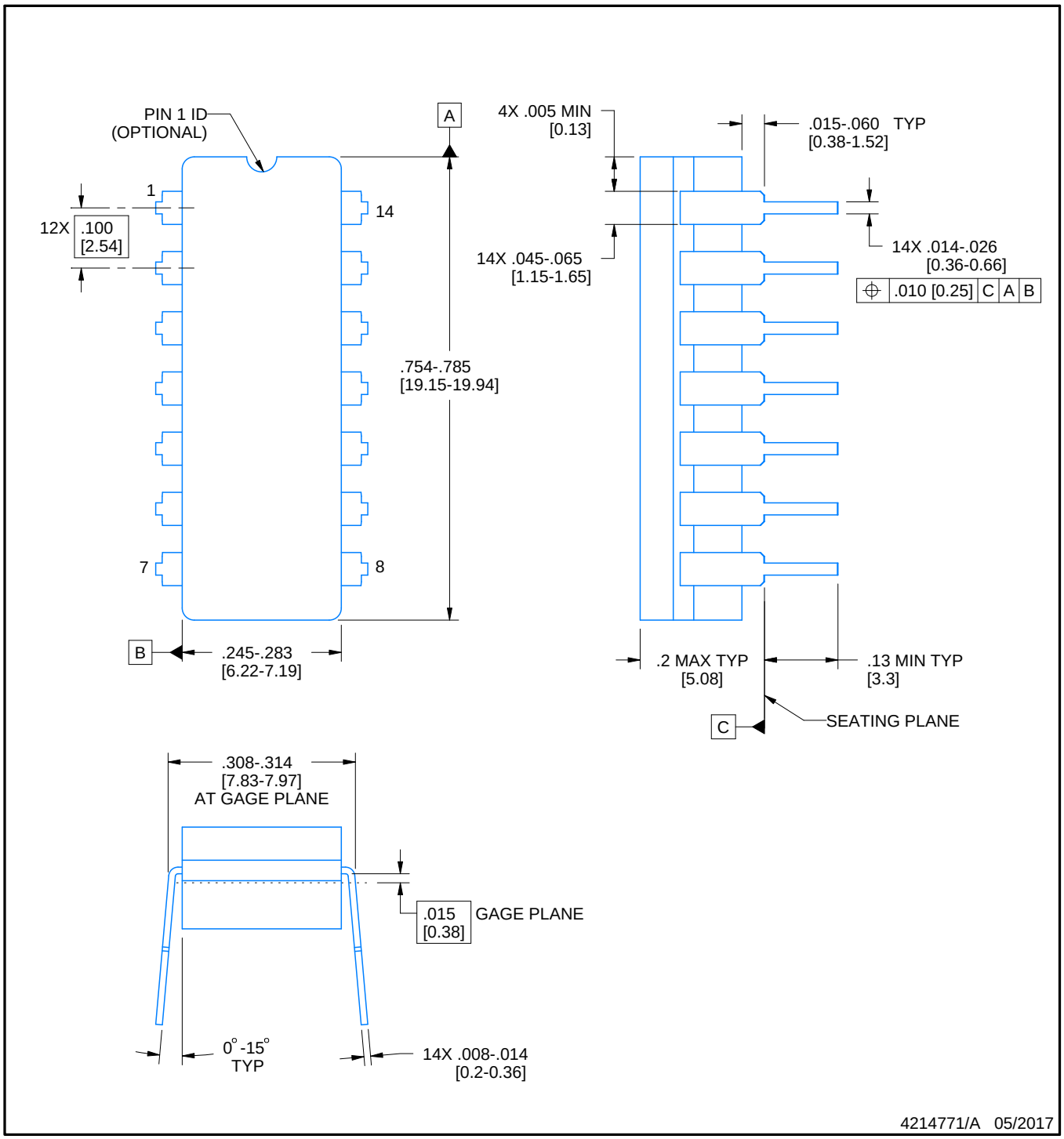
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

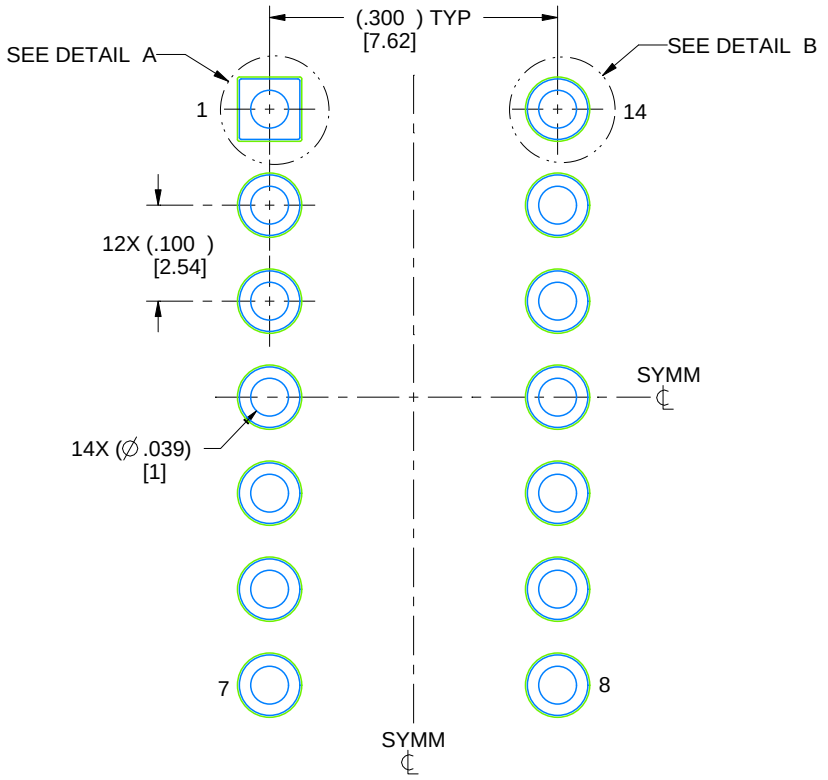
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

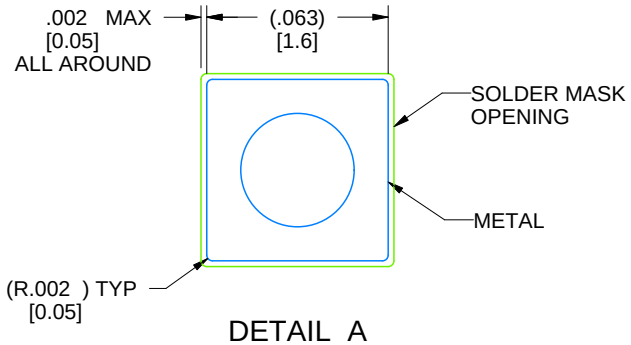
J0014A

CDIP - 5.08 mm max height

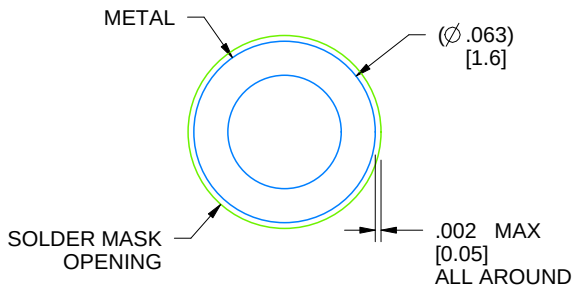
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



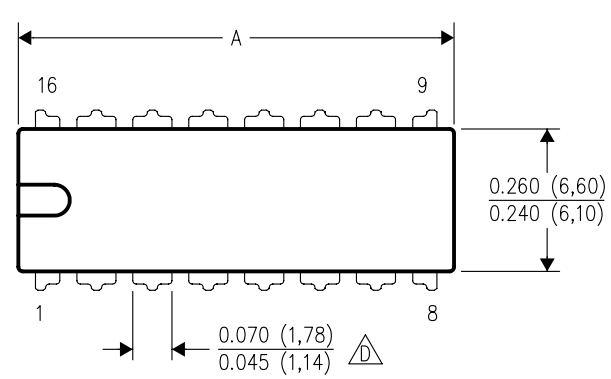
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

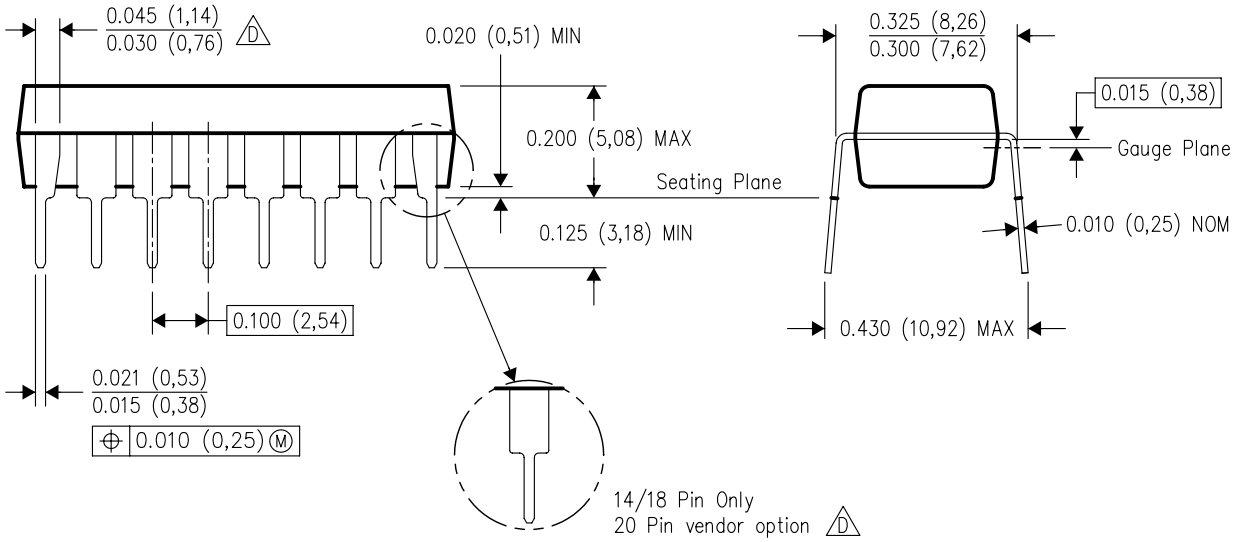
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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