TEXAS INSTRUMENTS
CSD16322Q5
ZHCSTH0C – AUGUST 2009 – REVISED OCTOBER 2023

# N 沟道 NexFET™ 功率 MOSFET

## 1 特性

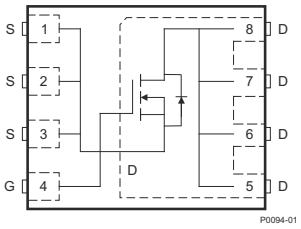
- 针对 5V 栅极驱动进行了优化
- 超低 $Q_g$ 和 $Q_{gd}$
- 低热阻
- 具有雪崩能力
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- SON 5mm × 6mm 塑料封装

## 2 应用

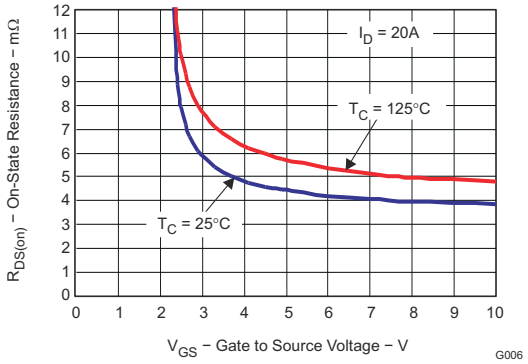
- 网络、电信和计算系统中的负载点同步降压转换器
- 同步或控制 FET 应用

## 3 说明

NexFET™ 功率 MOSFET 旨在更大限度地减少功率转换应用中的损耗，并针对 5V 栅极驱动应用进行了优化。




顶视图




$R_{DS(on)}$ 与 $V_{GS}$ 间的关系

### 产品概要

| | | | | |
|---|---|---|---|---|
| $V_{DS}$ | 漏源极电压 | 25 | | V |
| $Q_g$ | 总栅极电荷 (4.5V) | 6.8 | | nC |
| $Q_{gd}$ | 栅漏栅极电荷 | 1.3 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS}$=3V | 5.4 | mΩ |
| | | $V_{GS}$ = 4.5V | 4.6 | mΩ |
| | | $V_{GS}$ = 8V | 3.9 | mΩ |
| $V_{GS(th)}$ | 阈值电压 | 1.1 | | V |

### 订购信息

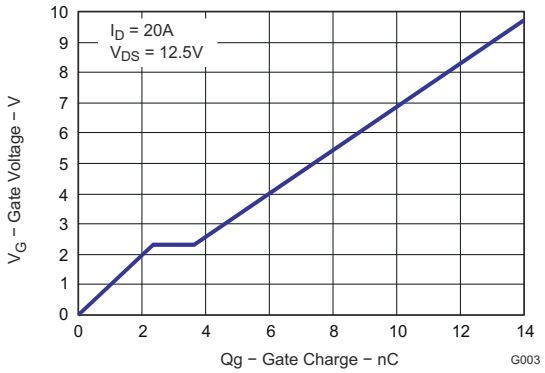
| 器件 | 封装 | 介质 | 数量 | 出货 |
|---|---|---|---|---|
| CSD16322Q5 | SON 5mm × 6mm 塑料封装 | 13 英寸卷带 | 2500 | 卷带包装 |

### 绝对最大额定值

| $T_A$ = 25°C 时测得，除非另外注明 | | 值 | 单位 |
|---|---|---|---|
| $V_{DS}$ | 漏源极电压 | 25 | V |
| $V_{GS}$ | 栅源电压 | +10 / –8 | V |
| $I_D$ | 持续漏极电流，$T_C$ = 25°C | 97 | A |
| | 持续漏极电流(1) | 21 | A |
| $I_{DM}$ | 脉冲漏极电流，$T_A$ = 25°C(2) | 136 | A |
| $P_D$ | 功率耗散(1) | 3.1 | W |
| $T_J$，$T_{STG}$ | 运行结温和储存温度范围 | -55 至 150 | °C |
| $E_{AS}$ | 雪崩能量，单一脉冲<br>$I_D$ = 50A，L = 0.1mH，$R_G$ = 25Ω | 125 | mJ |

(1) 典型 $R_{\theta JA}$ = 39°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm$^2$)、2oz、0.071mm 厚的铜焊盘时）。

(2) 脉冲持续时间 ≤ 300µs，占空比 ≤ 2%




栅极电荷

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision B (May 2010) to Revision C (October 2023) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 7 |

| Changes from Revision A (April 2010) to Revision B (May 2010) | Page |
|---|---|
| • Changed $R_{DS(on)}$, $V_{GS}$ = 3 V in the Electrical Characteristics table From: 7 To: 7.2 in the max column | 3 |

| Changes from Revision * (August 2009) to Revision A (April 2010) | Page |
|---|---|
| • 将“绝对最大额定值”的注释 1 从“$R_{\theta JA}$ = 39°C/W”更改为“典型 $R_{\theta JA}$ = 39°C/W” | 1 |
| • Changed 图 7-1 text From: $R_{\theta JA}$ = 99°C/W To: Typical $R_{\theta JA}$ = 98°C/W | 4 |
| • Changed 图 7-10 text From: $R_{\theta JA}$ = 99°C/W To: Typical $R_{\theta JA}$ = 98°C/W | 4 |
| • Changed 图 7-11 X-axis values | 4 |

## 5 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 25 | | | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V | | | 1 | µA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = +10/–8 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.9 | 1.1 | 1.4 | V |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 3 V, $I_D$ = 20 A | | 5.4 | 7.2 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 20 A | | 4.6 | 5.8 | mΩ |
| | | $V_{GS}$ = 8 V, $I_D$ = 20 A | | 3.9 | 5 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15 V, $I_D$ = 20 A | | 106 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 12.5 V, $f$ = 1 MHz | | 1050 | 1365 | pF |
| $C_{oss}$ | Output Capacitance | | | 740 | 950 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 55 | 70 | pF |
| $R_G$ | Series Gate Resistance | | | 1.1 | 2.2 | Ω |
| $Q_g$ | Gate Charge Total (4.5 V) | $V_{DS}$ = 12.5 V, $I_D$ = 20 A | | 6.8 | 9.7 | nC |
| $Q_{gd}$ | Gate Charge Gate to Drain | | | 1.3 | | nC |
| $Q_{gs}$ | Gate Charge Gate to Source | | | 2.4 | | nC |
| $Q_{g(th)}$ | Gate Charge at Vth | | | 1.3 | | nC |
| $Q_{oss}$ | Output Charge | $V_{DS}$ = 13 V, $V_{GS}$ = 0 V | | 17 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 12.5 V, $V_{GS}$ = 4.5 V, $I_D$ = 20 A, $R_G$ = 2 Ω | | 6.1 | | ns |
| $t_r$ | Rise Time | | | 10.7 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 12.3 | | ns |
| $t_f$ | Fall Time | | | 3.7 | | ns |
| **Diode Characteristics** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$ = 20 A, $V_{GS}$ = 0 V | | 0.8 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$ = 13 V, $I_F$ = 20 A, di/dt = 300 A/µs | | 19 | | nC |
| $t_{rr}$ | Reverse Recovery Time | $V_{DD}$ = 13 V, $I_F$ = 20 A, di/dt = 300 A/µs | | 21 | | ns |

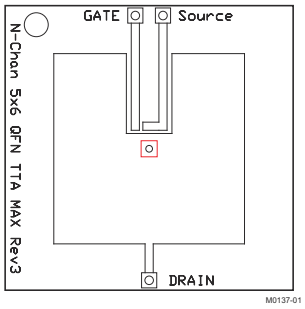
## 6 Thermal Characteristics

($T_A$ = 25°C unless otherwise stated)

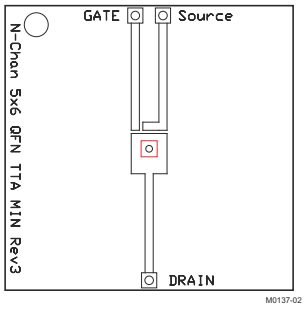
| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case(1) | | | 2.4 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient(1) (2) | | | 50 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 123°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

## 7 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

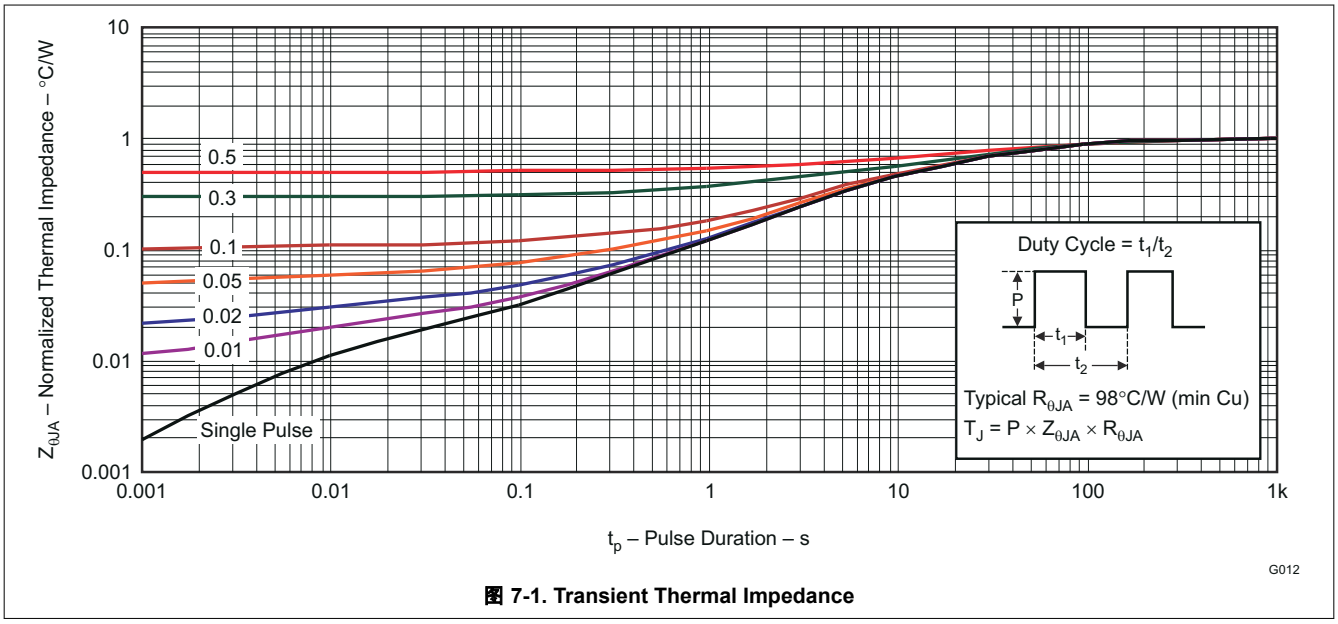



**图 7-1. Transient Thermal Impedance**

# 7 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

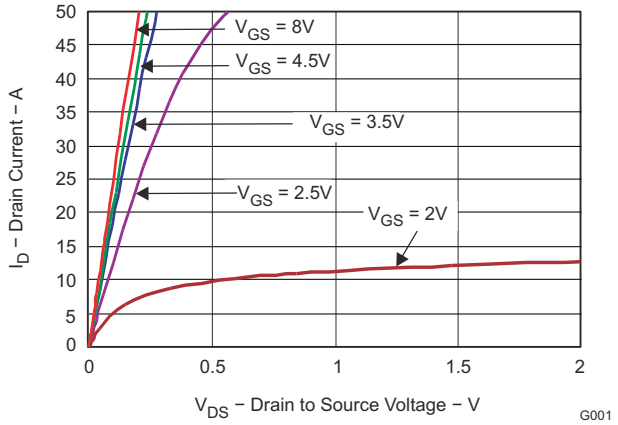



**图 7-2. Saturation Characteristics**

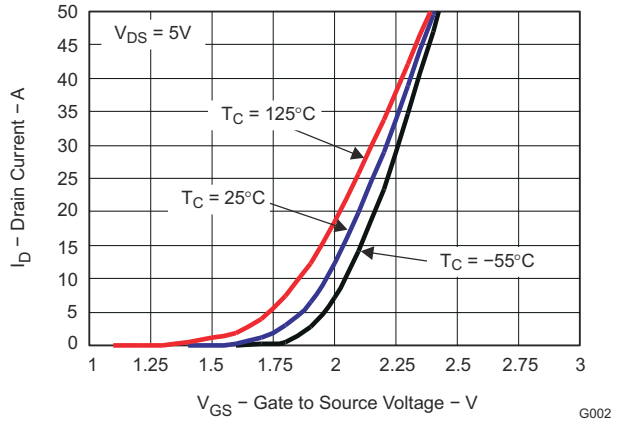



**图 7-3. Transfer Characteristics**

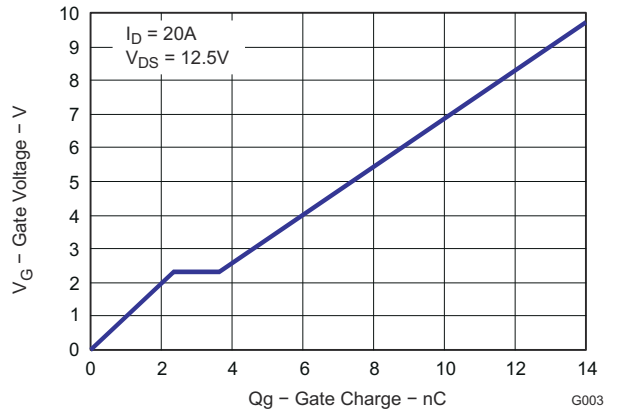



**图 7-4. Gate Charge**

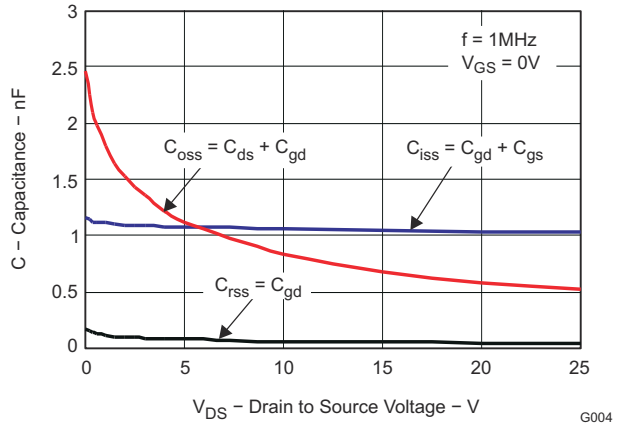



**图 7-5. Capacitance**

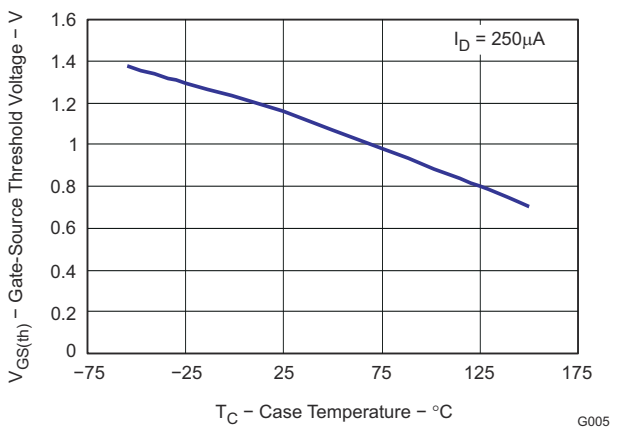



**图 7-6. Threshold Voltage vs. Temperature**

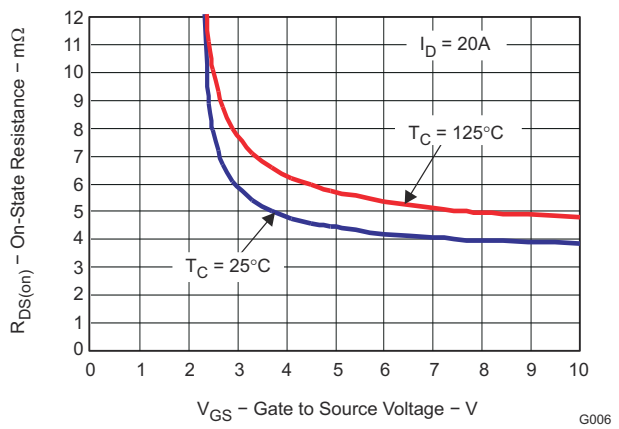



**图 7-7. On-State Resistance vs. Gate to Source Voltage**

## 7 Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

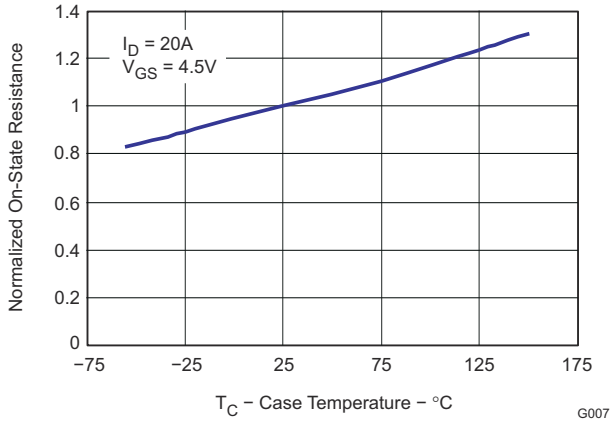



**图 7-8. Normalized On-State Resistance vs. Temperature**

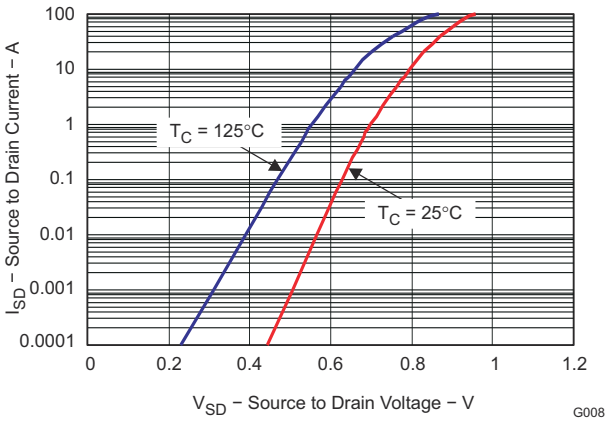



**图 7-9. Typical Diode Forward Voltage**

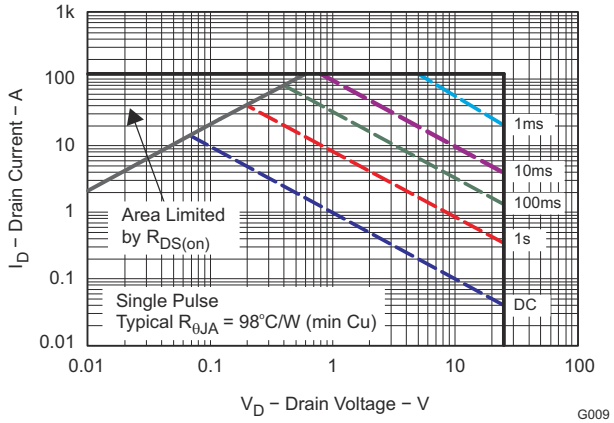



**图 7-10. Maximum Safe Operating Area**

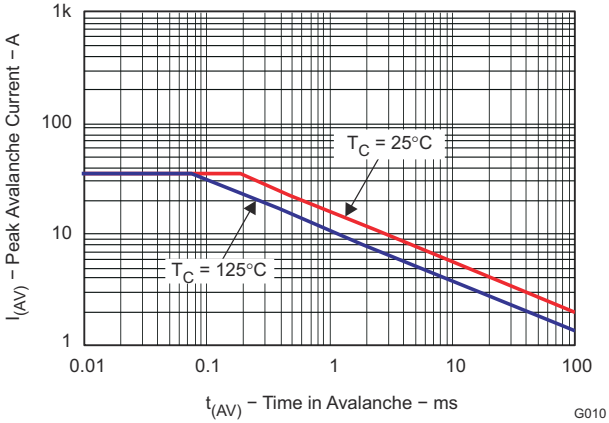



**图 7-11. Single Pulse Unclamped Inductive Switching**

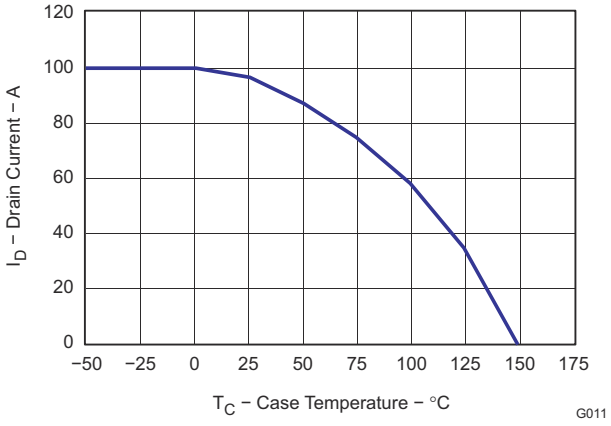



**图 7-12. Maximum Drain Current vs. Temperature**

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD16322Q5 | ACTIVE | VSON-CLIP | DQH | 8 | 2500 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16322 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

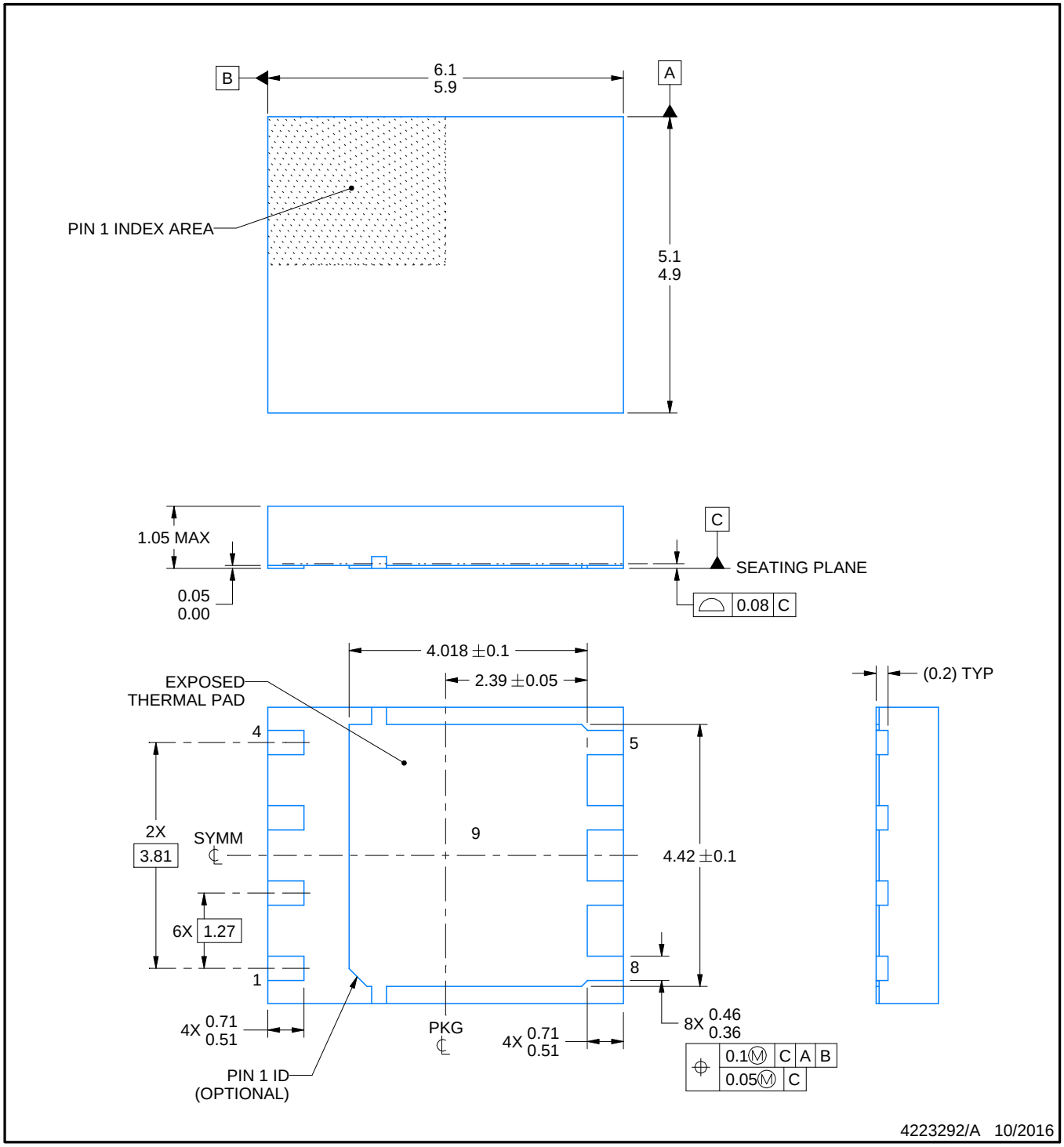
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OUTLINE

## DQH0008A

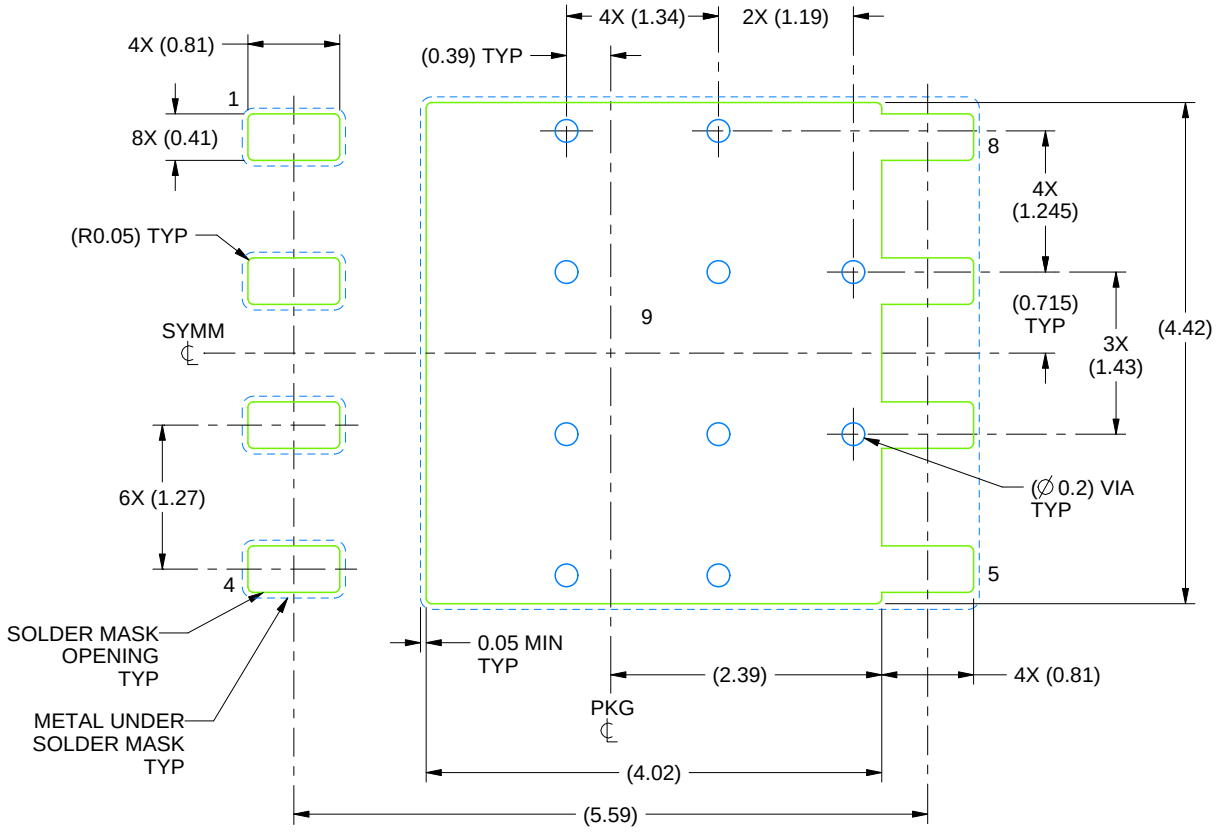
## VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

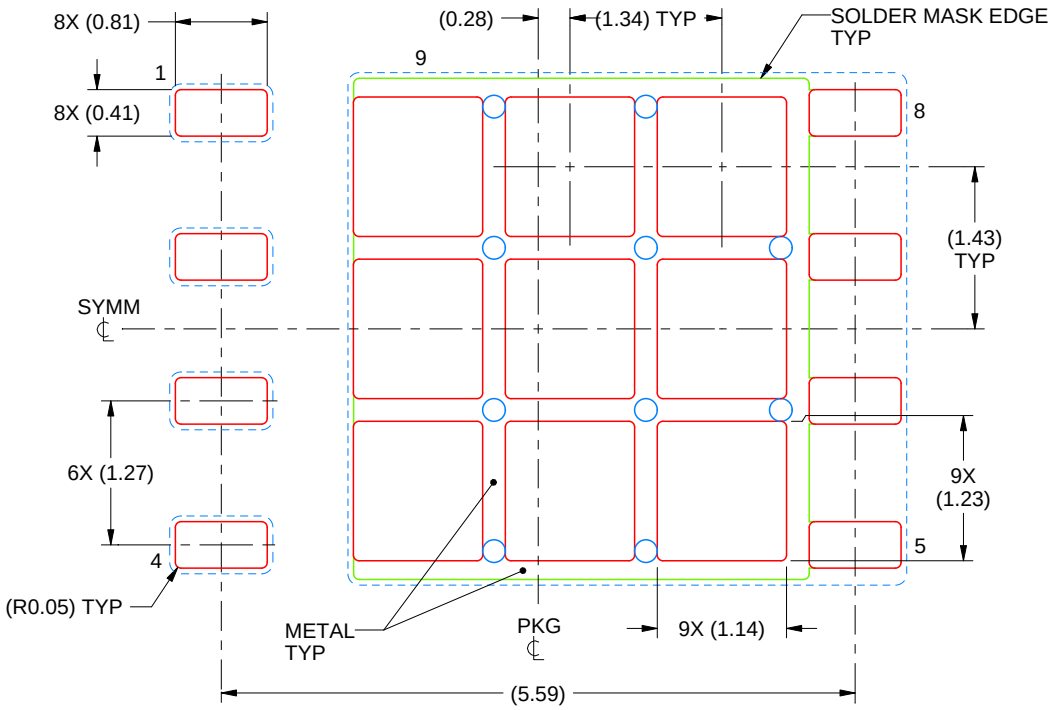



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

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