CSD17556Q5B 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

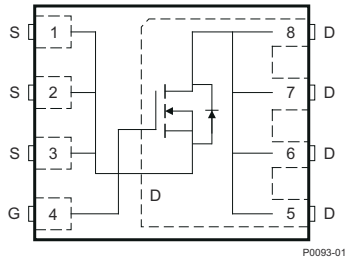
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅
- 符合 RoHS 标准
- 无卤素
- SON 3.3mm × 3.3mm 塑料封装

2 应用

- 网络互联、电信和计算系统中的负载点同步降压
- 针对控制 FET 应用进行了优化

3 说明

这款 30V 5.5mΩ 3.3mm × 3.3mm SON NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



顶视图

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	9.0		nC
Q_{gd}	栅极电荷（栅极到漏极）	2.3		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	6.5	mΩ
		V_{GS} = 10V	5.5	mΩ
$V_{GS(th)}$	阈值电压	1.5		V

订购信息(1)

器件	数量	介质	封装	出货
CSD17552Q3A	2500	13 英寸卷带	SON 3.3mm × 3.3mm 塑料封装	卷带包装
CSD17552Q3AT	250	7 英寸卷带		

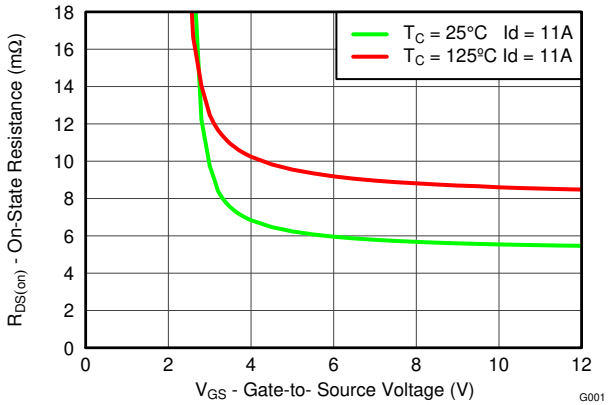
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

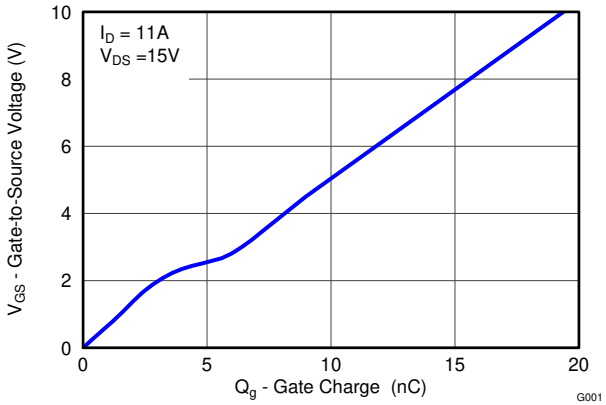
T_A = 25°C 时测得，除非另有说明		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流，T_C = 25°C	60	A
	持续漏极电流（受芯片限制）	74	A
	持续漏极电流，T_A=25°C 时测得(1)	15	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	84	A
P_D	功率耗散(1)	2.6	W
T_J、T_{stg}	工作结温，贮存温度	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D= 30A，L = 0.1mH，R_G = 25Ω	45	mJ

(1) $R_{\theta JA}$ = 48°C/W，这是在 0.06 英寸 (1.52mm) 厚 FR4 PCB 上的 1 平方英寸 (6.45cm^2)、2oz、0.071mm 厚铜焊盘上测得的典型值。

(2) 脉冲持续时间 ≤ 300µs，占空比 ≤ 2%



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

内容

4 规格

4.1 电气特性

（T_A = 25°C 时测得，除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
静态特性						
BV_{DSS}	漏源电压	V_{GS} = 0V，I_D = 250μA	30			V
I_{DSS}	漏源漏电流	V_{GS} = 0V，V_{DS} = 24V			1	μA
I_{GSS}	栅源漏电流	V_{DS} = 0V，V_{GS} = 20V			100	nA
$V_{GS(th)}$	栅源阈值电压	V_{DS} = V_{GS}，I_D = 250μA	1.1	1.5	1.9	V
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V，I_D = 11A		6.5	8.1	mΩ
		V_{GS} = 10V，I_D = 11A		5.5	6.0	mΩ
g_{fs}	跨导	V_{DS} = 15V，I_D = 11A		106		S
动态特性						
C_{iss}	输入电容	V_{GS} = 0V，V_{DS} = 15V，f = 1MHz		1580	2050	pF
C_{oss}	输出电容			385	500	pF
C_{rss}	反向传输电容			28	36	pF
R_G	串联栅极电阻			.9	1.8	Ω
Q_g	栅极电荷总量 (4.5V)	V_{DS} = 15V，I_D = 11A		9	12	nC
Q_{gd}	栅漏栅极电荷			2.3		nC
Q_{gs}	栅极电荷（栅源极）			3.6		nC
$Q_{g(th)}$	V_{th} 下的栅极电荷			1.8		nC
Q_{oss}	输出电荷	V_{DS} = 15V，V_{GS} = 0V		11		nC
$t_{d(on)}$	导通延时时间	V_{DS} = 15V，V_{GS} = 4.5V，I_{DS} = 11A，R_G = 2Ω		7.2		ns
t_r	上升时间			7.4		ns
$t_{d(off)}$	关闭延时时间			11.0		ns
t_f	下降时间			3.4		ns
二极管特性						
V_{SD}	二极管正向电压	I_{SD} = 11A，V_{GS} = 0V		0.8	1	V
Q_{rr}	反向恢复电荷	V_{DS}= 13.5V，I_F = 11A，di/dt = 300A/μs		17		nC
t_{rr}	反向恢复时间			15		ns

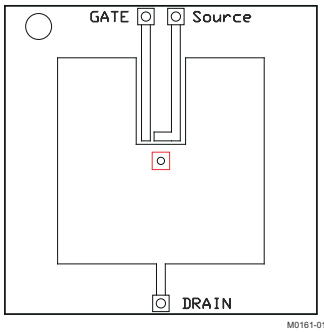
4.2 热性能信息

（T_A = 25°C 时测得，除非另有说明）

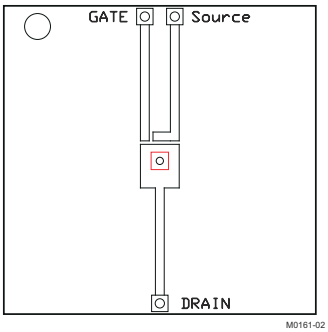
热指标		最小值	典型值	最大值	单位
$R_{\theta JC}$	结至外壳热阻(1)			2.3	°C/W
$R_{\theta JA}$	结至环境热阻(1) (2)			60	°C/W

(1) $R_{\theta JC}$ 是在器件安装在 1.5 英寸 × 1.5 英寸 (3.81cm × 3.81cm)、厚度为 0.06 英寸 (1.52mm) 的 FR4 PCB 上 1 平方英寸 (6.45cm^2)、2oz（厚度为 0.071mm）的铜焊盘上测得的。$R_{\theta JC}$ 由设计指定，而 $R_{\theta JA}$ 由用户的电路板设计确定。

(2) 器件安装在具有 1 平方英寸 (6.45cm^2)、2oz（厚度 0.071mm）铜焊盘的 FR4 材料上。



最大 $R_{\theta JA}$ = 60°C/W，安装在 1 平方英寸 (6.45cm^2) 2oz（厚度 0.071mm）铜焊盘上时。



最大 $R_{\theta JA}$ = 146°C/W，安装在最小面积的 2oz（厚度为 0.071mm）铜焊盘上时。

4.3 典型 MOSFET 特性

（T_A = 25°C 时测得，除非另有说明）

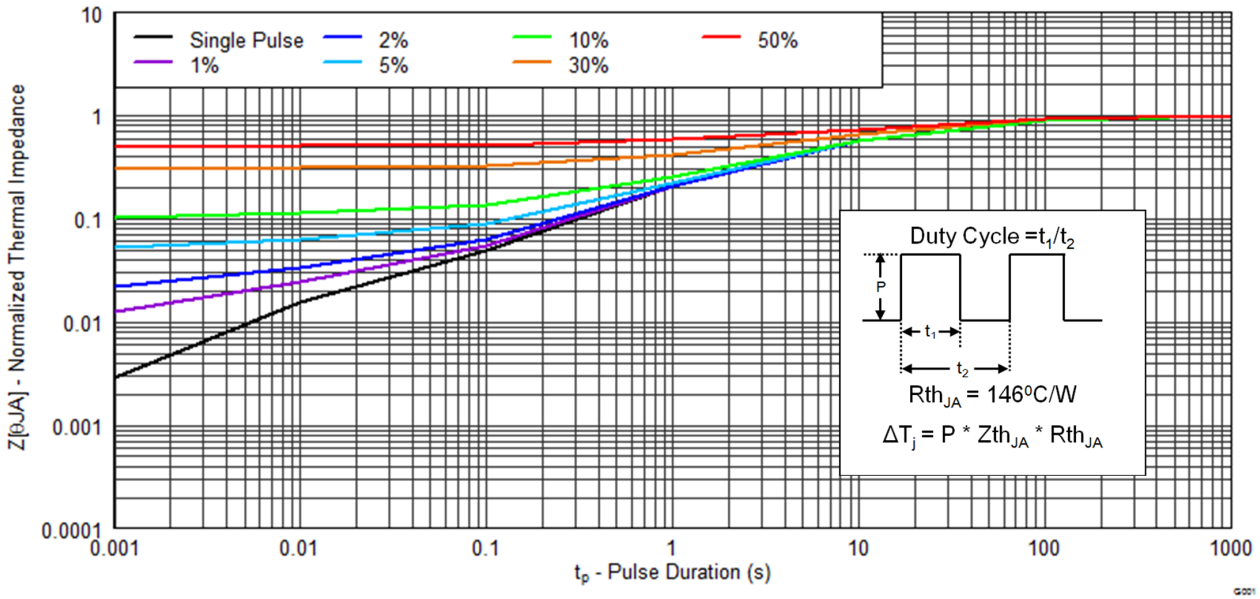


图 4-1. 瞬态热阻抗

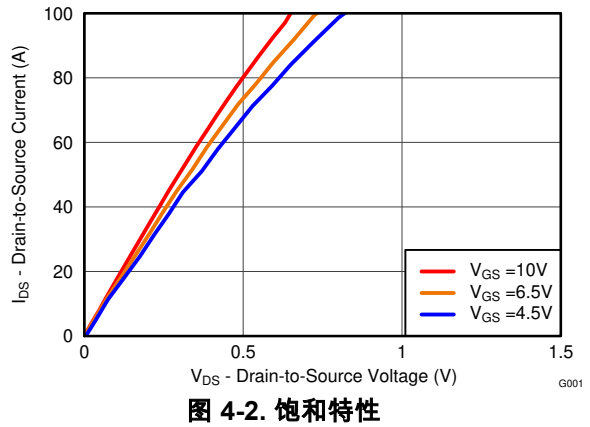


图 4-2. 饱和特性

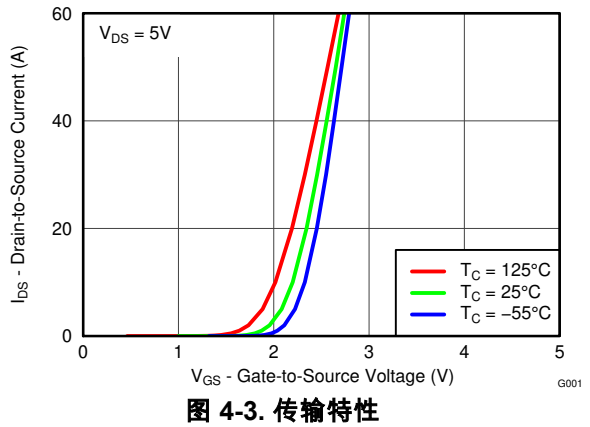


图 4-3. 传输特性

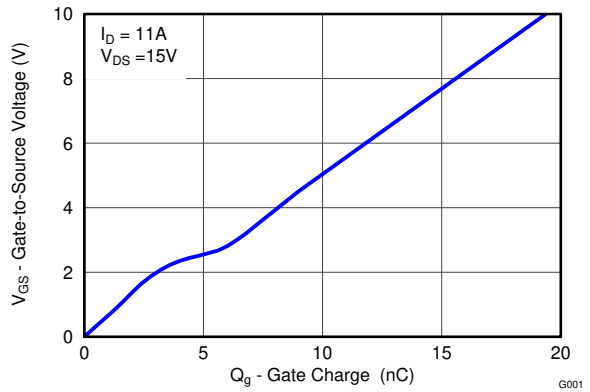


图 4-4. 栅极电荷

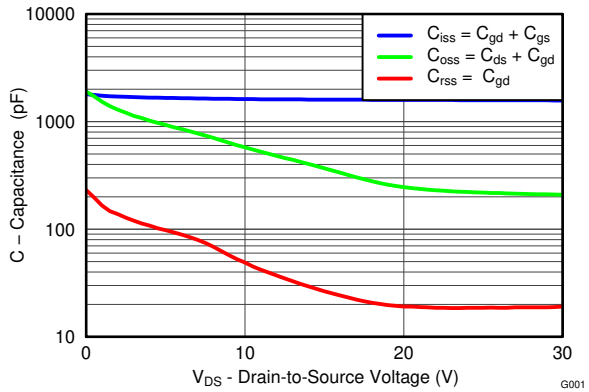


图 4-5. 电容

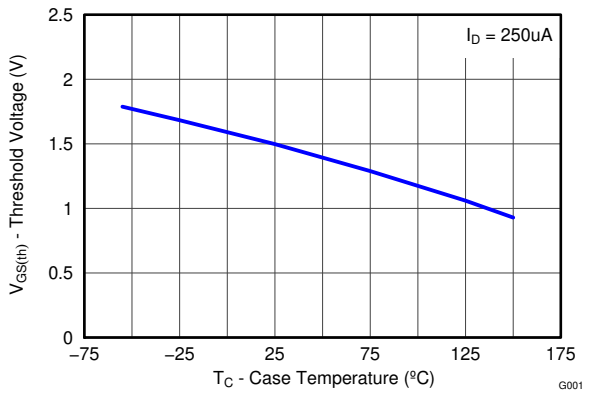


图 4-6. 阈值电压与温度间的关系

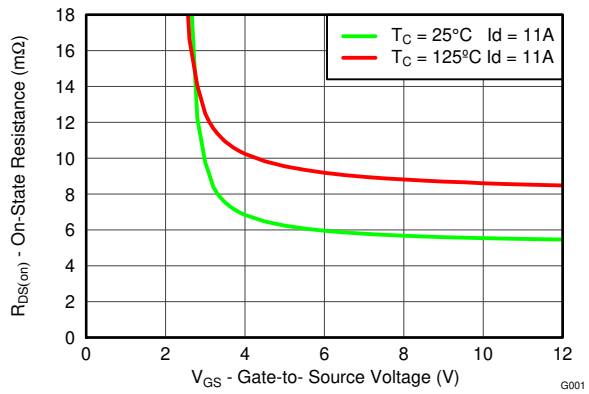


图 4-7. 导通电阻与栅源电压

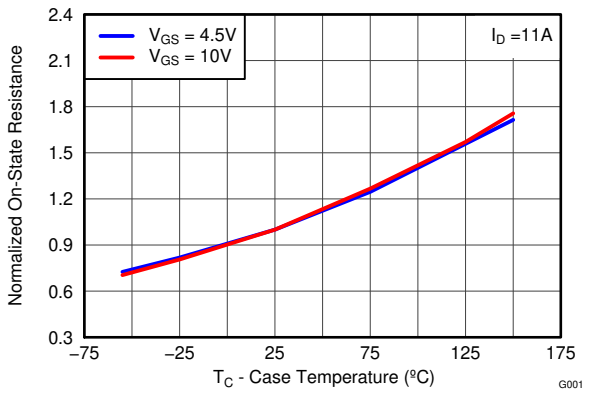


图 4-8. 标准化通态电阻与温度的关系

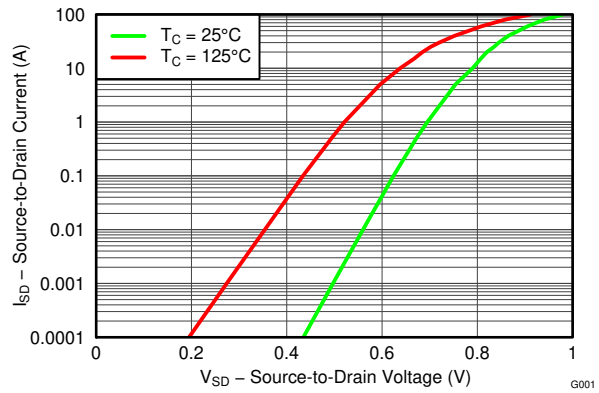


图 4-9. 典型二极管正向电压

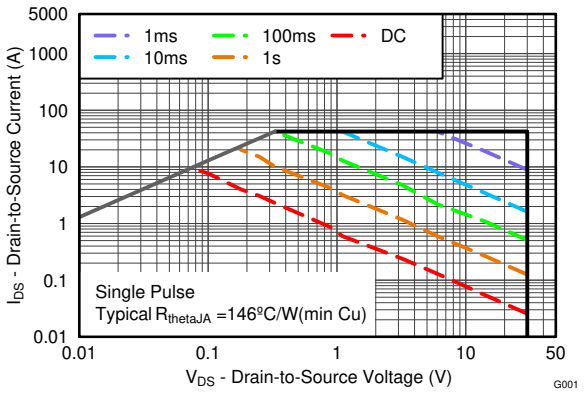


图 4-10. 最大安全工作区

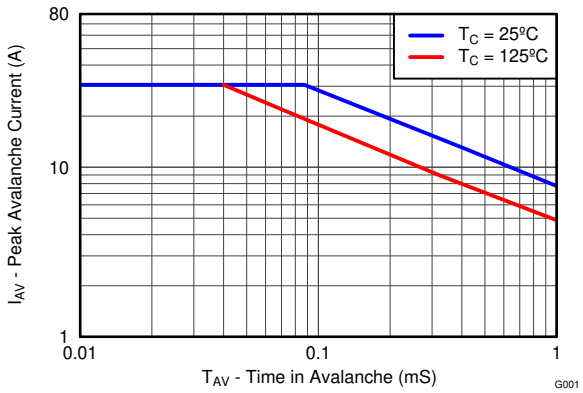


图 4-11. 单脉冲非钳位电感式开关

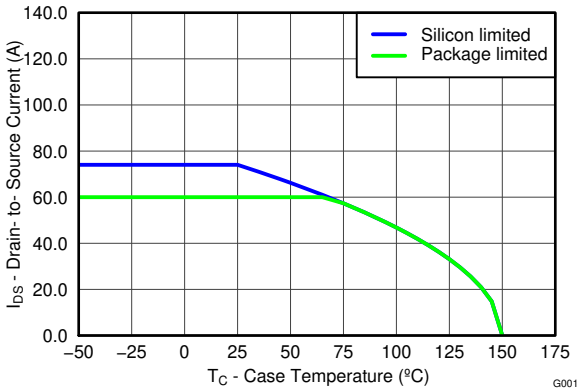


图 4-12. 最大漏极电流与温度间的关系

5 器件和文档支持

5.1 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.2 商标

NexFET™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

5.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.4 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (January 2016) to Revision C (November 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的格式	1

Changes from Revision A (June 2014) to Revision B (January 2016)	Page
• 改进了 *节 3* 文本	1

Changes from Revision * (September 2012) to Revision A (June 2014)	Page
• 将“无铅引脚镀层”特性更改成了“无铅”	1

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17552Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17552	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

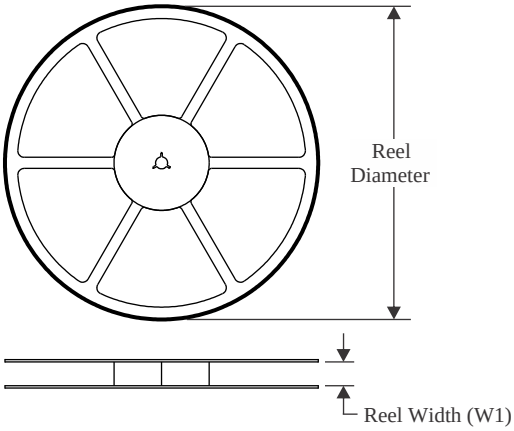
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

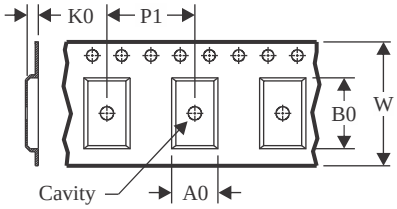
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

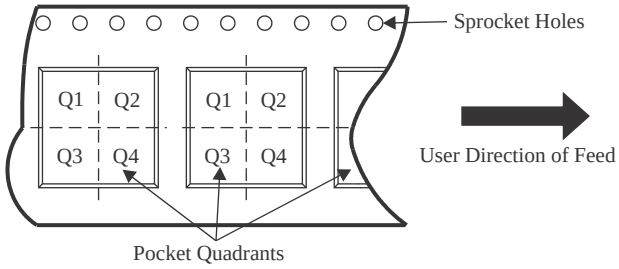


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

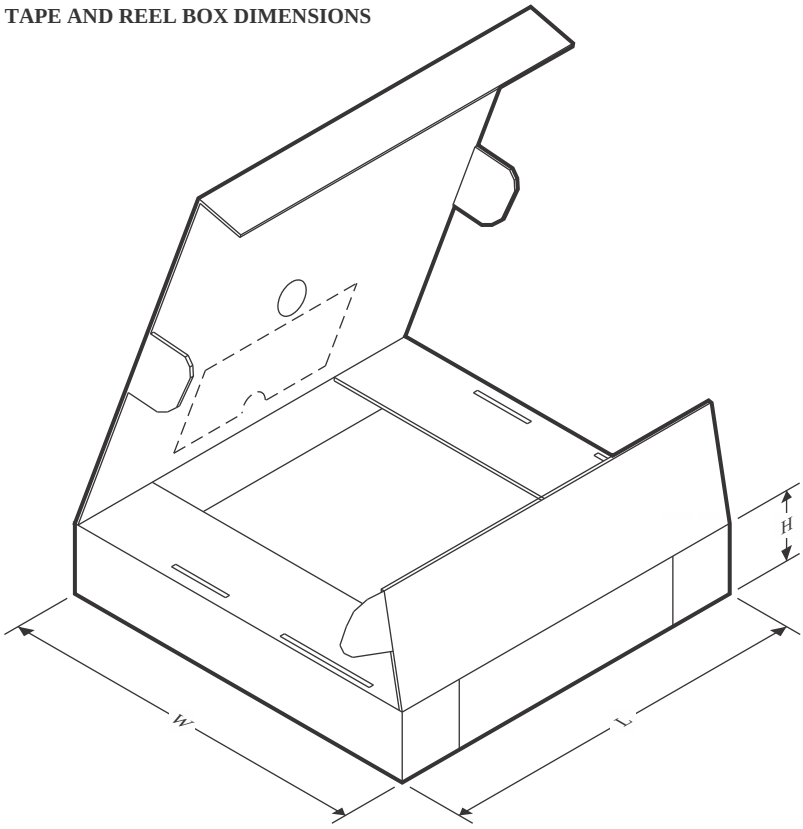
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17552Q3A	VSONP	DNH	8	2500	330.0	12.4	3.6	3.6	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

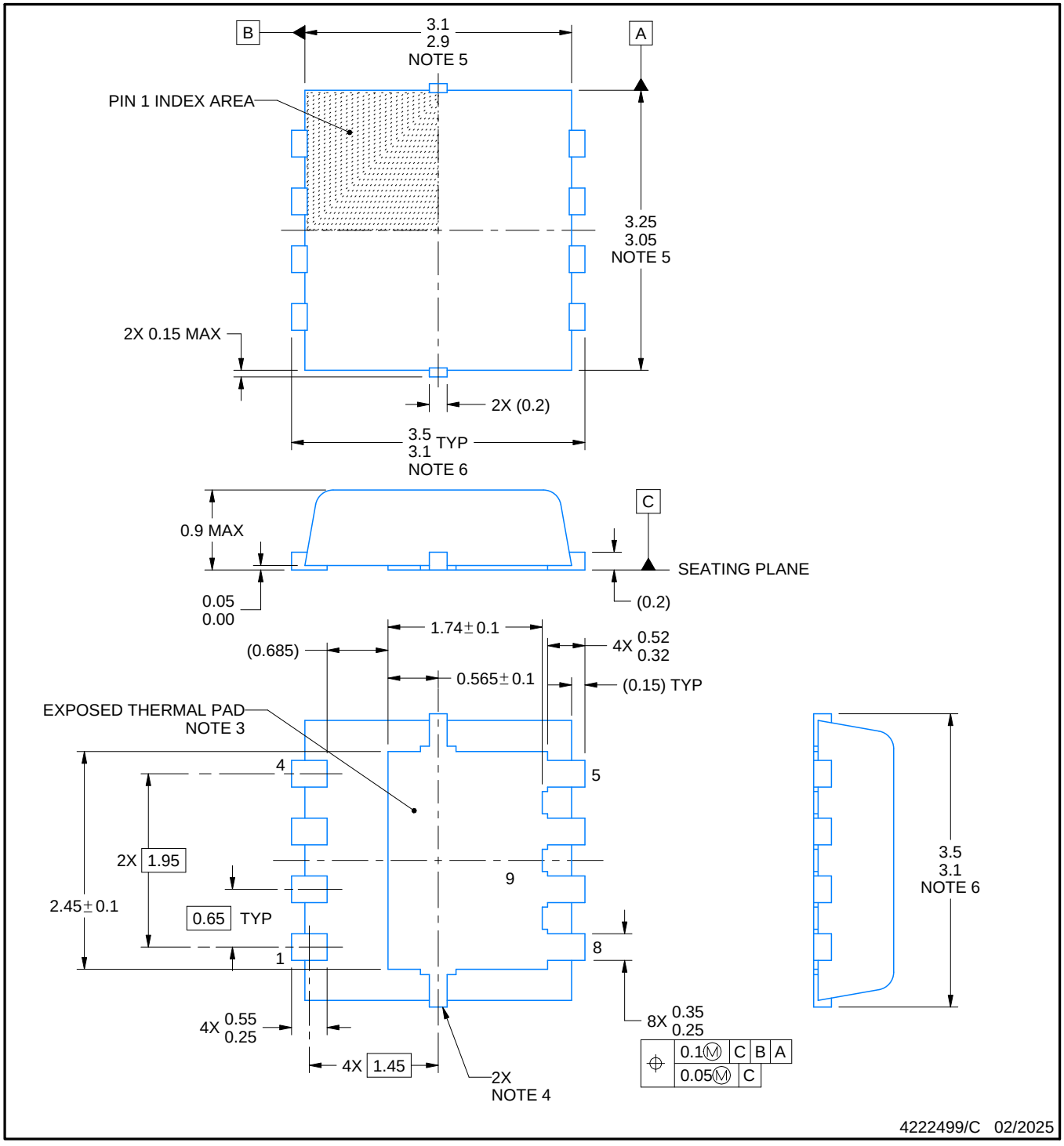
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17552Q3A	VSONP	DNH	8	2500	340.0	340.0	38.0

PACKAGE OUTLINE

DNH0008A

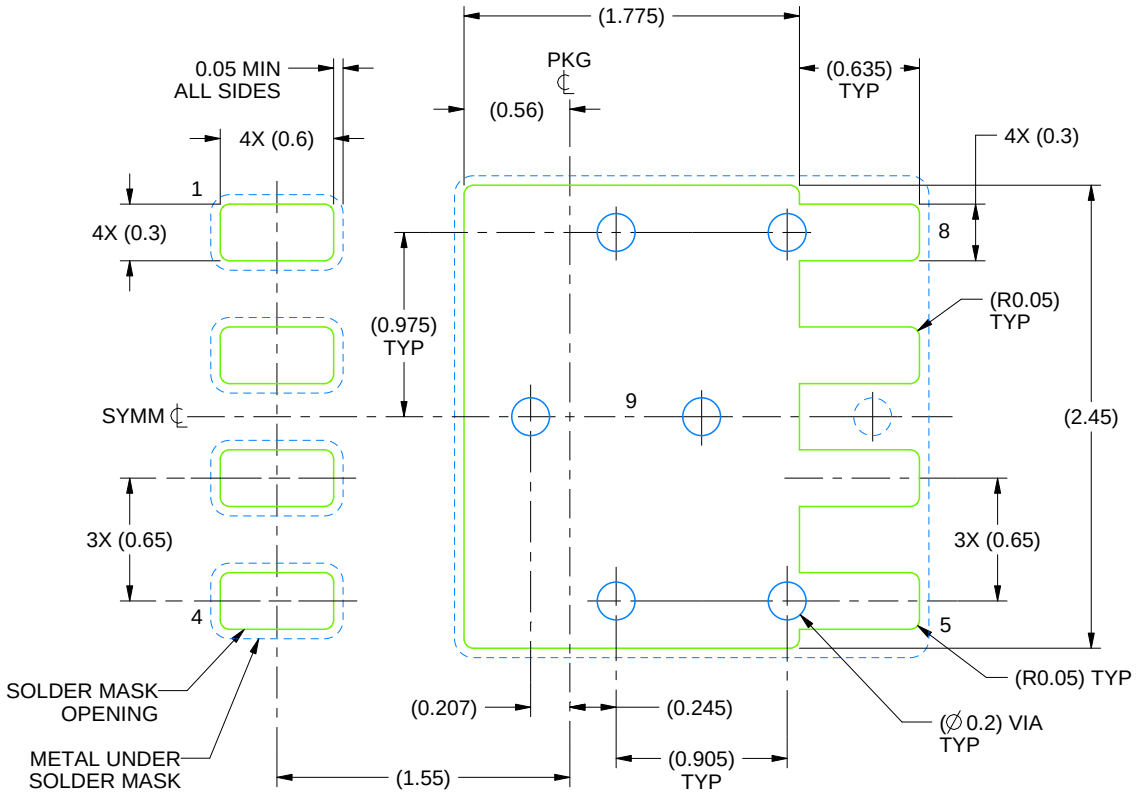
VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

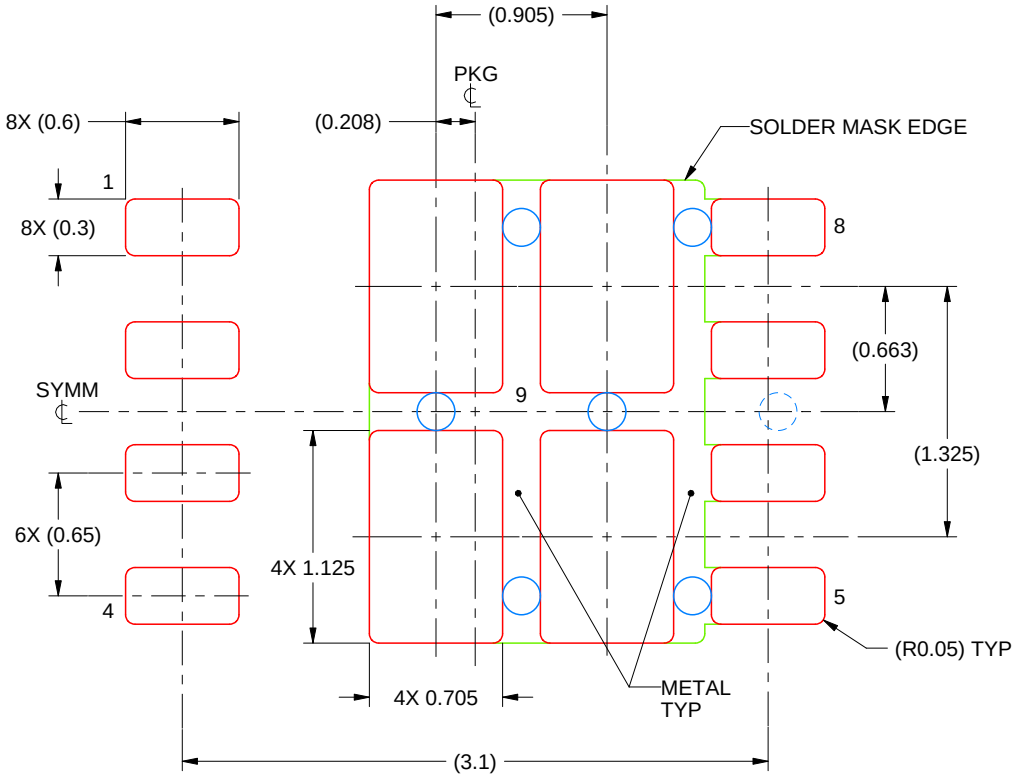
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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