CSD17575Q3 30V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(on)}$
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

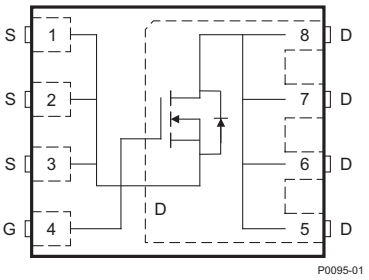
2 应用

- 用于网络互联，电信和计算系统的负载点同步降压转换器
- 已针对同步场效应晶体管 (FET) 应用进行优化

3 说明

这款 1.9mΩ，30V，SON 3×3 NexFET™ 功率 MOSFET 被设计成在功率转换应用中最大限度地降低功率损耗。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	23		nC
Q_{gd}	栅漏栅极电荷	5.4		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5 V	2.6	mΩ
		V_{GS} = 10V	1.9	
V_{th}	阀值电压	1.4		V

订购信息(1)

器件	介质	数量	封装	出货
CSD17575Q3	13 英寸卷带	2500	SON 3.3mm x 3.3mm 塑料封装	卷带封装
CSD17575Q3T	13 英寸卷带	250		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

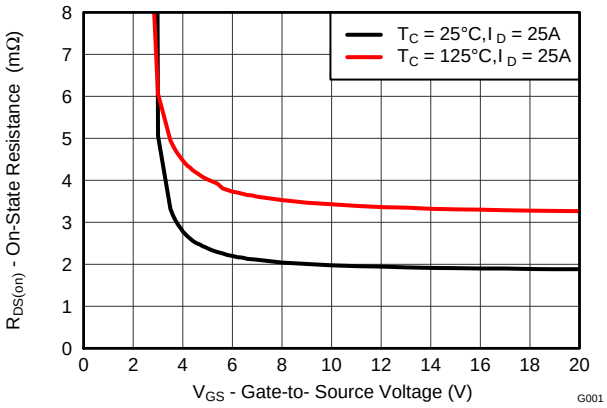
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	60	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	182	
	持续漏极电流(1)	27	
I_{DM}	脉冲漏极电流(2)	240	A
P_D	功率耗散(1)	2.8	W
	功率耗散，T_C = 25°C	108	
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 48，L = 0.1mH，R_G = 25Ω	115	mJ

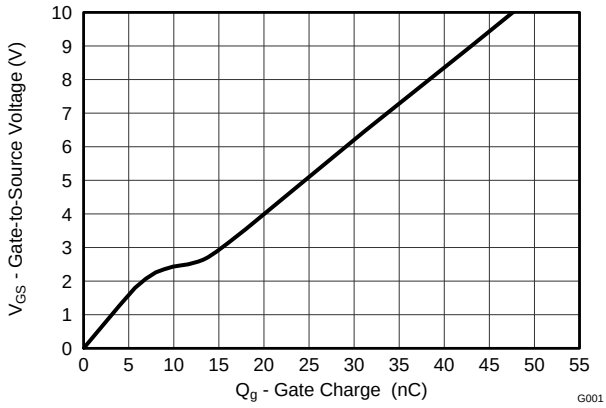
(1) $R_{\theta JA}$ = 45°C/W，这是在一块厚度为 0.060 英寸的 FR4 印刷电路板 (PCB) 上的 1 平方英寸 2 盎司铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.5°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

Changes from Original (June 2014) to Revision A **Page**

- 在机械信息表中增加了 b1、d、d1 和 K 尺寸 ... 9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

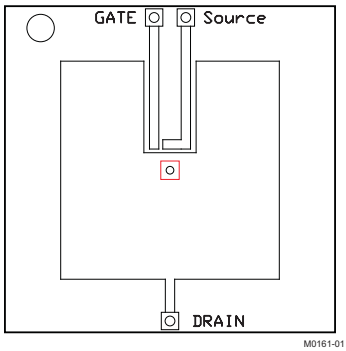
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 25 A		2.6	3.2	mΩ
		V_{GS} = 10 V, I_D = 25 A		1.9	2.3	
g_{fs}	Transconductance	V_{DS} = 3 V, I_D = 25 A		118		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		3400	4420	pF
C_{OSS}	Output Capacitance			393	511	pF
C_{RSS}	Reverse Transfer Capacitance			157	204	pF
R_g	Series Gate Resistance			0.9	1.8	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 25 A		23	30	nC
Q_{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q_{gs}	Gate Charge Gate-to-Source			8.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			4.6		nC
Q_{OSS}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		11.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 4.5 V I_D = 25 A R_G = 2 Ω		4		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15 V, I_F = 25 A, di/dt = 300 A/µs		15		nC
t_{rr}	Reverse Recovery Time			13		ns

5.2 Thermal Information

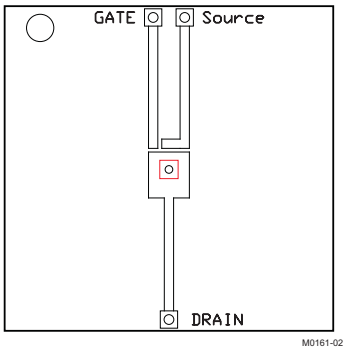
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			55	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), Cu pad on a 1.5-inches × 1.5-inches thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas RθJA is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 2-oz.Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 160°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

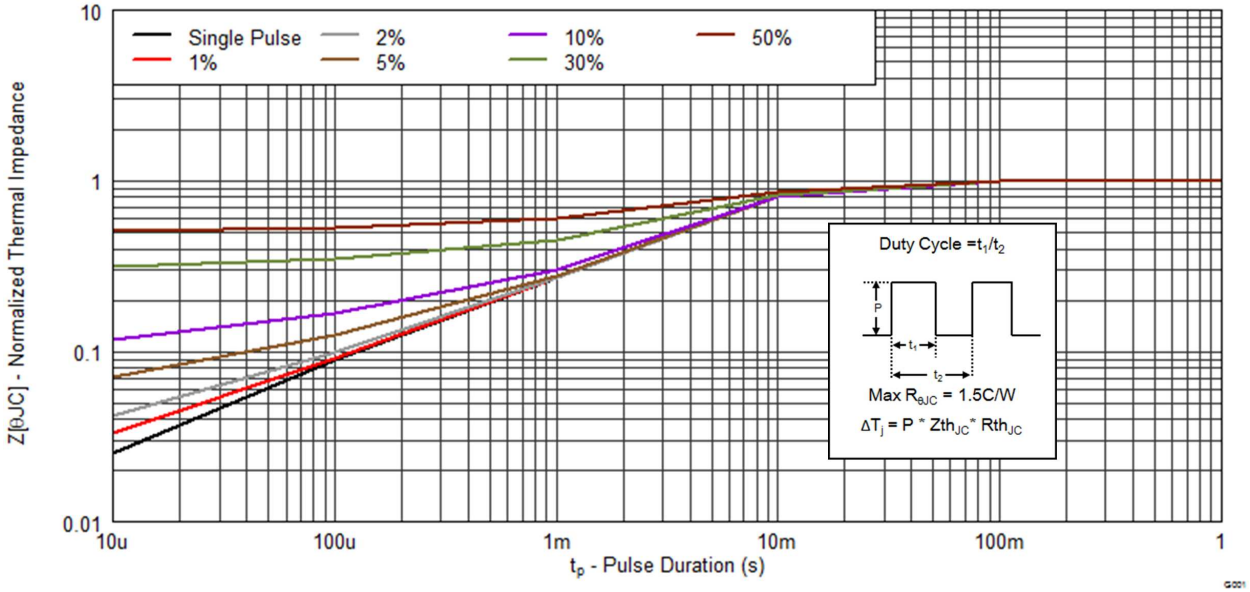


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

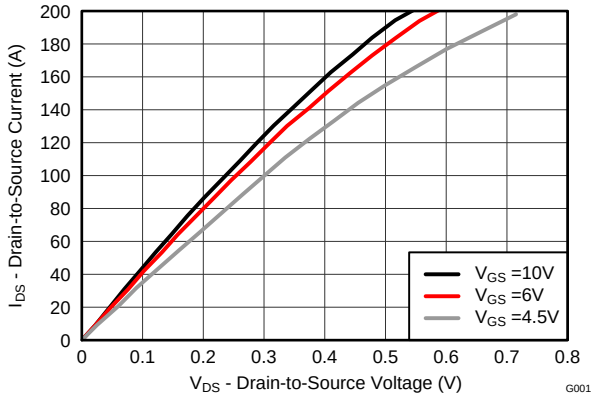


Figure 2. Saturation Characteristics

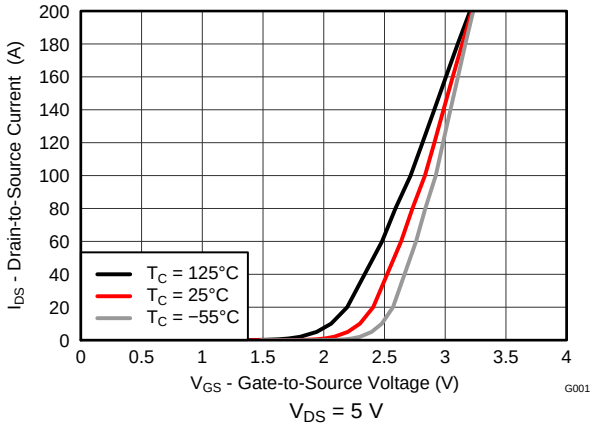


Figure 3. Transfer Characteristics

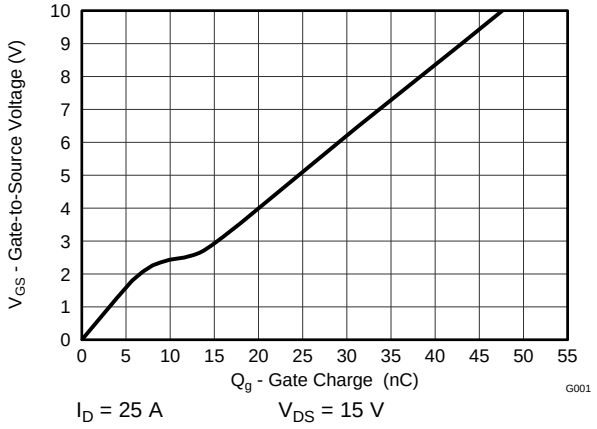


Figure 4. Gate Charge

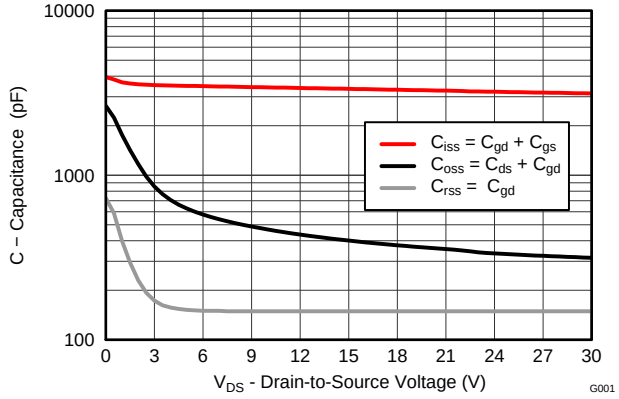


Figure 5. Capacitance

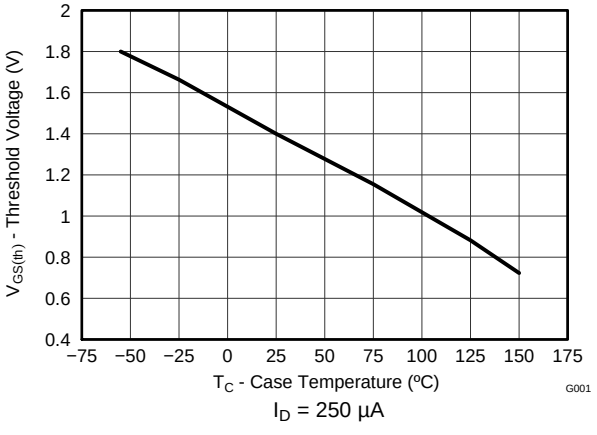


Figure 6. Threshold Voltage vs Temperature

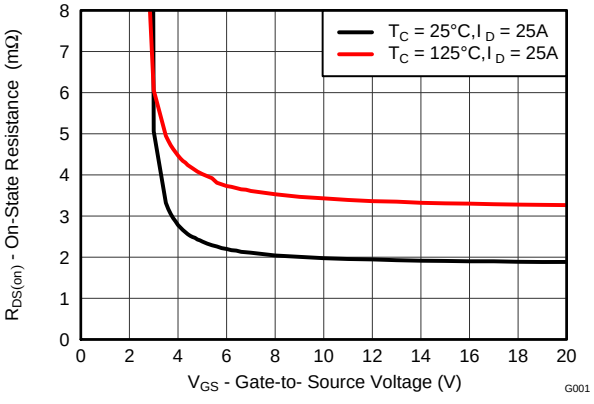


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

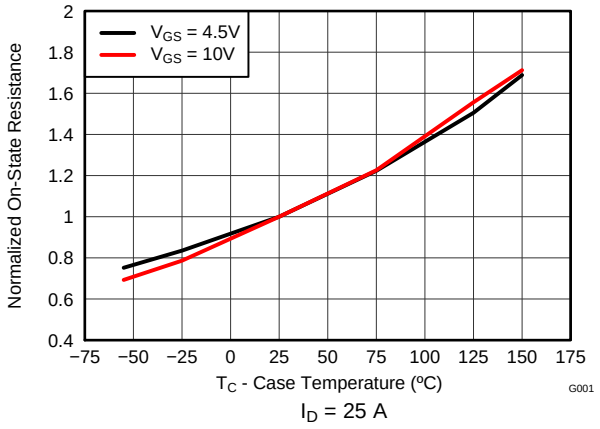


Figure 8. Normalized On-State Resistance vs Temperature

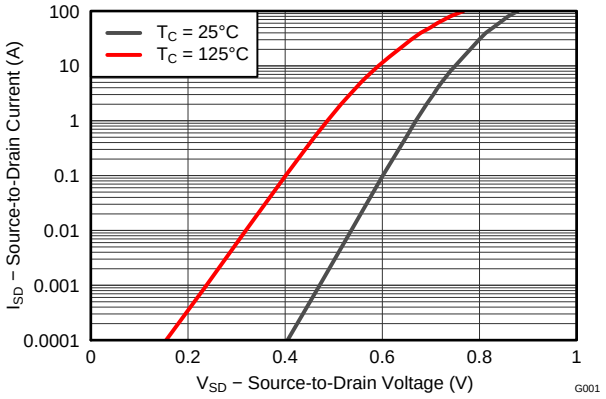


Figure 9. Typical Diode Forward Voltage

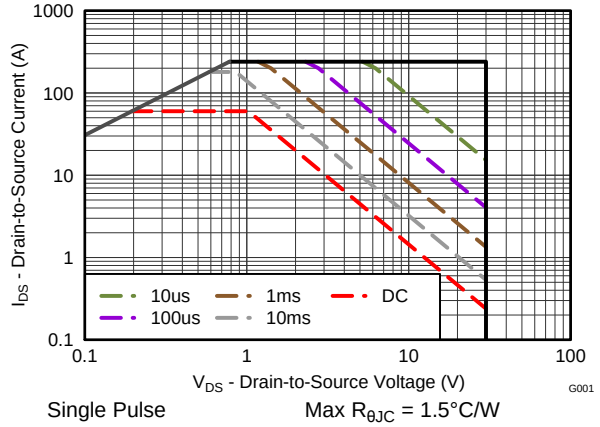


Figure 10. Maximum Safe Operating Area

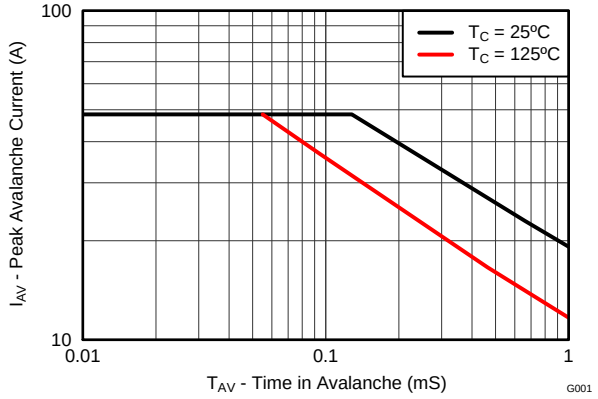


Figure 11. Single Pulse Unclamped Inductive Switching

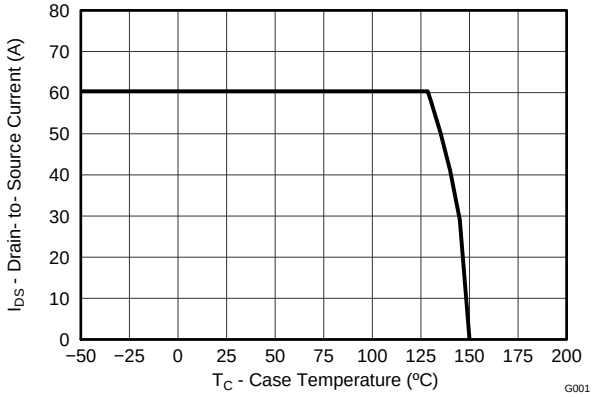


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 术语表

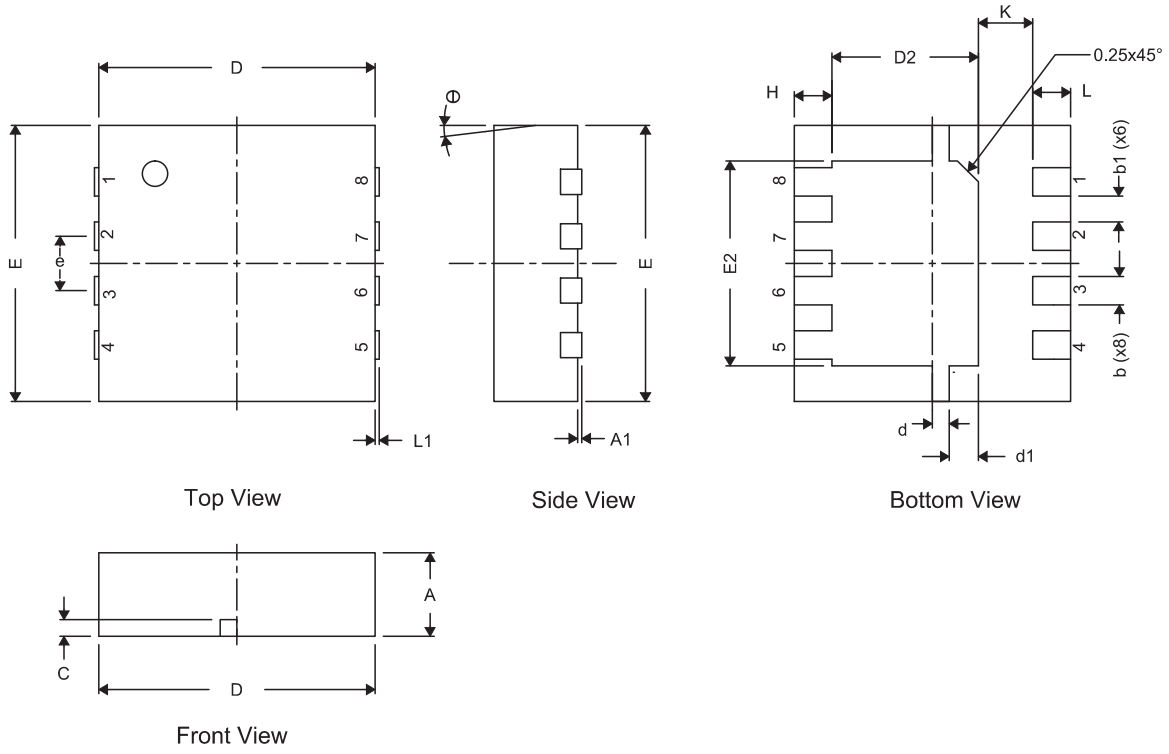
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

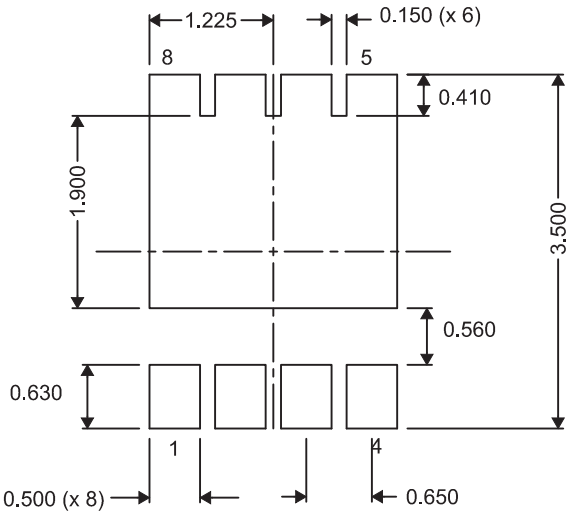
以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q3 封装尺寸



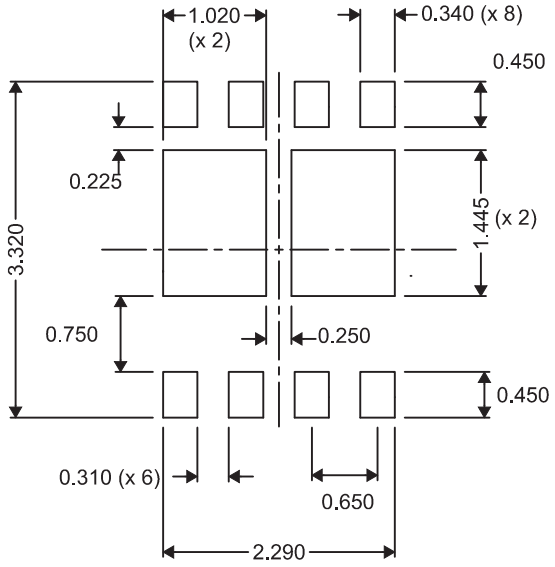
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310（标称值）			0.012（标称值）		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 典型值			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 典型值			0.026 典型值		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 建议 PCB 布局



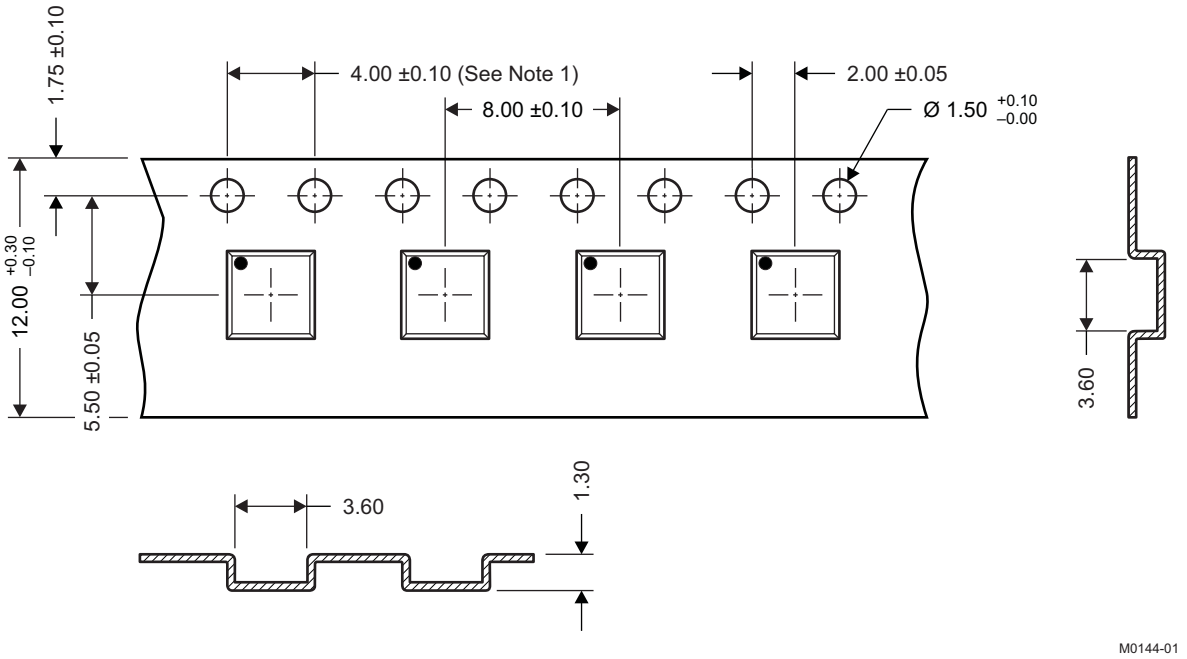
要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模板开口



全部尺寸单位为 mm，除非另外注明。

7.4 Q3 卷带信息



注释：

1. 10 链轮孔距累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）无铅 (PbF) 回流焊兼容

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17575Q3	ACTIVE	VSON-CLIP	DQG	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM		CSD17575	Samples
CSD17575Q3T	ACTIVE	VSON-CLIP	DQG	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD17575	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

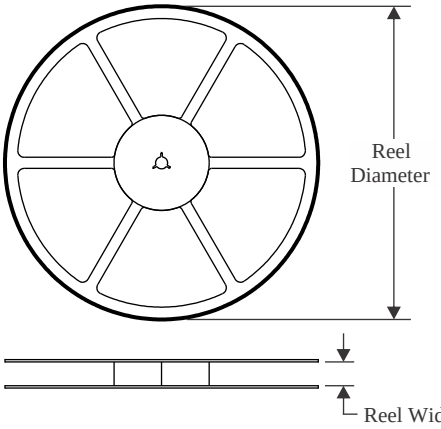
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

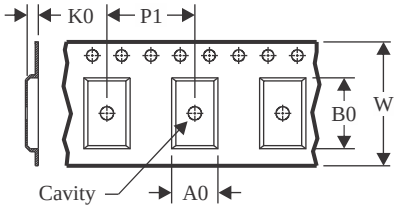
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

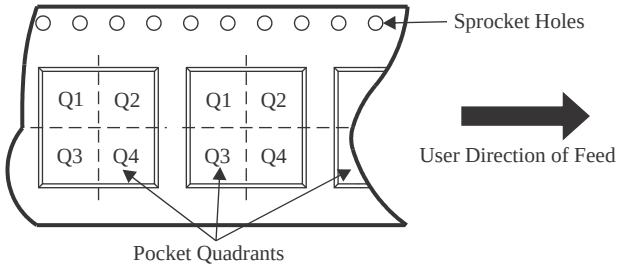


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

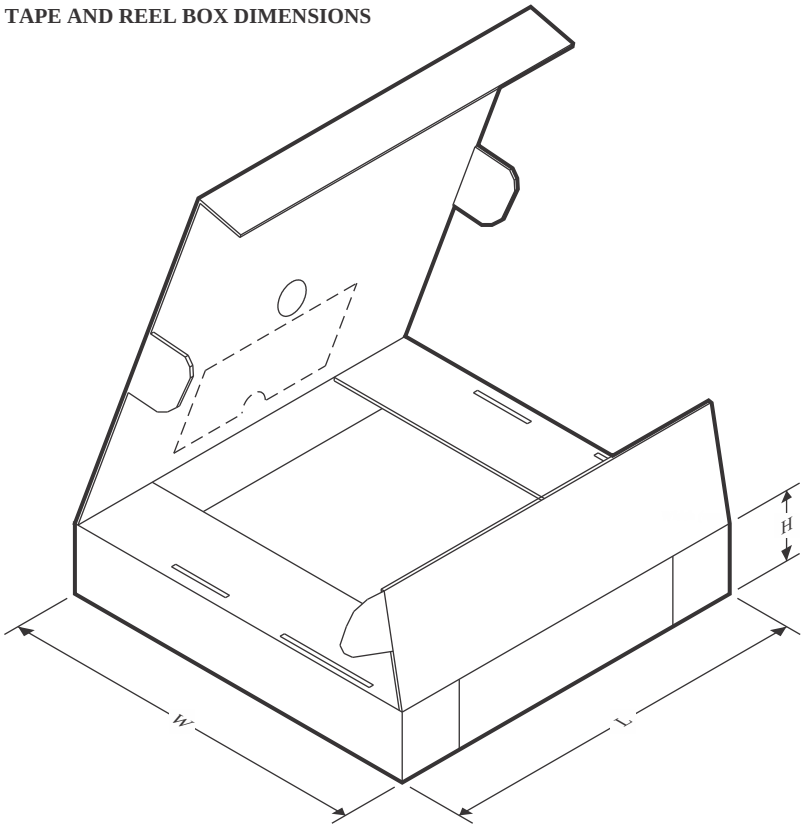
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17575Q3T	VSON-CLIP	DQG	8	250	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

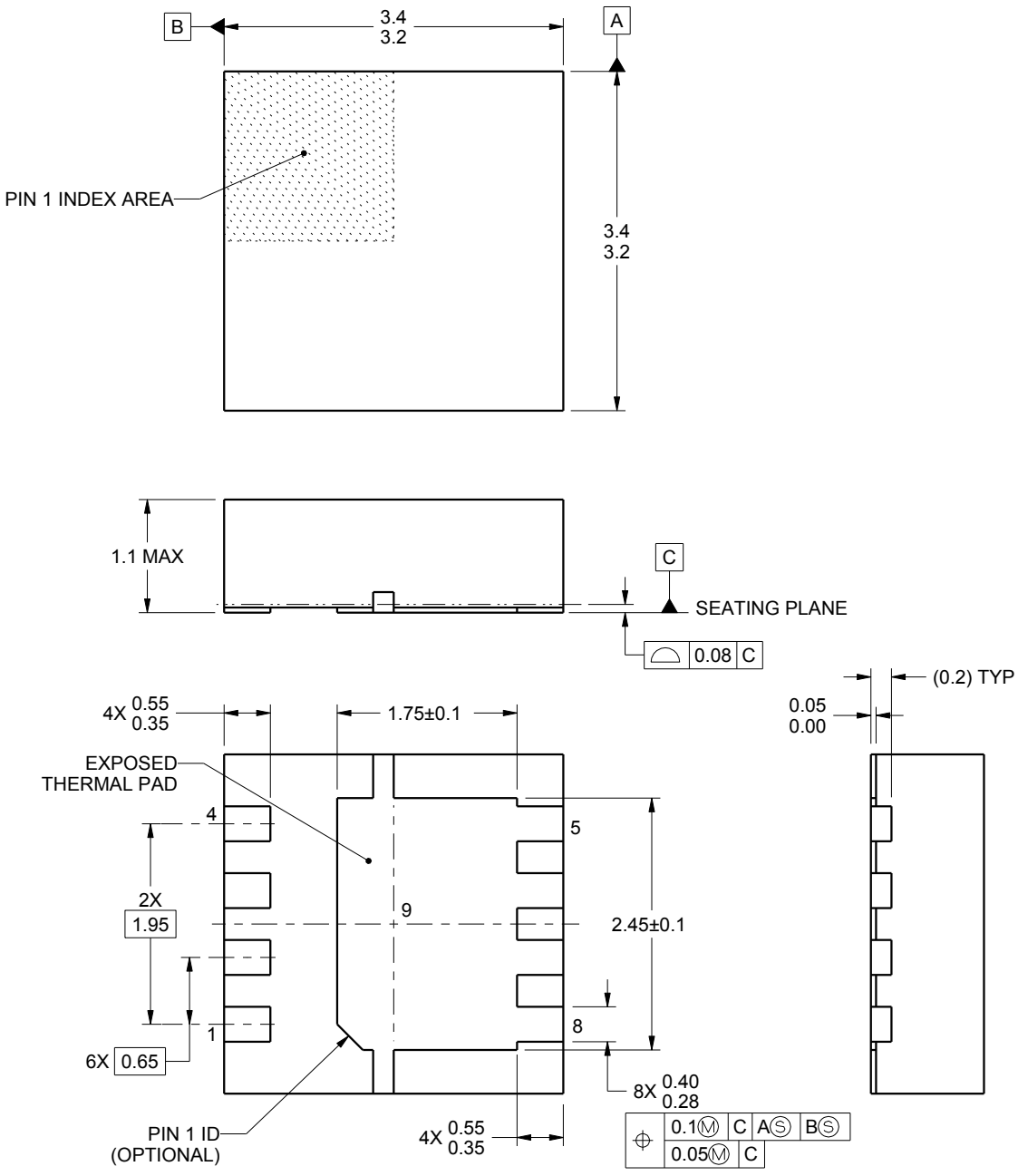
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17575Q3T	VSON-CLIP	DQG	8	250	336.6	336.6	41.3

PACKAGE OUTLINE

DQG0008A

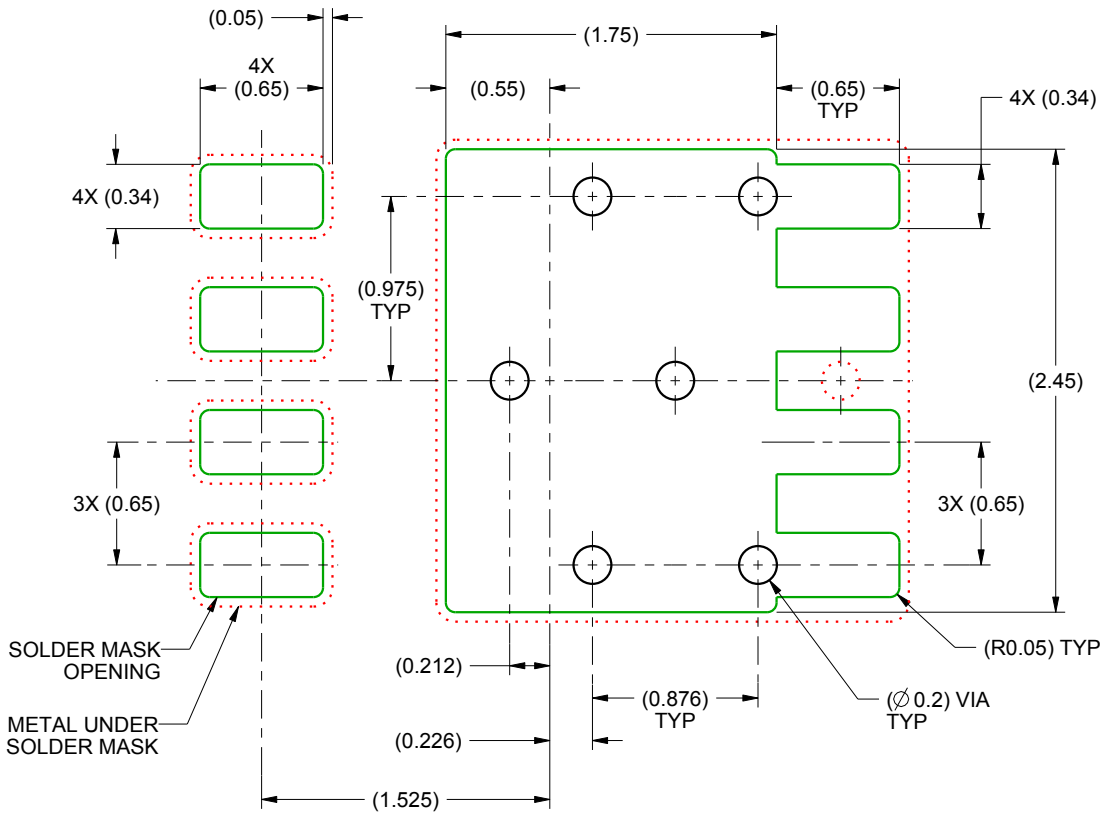
VSON-CLIP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 25X

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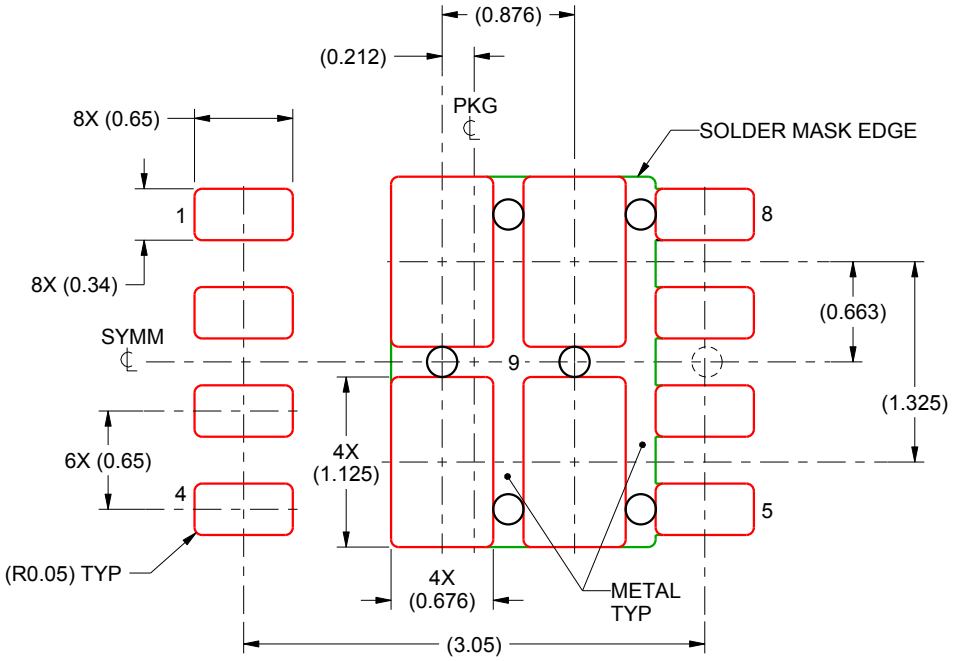
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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