CSD95378BQ5M 同步降压 NexFET™智能功率级

1 特性

- 60A 持续运行电流能力
- 电流 30A 时，系统效率为 93.4%
- 电流 30A 时，低功耗损耗为 2.8W
- 高频工作（高达 1.25MHz）
- 支持强制连续传导模式 (FCCM) 的二极管仿真模式
- 温度补偿双向电流感测
- 模拟温度输出（0°C 时 400mV）
- 故障监控
  - 高端短路、过流和过热保护
- 3.3V 和 5V 脉宽调制 (PWM) 信号兼容
- 三态 PWM 输入
- 集成型自举二极管
- 用于击穿保护的经优化死区时间
- 高密度 5mm × 6mm SON 封装
- 超低电感封装
- 系统已优化的 PCB 封装
- 符合 RoHS 环保标准 – 无铅引脚镀层
- 无卤素

2 应用

- 多相位同步降压转换器
  - 高频 应用
  - 高电流、低占空比 应用
- 负载点 (POL) 直流/直流转换器
- 内存和图形卡
- 台式机和服务器 VR11.x / VR12.x V 内核和存储器同步转换器

3 说明

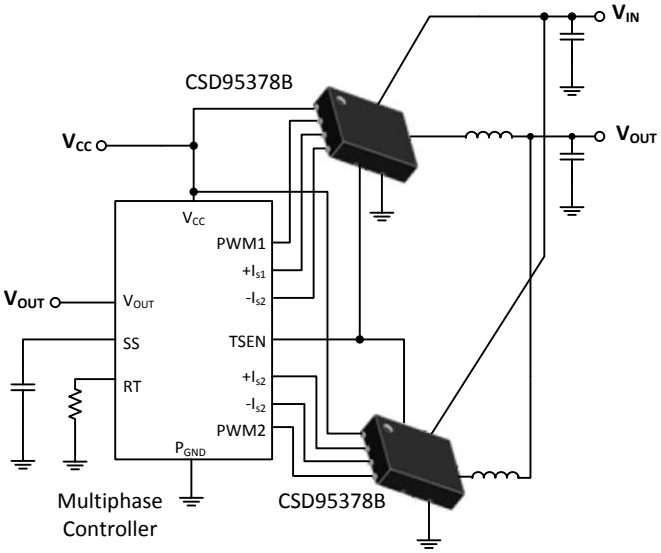
CSD95378BQ5M NexFET™智能功率级的设计针对高功率、高密度同步降压转换器中的使用进行了高度优化。这款产品集成了驱动器 IC 和功率 MOSFET 来完善功率级开关功能。该组合可在 5mm x 6mm 小型封装中提供高电流、高效率的高速切换功能。它还集成了准确电流感测和温度感测功能，以简化系统设计并提高准确度。此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计的完成。

器件信息(1)

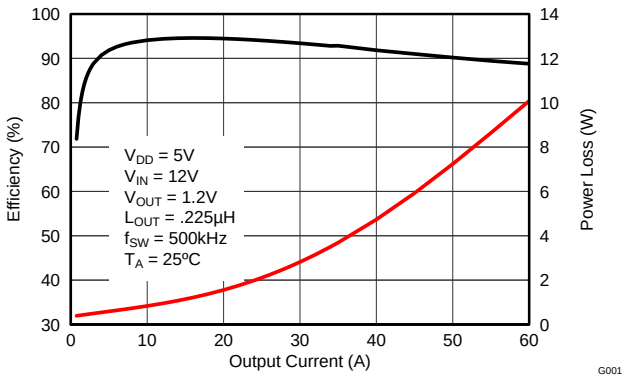
器件	包装介质	数量	封装	运输
CSD95378BQ5M	13 英寸卷带	2500	SON 5.00mm × 6.00mm 封装	卷带封装
CSD95378BQ5MT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用图表



典型功率级效率与功率损耗



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4 修订历史记录

Changes from Revision A (July 2014) to Revision B **Page**

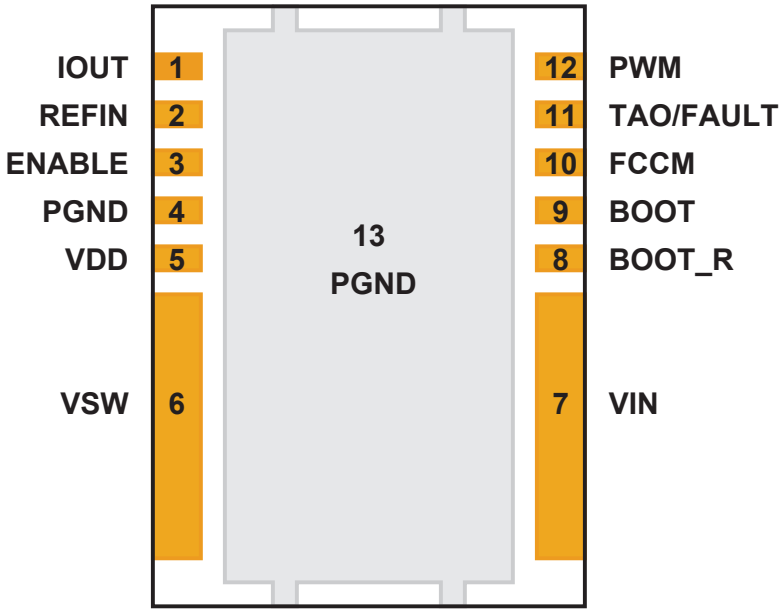
- Updated the CSD95378B parts in the *Application Schematic* ... 5
- 已添加 *器件和文档支持* 中的 *接收文档更新通知* 和 *社区资源*部分 ... 6

Changes from Original (April 2014) to Revision A **Page**

- Updated the controller IC in the *Application Schematic* to the TPS40428 ... 5

5 Pin Configuration and Functions

13-Pin SON
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
BOOT	9	Bootstrap capacitor connection. Connect a minimum of 0.1-µF, 16-V, X7R ceramic capacitor from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
BOOT_R	8	Return path for HS gate driver, connected to V_{SW} internally.
ENABLE	3	Enables device operation. If ENABLE = logic HIGH, turns on device. If ENABLE = logic LOW, the device is turned off and both MOSFET gates are actively pulled low. An internal 100-kΩ pulldown resistor will pull the ENABLE pin LOW if left floating.
FCCM	10	This pin enables the Diode Emulation function. When this pin is held LOW, Diode Emulation Mode is enabled for sync FET. When FCCM is HIGH, the device is operated in Forced Continuous Conduction Mode. An internal 5-µA current source will pull the FCCM pin to 3.3 V if left floating.
IOUT	1	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
P_{GND}	4	Power ground, connected directly to pin 13.
P_{GND}	13	Power ground.
PWM	12	Pulse width modulated tri-state input from external controller. Logic LOW sets control FET gate low and sync FET gate high. Logic HIGH sets control FET gate high and sync FET gate low. Open or Hi-Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time (t_{3HT}).
REFIN	2	External reference voltage input for current sensing amplifier.
TAO/ FAULT	11	Temperature analog output. Reports a voltage proportional to the die temperature. An ORing diode is integrated in the IC. When used in multiphase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown occurs. TAO should be bypassed to P_{GND} with a 1-nF, 16-V, X7R ceramic capacitor.
V_{DD}	5	Supply voltage to gate driver and internal circuitry.
V_{IN}	7	Input voltage pin. Connect input capacitors close to this pin.
V_{SW}	6	Phase node connecting the HS MOSFET source and LS MOSFET drain - pin connection to the output inductor.

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to P_{GND}	–0.3	25	V
V_{IN} to V_{SW}	–0.3	25	V
V_{IN} to V_{SW} (10 ns)	–7	27	V
V_{SW} to P_{GND}	–0.3	20	V
V_{SW} to P_{GND} (10 ns)	–7	23	V
V_{DD} to P_{GND}	–0.3	7	V
ENABLE, PWM, FCCM. TAO, IOUT, REFIN to P_{GND}	–0.3	V_{DD} + 0.3 V	V
BOOT to BOOT_R(2)	–0.3	V_{DD} + 0.3 V	V
Power dissipation, P_D		12	W
Operating junction temperature, T_J	–55	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Should not exceed 7 V.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	–2000	2000	V
		Charged-device model (CDM)	–500	500	

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)			16	V
V_{OUT}	Output voltage			5.5	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz, L_{OUT} = 0.225 µH(2)		60	
I_{OUT-PK}	Peak output current(3)			90	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1250	kHz
	On-time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on time		40		ns
	Operating temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 1. Peak output current is applied for t_p = 50 µs.

6.4 Thermal Information

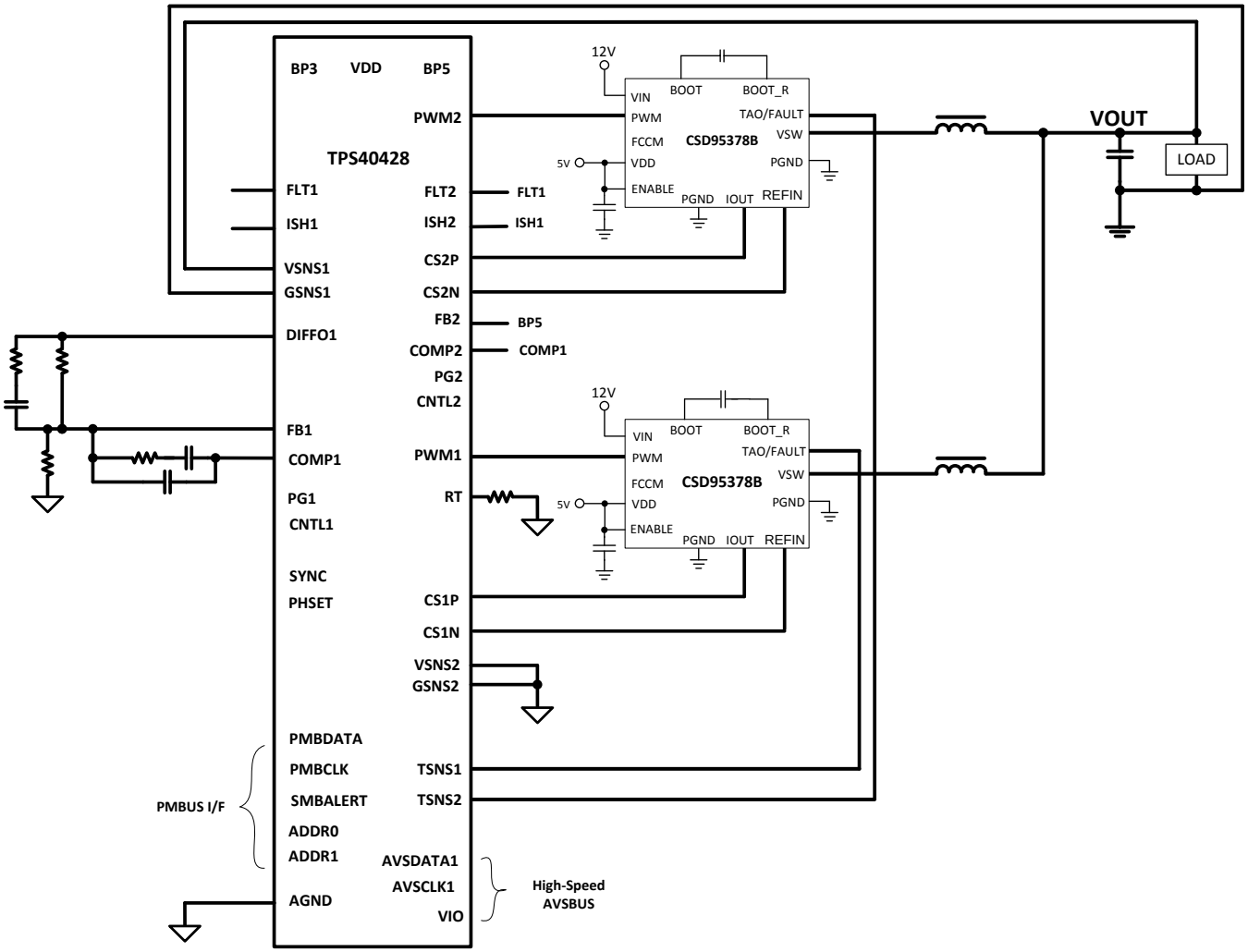
T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case (top-of-package) thermal resistance(1)			15	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(2)			1.5	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45 -cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in, 0.06-in (1.52-mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1 mm of the package.

7 Application Schematic

7.1 Typical Application



8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

8.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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8.3 商标

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8.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.5 Glossary

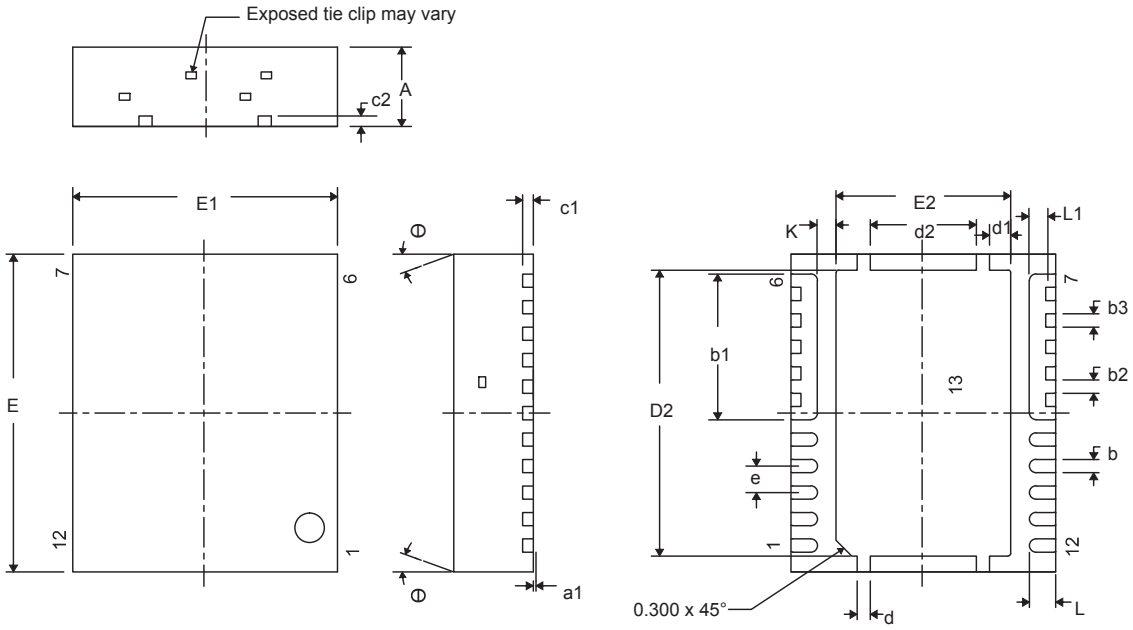
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

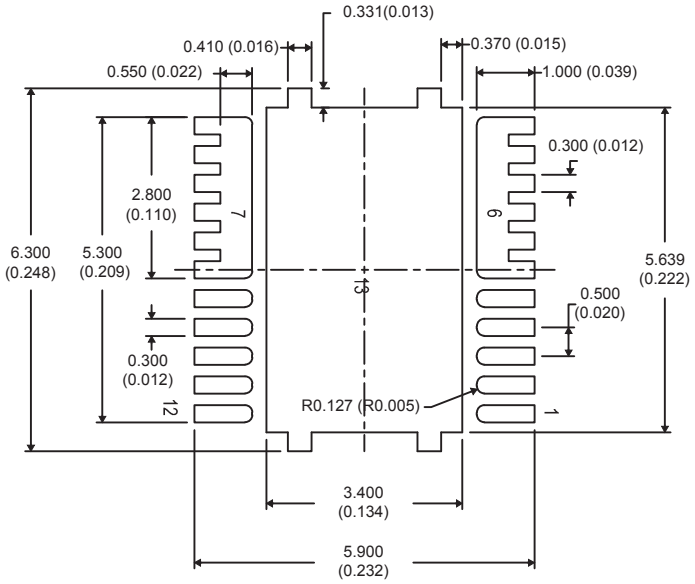
以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

9.1 机械制图



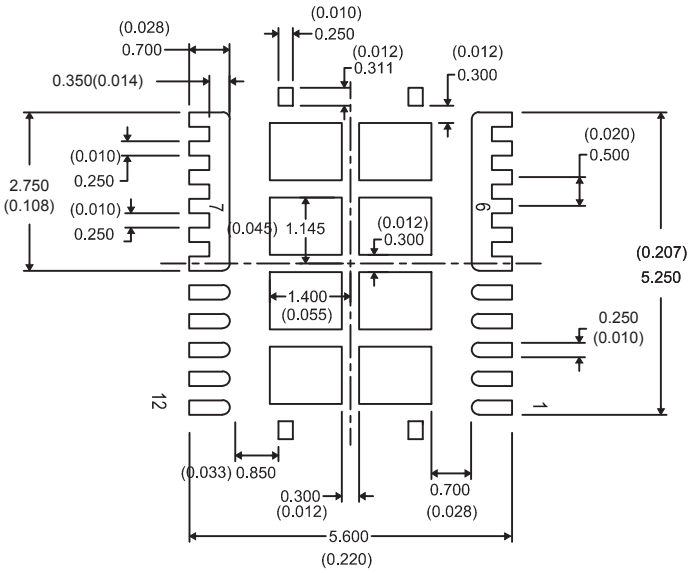
DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	1.400	1.450	1.500	0.057	0.059	0.061
a1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.200	0.250	0.320	0.008	0.010	0.013
b1		2.750 典型值			0.108 典型值	
b2	0.200	0.250	0.320	0.008	0.010	0.013
b3		0.250 典型值			0.010 典型值	
c1	0.150	0.200	0.250	0.006	0.008	0.010
c2	0.200	0.250	0.300	0.008	0.010	0.012
D2	5.300	5.400	5.500	0.209	0.213	0.217
d	0.200	0.250	0.300	0.008	0.010	0.012
d1	0.350	0.400	0.450	0.014	0.016	0.018
d2	1.900	2.000	2.100	0.075	0.079	0.083
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.900	5.000	5.100	0.193	0.197	0.201
E2	3.200	3.300	3.400	0.126	0.130	0.134
e		0.500 典型值			0.020 典型值	
K		0.350 典型值			0.014 典型值	
L	0.400	0.500	0.600	0.016	0.020	0.024
L1	0.210	0.310	0.410	0.008	0.012	0.016
θ	0.00	—	—	0.00	—	—

9.2 建议印刷电路板 (PCB) 焊盘图案



1. 尺寸单位为 mm（英寸）。

9.3 建议模板开口



1. 尺寸单位为 mm（英寸）。
2. 模板厚度为 100µm。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95378BQ5M	ACTIVE	LSON-CLIP	DQP	12	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95378BM	Samples
CSD95378BQ5MT	ACTIVE	LSON-CLIP	DQP	12	250	RoHS-Exempt & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 150	95378BM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

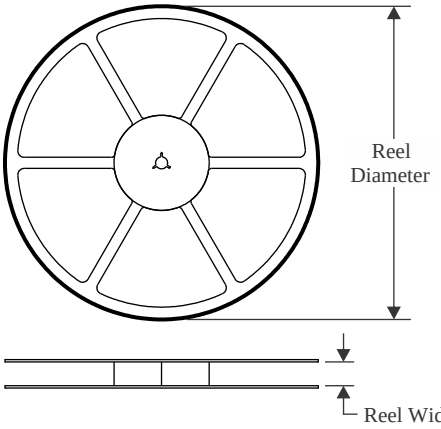
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

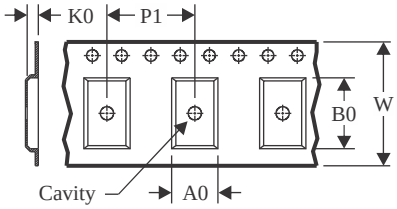
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

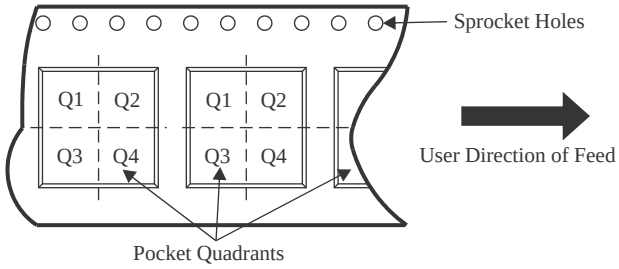


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

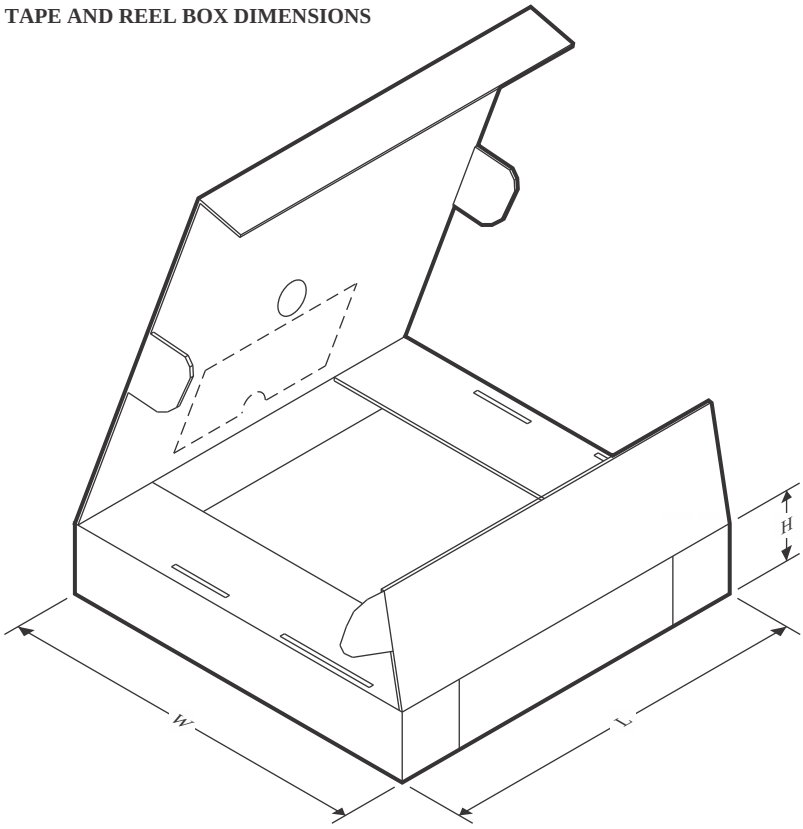
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95378BQ5M	LSON-CLIP	DQP	12	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
CSD95378BQ5MT	LSON-CLIP	DQP	12	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95378BQ5M	LSON-CLIP	DQP	12	2500	346.0	346.0	33.0
CSD95378BQ5MT	LSON-CLIP	DQP	12	250	210.0	185.0	35.0

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