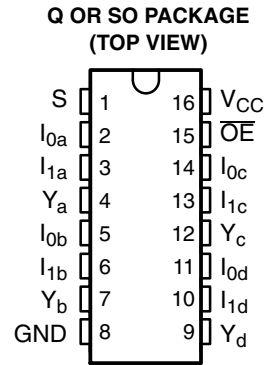


# CY74FCT257T QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

SCCS019D – MAY 1994 – REVISED NOVEMBER 2001

- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **64-mA Output Sink Current**  
**32-mA Output Source Current**
- **3-State Outputs**



## description

The CY74FCT257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data-select (S) input. The  $I_0$  inputs are selected when S is low, and the  $I_1$  inputs are selected when S is high. Data at the output is noninverted.

The CY74FCT257T is a logic implementation of a four-pole, two-position switch, where the position of the switch is determined by the logic levels at S. Outputs are in the high-impedance state when the output-enable ( $\overline{OE}$ ) input is high.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together.  $\overline{OE}$  inputs must ensure that there is no overlap when outputs of 3-state devices are tied together.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### PIN DESCRIPTION

NAME	DESCRIPTION
I	Data inputs
S	Common data-select input
$\overline{OE}$	Output-enable input (active low)
Y	Data outputs



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# CY74FCT257T

## QUAD 2-INPUT MULTIPLEXER

### WITH 3-STATE OUTPUTS

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#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.3	CY74FCT257CTQCT	FT257-3
	SOIC – SO	Tube	4.3	CY74FCT257CTSOC	FCT257C
		Tape and reel	4.3	CY74FCT257CTSOCT	
	QSOP – Q	Tape and reel	5	CY74FCT257ATQCT	FT257-1
	QSOP – Q	Tape and reel	6	CY74FCT257TQCT	FT257

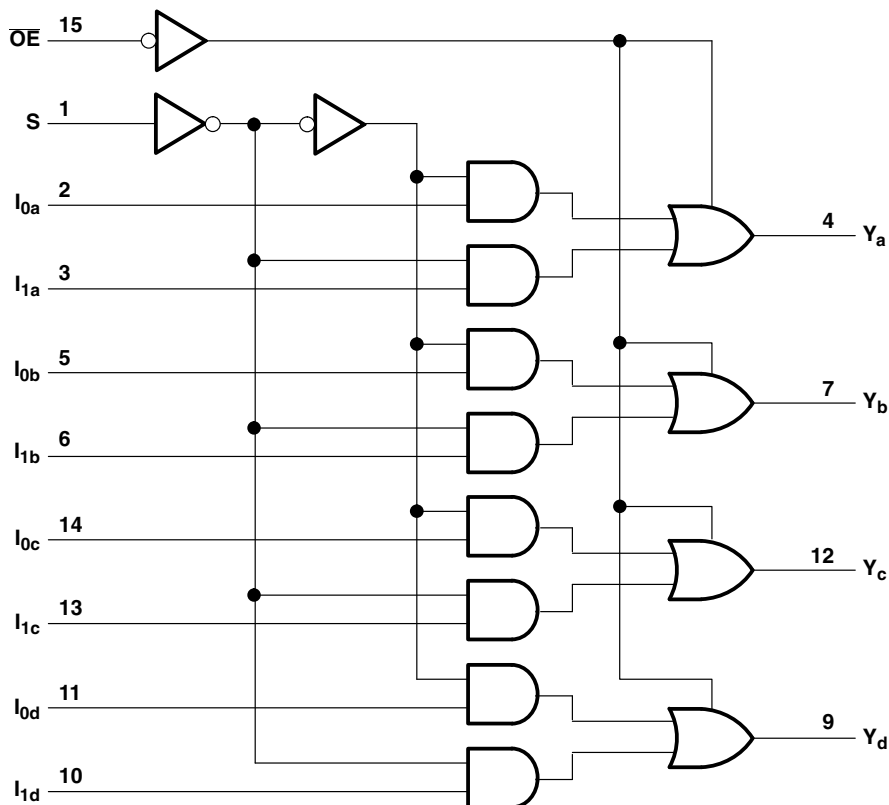
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE

INPUTS				OUTPUT
OE	S	I <sub>0</sub>	I <sub>1</sub>	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance state

#### logic diagram



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**CY74FCT257T**  
**QUAD 2-INPUT MULTIPLEXER**  
**WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	90°C/W
SO package .....	57°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



# CY74FCT257T

## QUAD 2-INPUT MULTIPLEXER

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75$ ,	$I_{IN} = -18$ mA		-0.7	-1.2	V
$V_{OH}$	$V_{CC} = 4.75$ ,	$I_{OH} = -32$ mA	2			V
$V_{OL}$	$V_{CC} = 4.75$ ,	$I_{OL} = 64$ mA		0.3	0.55	V
$V_{hys}$	All inputs			0.2		V
$I_I$	$V_{CC} = 5.25$ V,	$V_{IN} = 5.25$ V			5	μA
$I_{IH}$	$V_{CC} = 5.25$ V,	$V_{IN} = 2.7$ V			±1	μA
$I_{IL}$	$V_{CC} = 5.25$ V,	$V_{IN} = 0.5$ V			±1	μA
$I_{OZH}$	$V_{CC} = 5.25$ V,	$V_{OUT} = 2.7$ V			10	μA
$I_{OZL}$	$V_{CC} = 5.25$ V,	$V_{OUT} = 0.5$ V			-10	μA
$I_{OS}^{\ddagger}$	$V_{CC} = 5.25$ V,	$V_{OUT} = 0$ V	-60	-120	-225	mA
$I_{off}$	$V_{CC} = 0$ V,	$V_{OUT} = 4.5$ V			±1	μA
$I_{CC}$	$V_{CC} = 5.25$ V,	$V_{IN} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V		0.1	0.2	mA
$\Delta I_{CC}$	$V_{CC} = 5.25$ V, $V_{IN} = 3.4$ V <sup>§</sup> , $f_1 = 0$ , Outputs open			0.5	2	mA
$I_{CCD}^{\parallel}$	$V_{CC} = 5.25$ V, One input switching at 50% duty cycle, Outputs open, $\overline{OE} = GND$ , $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			0.06	0.12	mA/MHz
$I_C^{\#}$	$V_{CC} = 5.25$ V, Outputs open, $\overline{OE} = GND$	One input switching at $f_1 = 10$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	0.7	1.4	mA
			$V_{IN} = 3.4$ V or GND	1	2.4	
		Four bits switching at $f_1 = 2.5$ MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	0.7	1.4 <sup>  </sup>	
			$V_{IN} = 3.4$ V or GND	1.7	5.4 <sup>  </sup>	
$C_i$				5	10	pF
$C_o$				9	12	pF

† Typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4$  V); all other inputs at  $V_{CC}$  or GND

<sup>¶</sup> This parameter is derived for use in total power-supply calculations.

<sup>#</sup>  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD}(f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4$  V)

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

<sup>||</sup> Values for these conditions are examples of the  $I_C$  formula.



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switching characteristics over operating free-air temperature range (see Figure 1)

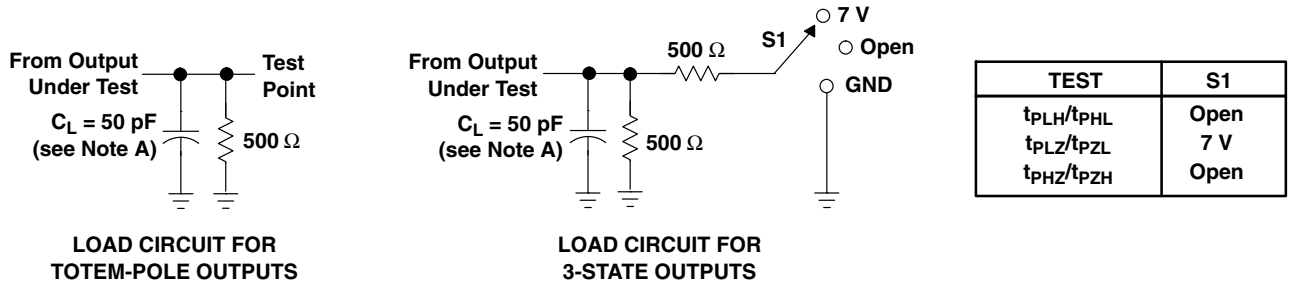
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT257T		CY74FCT257AT		CY74FCT257CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	I	Y	1.5	6	1.5	5	1.5	4.3	ns
t <sub>PHL</sub>			1.5	6	1.5	5	1.5	4.3	
t <sub>PLH</sub>	S	Y	1.5	10.5	1.5	7	1.5	5.2	ns
t <sub>PHL</sub>			1.5	10.5	1.5	7	1.5	5.2	
t <sub>PZH</sub>	OE	Y	1.5	8.5	1.5	7	1.5	6	ns
t <sub>PZL</sub>			1.5	8.5	1.5	7	1.5	6	
t <sub>PHZ</sub>	OE	Y	1.5	6	1.5	5.5	1.5	5	ns
t <sub>PLZ</sub>			1.5	6	1.5	5.5	1.5	5	



# CY74FCT257T QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

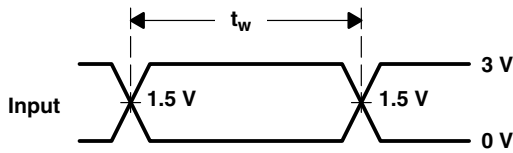
SCCS019D – MAY 1994 – REVISED NOVEMBER 2001

## PARAMETER MEASUREMENT INFORMATION

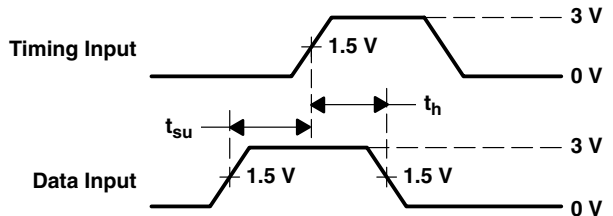


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

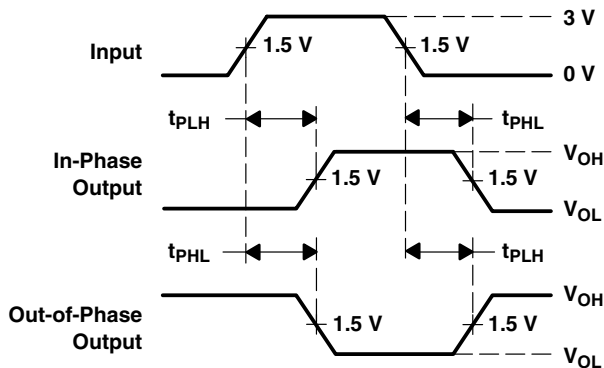
LOAD CIRCUIT FOR 3-STATE OUTPUTS



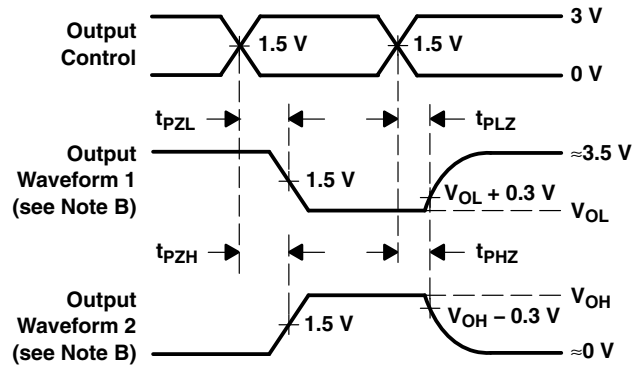
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT257ATD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT257AT	<a href="#">Samples</a>
CY74FCT257ATQCT	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT257-1	<a href="#">Samples</a>
CY74FCT257CTSOC	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT257C	<a href="#">Samples</a>
CY74FCT257TQCT	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FT257	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

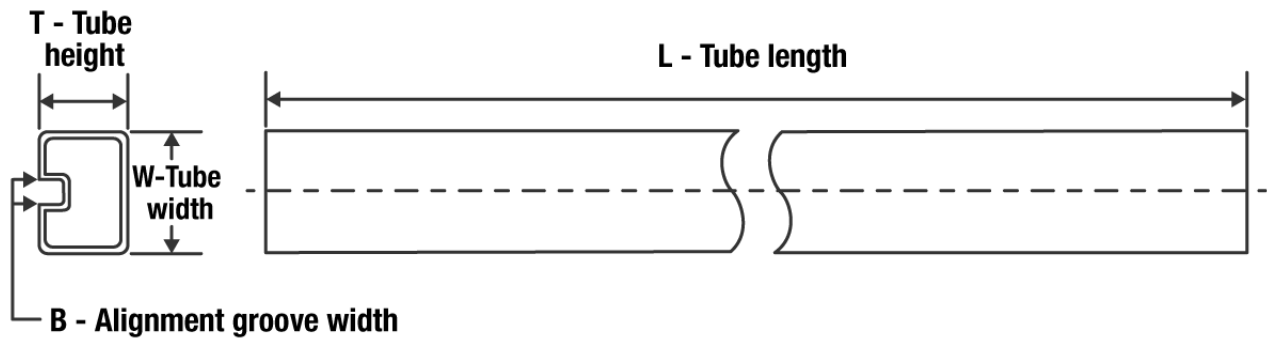

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT257ATQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
CY74FCT257TQCT	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT257ATQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6
CY74FCT257TQCT	SSOP	DBQ	16	2500	340.5	338.1	20.6

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT257ATD	D	SOIC	16	40	507	8	3940	4.32
CY74FCT257CTSOC	DW	SOIC	16	40	506.98	12.7	4826	6.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



# DW0016A

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

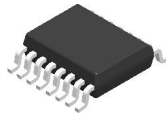
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# DBQ0016A



# PACKAGE OUTLINE

## SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



**NOTES:**

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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