DRV8412, DRV8432
ZHCSWR1H – DECEMBER 2009 – REVISED JULY 2024

DRV84x2 双路全桥 PWM 电机驱动器

1 特性

- 具有低 $R_{DS(on)}$ MOSFET（T_J = 25°C 时为 110mΩ）的高效功率级（高达 97%）
- 工作电源电压高达 52V
- DRV8412 (电源焊盘朝下)：在双路全桥模式下提供高达 2 × 3A 持续输出电流（峰值为 2 × 6A），在并行模式下提供高达 6A 持续电流（峰值为 12A）
- DRV8432 (电源焊盘朝上)：在双路全桥模式下提供高达 2 × 7A 持续输出电流（峰值为 2 × 12A），在并行模式下提供高达 14A 持续电流（峰值为 24A）
- PWM 工作频率高达 500kHz
- 包含欠压、过热、过载和短路保护的集成自保护电路
- 可编程逐周期电流限制保护
- 针对每个半桥的独立电源和接地引脚
- 智能栅极驱动和跨导保护
- 无需外部缓冲器或肖特基二极管

2 应用

- 有刷直流和步进电机
- 三相永磁同步电机
- 机器人和触觉控制系统
- 传动器和泵
- 精密仪器
- TEC 驱动器
- LED 照明驱动器

3 说明

DRV841x2 是具有先进保护系统的高性能、集成式双路全桥电机驱动器。

得益于 H 桥 MOSFET 的低 $R_{DS(on)}$ 和智能栅极驱动设计，这些电机驱动器的效率可高达 97%。这种高效率支持使用更小的电源和散热器，使得此类器件非常适合节能应用。

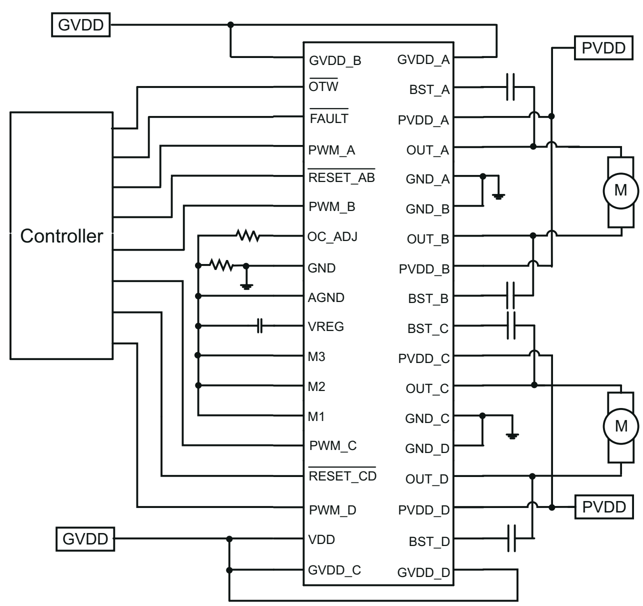
DRV841x2 需要两个电源，一个为 12V，用于 GVDD 和 VDD，另外一个可高达 50V，用于 PVDD。DRV841x2 可以在高达 500kHz 的开关频率下运行，同时仍保持精确控制和高效率。这些器件还具有创新的保护系统，可保护器件免受可能损坏系统的各种故障条件的影响。这些保护是短路保护、过流保护、欠压保护和两级过热保护。DRV841x2 有一个限流电路，此电路可在诸如电机启动等负载瞬态期间防止器件过流关断。一个可编程过流检测器可实现可调电流限值和保护级别，以满足不同的电机要求。

DRV841x2 的每个半桥都有独特的独立电源和接地引脚。借助这些引脚，可以通过外部分流电阻提供电流测量，并支持具有不同电源电压要求的多个电机。

封装信息

器件型号	封装(1)	封装尺寸(2)
DRV8412	HTSSOP (44)	14mm x 8.1mm
DRV8432	HSSOP (36)	15.9mm x 14.2mm

(1) 有关更多信息，请参阅节 9。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版应用示意图

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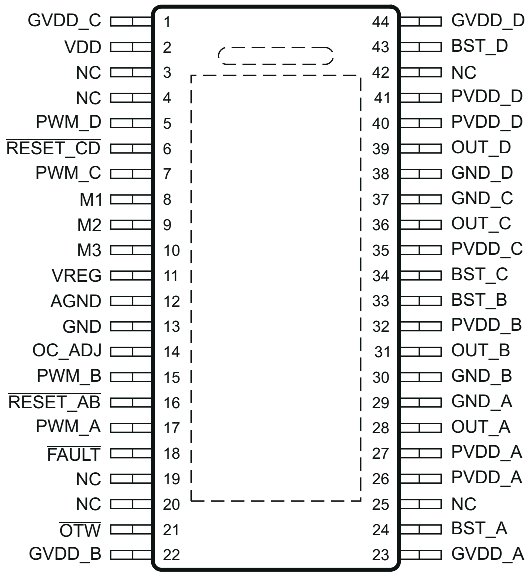
4 Pin Configuration and Functions

DRV8412
DDW Package
(Top View)



DRV8432
DKD Package
(Top View)

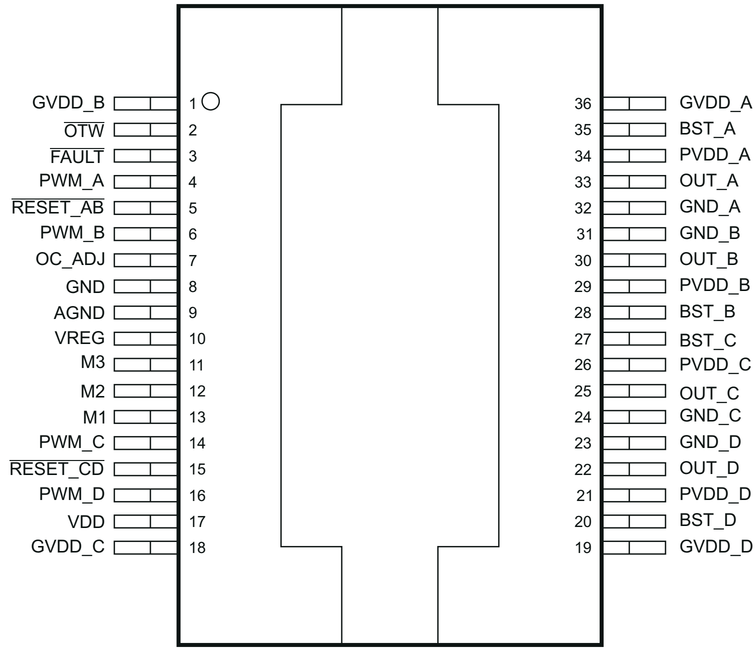


表 4-1. Pin Functions

PIN			I/O TYPE [1]	DESCRIPTION
NAME	DRV8412	DRV8432		
AGND	12	9	P	Analog ground
BST_A	24	35	P	High side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	33	28	P	High side bootstrap supply (BST), external capacitor to OUT_B required
BST_C	34	27	P	High side bootstrap supply (BST), external capacitor to OUT_C required
BST_D	43	20	P	High side bootstrap supply (BST), external capacitor to OUT_D required
GND	13	8	P	Ground
GND_A	29	32	P	Power ground for half-bridge A
GND_B	30	31	P	Power ground for half-bridge B
GND_C	37	24	P	Power ground for half-bridge C
GND_D	38	23	P	Power ground for half-bridge D
GVDD_A	23	36	P	Gate-drive voltage supply
GVDD_B	22	1	P	Gate-drive voltage supply
GVDD_C	1	18	P	Gate-drive voltage supply
GVDD_D	44	19	P	Gate-drive voltage supply
M1	8	13	I	Mode selection pin
M2	9	12	I	Mode selection pin
M3	10	11	I	Reserved mode selection pin, AGND connection is recommended
NC	3, 4, 19, 20, 25, 42	—	—	No connection pin. Ground connection is recommended
OC_ADJ	14	7	O	Analog overcurrent programming pin, requires resistor to AGND
OTW	21	2	O	Overtemperature warning signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
OUT_A	28	33	O	Output, half-bridge A
OUT_B	31	30	O	Output, half-bridge B
OUT_C	36	25	O	Output, half-bridge C

表 4-1. Pin Functions （续）

PIN			I/O TYPE (1)	DESCRIPTION
NAME	DRV8412	DRV8432		
OUT_D	39	22	O	Output, half-bridge D
PVDD_A	26, 27	34	P	Power supply input for half-bridge A requires close decoupling capacitor to ground.
PVDD_B	32	29	P	Power supply input for half-bridge B requires close decoupling capacitor to gound.
PVDD_C	35	26	P	Power supply input for half-bridge C requires close decoupling capacitor to ground.
PVDD_D	40, 41	21	P	Power supply input for half-bridge D requires close decoupling capacitor to ground.
PWM_A	17	4	I	Input signal for half-bridge A
PWM_B	15	6	I	Input signal for half-bridge B
PWM_C	7	14	I	Input signal for half-bridge C
PWM_D	5	16	I	Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	16	5	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	6	15	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{FAULT}}$	18	3	O	Fault signal, open-drain, active-low. An internal pullup resistor to VREG (3.3 V) is provided on output. Level compliance for 5-V logic can be obtained by adding external pullup resistor to 5 V
VDD	2	17	P	Power supply for digital voltage regulator requires capacitor to ground for decoupling.
VREG	11	10	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND.
THERMAL PAD	—	N/A	T	Solder the exposed thermal pad to the landing pad on the pcb. Connect landing pad to bottom side of pcb through via for better thermal dissipation. This pad should be connected to GND.
HEAT SLUG	N/A	—	T	Mount heat sink with thermal interface on top of the heat slug for best thermal performance.

(1) I = input, O = output, P = power, T = thermal

表 4-2. Mode Selection Pins

MODE PINS			OUTPUT CONFIGURATION	DESCRIPTION
M3	M2	M1		
0	0	0	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with cycle-by-cycle current limit
0	0	1	2 FB or 4 HB	Dual full bridges (two PWM inputs each full bridge) or four half bridges with OC latching shutdown (no cycle-by-cycle current limit)
0	1	0	1 PFB	Parallel full bridge with cycle-by-cycle current limit
0	1	1	2 FB	Dual full bridges (one PWM input each full bridge with complementary PWM on second half bridge) with cycle-by-cycle current limit
1	x	x	Reserved	

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
VDD to GND	–0.3	13.2	V
GVDD_X to GND	–0.3	13.2	V
PVDD_X to GND_X [(2)]	–0.3	70	V
OUT_X to GND_X [(2)]	–0.3	70	V
BST_X to GND_X [(2)]	–0.3	80	V
Transient peak output current (per pin), pulse width limited by internal overcurrent protection circuit		16	A
Transient peak output current for latch shut down (per pin)		20	A
VREG to AGND	–0.3	4.2	V
GND_X to GND	–0.3	0.3	V
GND to AGND	–0.3	0.3	V
PWM_X to GND	–0.3	V_{REG} + 0.5	V
OC_ADJ, M1, M2, M3 to AGND	–0.3	4.2	V
$\overline{\text{RESET\_X}}$, $\overline{\text{FAULT}}$, $\overline{\text{OTW}}$ to GND	–0.3	7	V
Continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$)		9	mA
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *节 5.3* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These are the maximum allowed voltages for transient spikes. Absolute maximum DC voltages are lower.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(1)]	±1500	V

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
PVDD_X	Half bridge X (A, B, C, or D) DC supply voltage	0	50	52.5	V
GVDD_X	Supply for logic regulators and gate-drive circuitry	10.8	12	13.2	V
VDD	Digital regulator supply voltage	10.8	12	13.2	V
I_{O_PULSE}	Pulsed peak current per output pin (could be limited by thermal)			15	A
I_O	Continuous current per output pin (DRV8432)			9	mA
F_{SW}	PWM switching frequency			500	kHz
R_{OCP_CBC}	OC programming resistor range in cycle-by-cycle current limit modes	24		200	kΩ
R_{OCP_OCL}	OC programming resistor range in OC latching shutdown modes	22		200	kΩ
C_{BST}	Bootstrap capacitor range	33		220	nF
t_{ON_MIN}	Minimum PWM pulse duration, low side, for charging the Bootstrap capacitor		50		ns

5.3 Recommended Operating Conditions（续）

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		DRV8412 DDW PACKAGE 44 PINS	DRV8432 DKD PACKAGE 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.5	13.3 (with heat sink)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.8	0.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	13.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	5.4	13.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	N/A	

(1) for more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.5 Package Heat Dissipation Ratings

PARAMETER	DRV8412	DRV8432
$R_{\theta JC}$, junction-to-case (power pad / heat slug) thermal resistance	1.1 °C/W	0.9 °C/W
$R_{\theta JA}$, junction-to-ambient thermal resistance	25 °C/W	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.
Exposed power pad / heat slug area	34 mm^2	80 mm^2

5.6 Package Power Deratings (DRV8412) [1]

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
44-PIN TSSOP (DDW)	5.0 W	40.0 mW/°C	3.2 W	2.6 W	1.0 W

(1) Based on EVM board layout

5.7 Electrical Characteristics

T_A = 25°C, PVDD = 50V, GVDD = VDD = 12V, f_{SW} = 400kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
V_{REG}	Voltage regulator, only used as a reference node	VDD = 12 V	2.95	3.3	3.65	V
I_{VDD}	VDD supply current	Idle, reset mode		9	12	mA
		Operating, 50% duty cycle		10.5		
I_{GVDD_X}	Gate supply current per half-bridge	Reset mode		1.7	2.5	mA
		Operating, 50% duty cycle		8		
I_{PVDD_X}	Half-bridge X (A, B, C, or D) idle current	Reset mode		0.7	1	mA
OUTPUT STAGE						
$R_{DS(on)}$	MOSFET drain-to-source resistance, low side (LS)	T_J = 25°C, GVDD = 12 V, Includes metallization bond wire and pin resistance		110		mΩ
	MOSFET drain-to-source resistance, high side (HS)	T_J = 25°C, GVDD = 12 V, Includes metallization bond wire and pin resistance		110		
V_F	Diode forward voltage drop	T_J = 25°C - 125°C, I_O = 5 A		1		V
t_R	Output rise time	Resistive load, I_O = 5 A		14		ns
t_F	Output fall time	Resistive load, I_O = 5 A		14		
t_{PD_ON}	Propagation delay when FET is on	Resistive load, I_O = 5 A		38		
t_{PD_OFF}	Propagation delay when FET is off	Resistive load, I_O = 5 A		38		
t_{DT}	Dead time between HS and LS FETs	Resistive load, I_O = 5 A		5.5		
I/O PROTECTION						
$V_{uvp,G}$	Gate supply voltage GVDD_X undervoltage protection threshold			8.5		V
$V_{uvp,hyst}$ (1)	Hysteresis for gate supply undervoltage event			0.8		
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Hysteresis temperature to reset $\overline{\text{OTW}}$ event			25		
OTSD(1)	Overtemperature shut down			150		
OTE-$OTW_{differential}$ (1)	OTE-OTW overtemperature detect temperature difference			25		
$OTSD_{HYST}$ (1)	Hysteresis temperature for $\overline{\text{FAULT}}$ to be released following an OTSD event			25		
I_{OC}	Overcurrent limit protection	Resistor—programmable, nominal, R_{OCP} = 27 kΩ		9.7		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected FET(s)		250		ns
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ is active to provide bootstrap capacitor charge		1		kΩ
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3	2		3.6	V
V_{IH}	High-level input voltage	$\overline{\text{RESET\_AB}}$, $\overline{\text{RESET\_CD}}$	2		5.5	
V_{IL}	Low-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, $\overline{\text{RESET\_AB}}$, $\overline{\text{RESET\_CD}}$			0.8	
I_{lkg}	Input leakage current		–100		100	μA
OTW / FAULT						
R_{INT_PU}	Internal pullup resistance, $\overline{\text{OTW}}$ to VREG, $\overline{\text{FAULT}}$ to VREG		20	26	35	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor only	2.95	3.3	3.65	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	

(1) Specified by design

5.8 Typical Characteristics

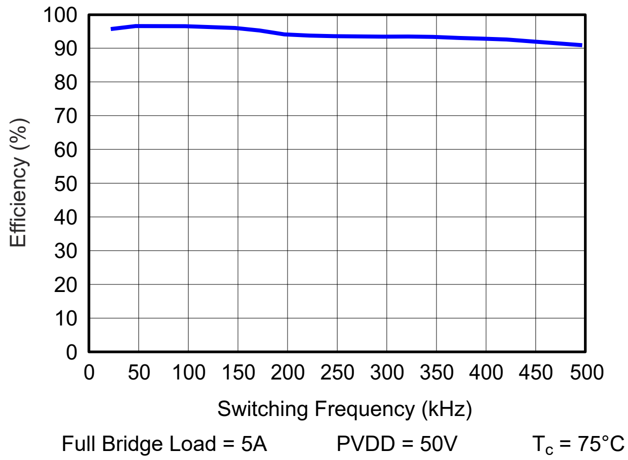


图 5-1. Efficiency vs Switching Frequency (DRV8432)

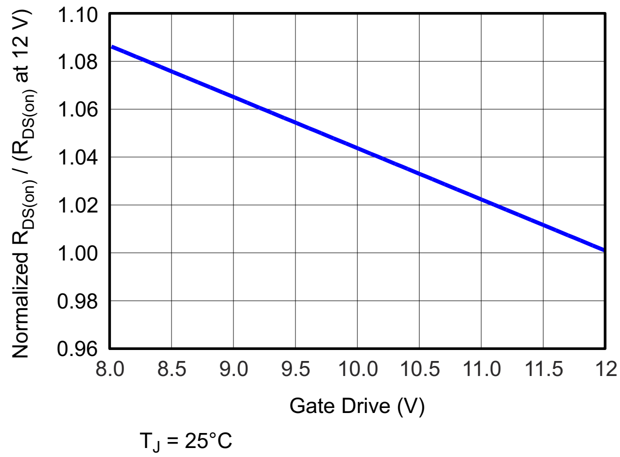


图 5-2. Normalized RDS(On) vs Gate Drive

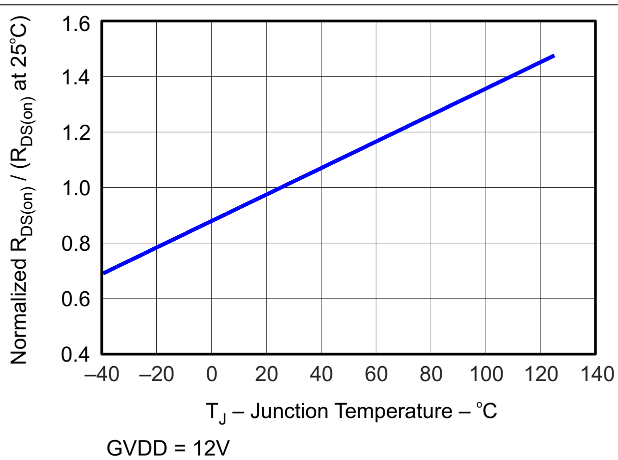


图 5-3. Normalized Rds(On) vs Junction Temperature

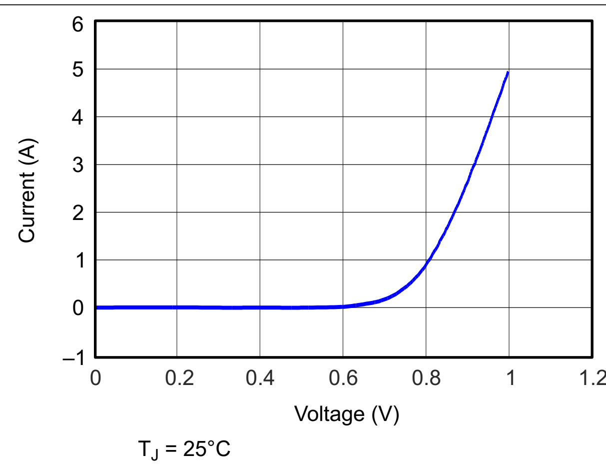


图 5-4. Drain To Source Diode Forward On Characteristics

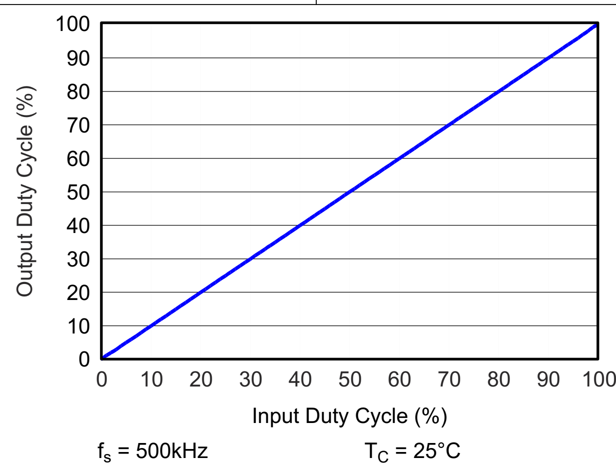


图 5-5. Output Duty Cycle vs Input Duty Cycle

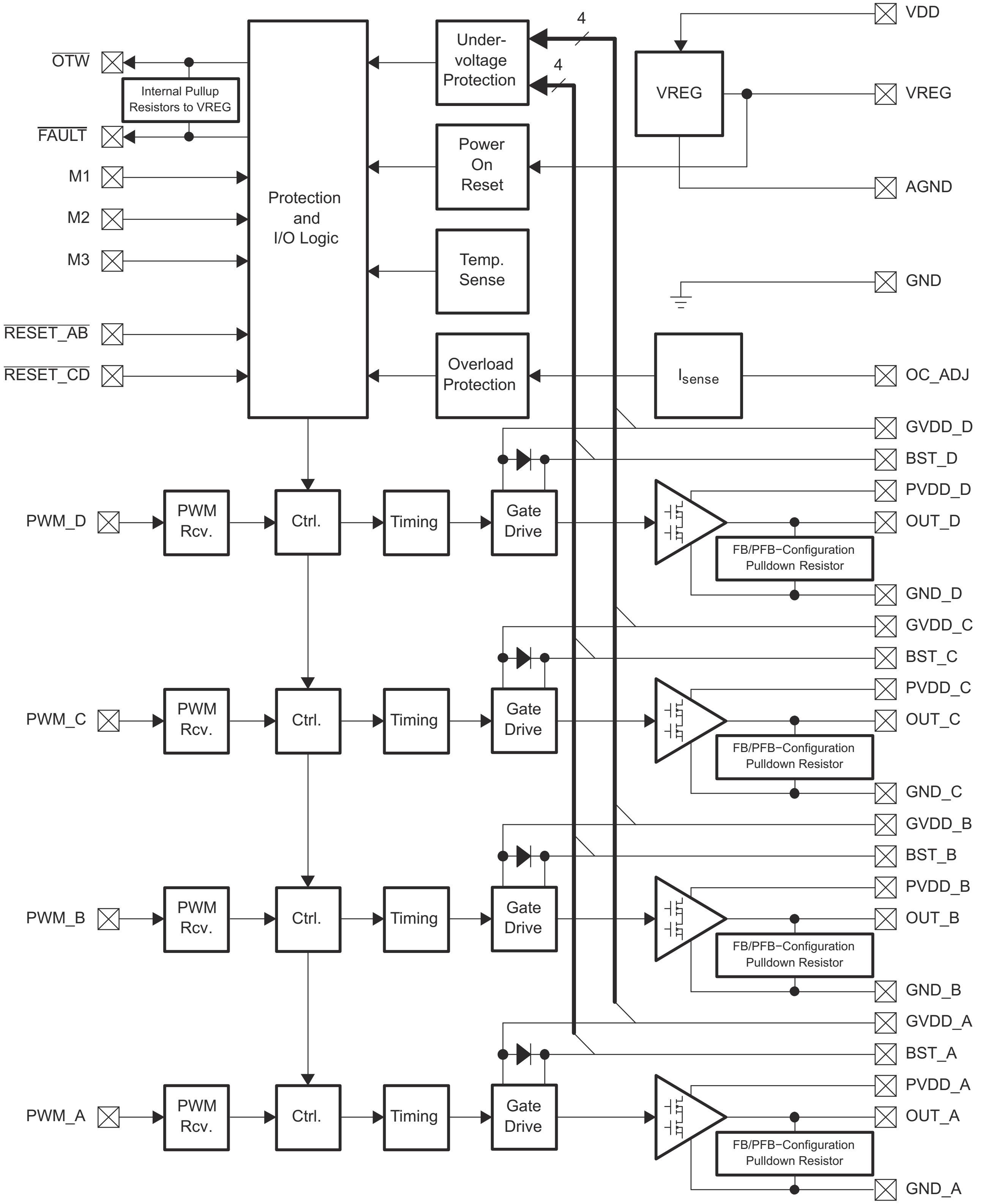
6 Detailed Description

6.1 Overview

The DRV841x2 is a high performance, integrated dual full bridge motor driver with an advanced protection system.

Because of the low $R_{DS(on)}$ of the H-Bridge MOSFETs and intelligent gate drive design, the efficiency of these motor drivers can be up to 97%, which enables the use of smaller power supplies and heatsinks, and are good candidates for energy efficient applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Error Reporting

The FAULT and OTW pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown, such as overtemperatue shutdown, overcurrent shutdown, or undervoltage protection, is signaled by the FAULT pin going low. Also, OTW goes low when the device junction temperature exceeds 125°C (see 表 6-1).

表 6-1. Protection Mode Signal Descriptions

FAULT	OTW	DESCRIPTION
0	0	Overtemperature warning and (overtemperature shut-down or overcurrent shut-down or undervoltage protection) occurred
0	1	Overcurrent shut-down or GVDD undervoltage protection occurred
1	0	Overtemperature warning
1	1	Device under normal operation

TI recommends monitoring the OTW signal using the system microcontroller and responding to an OTW signal by reducing the load current to prevent further heating of the device resulting in device overtemperature shutdown (OTSD).

To reduce external component count, an internal pullup resistor to VREG (3.3V) is provided on both FAULT and OTW outputs. Level compliance for 5V logic can be obtained by adding external pullup resistors to 5V (see the *Electrical Characteristics* section of this data sheet for further specifications).

6.3.2 Device Protection System

The DRV841x2 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overcurrent, overtemperature, and undervoltage. The DRV841x2 responds to a fault by immediately setting the half bridge outputs in a high-impedance (Hi-Z) state and asserting the FAULT pin low. In situations other than overcurrent or overtemperature, the device automatically recovers when the fault condition has been removed or the gate supply voltage has increased. For highest possible reliability, reset the device externally no sooner than 1 second after the shutdown when recovering from an overcurrent shut down (OCSD) or OTSD fault.

6.3.2.1 Bootstrap Capacitor Undervoltage Protection

When the device runs at a low switching frequency (for example, less than 10 kHz with a 100-nF bootstrap capacitor), the bootstrap capacitor voltage might not be able to maintain a proper voltage level for the high-side gate driver. A bootstrap capacitor undervoltage protection circuit (BST_UVP) prevents potential failure of the high-side MOSFET. When the voltage on the bootstrap capacitors is less than the required value for safe operation, the DRV841x2 initiates bootstrap capacitor recharge sequences (turn off high side FET for a short period) until the bootstrap capacitors are properly charged for safe operation. This function may also be activated when PWM duty cycle is too high (for example, less than 20ns off time at 10kHz). Note that bootstrap capacitor might not be able to be charged if no load or extremely light load is presented at output during BST_UVP operation, so it is recommended to turn on the low side FET for at least 50 ns for each PWM cycle to avoid BST_UVP operation if possible.

For applications with lower than 10-kHz switching frequency and not to trigger BST_UVP protection, a larger bootstrap capacitor can be used (for example, 1-µF capacitor for 800-Hz operation). When using a bootstrap cap larger than 220 nF, it is recommended to add 5-Ω resistors between 12-V GVDD power supply and GVDD_X pins to limit the inrush current on the internal bootstrap circuitry.

6.3.2.2 Overcurrent (OC) Protection

The DRV841x2 has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. There are two settings for OC protection through mode selection pins: cycle-by-cycle (CBC) current limiting mode and OC latching (OCL) shut down mode.

In CBC current limiting mode, the detector outputs are monitored by two protection systems. The first protection system controls the power stage to prevent the output current from further increasing, that is, performing as a CBC current-limiting function rather than prematurely shutting down the device. This feature could effectively limit the inrush current during motor start-up or transient without damaging the device. During short to power and short to ground conditions, the current limit circuitry might not be able to control the current to a proper level, a second protection system triggers a latching shutdown, resulting in the related half bridge being set in the high-impedance (Hi-Z) state. Current limiting and overcurrent protection are independent for half-bridges A, B, C, and, D, respectively.

图 6-1 illustrates cycle-by-cycle operation with high side OC event and 图 6-2 shows cycle-by-cycle operation with low side OC. Dashed lines are the operation waveforms when no CBC event is triggered and solid lines show the waveforms when CBC event is triggered. In CBC current limiting mode, when low side FET OC is detected, the device turns off the affected low side FET and keep the high side FET at the same half bridge off until the next PWM cycle. When high side FET OC is detected, the device turns off the affected high side FET and turn on the low side FET at the half bridge until next PWM cycle.

It is important to note that if the input to a half bridge is held to a constant value when an over current event occurs in CBC, then the associated half bridge will be in a HI-Z state upon the over current event ending. Cycling IN_X allows OUT_X to resume normal operation.

In OC latching shut down mode, the CBC current limit and error recovery circuits are disabled and an overcurrent condition will cause the device to shutdown immediately. After shutdown, $\overline{\text{RESET\_AB}}$ and/or $\overline{\text{RESET\_CD}}$ must be asserted to restore normal operation after the overcurrent condition is removed.

For added flexibility, the OC threshold is programmable using a single external resistor connected between the OC_ADJ pin and GND pin. See 表 6-2 for information on the correlation between programming-resistor value and the OC threshold. The values in 表 6-2 show typical OC thresholds for a given resistor. Assuming a fixed resistance on the OC_ADJ pin across multiple devices, a 20% device-to-device variation in OC threshold measurements is possible. Therefore, this feature is designed for system protection and not for precise current control. Noter that a properly functioning overcurrent detector assumes the presence of a proper inductor or power ferrite bead at the power-stage output. Short-circuit protection is not guaranteed with direct short at the output pins of the power stage.

For normal operation, inductance in motor (assume larger than 10µH) is sufficient to provide low di/dt output (for example, for EMI) and proper protection during overload condition (CBC current limiting feature). So no additional output inductors are needed during normal operation.

However, during a short condition, the motor (or other load) is shorted, so the load inductance is not present in the system anymore; the current in the device can reach such a high level that may exceed the abs max current rating due to extremely low impenitence in the short circuit path and high di/dt before oc detection circuit kicks in. So, a ferrite bead or inductor is recommended to use the short-circuit protection feature in DRV841x2. With an external inductance or ferrite bead, the current rises at a much slower rate and reach a lower current level before oc protection starts. The device then either operates CBC current limit or OC shut down automatically (when current is well above the current limit threshold) to protect the system.

For a system that has limited space, a power ferrite bead can be used instead of an inductor. The current rating of ferrite bead has to be higher than the RMS current of the system at normal operation. A ferrite bead designed for very high frequency is NOT recommended. A minimum impedance of 10Ω or higher is recommended at 10MHz or lower frequency to effectively limit the current rising rate during short circuit condition.

The TDK MPZ2012S300A (with size of 0805 inch type) have been tested in our system to meet a short circuit condition in the DRV8412. But other ferrite beads that have similar frequency characteristics can be used as well.

For higher power applications, such as in the DRV8432, there might be limited options to select suitable ferrite bead with high current rating. If an adequate ferrite bead cannot be found, an inductor can be used.

The inductance can be calculated as:

$$Loc\_min = \frac{PVDD \cdot Toc\_delay}{Ipeak - Iave} \tag{1}$$

where

- Toc_delay = 250nS
- Ipeak = 15A (below abs max rating)

Because an inductor usually saturates after reaching the current rating, the recommendation is to use an inductor with a doubled value or an inductor with a current rating well above the operating condition.

表 6-2. Programming-Resistor Values and OC Threshold

OC-ADJUST RESISTOR VALUES (kΩ)	MAXIMUM CURRENT BEFORE OC OCCURS (A)
22[(1)]	11.6
24	10.7
27	9.7
30	8.8
36	7.4

(1) Recommended to use in OC Latching Mode Only

6.3.2.3 Overtemperature Protection

The DRV841x2 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTSD is latched in this case and $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ must be asserted low to clear the latch.

6.3.2.4 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the DRV841x2 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overcurrent circuit and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltage on the bootstrap capacitors have increased above the UVP threshold.

6.3.3 Device Reset

Two reset pins are provided for independent control of half-bridges A/B and C/D. When $\overline{\text{RESET\_AB}}$ is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance (Hi-Z) state. Likewise, asserting $\overline{\text{RESET\_CD}}$ low forces all four power-stage FETs in half-bridges C and D into a high- impedance state. To accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs.

A rising-edge transition on reset input allows the device to resume operation after a shut-down fault. For example, when either or both half-bridge A and B have OC shutdown, a low to high transition of $\overline{\text{RESET\_AB}}$ pin clears the fault and $\overline{\text{FAULT}}$ pin; when either or both half-bridge C and D have OC shutdown, a low to high transition of $\overline{\text{RESET\_CD}}$ pin will clear the fault and $\overline{\text{FAULT}}$ pin as well. When an OTSD occurs, both $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ need to have a low to high transition to clear the fault and $\overline{\text{FAULT}}$ signal.

6.4 Device Functional Modes

The DRV841x2 supports four different modes of operation:

1. Dual full bridges (FB) (two PWM inputs each full bridge) or four half bridges (HB) with CBC current limit
2. Dual full bridges (two PWM inputs each full bridge) or four half bridges with OC latching shutdown (no CBC current limit)
3. Parallel full bridge (PFB) with CBC current limit
4. Dual full bridges (one PWM input each full bridge) with CBC current limit

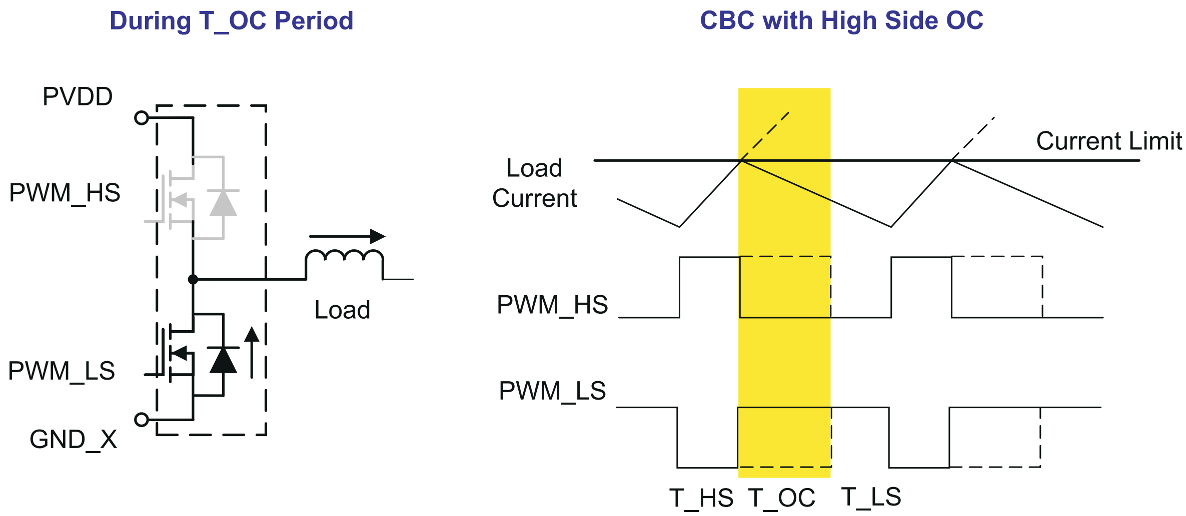
In mode 1 and 2, PWM_A controls half bridge A, PWM_B controls half bridge B, and so forth 图 7-1 shows an application example for full bridge mode operation.

In parallel full bridge mode (mode 3), PWM_A controls both half bridges A and B, and PWM_B controls both half bridges C and D, while PWM_C and PWM_D pins are not used (recommended to connect to ground). Bridges A and B are synchronized internally (even during CBC), and so are bridges C and D. OUT_A and OUT_B should be connected together and OUT_C and OUT_D should be connected together after the output inductor or ferrite bead. If $\overline{\text{RESET\_AB}}$ or $\overline{\text{RESET\_CD}}$ are low, all four outputs become high-impedance. 图 7-8 shows an example of parallel full bridge mode connection.

In mode 4, one PWM signal controls one full bridge to relieve some I/O resource from MCU, that is, PWM_A controls half bridges A and B and PWM_C controls half bridges C and D. In this mode, the operation of half bridge B is complementary to half bridge A, and the operation of half bridge D is complementary to half bridge C. For example, when PWM_A is high, high side FET in half bridge A and low side FET in half bridge B will be on and low side FET in half bridge A and high side FET in half bridge B will be off. Since PWM_B and PWM_D pins are not used in this mode, it is recommended to connect them to ground.

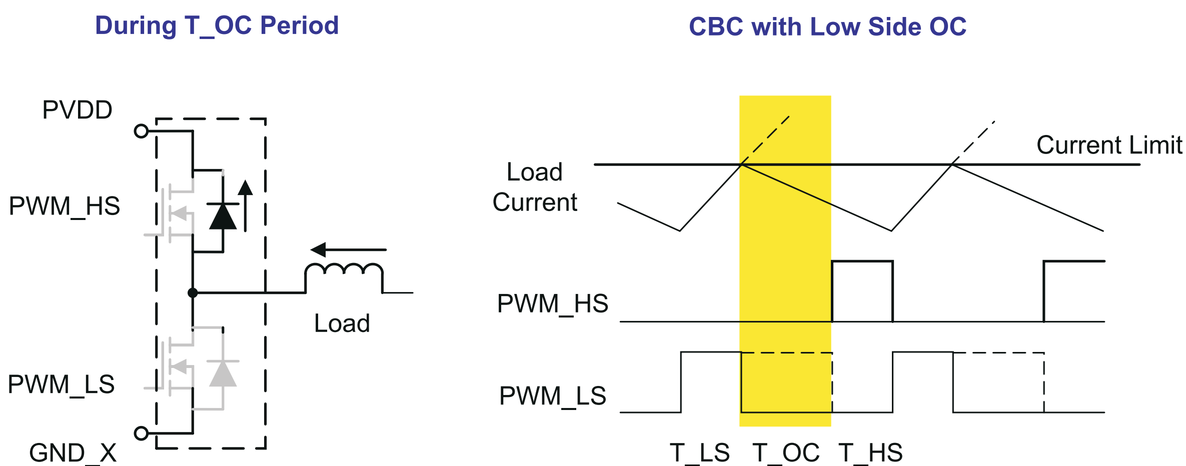
In operation modes 1, 2, and 4 (CBC current limit is used), once the CBC current limit is hit, the driver will be deactivated until the next PWM cycle starts. However, in order for the output to be recovered, the PWM input corresponding to that driver in CBC must be toggled. Because of this, CBC mode does not support operation when one half-bridge PWM input is tied to dc logic level.

Because each half bridge has independent supply and ground pins, a shunt sensing resistor can be inserted between PVDD to PVDD_X or GND_X to GND (ground plane). A high side shunt resistor between PVDD and PVDD_X is recommended for differential current sensing because a high bias voltage on the low side sensing could affect device operation. If low side sensing has to be used, a shunt resistor value of 10 mΩ or less or sense voltage 100mV or less is recommended.



Dashed line: normal operation; solid line: CBC event

图 6-1. Cycle-by-Cycle Operation With High-Side OC



Dashed line: normal operation; solid line: CBC event

图 6-2. Cycle-by-Cycle Operation With Low-Side OC

Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The DRV841x2 devices are typically used to drive 2 brushed DC or 1 stepper motor.

The DRV841x2 can be used for stepper motor applications as illustrated in 图 7-9; the devices can be also used in three phase permanent magnet synchronous motor (PMSM) and sinewave brushless DC motor applications.

图 7-10 shows an example of a TEC driver application. The same configuration can also be used for DC output applications.

2 Typical Applications

2.1 Full Bridge Mode Operation

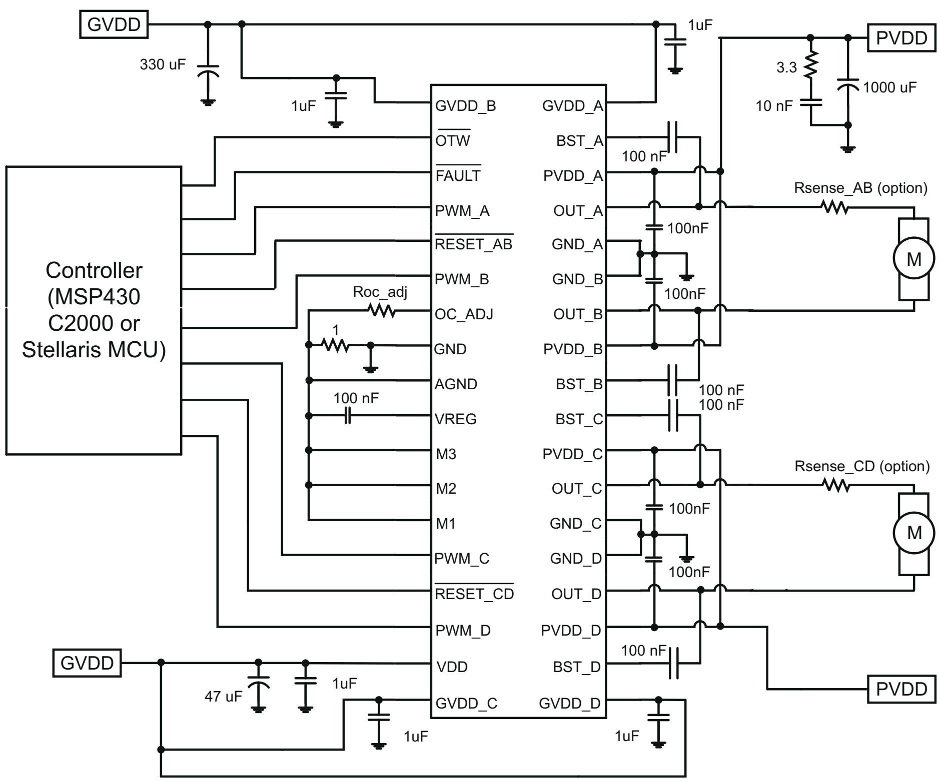


图 7-1. Application Diagram Example for Full Bridge Mode Operation Schematic

2.1.1 Design Requirements

This section describes design considerations.

表 7-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor voltage	PVDD_x	24V
Motor current (peak and RMS)	I_{PVDD}	6A peak, 3A RMS
Overcurrent threshold	OC_{TH}	OC_ADJ = 27kΩ, 9.7A
Bridge mode	M1M2	Parallel full bridge

2.1.2 Detailed Design Procedure

2.1.2.1 Motor Voltage

Higher voltages generally have the advantage of causing current to change faster through the inductive windings, which allows for higher RPMs. Lower voltages allow for more accurate control of phase currents.

2.1.2.2 Current Requirement of 12V Power Supply

The DRV83x2 requires a 12V power supply for GVDD and VDD pins. The total supply current is relatively low at room temperature (less than 50mA), but the current could increase significantly when the device temperature goes too high (for example, above 125°C), especially at heavy load conditions due to substrate current collection by 12V guard rings. TI recommends designing the 12V power supply with a current capability at least 5-10% of the load current, and no less than 100mA for the device performance across all temperature ranges.

2.1.2.3 Voltage of Decoupling Capacitor

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. The high frequency decoupling capacitor should use ceramic capacitor with X5R or better rating. For a 50V application, a minimum voltage rating of 63V is recommended.

2.1.2.4 Overcurrent Threshold

When choosing the resistor value for OC_ADJ, consider the peak current allowed under normal system behavior, the resistor tolerance, and that 表 6-2 currents have a ±10% tolerance. For example, if 6A is the highest system current allowed across all normal behavior, a 27kΩ OC_ADJ resistor with 10% tolerance is a reasonable choice, as it would set the OC_{TH} to approximately 8A to 12A.

2.1.2.5 Sense Resistor

For optimal performance, the sense resistor must be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}{}^2 \times R$. For example, if peak motor current is 3A, RMS motor current is 2A, and a 0.05Ω sense resistor is used, the resistor will dissipate $2A^2 \times 0.05\Omega = 0.2W$. The power increases quickly with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. Always measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

2.1.3 Application Curves

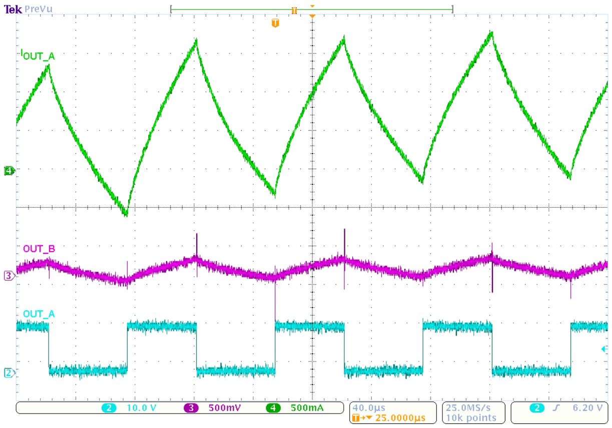


图 7-2. Brushed DC Driving

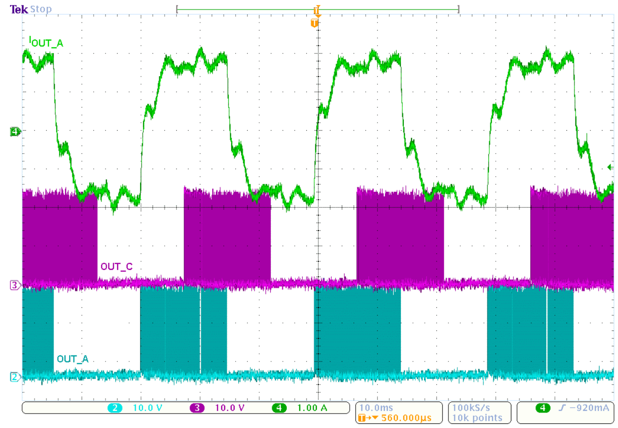


图 7-3. Stepper Control, Full Stepping, 24V

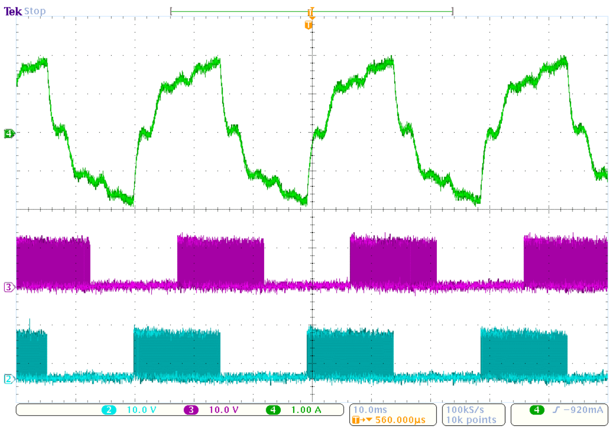


图 7-4. Stepper Control, Full Stepping, 12V

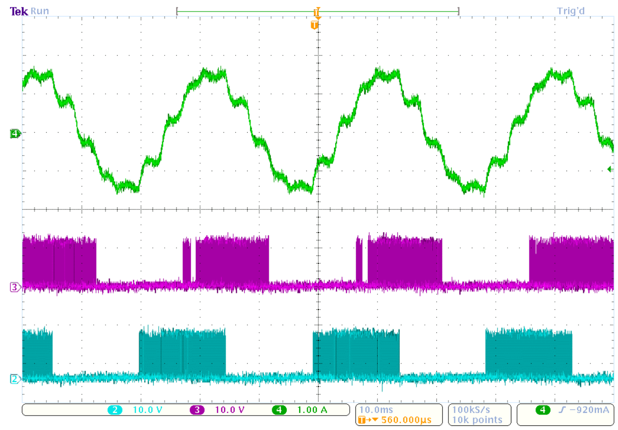


图 7-5. Stepper Control, Half Stepping, 12V

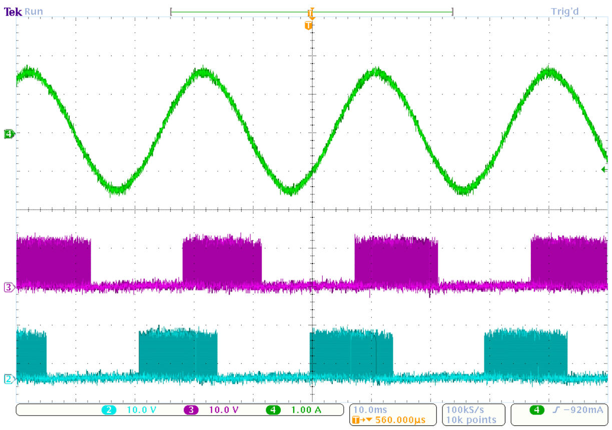


图 7-6. Stepper Control, 128 Microstepping, 12V

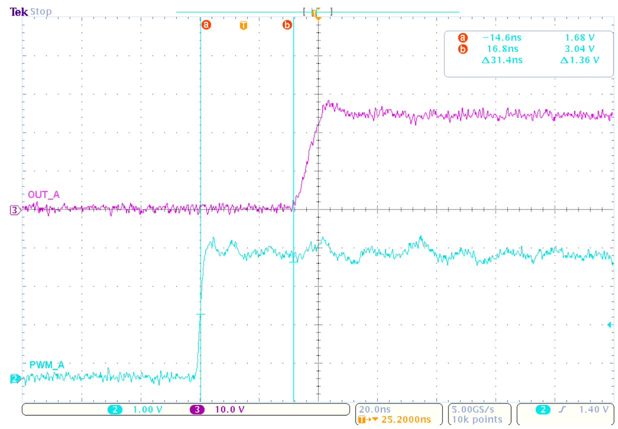
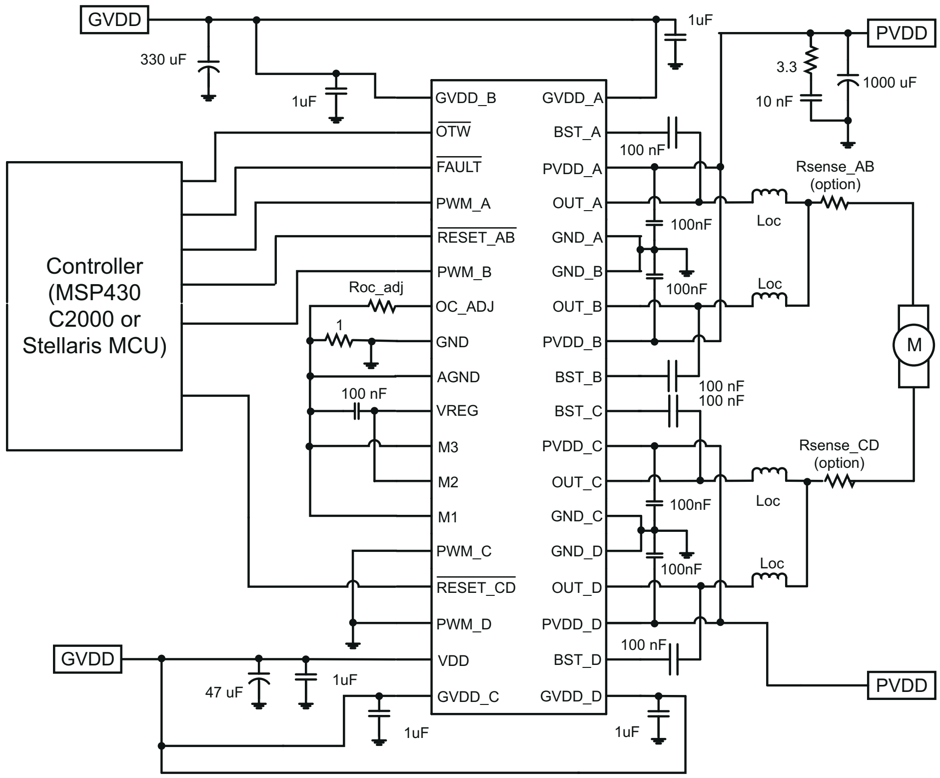


图 7-7. PWM_A to OUTA

2.2 Parallel Full Bridge Mode Operation



PWM_A controls OUT_A and OUT_B; PWM_B controls OUT_C and OUT_D.

图 7-8. Application Diagram Example for Parallel Full Bridge Mode Operation Schematic

2.3 Stepper Motor Operation

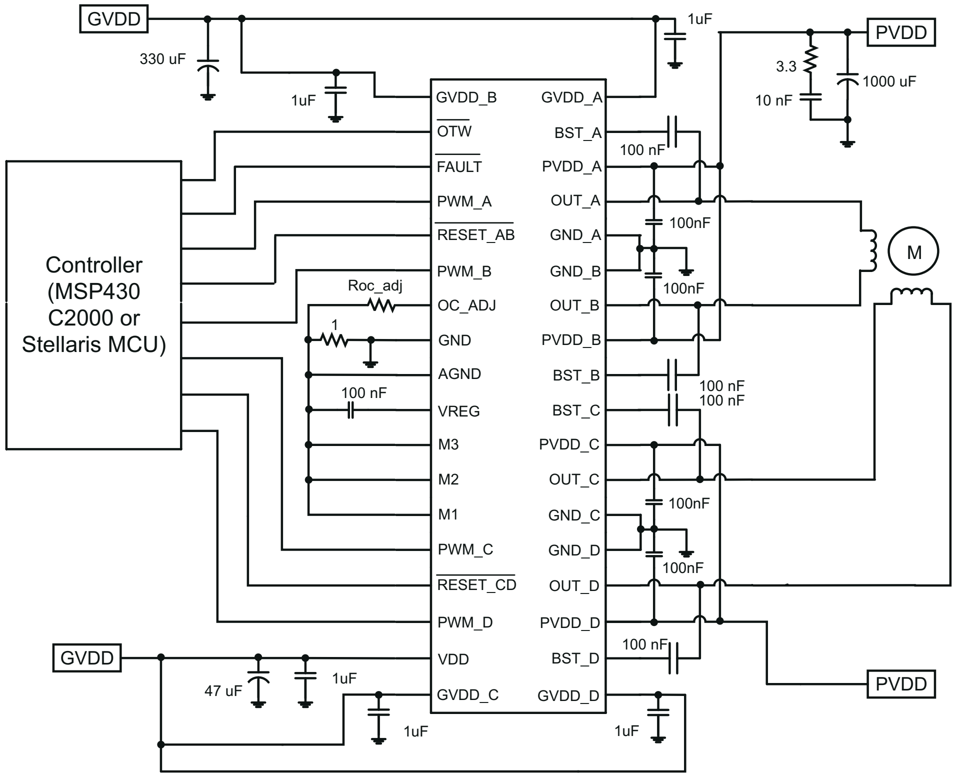


图 7-9. Application Diagram Example for Stepper Motor Operation Schematic

2.4 TEC Driver

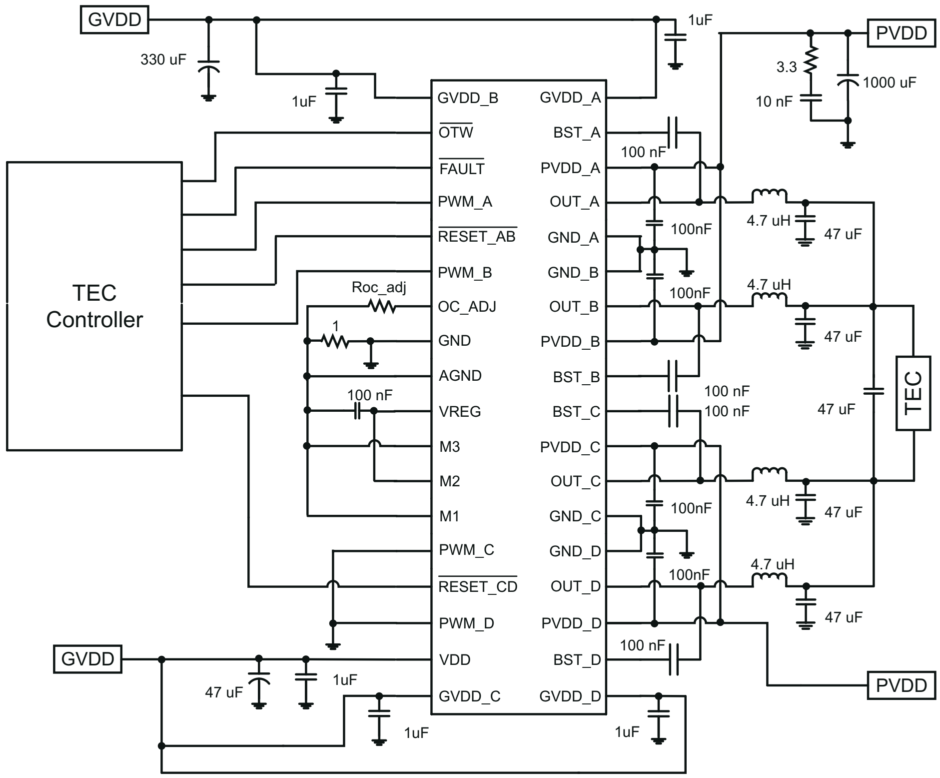


图 7-10. Application Diagram Example for TEC Driver Schematic

2.5 LED Lighting Driver

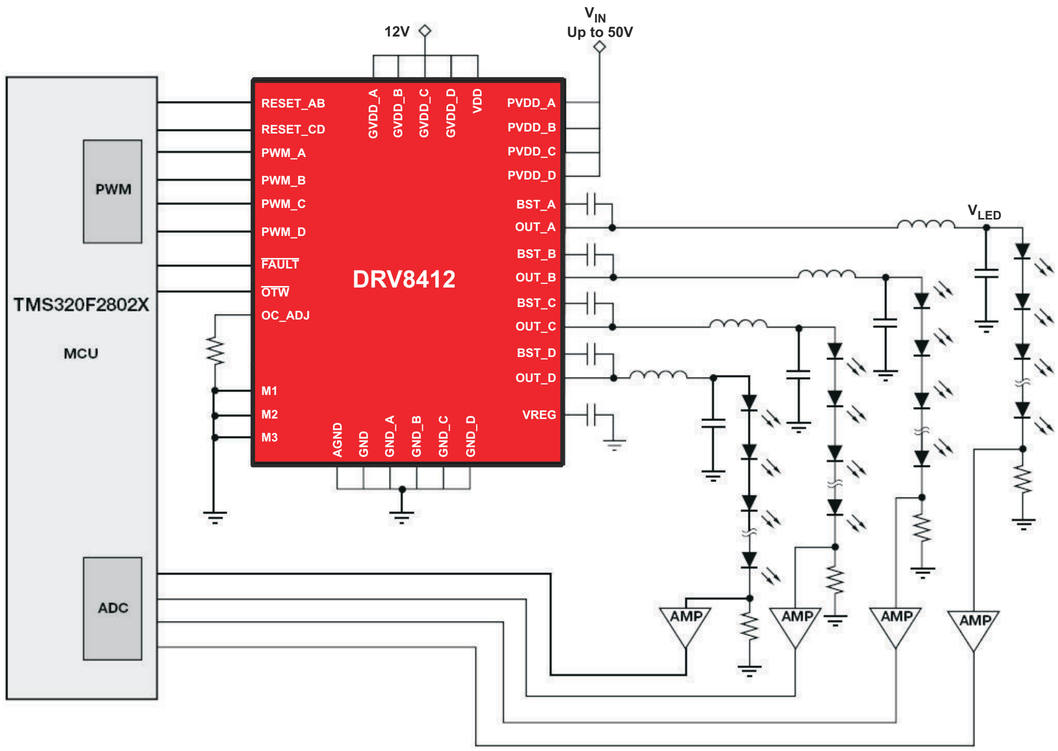


图 7-11. Application Diagram Example for LED Lighting Driver Schematic

3 Power Supply Recommendations

3.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

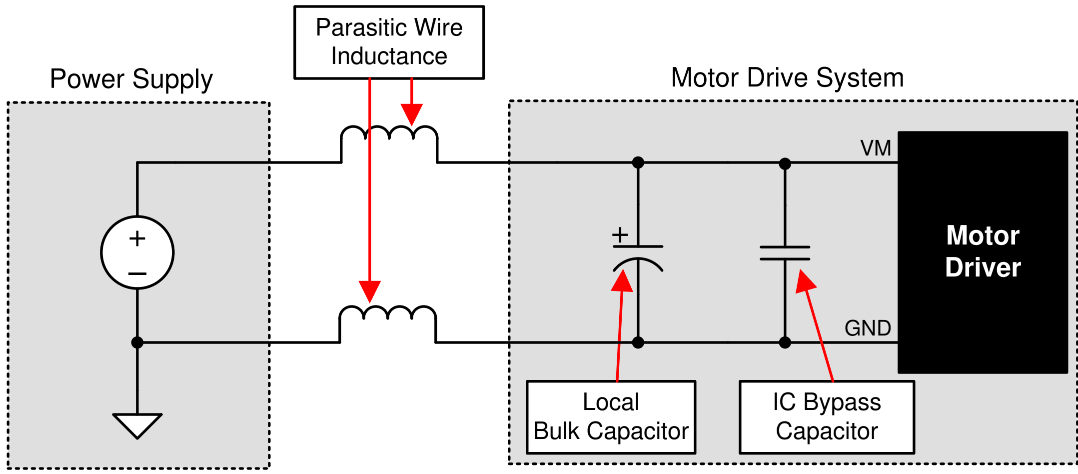


图 7-12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

3.2 Power Supplies

To facilitate system design, the DRV841x2 needs only a 12V supply in addition to H-Bridge power supply (PVDD). An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, the high-side gate drive requires a floating voltage supply, which is accommodated by built-in bootstrap circuitry requiring external bootstrap capacitor.

To provide symmetrical electrical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has a separate gate drive supply (GVDD_X), a bootstrap pin (BST_X), and a power-stage supply pin (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Special attention should be paid to place all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. Furthermore, decoupling capacitors need a short ground path back to the device.

For a properly functioning bootstrap circuit, a small ceramic capacitor (an X5R or better) must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 10kHz to 500kHz, the use of 100-nF ceramic capacitors (X5R or better), size 0603 or 0805, is recommended for the bootstrap supply. These 100nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET fully turned on during the remaining part of the PWM cycle. In an application running at a switching frequency lower than 10 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pin (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a ceramic capacitor (X5R or better) placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the DRV841x2 EVM board.

The 12V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the DRV841x2 is fully protected against erroneous power-stage turn-on due to parasitic gate charging. Thus, voltage-supply ramp rates (dv/dt) are non-critical within the specified voltage range (see 节 5.3 of this data sheet).

3.3 System Power-Up and Power-Down Sequence

3.3.1 Powering Up

The DRV841x2 does not require a power-up sequence. The outputs of the H-bridges remain in a high impedance state until the gate-drive supply voltage GVDD_X and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, holding $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ in a low state while powering up the device is recommended. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

3.3.2 Powering Down

The DRV841x2 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the UVP voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ low during power down to prevent any unknown state during this transition.

3.4 System Design Recommendations

3.4.1 VREG Pin

The VREG pin is used for internal logic and not recommended to be used as a voltage source for external circuitry.

3.4.2 VDD Pin

The transient current in VDD pin could be significantly higher than average current through that pin. A low resistive path to GVDD should be used. A 22µF to 47µF capacitor should be placed on VDD pin beside the 100nF to 1µF decoupling capacitor to provide a constant voltage during transient.

3.4.3 OTW Pin

$\overline{\text{OTW}}$ reporting indicates the device approaching high junction temperature. This signal can be used with MCU to decrease system power when $\overline{\text{OTW}}$ is low in order to prevent OT shut down at a higher temperature.

3.4.4 Mode Select Pin

Mode select pins (M1, M2, and M3) should be connected to either VREG (for logic high) or AGND for logic low. The recommendation is to not connect mode pins to board ground if 1 Ω resistor is used between AGND and GND.

3.4.5 Parallel Mode Operation

For a device operated in parallel mode, a minimum of 30 nH to 100 nH inductance or a ferrite bead is required after the output pins (for example, OUT_A and OUT_B) before connecting the two channels together. This helps to prevent any shoot through between two paralleled channels during switching transient due to mismatch of paralleled channels (for example, processor variation, unsymmetrical PCB layout, and so on).

3.4.6 TEC Driver Application

For TEC driver or other non-motor related applications (for example, resistive load or dc output), a low-pass LC filter can be used to meet the requirement.

4 Layout

4.1 Layout Guidelines

4.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 2oz. copper on both top and bottom layer is recommended for improved thermal performance (better heat sinking) and less noise susceptibility (lower PCB trace inductance).

4.1.2 Ground Plane

Because of the power level of these devices, it is recommended to use a big unbroken single ground plane for the whole system / board. The ground plane can be easily made at bottom PCB layer. In order to minimize the impedance and inductance of ground traces, the traces from ground pins should keep as short and wide as possible before connected to bottom ground plane through vias. Multiple vias are suggested to reduce the impedance of vias. Try to clear the space around the device as much as possible especially at bottom PCB side to improve the heat spreading.

4.1.3 Decoupling Capacitor

High frequency decoupling capacitors (100 nF) on PVDD_X pins should be placed close to these pins and with a short ground return path to minimize the inductance on the PCB trace.

4.1.4 AGND

AGND is a localized internal ground for logic signals. A 1Ω resistor is recommended to be connected between GND and AGND to isolate the noise from board ground to AGND. There are other two components are connected to this local ground: 0.1μF capacitor between VREG to AGND and Roc_adj resistor between OC_ADJ and AGND. Capacitor for VREG should be placed close to VREG and AGND pin and connected without vias.

4.2 Layout Example

4.2.1 Current Shunt Resistor

If current shunt resistor is connected between GND_X to GND or PVDD_X to PVDD, make sure there is only one single path to connect each GND_X or PVDD_X pin to shunt resistor, and the path is short and symmetrical on each sense path to minimize the measurement error due to additional resistance on the trace.

An example of the schematic and PCB layout of DRV8412 are shown in 图 7-13, 图 7-14, and 图 7-15.

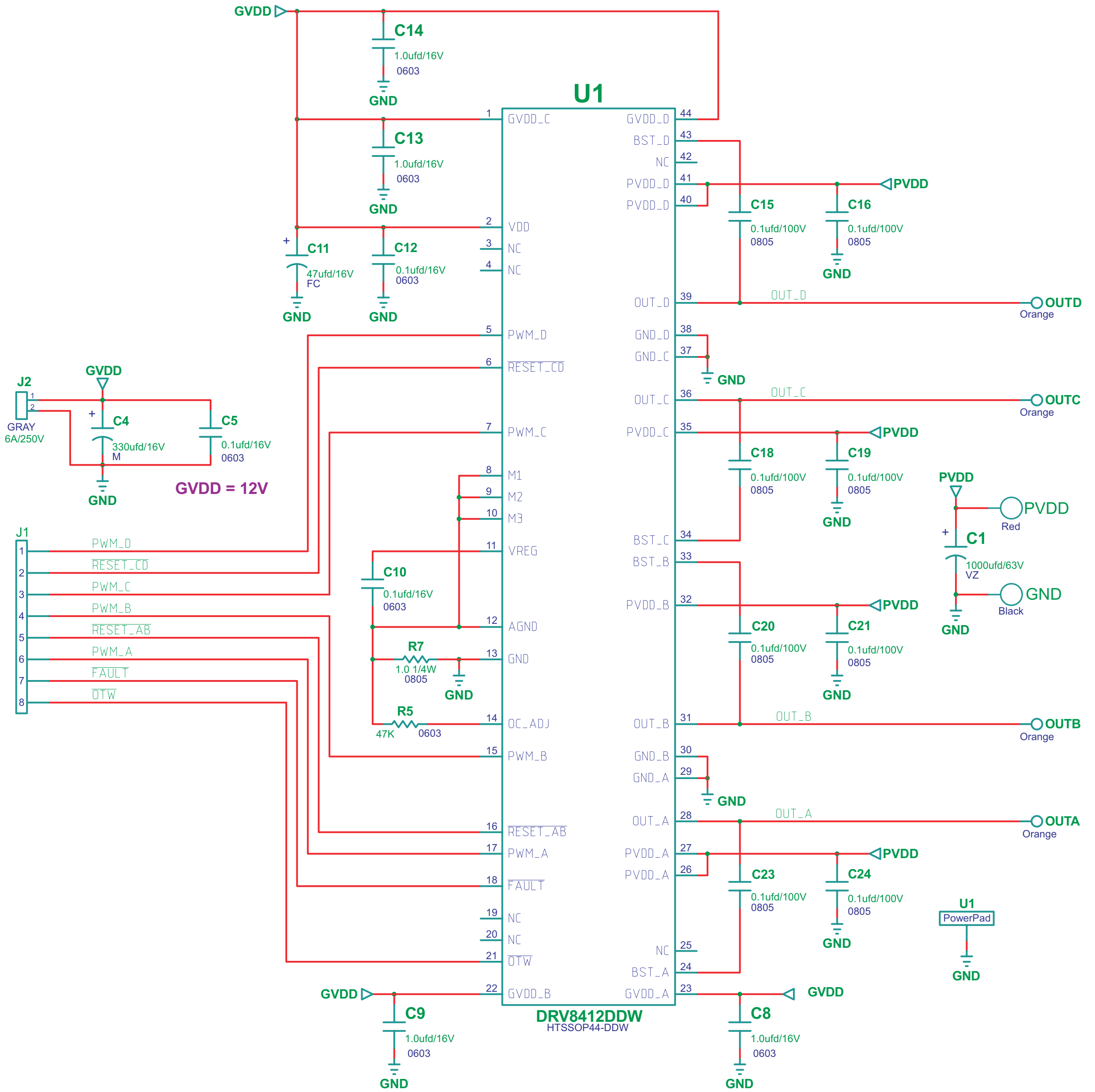
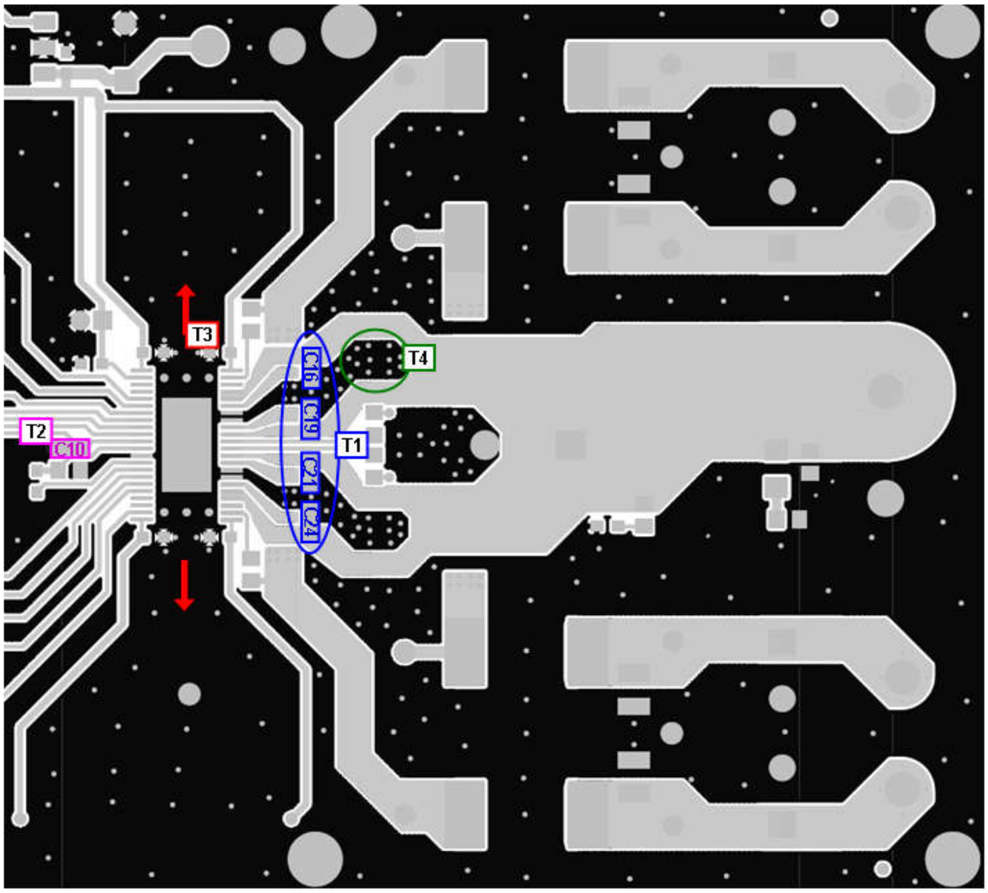
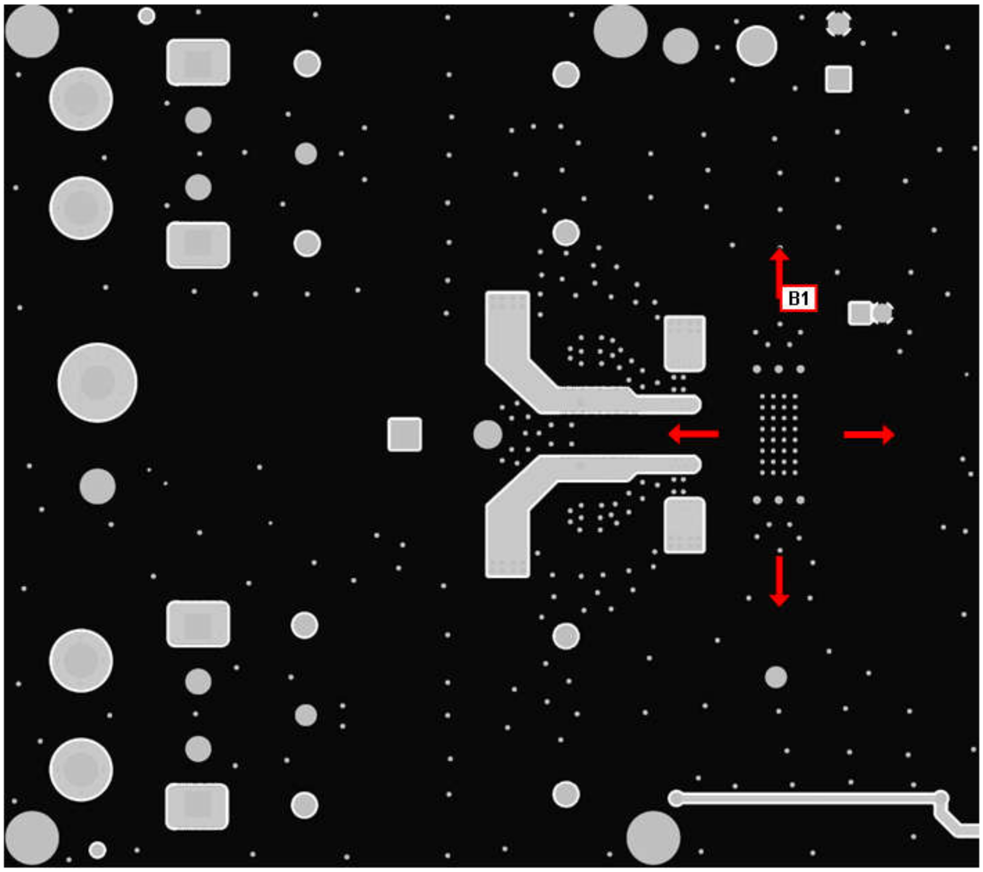


图 7-13. DRV8412 Schematic Example



T1: PVDD decoupling capacitors C16, C19, C21, and C24 should be placed very close to PVDD_X pins and ground return path.
T2: VREG decoupling capacitor C10 should be placed very close to VREG abd AGND pins.
T3: Clear the space above and below the device as much as possible to improve the thermal spreading.
T4: Add many vias to reduce the impedance of ground path through top to bottom side. Make traces as wide as possible for ground path such as GND_X path.

图 7-14. Printed Circuit Board – Top Layer



B1: Do not block the heat transfer path at bottom side. Clear as much space as possible for better heat spreading.

图 7-15. Printed Circuit Board – Bottom Layer

4.3 Thermal Considerations

The thermally enhanced package provided with the DRV8432 is designed to interface directly to heat sink using a thermal interface compound, (for example, Ceramique from Arctic Silver, TIMTronics 413, and so on). The heat sink then absorbs heat from the ICs and couples to the local air. A good practice is to connect the heatsink to system ground on the PCB board to reduce the ground noise.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. The system parameters have the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this example the power pad or heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed power pad or heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The approximate exposed heat slug size is as follows:

- DRV8432, 36-pin PSOP3 ······ 0.124 in^2 (80mm^2)

The thermal resistance of thermal pads is considered higher than a thin thermal grease layer and is not recommended. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

See the TI application report, *IC Package Thermal Metrics* (SPRA953), for more thermal information.

4.3.1 DRV8412 Thermal Via Design Recommendation

Thermal pad of the DRV8412 is attached at bottom of device to improve the thermal capability of the device. The thermal pad has to be soldered with a very good coverage on PCB to deliver the power specified in the data sheet. 图 7-16 shows the recommended thermal via and land pattern design for the DRV8412. For additional information, see TI application report, PowerPad™ Made Easy (SLMA004) and PowerPad Layout Guidelines (SOLA120).

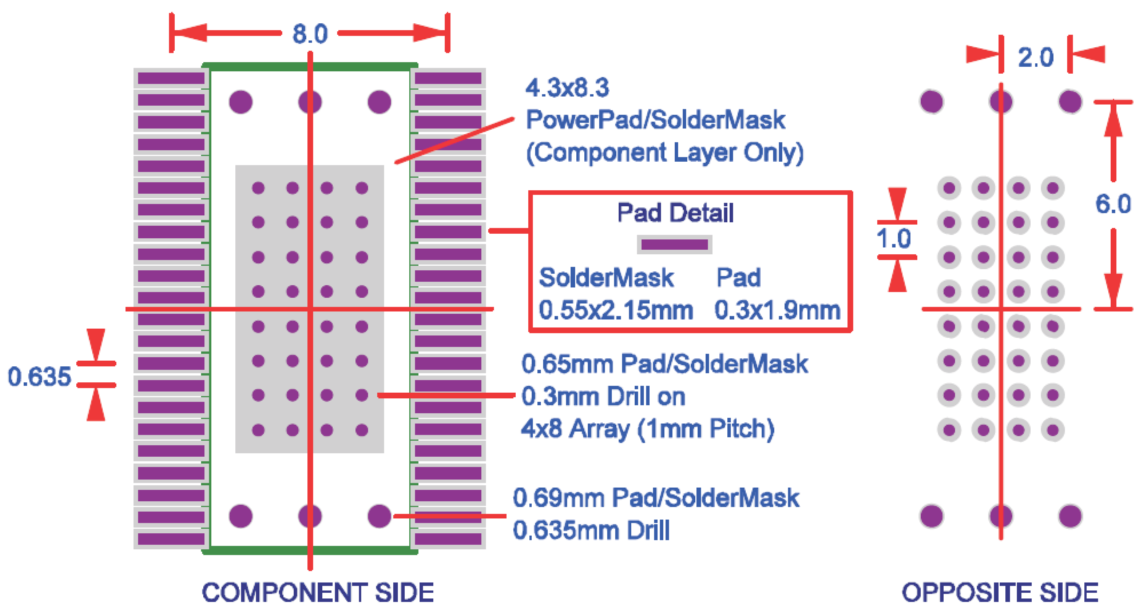


图 7-16. DRV8412 Thermal Via Footprint

7 Device and Documentation Support

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.3 Trademarks

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7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (July 2014) to Revision H (July 2024) — **Page**

- 将“器件信息”表更改为*封装信息* 表 1
- Deleted values in 39 to 200 in 表 6-2 12

Changes from Revision F (January 2014) to Revision G (July 2014) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1

Changes from Revision E (October 2013) to Revision F (January 2014) — **Page**

- Changed GND_A, GND_B, GND_C, and GND_D pins description to remove text "requires close decoupling capacitor to ground" 3
- Changed the t_{ON_MIN} description to include "for charging the Bootstrap capacitor" 5
- Added text to the Overcurrent (OC) Protection section - "It is important to note..." 12

Changes from Revision D (July 2011) to Revision E (October 2013) — **Page**

- Added last sentence in description of Thermal Pad in Pin Functions table 3
- Added THERMAL INFORMATION table 6

- Added a new paragraph in DIFFERENT OPERATIONAL MODES section: In operation modes.....DC logic level.. 14

Changes from Revision C (May 2010) to Revision D (July 2011)	Page
• 将第一个特性中的 80mΩ 更改为 110mΩ	1
• 将第二个特性中的 50V 更改为 52V	1
• 删除了第二个特性中的“(70V 绝对最大值)”	1
• 向“应用”中添加了 LED 照明驱动器	1
• Added Includes metallization bond wire and pin resistance to $R_{DS(on)}$ test conditions	7
• Changed $R_{DS(on)}$ typ from 80 mΩ to 110 mΩ	7
• Added text to 5th paragraph of Overcurrent (OC) Protection section	12
• Deleted Output Inductor Selection section and moved information into Overcurrent (OC) Protection section	12
• Changed 图 7-1	16
• Changed 图 7-9	20
• Deleted Application Diagram Example for Three Phase PMSM PVDD Sense Operation and Application Diagram Example for Three Phase PMSM GND Sense Operation figures	21
• Added 图 7-11	22
• Changed 图 7-13	25

Changes from Revision B (Jan 2010) to Revision C ()	Page
• 删除了数据表中所有与 DRV8422 相关的描述	1
• Changed the DRV8432 pinout	3
• Added Thermal Pad and Heat slug rows to end of Pin Functions table. Also added T=thermal in note	3
• Added second paragraph to Bootstrap Capacitor....section	11
• Deleted or GVDD undervoltage from DEVICE RESET section second paragraph	13

Changes from Revision A (December 2009) to Revision B ()	Page
• Added T_A = 125°C power rating of 1.0 W to package power deratings table	6

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8412DDW	LIFEBUY	HTSSOP	DDW	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8412	
DRV8412DDWR	ACTIVE	HTSSOP	DDW	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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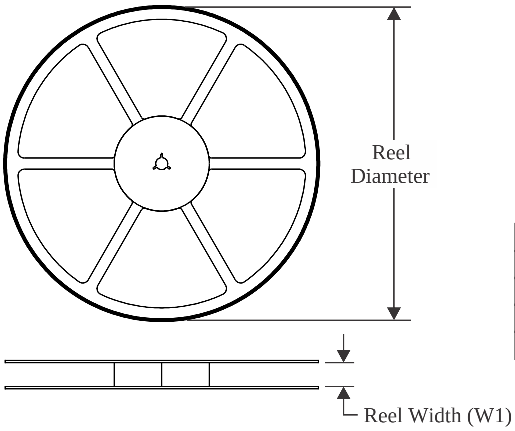
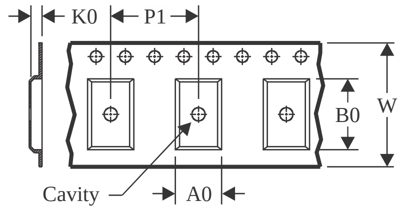
TAPE AND REEL INFORMATION

REEL DIMENSIONS

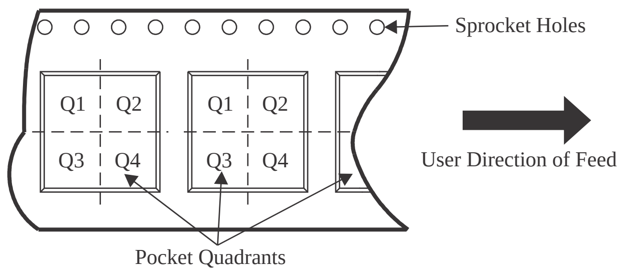


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

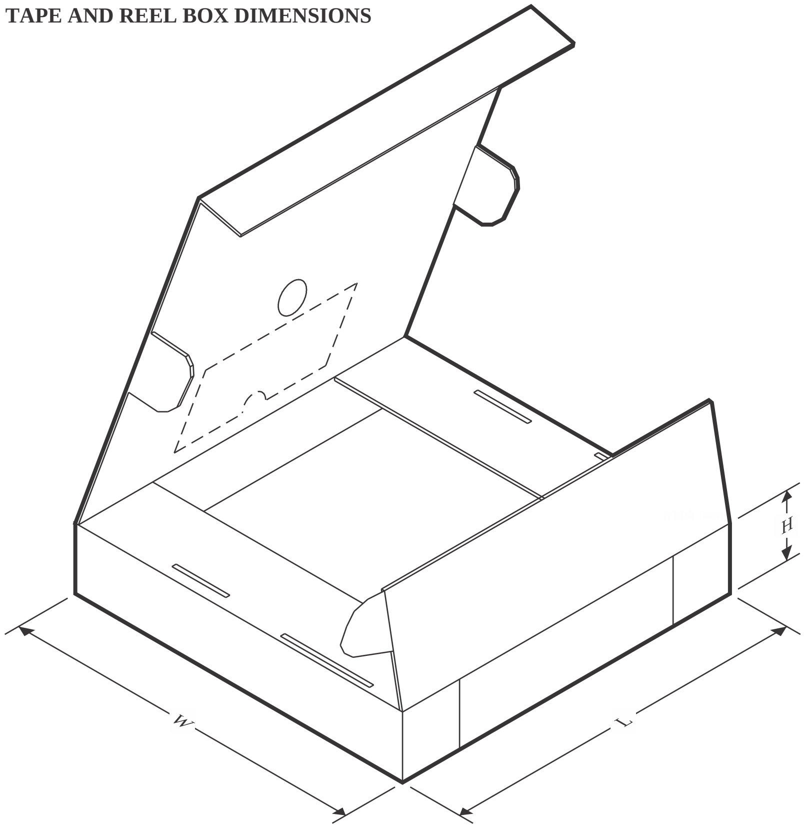
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8412DDWR	HTSSOP	DDW	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

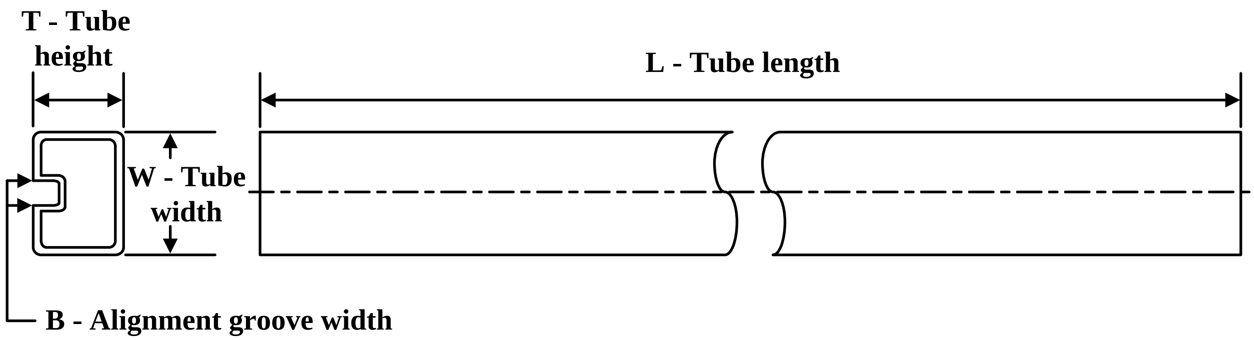
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8412DDWR	HTSSOP	DDW	44	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8412DDW	DDW	HTSSOP	44	35	530	11.89	3600	4.9

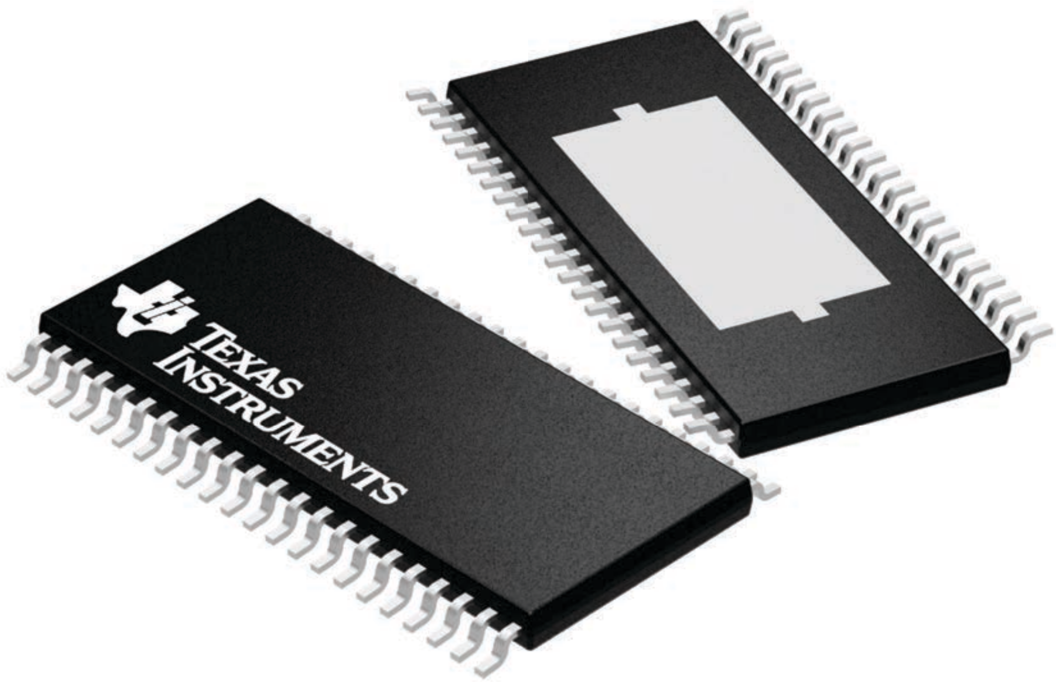
DDW 44

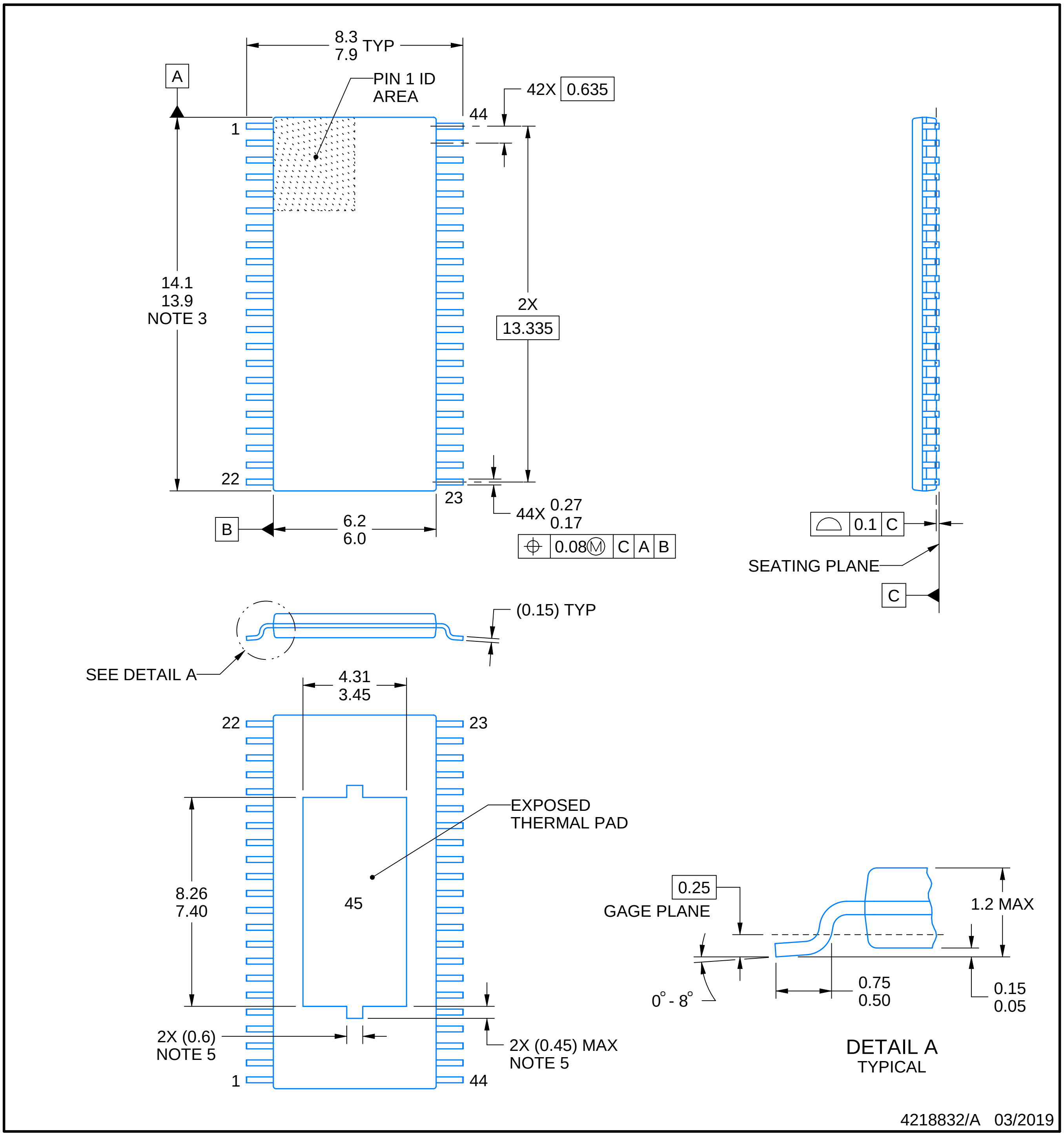
PowerPAD TSSOP - 1.2 mm max height

6.1 x 14, 0.635 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

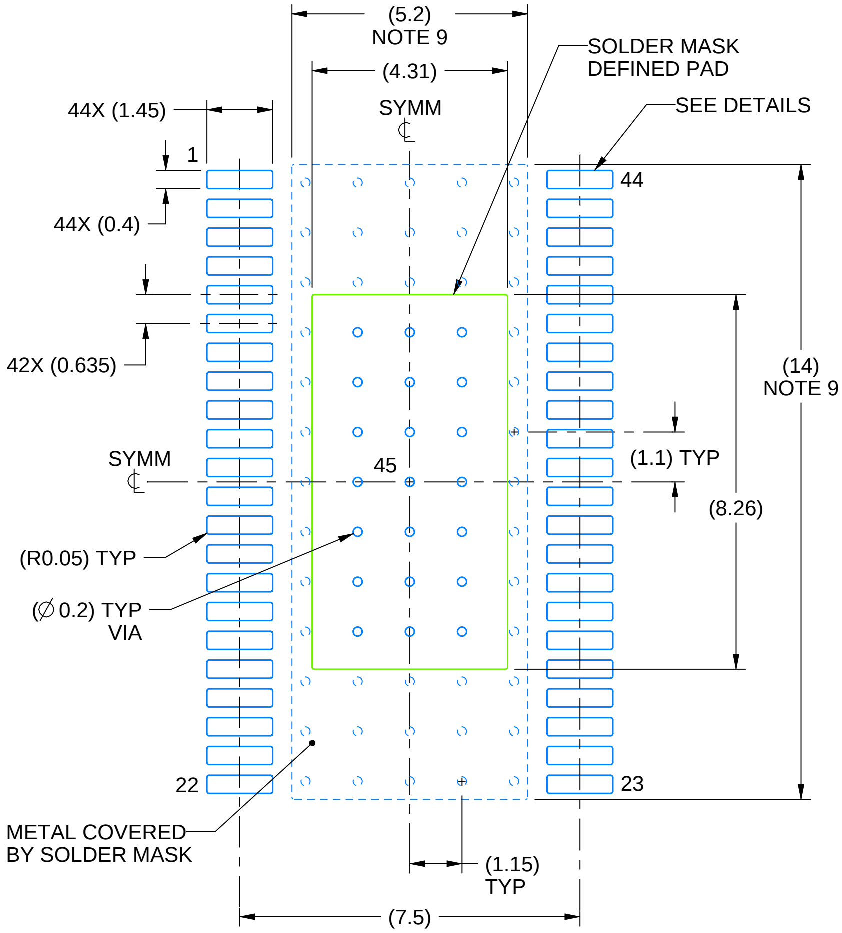




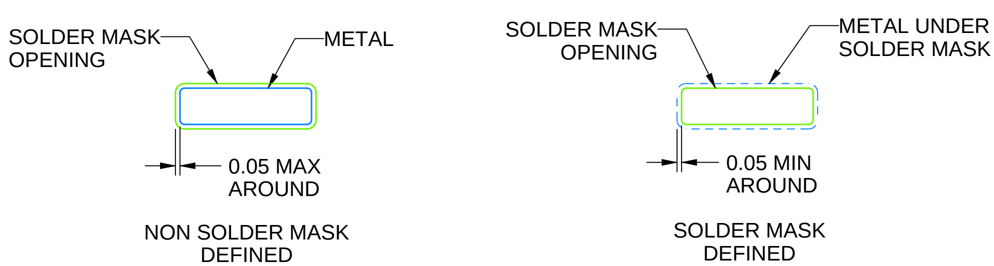
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

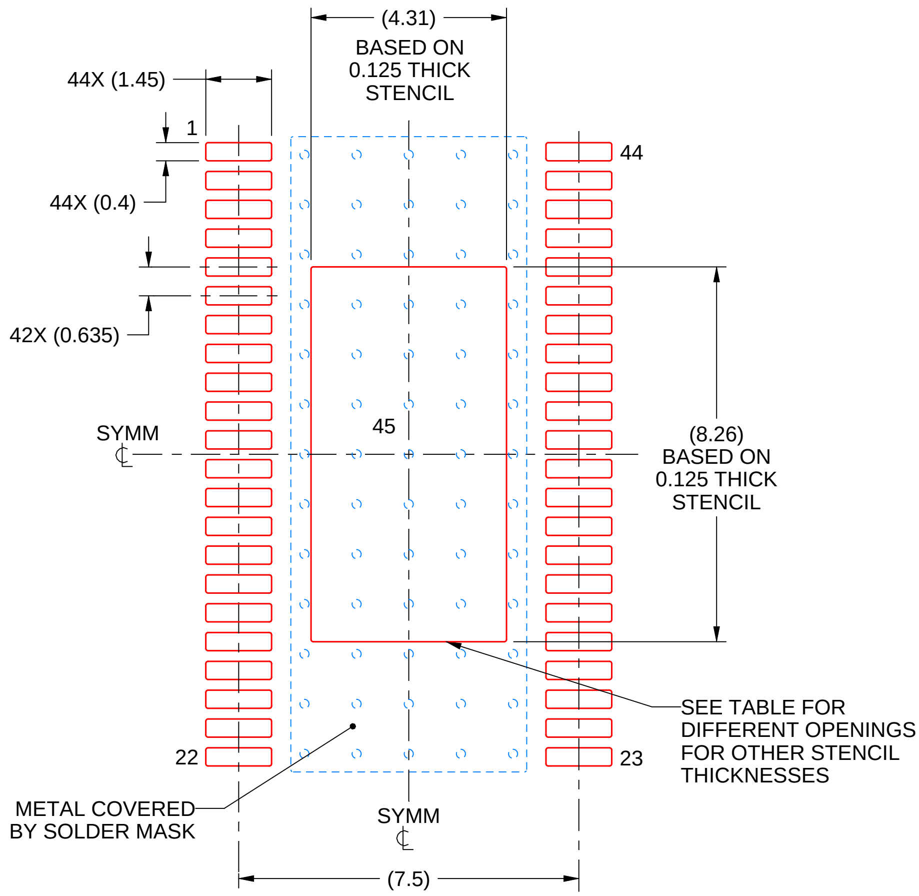


SOLDER MASK DETAILS
NOT TO SCALE

4218832/A 03/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
PAD 45:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.82 X 9.23
0.125	4.31 X 8.26 (SHOWN)
0.15	3.93 X 7.54
0.175	3.64 X 6.98

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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