ESD1LIN24 24V 单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级 ESD 保护：
  - ±30 kV 接触放电
  - ±30 kV 气隙放电
- 强大的浪涌保护：
  - IEC 61000-4-5 (8/20μs)：4.3A
- 24V 工作电压
- 双向 ESD 保护
- 低钳位电压可保护下游元件
- 温度范围：–55°C 至 +150°C
- I/O 电容 = 2.3pF（典型值）
- 采用业界通用封装：SOD-323 (DYF)
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- USB 电力传输 (USB-PD)
  - VBUS 保护
  - IO 保护
- 工业控制网络：
  - 本地互连网络 (LIN)
  - 单线 CAN ESD 保护
  - DeviceNet
  - 智能配电系统

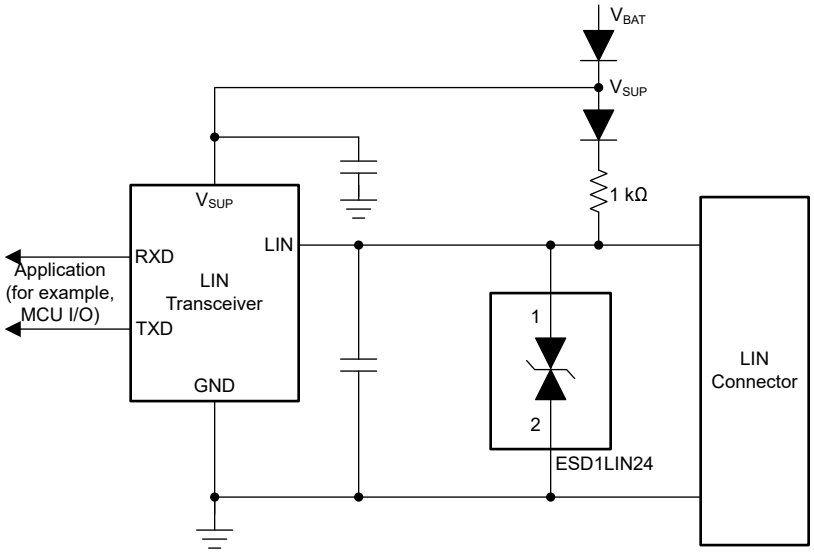
3 说明

ESD1LIN24 是适用于本地互连网络 (LIN) 的单通道低电容双向 ESD 保护器件。该器件旨在耗散超过 IEC 61000-4-2 国际标准所规定最高水平（±30kV 接触放电，±30kV 气隙放电）的接触 ESD 冲击。低动态电阻和低钳位电压有助于保护系统免受瞬态事件的影响。在对鲁棒性和可靠性要求很高的安全系统中，这种保护至关重要。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
ESD1LIN24	DYF（SOD-323，2）	2.50mm × 1.20mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (November 2022) to Revision A (December 2022)	Page
• 将数据表的状态从*预告信息*更改为*“量产数据”*	1

5 Pin Configuration and Functions

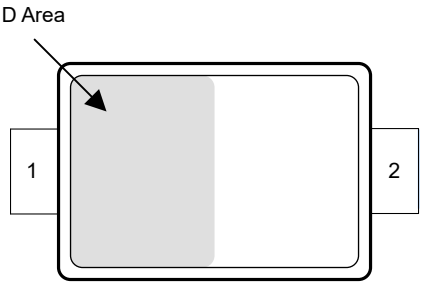


图 5-1. DYF Package, 2-Pin SOD-323 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C		159.1	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		4.3	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD1LIN24 DYF (SOD-323) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	705.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	315	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	561.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	145	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	550.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		– 24		24	V
V_{BRF}	Breakdown voltage(1)	I_{IO} = 10 mA	25.5		35.5	V
V_{BRR}		I_{IO} = – 10 mA	– 35.5		– 25.5	
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 4.3 A, t_p = 8/20 µs, from IO to GND		37	42	V
	Clamping voltage(3)	I_{PP} = 16 A, TLP, from IO to GND		40		
I_{LEAK}	Leakage current, any IO pin to GND	V_{IO} = ±24 V	-50	1	50	nA
R_{DYN}	Dynamic resistance(3)			0.5		Ω
C_L	Line capacitance, any IO to GND	V_{IO} = 0 V, f = 1 MHz, V_{p-p} = 30 mV		2.3	3.8	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

7 Typical Characteristics – ESD1LIN24

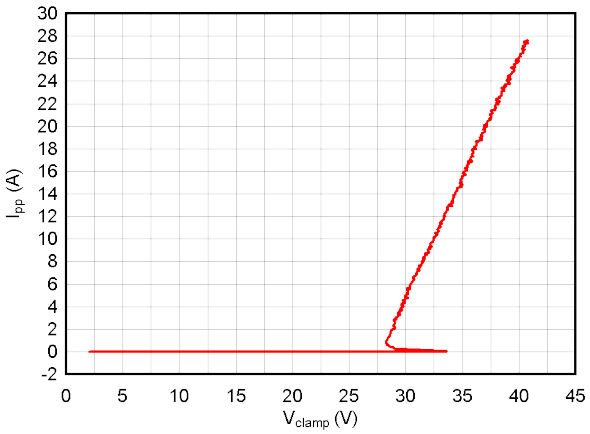


图 7-1. Positive TLP Curve

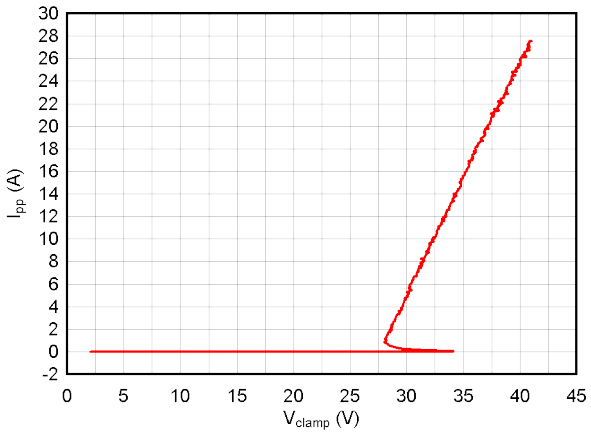


图 7-2. Negative TLP Curve

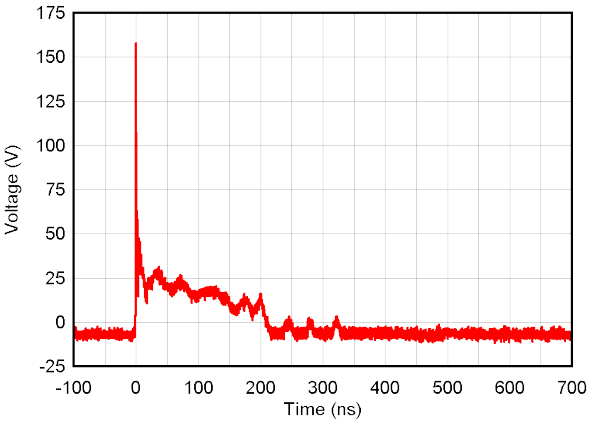


图 7-3. +8-kV Clamped IEC Waveform

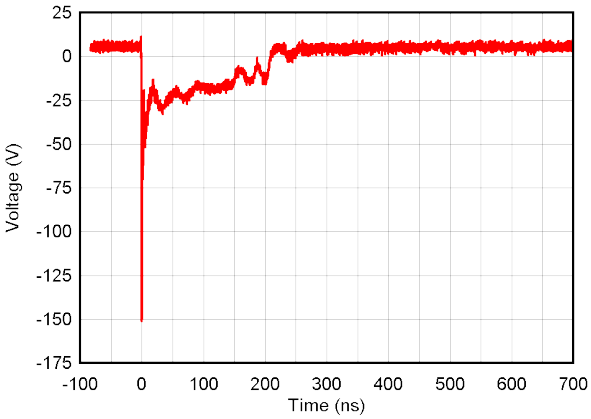


图 7-4. −8-kV Clamped IEC Waveform

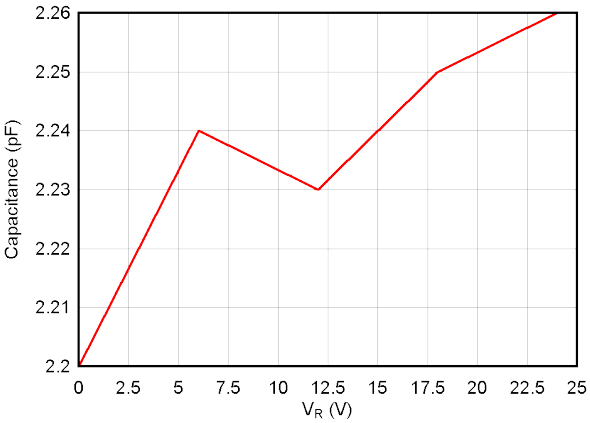


图 7-5. Capacitance vs. Bias Voltage

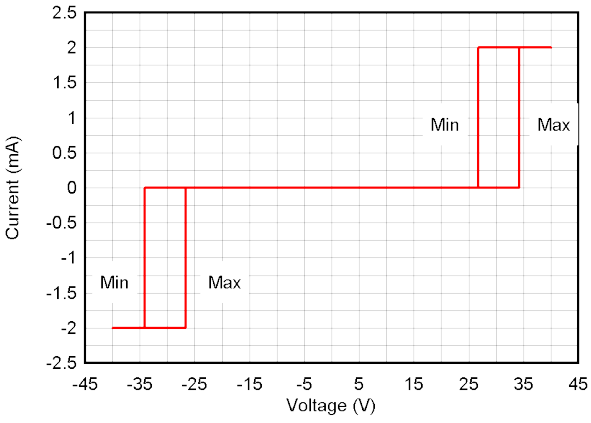


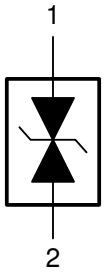
图 7-6. DC Voltage Sweep I-V Curve

8 Detailed Description

8.1 Overview

The ESD1LIN24 is a single-channel bidirectional ESD diode. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 standard. The low capacitance between the I/O pins make this device suitable for slower speed signals such as LIN, USB-PD, or industrial I/O applications. The surge current capability is suitable for VBUS protection or industrial I/Os requiring 4.3 A of surge current protection.

8.2 Functional Block Diagram



8.3 Feature Description

This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this device work at extensive temperatures in most environments. The leaded SOD-323 package is good for applications requiring autmotic optical inspection (AOI).

8.3.1 IO Capacitance

The capacitance between the I/O pins is 2.3 pF. The capacitance of this device can support data rates up to 1 Gbps.

8.3.2 IEC 61000-4-5 Surge Protection

The I/O pins of this device have a surge rating of 4.3 A (8/20 µs waveform).

8.4 Device Functional Modes

The ESD1LIN24 is a single channel passive clamp that has low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. During ESD events, transient voltages up to ±30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ESD1LIN24 is a single channel TVS diode which is used to provide a path to ground for dissipating ESD events on USB-PD or industrial I/O lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

9.2 Typical Application

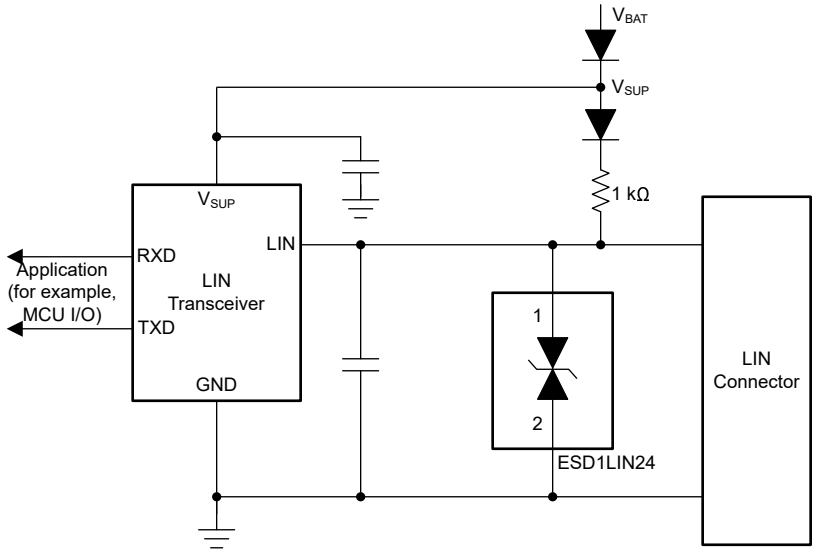


图 9-1. Typical Application

9.2.1 Design Requirements

For this design example, the ESD1LIN24 is used to provide ESD protection to a LIN transceiver. 表 9-1 lists the known design paramters for this application.

表 9-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} signal range	Up to 18 V
V_{RWM}	±24 V
Jumpstart short to battery event on V_{IO}	±24 V
Data rate	Up to 10 Mbps
Pullup resistor	1 kΩ

9.2.2 Detailed Design Procedure

The ESD1LIN24 has a V_{RWM} of ±24 V to prevent the diode from being damaged during a short event. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 2.3 pF permits data rates up to 1 Gbps, which allows the designer to meet the requirements for LIN. The 1 kΩ and V_{SUP} diode allows the LIN signal to be pulled up to a diode drop below the battery voltage.

9.2.3 Application Curves

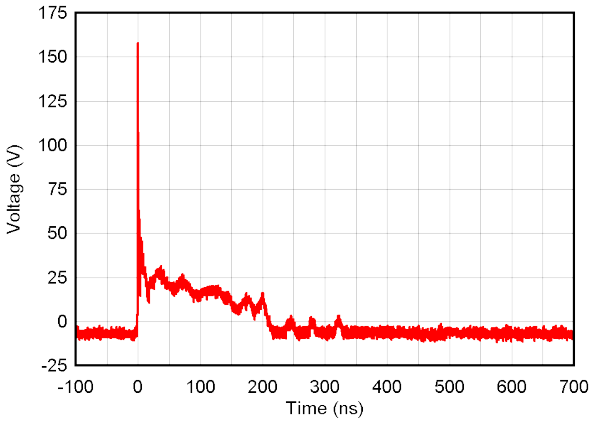


图 9-2. +8-kV Clamped IEC Waveform

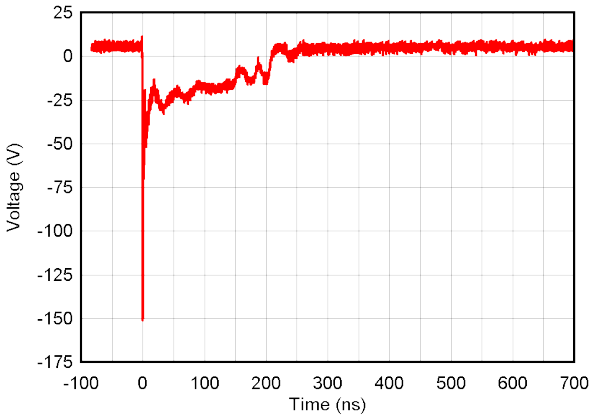


图 9-3. -8-kV Clamped IEC Waveform

10 Power Supply Recommendations

These devices are passive TVS diode-based ESD protection devices, therefore there is no requirement to power them. Ensure that the maximum voltage specifications for each pin is not violated.

11 Layout

11.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

11.2 Layout Example

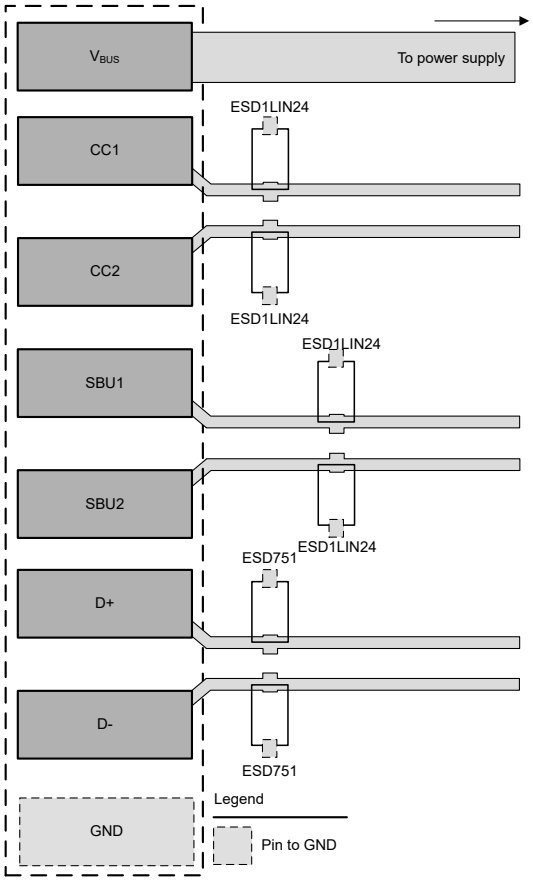


图 11-1. Layout Recommendation

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD1LIN24DYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-50 to 150	2QJF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ESD1LIN24 :

- Automotive : ESD1LIN24-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

重要声明和免责声明

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