

ESDS552 采用 SOT-23 封装的 12V 双向浪涌保护二极管

1 特性

- IEC 61000-4-5 浪涌保护：
 - 25A (8/20 μ s)
- IEC 61000-4-2 ESD 保护：
 - ± 30 kV 接触放电
 - ± 30 kV 空气间隙放电
- 12V 工作电压
- 双向极性，支持正负电压摆幅
- 双通道器件通过单个元件提供全面的 ESD/浪涌保护
- 小型引线式 SOT-23 可实现低成本的自动光学检测 (AOI)

2 应用

- 终端设备：
 - 工厂自动化和控制
 - 楼宇自动化
 - 电网基础设施
 - HVAC 系统
 - 安全系统
- 接口：
 - RS-485
 - RS-422

3 说明

ESDS552 是一个双向 ESD 和浪涌保护二极管，用于 RS-485 和 RS-422 接口保护。ESDS552 的额定 ESD 冲击消散值超出了 IEC 61000-4-2 国际标准所规定的最高水平 (± 30 kV 接触放电, ± 30 kV 空气间隙放电)。根据 IEC 61000-4-5 标准，该器件可以钳制峰值脉冲电流高达 25A 的 8/20 μ s 浪涌。

低动态电阻和低钳位电压有助于保护系统免受瞬态事件的影响。这种保护至关重要，因为工业系统对鲁棒性和可靠性的要求很高。

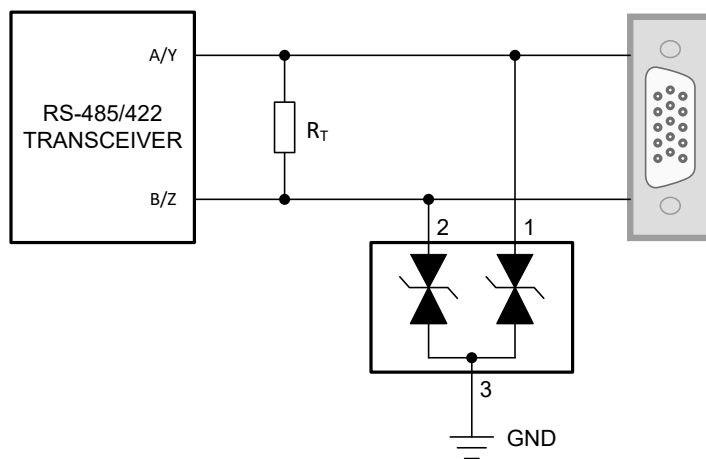
ESDS552 采用小型引线式 SOT-23 (DBZ) 封装。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
ESDS552	DBZ (SOT-23, 3)	2.92mm x 2.37mm

(1) 有关更多信息，请参阅节 9。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



典型应用原理图



Table of Contents

1 特性.....	1	6 Application and Implementation.....	6
2 应用.....	1	6.1 Application Information.....	6
3 说明.....	1	7 Device and Documentation Support.....	7
4 Pin Configuration and Functions.....	2	7.1 Documentation Support.....	7
5 Specifications.....	3	7.2 接收文档更新通知.....	7
5.1 Absolute Maximum Ratings.....	3	7.3 支持资源.....	7
5.2 ESD Ratings - JEDEC Specifications.....	3	7.4 商标.....	7
5.3 ESD Ratings - IEC Specifications.....	3	7.5 静电放电警告.....	7
5.4 Recommended Operating Conditions.....	3	7.6 术语表.....	7
5.5 Thermal Information.....	3	8 Revision History.....	7
5.6 Electrical Characteristics.....	4	9 机械、封装和可订购信息.....	7
5.7 Typical Characteristics.....	5		

4 Pin Configuration and Functions

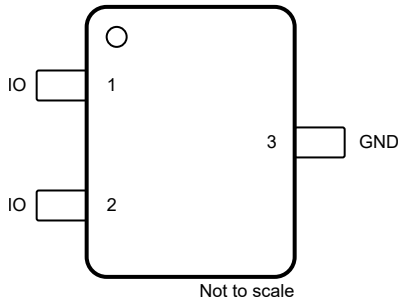


图 4-1. ESDS552 DBZ Package, 3-Pin SOT-23 (Top View)

表 4-1. Pin Functions for ESDS552

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	Surge and ESD protected IO
GND	3	GND	Ground. Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Surge (t_p 8/20 μ s) Peak Pulse Power at 25 °C		500	W
I_{PP}	IEC 61000-4-5 Surge (t_p 8/20 μ s) Peak Pulse Current at 25 °C		25	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings - JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage between any 2 pins	-12		12	V
T_A	Operating Free Air Temperature	-40		125	°C

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ESDS552	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	244.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	84.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics

At $T_A = 25^\circ\text{C}$ unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	$I_{IO} < 50\text{nA}$	-12		12	V
$I_{LEAKAGE}$	Leakage current at V_{RWM}	$V_{IO} = \pm 12\text{V}$		10	50	nA
V_{BR}	Breakdown voltage, IO to GND and GND to IO ⁽¹⁾	$I_{IO} = \pm 1\text{mA}$	13.2		18	V
V_{CLAMP}	Surge clamping voltage, $t_p = 8/20\mu\text{s}$ ⁽²⁾	$I_{PP} = 1\text{A}$, I/O to GND			19	V
		$I_{PP} = 1\text{A}$, GND to I/O			19	V
		$I_{PP} = 20\text{A}$, I/O to GND			23.5	V
		$I_{PP} = 20\text{A}$, GND to I/O			23.5	V
R_{DYN}	8/20 μs surge Dynamic Resistance	I/O to GND		0.4		Ω
		GND to I/O		0.38		
C_{Line}	Line capacitance, IO to GND	$V_{IO} = 0\text{V}$, $f = 1\text{MHz}$		9.5	11	pF

(1) V_{BR} is defined as the voltage obtained at 1mA when sweeping the voltage up, before the device latches into the snapback state

5.7 Typical Characteristics

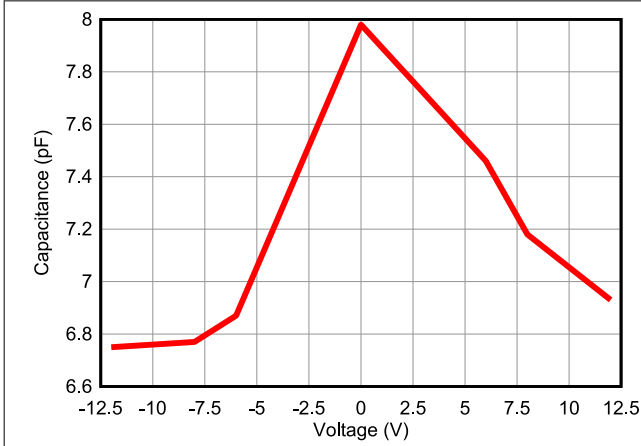


图 5-1. Capacitance vs. Bias Voltage

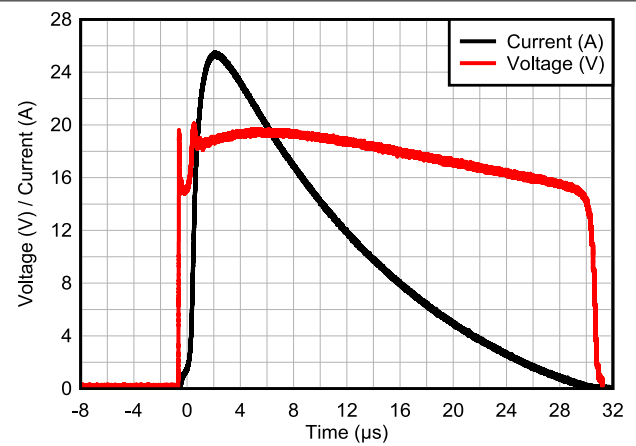


图 5-2. 8/20 μ s Surge Response

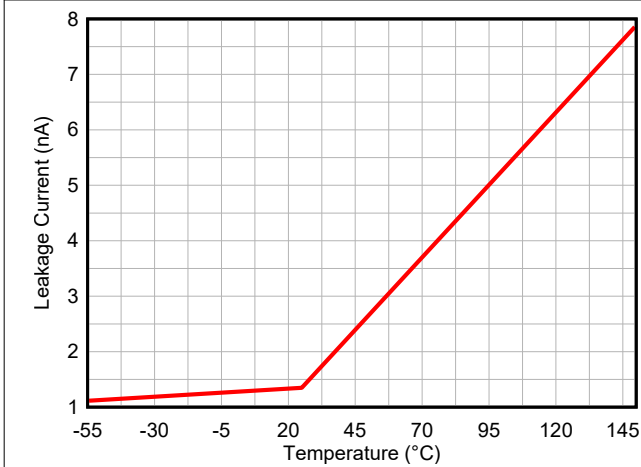


图 5-3. Leakage Current vs Temperature

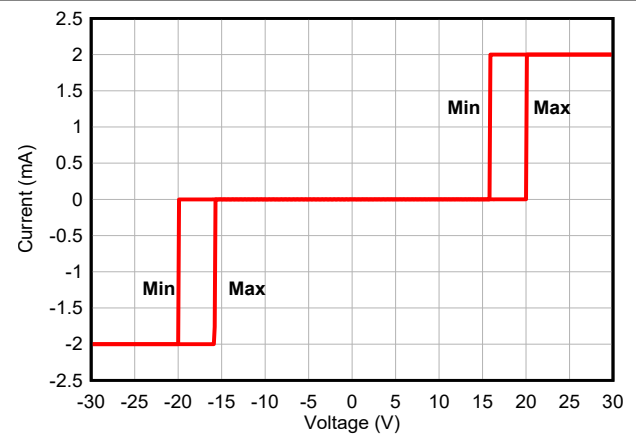


图 5-4. DC Voltage Sweep I-V Curve

6 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

6.1 Application Information

The ESDS552 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the [ESD Packaging and Layout Guide](#) for details.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Packaging and Layout Guide](#)
- Texas Instruments, [TI's IEC 61000-4-x Testing application note](#)
- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet user's guide](#)

7.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

7.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

7.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

Changes from Revision * (December 2023) to Revision A (February 2024)

Page

- | | |
|--|---|
| • 将数据表的状态从 预告信息 更改为 量产数据 | 1 |
|--|---|

9 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESDS552DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	36A8	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS552DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

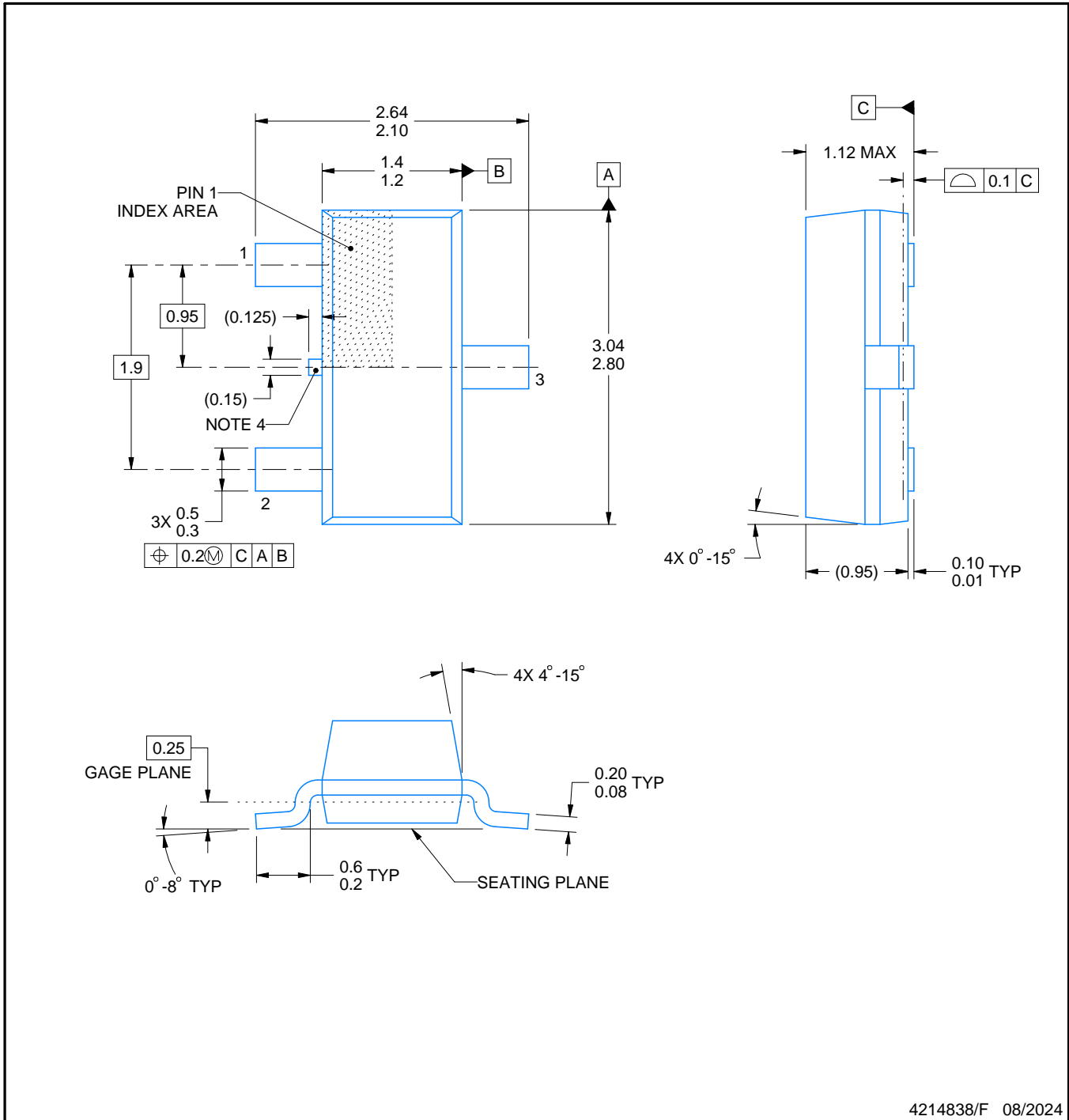
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS552DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

DBZ0003A



PACKAGE OUTLINE SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司