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ISO7821LLS 高性能 8000 V_{PK} 增强型隔离式双 LVDS 缓冲器

1 特性

- 符合 TIA/EIA-644-A LVDS 标准
- 信号传输速率：50Mbps 至 150Mbps
- 针对直流均衡数据进行了优化
- 宽电源电压范围：3V 至 5.5V
- 宽温度范围：-55°C 至 125°C
- 低功耗：电流典型值为 10.3mA/通道（150Mbps 时）
- 低传播延迟：17ns（典型值）
- 行业领先的 CMTI（最小值）：±100kV/µs
- 优异的电磁兼容性 (EMC)
- 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
- 低辐射
- 隔离栅寿命：> 40 年
- SOIC-16 宽体 (DW) 和超宽体 (DWW) 封装选项
- 可承受的隔离浪涌电压高达 12800 V_{PK}
- 安全相关认证：
  - 符合 DIN V VDE V 0884–10 (VDE V 0884–10): 2006–12 标准的 8000 V_{PK} 增强型隔离
  - 符合 UL 1577 标准且长达 1 分钟的 5700 V_{RMS} 隔离
  - CSA 组件验收通知 5A，IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
  - 符合 GB4943.1–2011 标准的 CQC 认证
  - 已通过所有认证

2 应用

- 电机控制
- 测试和测量
- 工业自动化
- 医疗设备
- 通信系统

3 说明

ISO7821LLS 器件是一款高性能、隔离式双 LVDS 缓冲器，隔离电压为 8000 V_{PK}。在隔离 LVDS 总线信号时，该器件可提供高电磁抗扰度，辐射较低，并且具有低功耗特性。各隔离通道具有一个 LVDS 接收和传输缓冲器。ISO7821LLS 器件的定时性能针对与通信系统结合使用进行了优化。通信采用通过内部失真校正方案实现的直流均衡数据流。

ISO7821LLS 器件有一条正向通道和一条反向通道。

凭借创新的芯片设计和布线技术，ISO7821LLS 器件的电磁兼容性得到了显著增强，从而可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。

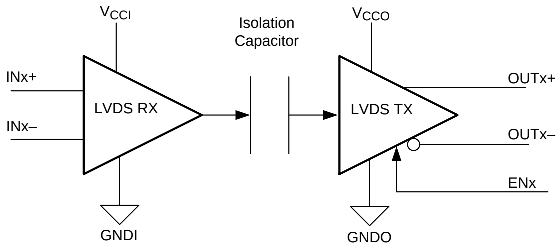
ISO7821LLS 器件采用 16 引脚小外形尺寸集成电路 (SOIC) 宽体 (DW) 和超宽体 (DWW) 封装。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
ISO7821LLS	DW (16)	10.30mm x 7.50mm
	DWW (16)	10.30mm x 14.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接。

English Data Sheet: SLLSET5

目录

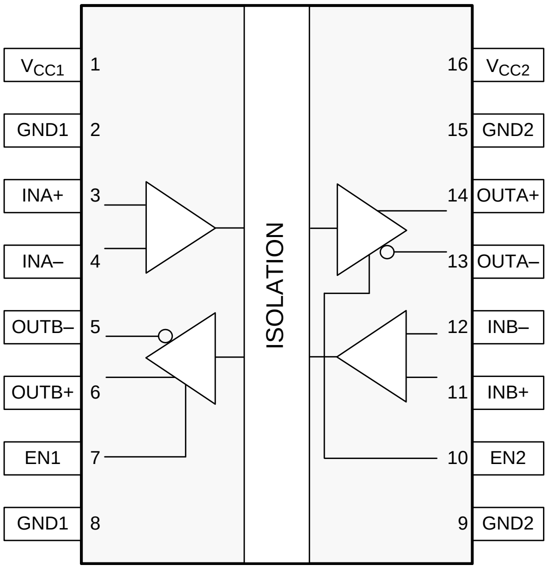
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (March 2016) to Revision A	**Page**
• 已更改 器件状态“*产品预览*”至“*量产数据*”并且已发布完整版本数据表	1

5 Pin Configuration and Functions

DW and DWW Packages
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high impedance state when EN2 is low.
GND1	2 8	—	Ground connection for V_{CC1}
GND2	9 15	—	Ground connection for V_{CC2}
INA+	3	I	Positive differential input, channel A
INA–	4	I	Negative differential input, channel A
INB+	11	I	Positive differential input, channel B
INB–	12	I	Negative differential input, channel B
OUTA+	14	O	Positive differential output, channel A
OUTA–	13	O	Negative differential output, channel A
OUTB+	6	O	Positive differential output, channel B
OUTB–	5	O	Negative differential output, channel B
V_{CC1}	1	—	Power supply, side 1, V_{CC1}
V_{CC2}	16	—	Power supply, side 2, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCx}	Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
V	Voltage on input, output, and enable pins	OUTx, INx, ENx	–0.5	V_{CCx} + 0.5(3)	V
I_O	Maximum current through OUTx pins		–20	20	mA
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		3	3.3	5.5	V
$\|V_{ID}\|$	Magnitude of RX input differential voltage	Driven with voltage sources on RX pins	100		600	mV
V_{IC}	RX input common-mode voltage	V_{CC1}, V_{CC2} ≥ 3 V	0.5 $\|V_{ID}\|$		2.4 – 0.5 $\|V_{ID}\|$	V
R_L	TX far-end differential termination			100		Ω
DR	Signaling rate		50		150	Mbps
T_A	Ambient temperature		–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		ISO7821LLS		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	44.6	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.6	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.8	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.1	54.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 5 pF, R_L = 100-Ω differential, input a 75-MHz 50% duty-cycle square wave, EN1 = EN2 = 5.5 V

PARAMETER		TEST CONDITIONS	MAX	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)				180	mW
P_{D1}	Maximum power dissipation (side 1)				90	mW
P_{D2}	Maximum power dissipation (side 2)				90	mW

6.6 Insulation Specifications

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
GENERAL					
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	>14.5	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	>14.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303–11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	I–IV	
DIN V VDE V 0884–10 (VDE V 0884–10):2006–12(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test; see Figure 1 and Figure 2	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) t = 1 s (100% production)	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$ (DW) and 3394 V_{PK} (DWW), t_m = 10 s	≤5	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$ (DW) and 4525 V_{PK} (DWW), t_m = 10 s	≤5	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IORM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$ (DW) and 5303 V_{PK} (DWW), t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~0.7	~0.7	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW), 2828 V_{PK} (DWW); Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage (DW package)	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW package) and 1000 V_{RMS} (DWW package) 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/ A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package)
Certification planned	Certification planned	Certification planned	Certification planned	Certification planned

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 82°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			277	mA
		$R_{\theta JA}$ = 82°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			423	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 82°C/W, T_J = 150°C, T_A = 25°C, see Figure 5			1524	mW
T_S	Maximum safety temperature				150	°C
DWW PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.6°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 4			269	mA
		$R_{\theta JA}$ = 84.6°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 4			410	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C, see Figure 6			1478	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a High-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
$I_{IN(EN)}$	Leakage Current on ENx pins	Internal pullup on ENx pins		13	40	µA
$V_{CC+(UVLO)}$	Positive-going undervoltage-lockout (UVLO) threshold				2.25	V
$V_{CC-(UVLO)}$	Negative-going UVLO threshold		1.7			V
$V_{HYS(UVLO)}$	UVLO threshold hysteresis			0.2		V
$V_{EN(ON)}$	EN pin turn-on threshold				0.7 V_{CCx}	V
$V_{EN(OFF)}$	EN pin turn-off threshold		0.3 V_{CCx}			V
$V_{EN(HYS)}$	EN pin threshold hysteresis			0.1 V_{CCx}		V
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ (1) or 0 V; V_{CM} = 1000 V, see Figure 22	100	120		kV/µs
LVDS TX						
$\lvert V_{OD}\rvert$	TX DC output differential voltage	$R_L = 100\ \Omega$, see Figure 23	250	350	450	mV
ΔV_{OD}	Change in TX DC output differential between logic 1 and 0 states	$R_L = 100\ \Omega$, see Figure 23	–10	0	10	mV
V_{OC}	TX DC output common-mode voltage	$R_L = 100\ \Omega$, see Figure 23	1.125	1.2	1.375	V
ΔV_{OC}	TX DC common-mode voltage difference	$R_L = 100\ \Omega$, see Figure 23	–25	0	25	mV
I_{OS}	TX output short circuit current through OUTx	OUTx = 0			10	mA
		OUTxP = OUTxM			10	
I_{OZ}	TX output current when in high impedance	ENx = 0, OUTx from 0 to V_{CCx}	–5		5	µA
C_{OUT}	TX output pad capacitance on OUTx at 1 MHz	DW package: ENx = 0, DC offset = V_{CC} / 2, Swing = 200 mV, Frequency (f) = 1 MHz		10		pF
		DWW package: ENx = 0, DC offset = V_{CC} / 2, Swing = 200 mV, Frequency (f) = 1 MHz		10		
LVDS RX						
V_{IC}	RX input common mode voltage	$V_{CCx} \geq 3$ V	0.5 $\lvert V_{ID}\rvert$	1.2	2.4 – 0.5 $\lvert V_{ID}\rvert$	V
V_{IT1}	Positive going RX input differential threshold	Across V_{IC}			50	mV
V_{IT2}	Negative going RX input differential threshold	Across V_{IC}	–50			mV
I_{INx}	Input current on INx	From 0 to V_{CC} (each input independently)		10	20	µA
$I_{INxP} - I_{INxM}$	Input current balance	From 0 to V_{CC}	–6		6	µA
C_{IN}	RX input pad capacitance on INx at 1 MHz	DW package: DC offset = 1.2 V, Swing = 200 mV, f = 1 MHz		6.6		pF
		DWW package: DC offset = 1.2 V, Swing = 200 mV, f = 1 MHz		7.5		

(1) V_{CCI} = Input-side V_{CCx}; V_{CCO} = Output-side V_{CCx}.

6.10 DC Supply Current Characteristics

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1} I_{CC2}	Supply current side 1 and side 2	3 V < V_{CC1}, V_{CC2} < 3.6 V	EN1 = EN2 = 0, OUTx floating, $V_{ID} \geq 50$ mV		2.3	3.6	mA
			EN1 = EN2 = 0, OUTx floating, $V_{ID} \leq -50$ mV		3.5	5.6	
			EN1 = EN2 = 1, R_L = 100-Ω differential, $V_{ID} \geq 50$ mV		6.2	9.9	
			EN1 = EN2 = 1, R_L = 100-Ω differential, $V_{ID} \leq -50$ mV		7.5	12	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 50 Mbps		7.6	12.1	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 125 Mbps		8.5	13.6	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 150 Mbps		8.9	14.2	
		4.5 V < V_{CC1}, V_{CC2} < 5.5 V	EN1 = EN2 = 0, OUTx floating, $V_{ID} \geq 50$ mV		2.3	3.6	
			EN1 = EN2 = 0, OUTx floating, $V_{ID} \leq -50$ mV		3.6	5.7	
			EN1 = EN2 = 1, R_L = 100-Ω differential, $V_{ID} \geq 50$ mV		6.6	10.5	
			EN1 = EN2 = 1, R_L = 100-Ω differential, $V_{ID} \leq -50$ mV		7.9	12.6	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 50 Mbps		8.3	13.2	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 125 Mbps		9.7	15.5	
			EN1 = EN2 = 1, R_L = 100-Ω differential, data communication at 150 Mbps		10.3	16.4	

6.11 Timing Requirements for Distortion Correction Scheme

Valid data = 8b10b like data with DC balance and bounded disparity. See Figure 25.

		MIN	NOM	MAX	UNIT
t_{CALIB}	Time to complete internal calibration, after exiting idle state. LVDS TX output is held high during this time. During this time valid data must be presented at the receiver.	250		750	µs
t_{IDLE}	The minimum duration of any idle state that must be maintained between valid data transmissions.	10			µs
t_{IDLE_OUT}	After a channel enters idle state, the internal calibration loses lock after this time, and the LVDS outputs are gated high.	200		600	ns

6.12 Switching Characteristics

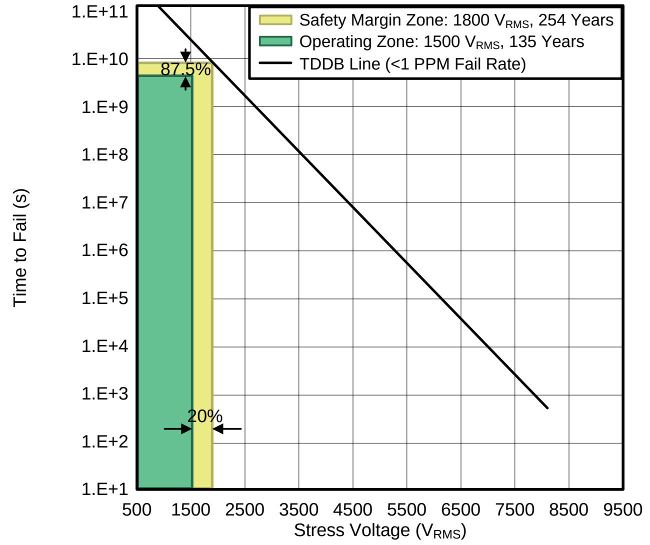
(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS CHANNEL						
t_{PLH} t_{PHL}	Propagation delay time			17	25	ns
$t_{sk(o)}$	Channel-to-channel output skew time	Opposite directional channels, same voltage and temperature			4.5	ns
$t_{sk(pp)}$	Part-part skew	Same directional channels, same voltage and temperature			4.5	ns
t_{CMset}	Common-mode setting time after EN = 0 to EN = 1 transition	Common-mode capacitive load = 100 pF to 0.5 nF			20	µs
	Total eye closure	DC balanced data with maximum run length of 6 at 125 Mbps, RX V_{ID} = 350 mV_{PP}, 1 ns t_{rf} 10%-90%, –40 < T_A < 125°C, 3 V < V_{CC1}, V_{CC2} < 5 V			30%	
		DC balanced data with maximum run length of 6 at 150 Mbps, RX V_{ID} = 350 mV_{PP}, 1 ns t_{rf} 10%-90%, –40 < T_A < 125°C, 3 V < V_{CC1}, V_{CC2} < 5 V			40%	
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V, see Figure 21		0.2	9	µs
LVDS TX AND RX						
t_{rf}	TX differential rise and fall times (20% to 80%)	See Figure 19	300	780	1380	ps
$\Delta V_{OC(pp)}$	TX common-mode voltage peak-to-peak at 100 Mbps			0	150	mV_{PP}
t_{PLZ}, t_{PHZ}	TX disable time—valid output to HiZ	See Figure 20		10	20	ns
t_{PZH}	TX enable time—HiZ to valid high output(1)	See Figure 20		10	20	ns
$\|V_{ID}\|$	Magnitude of RX input differential voltage for valid operation	Driven with voltage sources on RX pins, see figures in the *Parameter Measurement Information* section	100		600	mV
$t_{rf(RX)}$	Allowed RX input differential rise and fall times (20% to 80%)	See Figure 24		1	0.3 × UI(2)	ns

(1) The t_{PZL} parameter is not defined because of the distortion-correction scheme. See the *Distortion-Correction Scheme* section for more information.

(2) UI is the unit interval.

6.13 Insulation Characteristics Curves



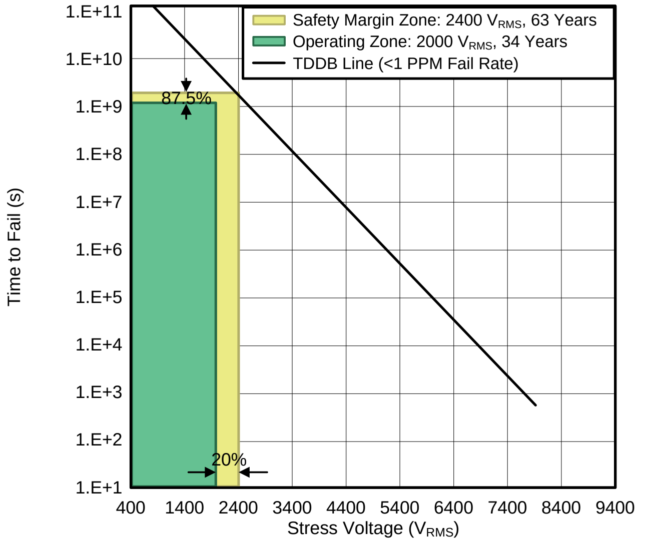
T_A upto 150°C

Operating lifetime = 135 years

Stress-voltage frequency = 60 Hz

Isolation working voltage = 1500 V_{RMS}

Figure 1. Reinforced Isolation Capacitor Lifetime Projection for Devices in DW Package



T_A upto 150°C

Operating lifetime = 34 years

Stress-voltage frequency = 60 Hz

Isolation working voltage = 2000 V_{RMS}

Figure 2. Reinforced Isolation Capacitor Lifetime Projection for Devices in DWW Package

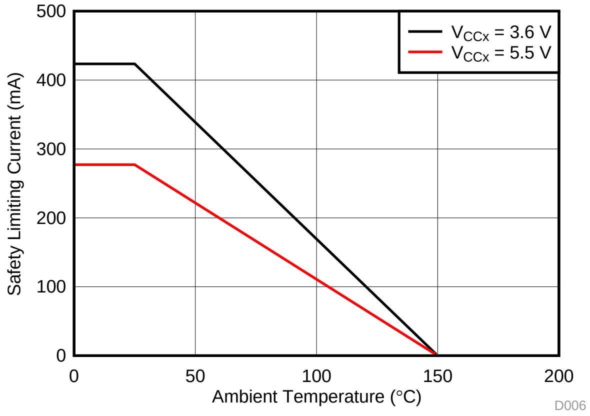


Figure 3. Thermal Derating Curve for Limiting Current for DW Package

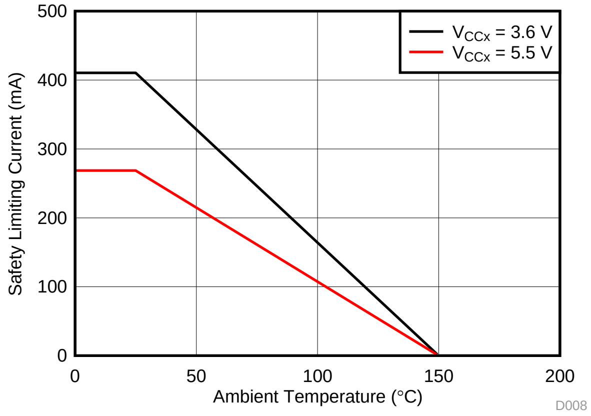


Figure 4. Thermal Derating Curve for Limiting Current for DWW Package

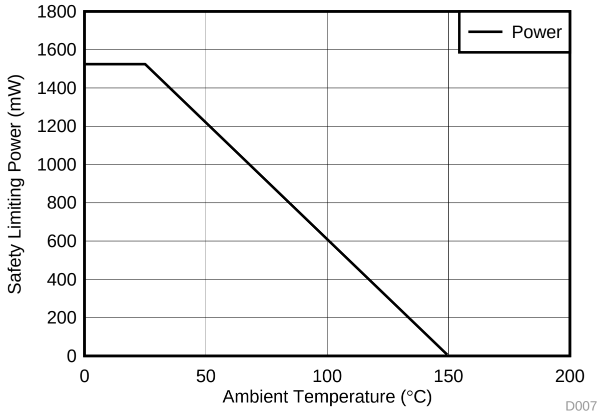


Figure 5. Thermal Derating Curve for Limiting Power for DW Package

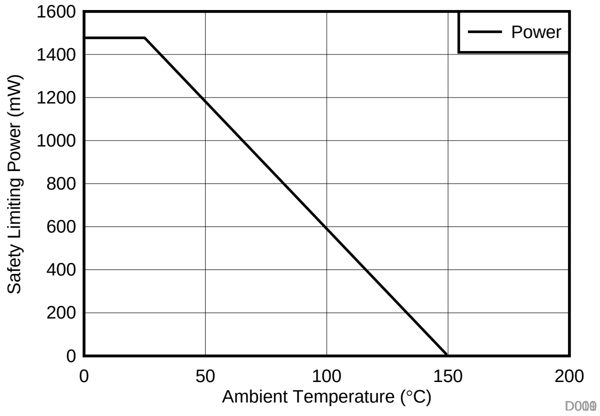
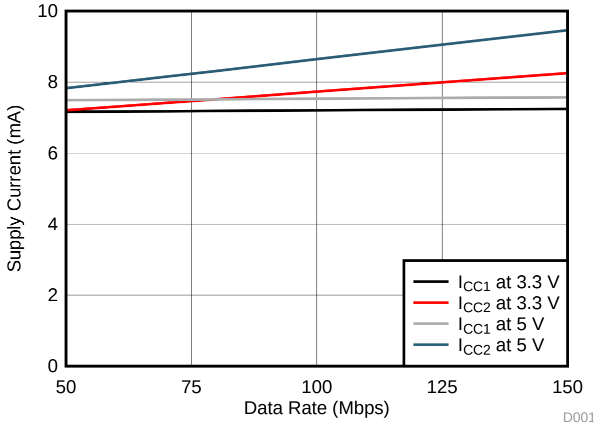


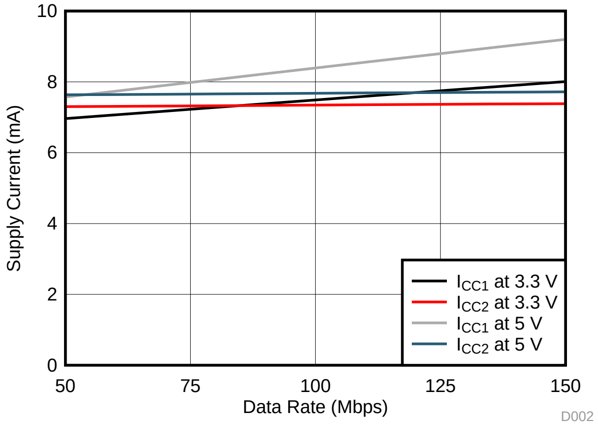
Figure 6. Thermal Derating Curve for Limiting Power for DWW Package

6.14 Typical Characteristics



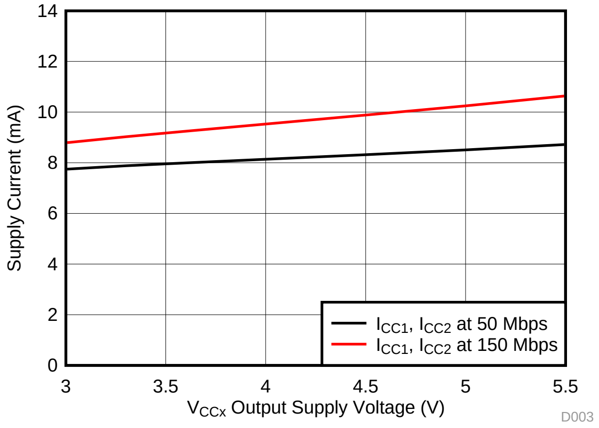
T_A = 25°C CH-A toggle

Figure 7. Supply Current vs Data Rate (CH-A)



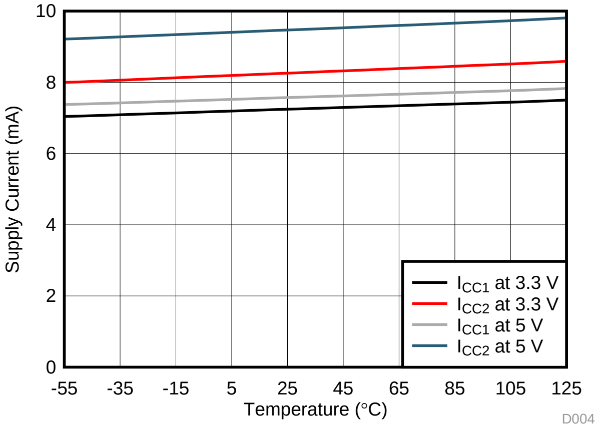
T_A = 25°C CH-B toggle

Figure 8. Supply Current vs Data Rate (CH-B)



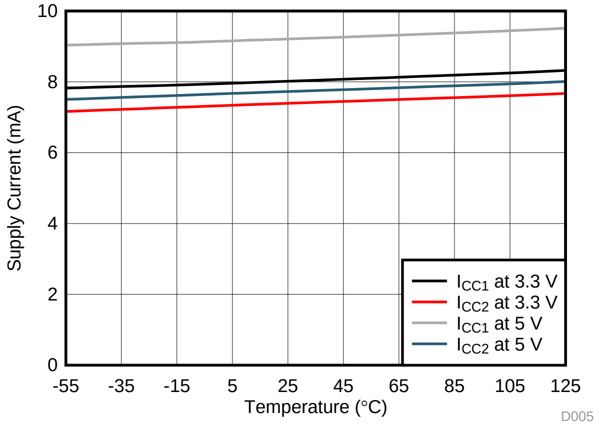
T_A = 25°C

Figure 9. Supply Current vs V_{CCx} Output Supply Voltage



Data rate = 150 Mbps CH-A toggle

Figure 10. Supply Current vs Temperature (CH-A)



Data rate = 150 Mbps CH-B toggle

Figure 11. Supply Current vs Temperature (CH-B)

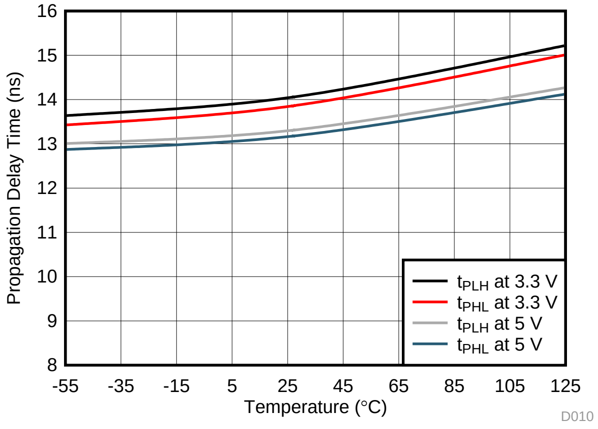
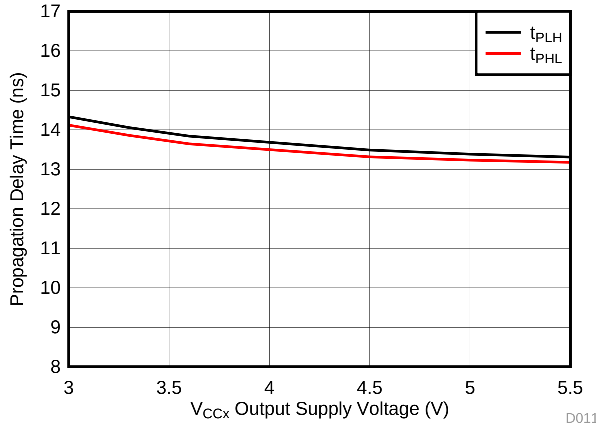


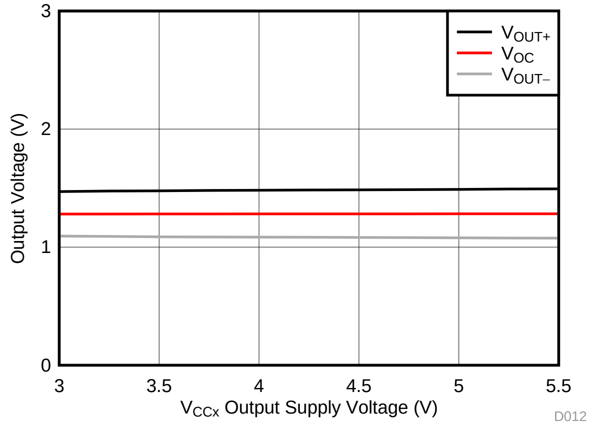
Figure 12. Propagation Delay Time vs Temperature

Typical Characteristics (continued)



T_A = 25°C

Figure 13. Propagation Delay Time vs V_{CCx} Output Supply Voltage



T_A = 25°C

Figure 14. Output Voltage vs V_{CCx} Output Supply Voltage

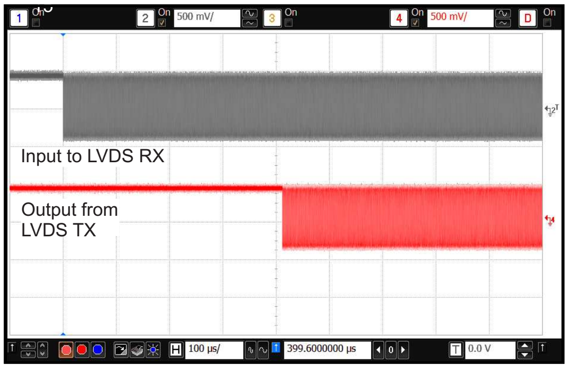


Figure 15. Distortion Correction Scheme Calibration Time (t_{CALIB})

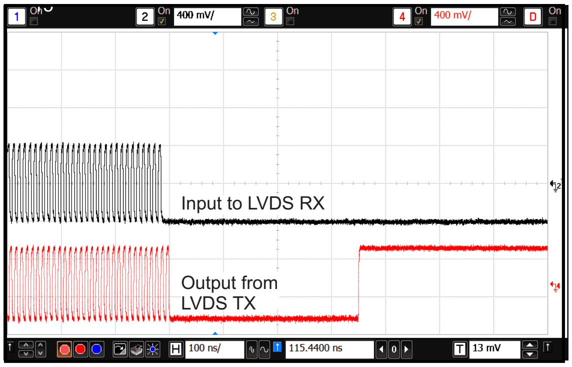


Figure 16. Transition From Valid Data to Idle (t_{IDLE_OUT})

Figure 17. Disable to Enable Time (t_{PZH})

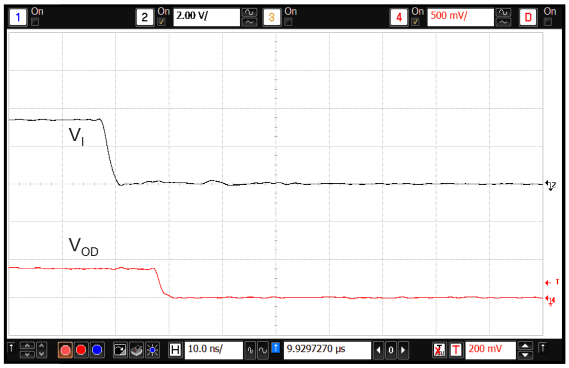
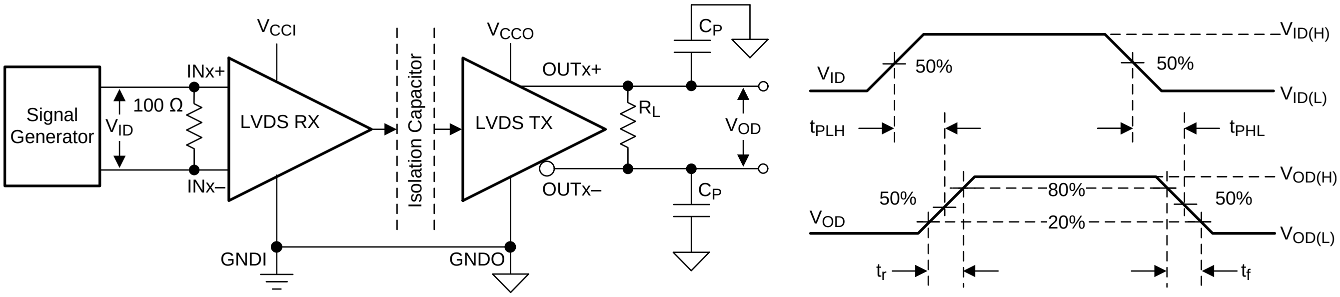


Figure 18. Disable Time (t_{PLZ}, t_{PHZ})

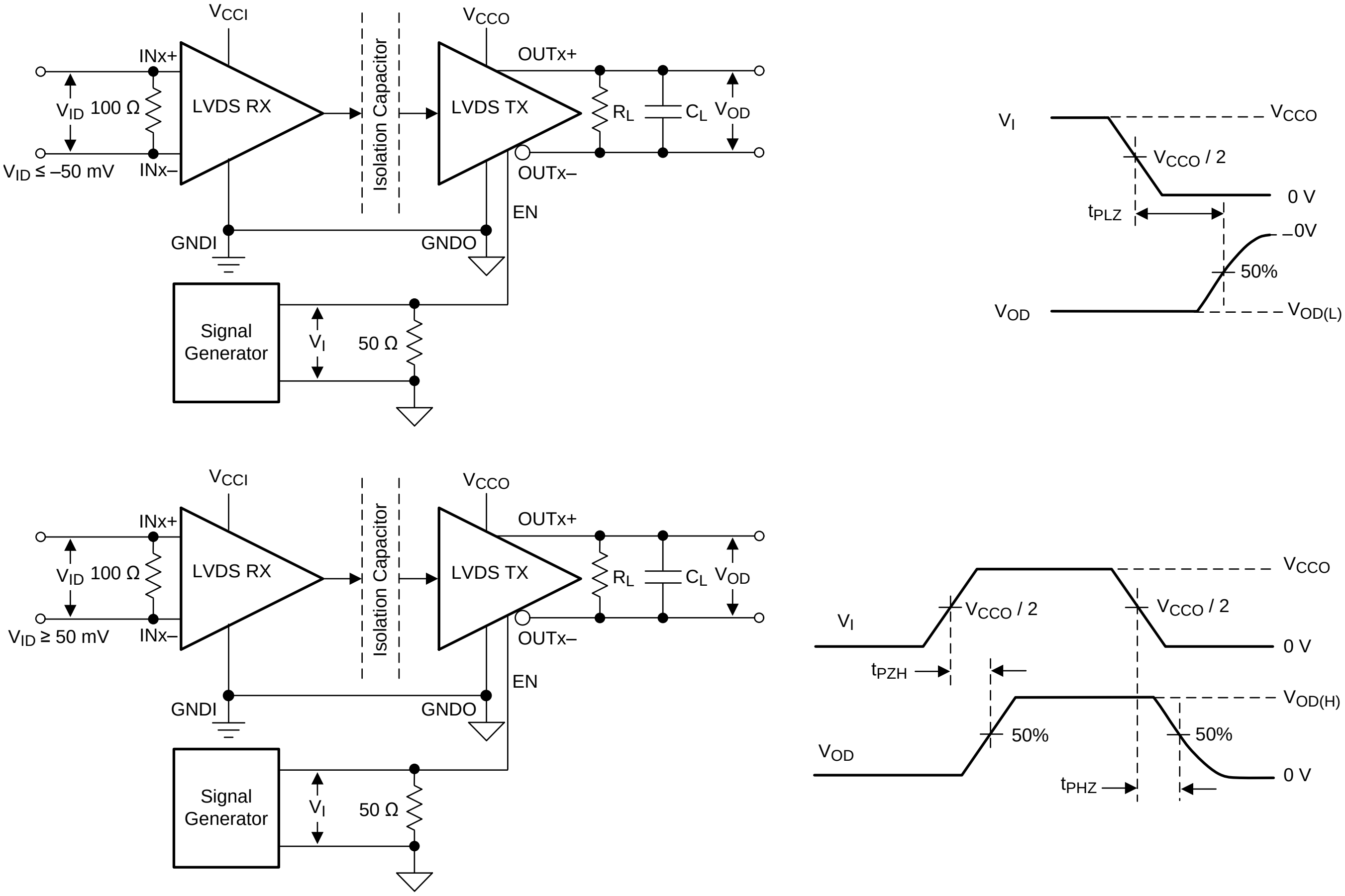
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50\ \Omega$.

B. $C_P = 5$ pF and includes instrumentation and fixture capacitance within ±20%.

Figure 19. Switching Characteristics Test Circuit and Voltage Waveforms

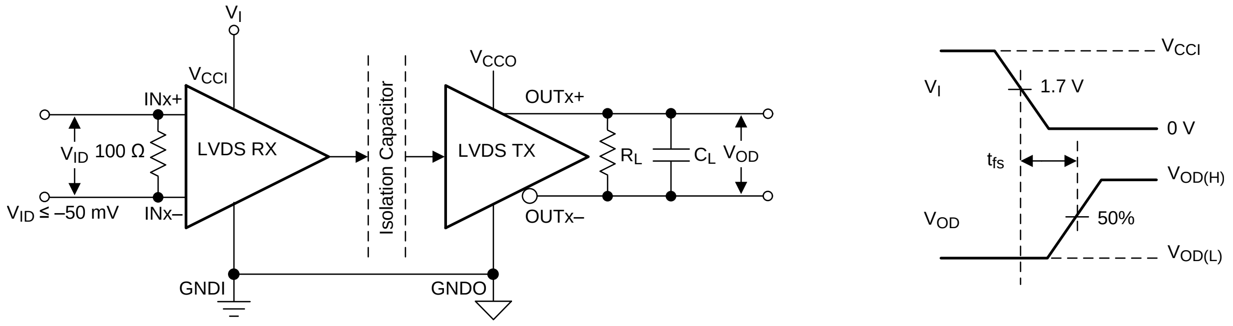


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50\ \Omega$.

B. $C_L = 5$ pF and includes instrumentation and fixture capacitance within ±20%.

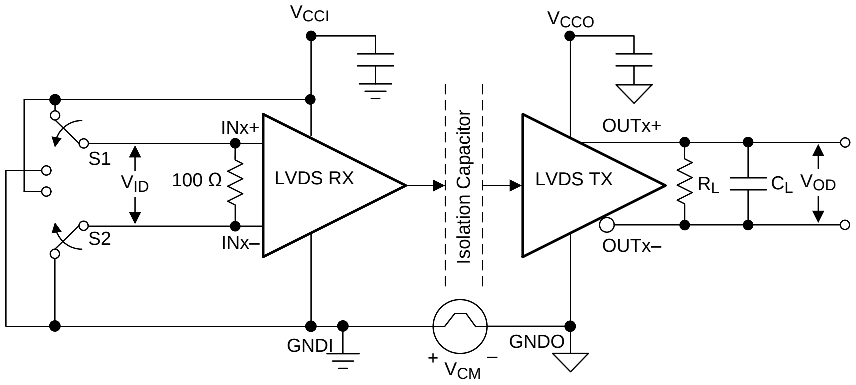
Figure 20. Enable and Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 5 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 21. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 5 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 22. Common-Mode Transient Immunity Test Circuit

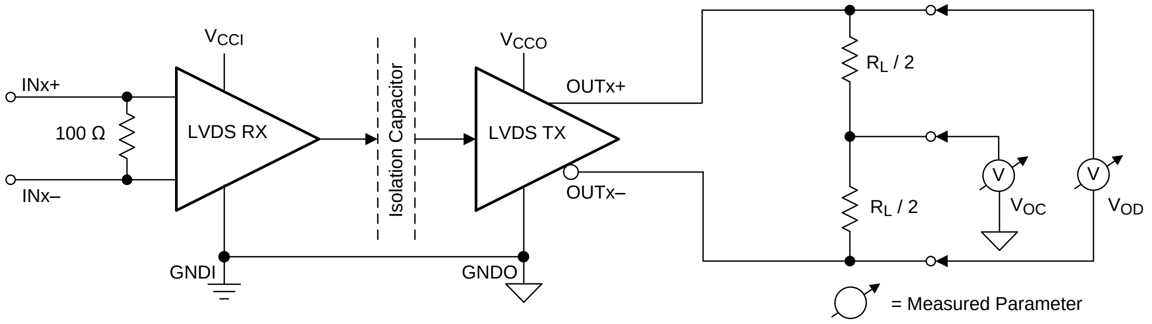


Figure 23. Driver Test Circuit

Parameter Measurement Information (continued)

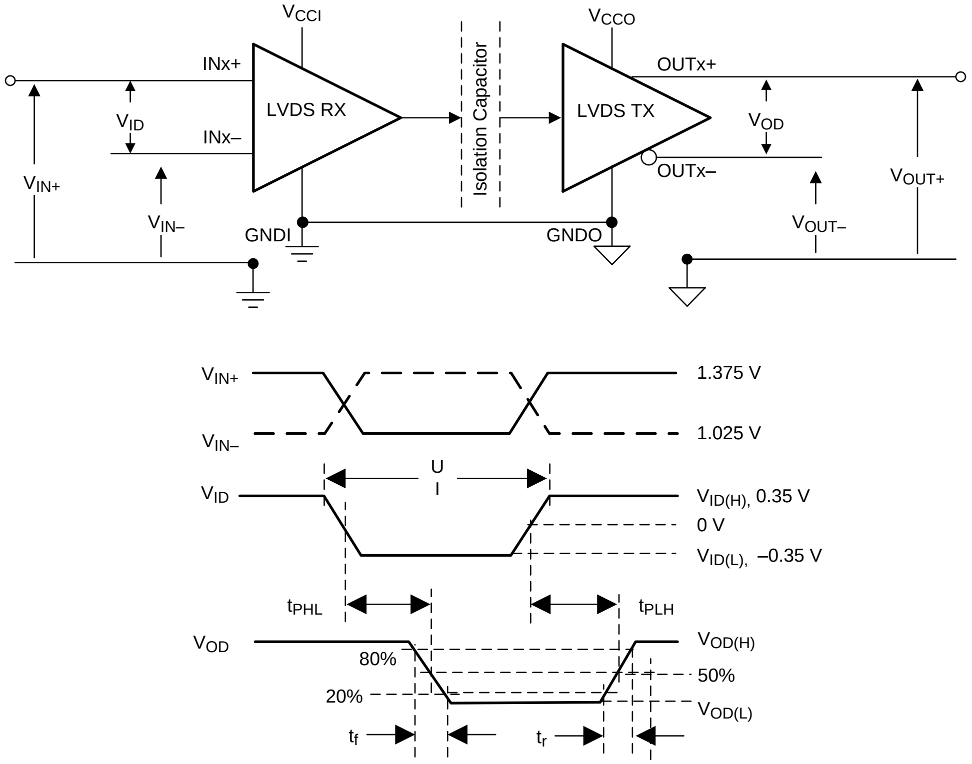


Figure 24. Voltage Definitions and Waveforms

8 Detailed Description

8.1 Overview

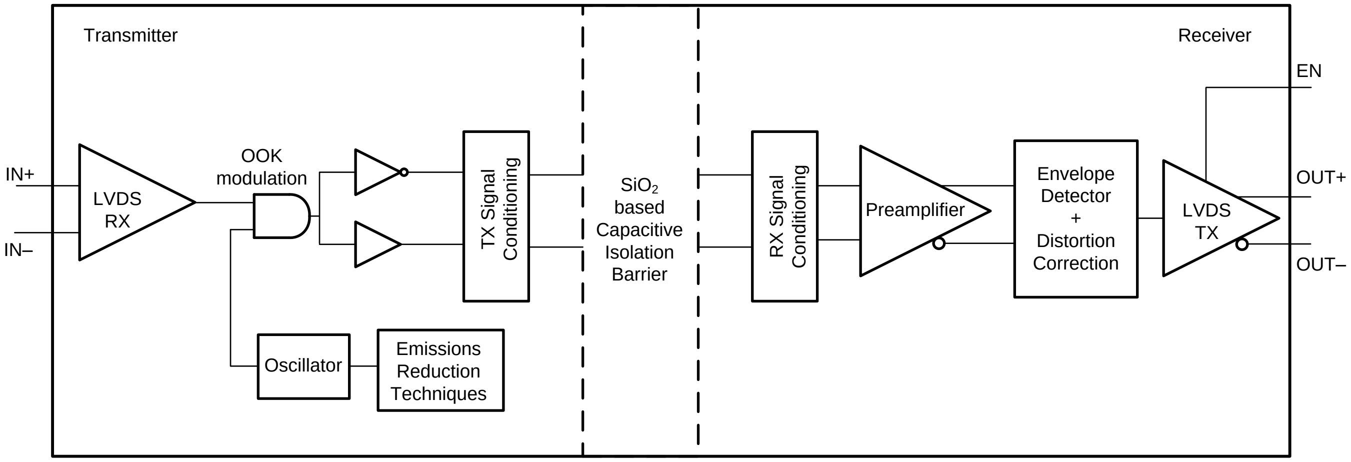
The ISO7821LLS device is an isolated LVDS buffer. The differential signal received on the LVDS input pins is first converted to CMOS logic levels. It is then transmitted across a silicon dioxide based capacitive isolation barrier using an On-Off Keying (OOK) modulation scheme. A high frequency carrier transmitted across the barrier represents one logic state and an absence of a carrier represents the other logic state. On the other side of the barrier a demodulator converts the OOK signal back to logic levels, which is then converted to LVDS outputs by a differential driver. This device incorporates advanced circuit techniques to maximize CMTI performance and minimize radiated emissions.

The ISO7821LLS device implements an eye-diagram improvement scheme to correct for signal distortions that are introduced in the LVDS receiver as well as the isolation channel. This enables the device to guarantee an eye closure of less than 30% at 125 Mbps, and less than 40% at 150 Mbps. The distortion correction scheme is optimized for operation with DC balanced data (for example 8b10b or equivalent) with a maximum run length of 6. The minimum data-rate of operation is also constrained to 50 Mbps. For general purpose data communication from 0 to 100 Mbps, the ISO782xLL family of devices should be considered.

The ISO7821LLS device is TIA/EIA-644-A standard compliant. The LVDS transmitter drives a minimum differential-output voltage magnitude of 250 mV into a 100-Ω load, and the LVDS receiver is capable of detecting differential signal ≥50 mV in magnitude. The device consumes 11 mA per channel at 150 Mbps with 5-V supplies.

The *Functional Block Diagram* section shows a conceptual block diagram of one channel of the ISO7821LLS device.

8.2 Functional Block Diagram



8.3 Feature Description

The ISO7821LLS device is available in a two-channel configuration with a default differential-high output state. Table 1 lists the device features.

Table 1. Device Features

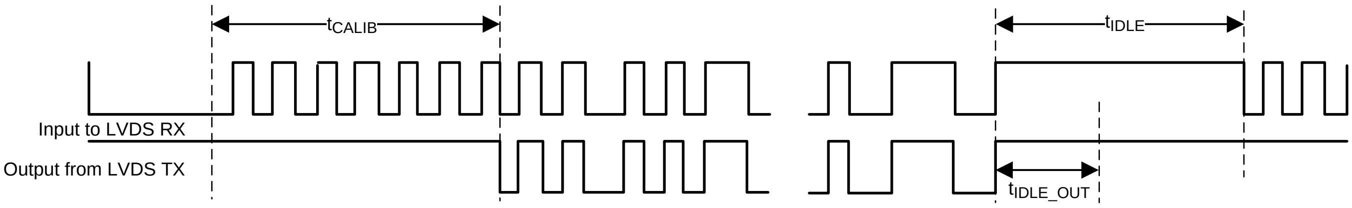
PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT DIFFERENTIAL OUTPUT
ISO7821LLS	1 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	150 Mbps	High

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

8.3.1 Distortion-Correction Scheme

The ISO7821LLS device implements a distortion-correction scheme to correct for signal distortions that are introduced in the LVDS receiver as well as the isolation channel. This scheme is optimized for a DC-balanced data-stream with a maximum run length of 6. One example of such a data stream is 8b10b encoded data. The minimum data rate supported by the ISO7821LLS device is 50 Mbps and the maximum is 150 Mbps.

Figure 25 shows the timing requirements associated with the distortion correction scheme (see the *Timing Requirements for Distortion Correction Scheme* table for timing parameters). The input to the LVDS channel should be either idle low, idle high, or should have clock or DC-balanced data transitions at 25 MHz / 50 Mbps or higher. Low frequency or DC-unbalanced data is not allowed. The distortion-correction scheme runs an internal calibration each time the LVDS channel transitions from an idle state to a data transmission state. The calibration runs for a period of t_{CALIB} during which the LVDS channel output is held at logic high. This calibration is also run at power up. Lack of activity on the receive inputs for a period greater than t_{IDLE_OUT} takes the channel to an uncalibrated state. If the communication protocol requires the channel to transition to the idle state, the idle-high or idle-low state must be held for at least duration of t_{IDLE}.



A. Signals shown are differential logic states.
   Logic high → $V_{IN+} > V_{IN-}$
   Logic low → $V_{IN-} > V_{IN+}$

B. The data to ISOLVDS channel should be either idle high, idle low, clock, or valid data.
   Valid data = 8b10b like data with DC balance and bounded disparity.

C. When transitioning from an uncalibrated sate to a calibrated state, the ISOLVDS channel output is gated high for up to t_{CALIB}, during which the channel is calibrated.

D. If the channel finds no transitions in the incoming data for a period of t_{IDLE_OUT}, the channel goes to an uncalibrated state.

E. Power loss (which implies no data transitions) takes the channel to an uncalibrated state.

F. If, for some reason, the idle-high or idle-low state must be held on the line, this state must be held for at least t_{IDLE}.

Figure 25. DCD Correction Timing Diagram

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO7821LLS device.

Table 2. ISO7821LLS Function Table[1]

V_{CCI}	V_{CCO}	INPUT (INx±)[2]	OUTPUT ENABLE (ENx)	OUTPUT (OUTx±)[3]	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		I	H or open	H or L	
X	PU	X	L	Z	A low-logic state at the output enable causes the outputs to be in high impedance.
PD	PU	X	H or open	H	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic high state. When V_{CCI} transitions from unpowered to powered up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered up to unpowered, a channel output assumes the selected default high state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined. When V_{CCO} transitions from unpowered to powered up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CCx} \geq 2.25$ V); PD = Powered down ($V_{CCx} \leq 1.7$ V); X = Irrelevant
(2) Input (INx±): H = high level ($V_{ID} \geq 50$ mV); L = low level ($V_{ID} \leq -50$ mV); I = indeterminate (-50 mV < V_{ID} < 50 mV)
(3) Output (OUTx±): H = high level ($V_{OD} \geq 250$ mV); L = low level ($V_{OD} \leq -250$ mV); Z = high impedance.

8.4.1 Device I/O Schematics

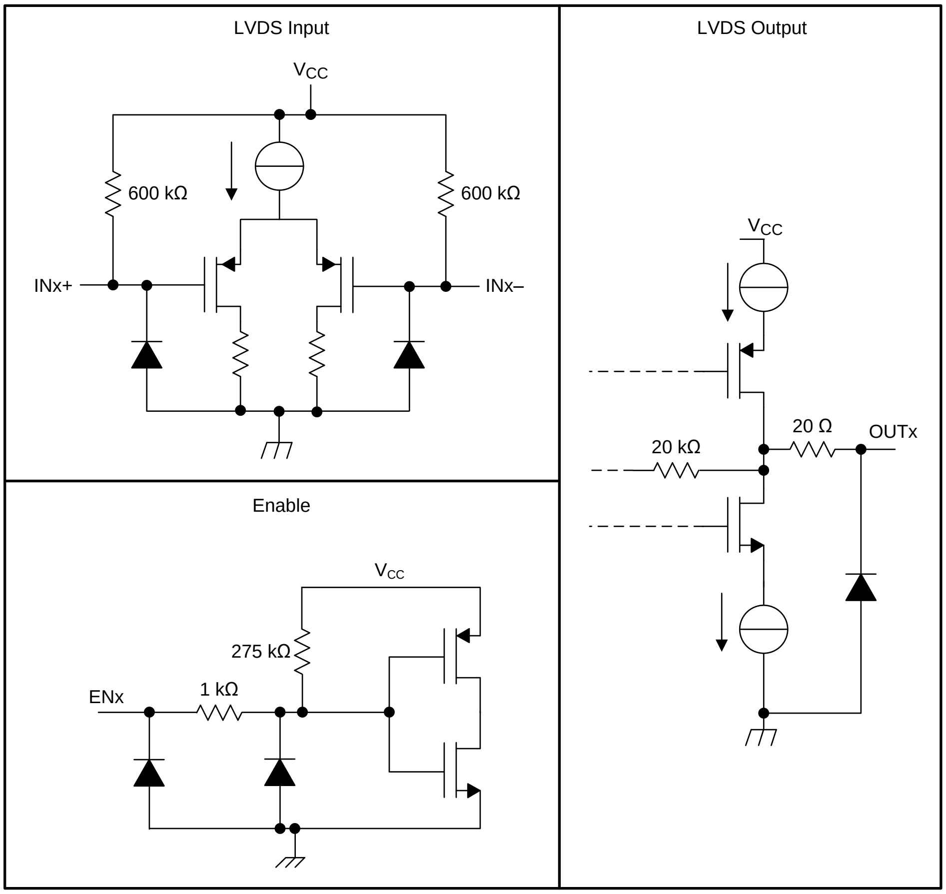


Figure 26. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7821LLS device is a high-performance, reinforced isolated dual-LVDS buffer. Isolation can be used to help achieve human and system safety, to overcome ground potential difference (GPD), or to improve noise immunity and system performance.

The LVDS signaling can be used over most interfaces to achieve higher data rates because the LVDS is only a physical layer. LVDS can also be used for a proprietary communication scheme implemented between a host controller and a slave. Example use cases include connecting a high-speed I/O module to a host controller, a subsystem connecting to a backplane, and connection between two high-speed subsystems. Many of these systems operate under harsh environments making them susceptible to electromagnetic interferences, voltage surges, electrical fast transients (EFT), and other disturbances. These systems must also meet strict limits on radiated emissions. Using isolation in combination with a robust low-noise signaling standard such as LVDS, achieves both high immunity to noise and low emissions.

Example end applications that could benefit from the ISO7821LLS device include high-voltage motor control, test and measurement, industrial automation, and medical equipment.

9.2 Typical Application

One application for isolated LVDS buffers is for point-to-point communication between two high-speed capable, application-specific integrated circuits (ASICs) or FPGAs. In a high-voltage motor control application, for example, Node 1 could be a controller on a low-voltage or earth referenced board, and Node 2, could be controller placed on the power board, biased to high voltage. Figure 27 and Figure 28 show the application schematics.

Figure 28 provides further details of using the ISO7821LLS device to isolate the LVDS interface. The LVDS connection to the ISO7821LLS device can be traces on a board (shown as straight lines between Node 1 and the ISO7821LLS device), a twisted pair cable (as shown between Node 2 and the ISO7821LLS device), or any other controlled impedance channel. Differential 100-Ω terminations are placed near each LVDS receiver. The characteristic impedance of the channel should also be 100-Ω differential.

In the example shown in Figure 27 and Figure 28, the ISO7821LLS device provides reinforced or safety isolation between the high-voltage elements of the motor drive and the low-voltage control circuitry. This configuration also ensures reliable communication, regardless of the high conducted and radiated noise present in the system.

Typical Application (continued)

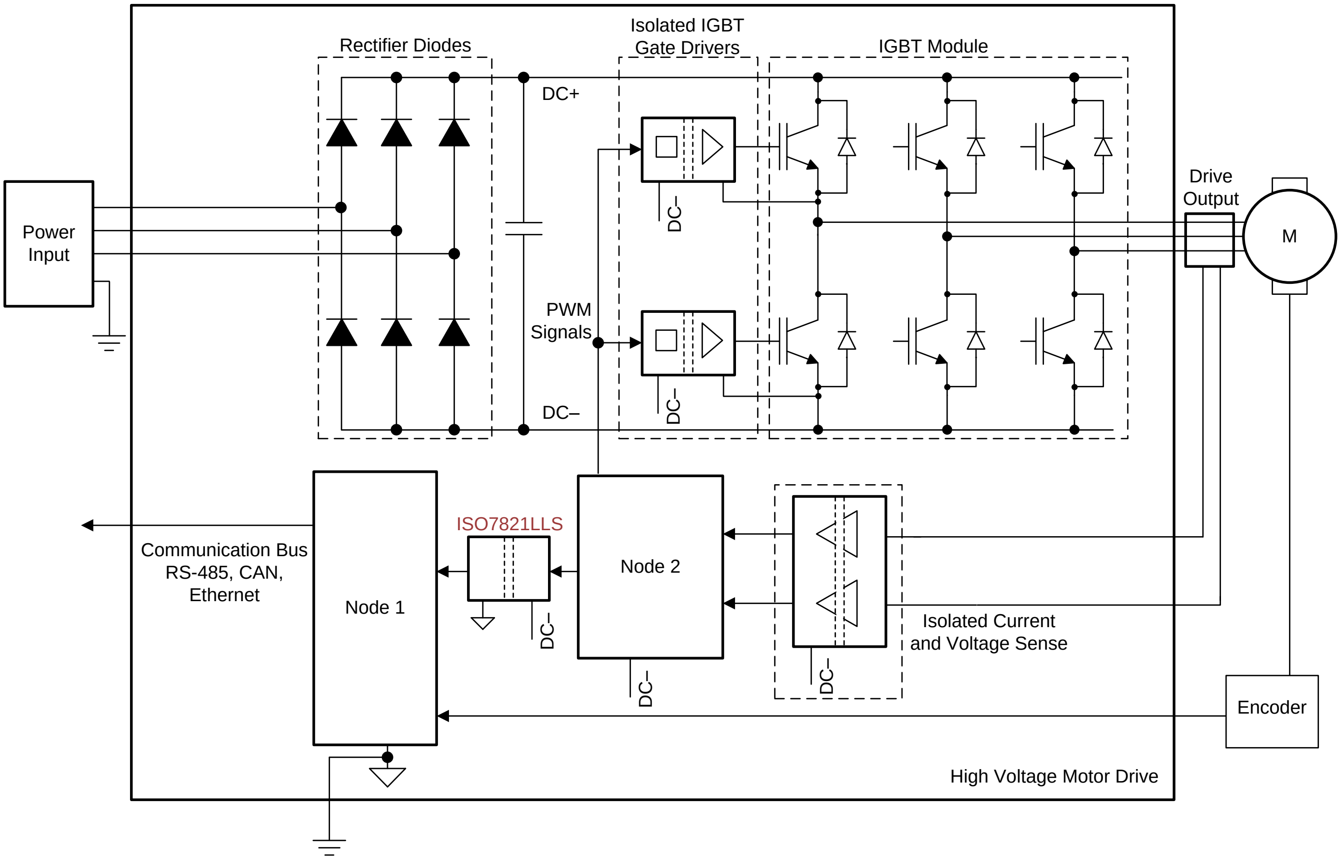


Figure 27. Isolated LVDS Interface in Motor Control Application

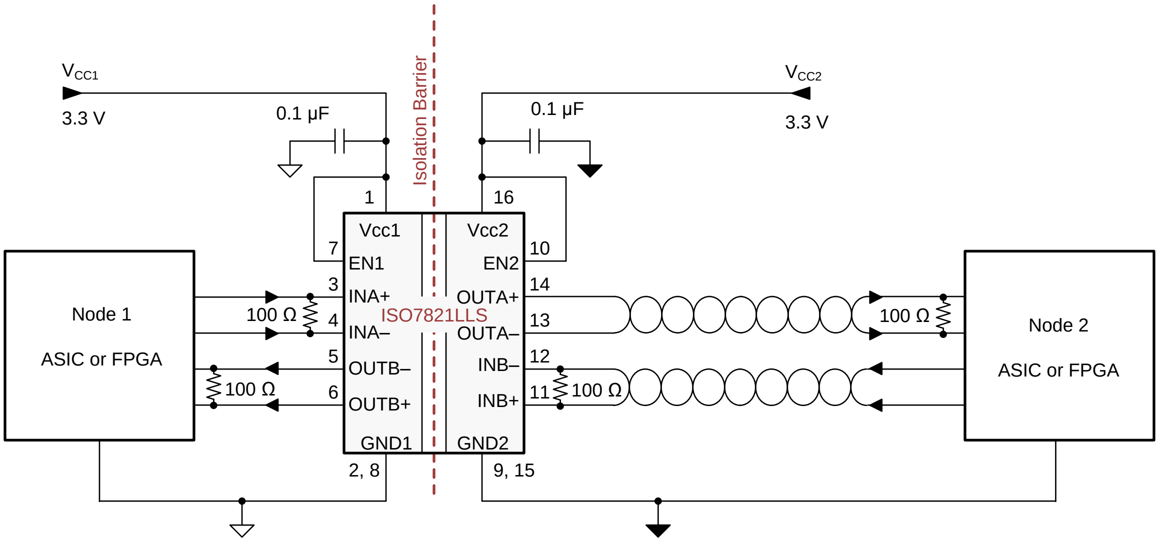


Figure 28. Isolated LVDS Interface Between Two Nodes (ASIC or FPGA)

Typical Application (continued)

9.2.1 Design Requirements

For the ISO7821LLS device, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage range, V_{CC1} and V_{CC2}	3 V to 5.5 V
Receiver common-mode voltage range	0.5 $\|V_{ID}\|$ to 2.4 – 0.5 $\|V_{ID}\|$
External termination resistance	100 Ω
Interconnect differential characteristic impedance	100 Ω
Signaling rate	50 to 150 Mbps
Decoupling capacitor from V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

The ISO7821LLS device has minimum requirements on external components for correct operation. External bypass capacitors (0.1 µF) are required for both supplies (V_{CC1} and V_{CC2}). A termination resistor with a value of 100 Ω is required between each differential input pair (INx+ and INx–), with the resistors placed as close to the device pins as possible. A differential termination resistor with a value of 100 Ω is required on the far end for the LVDS transmitters. Figure 29 shows these connections.

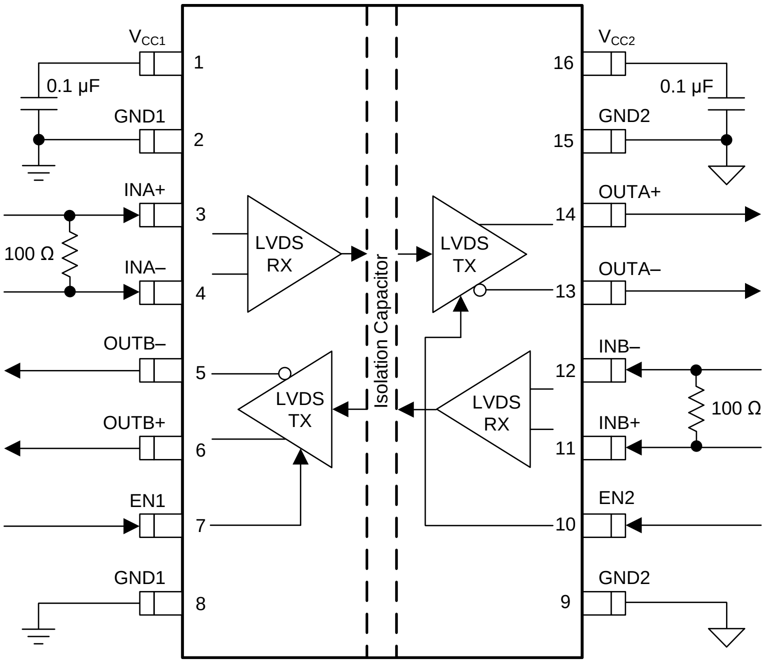


Figure 29. Typical ISO7821LLS Circuit Hook-Up

9.2.2.1 *Electromagnetic Compatibility (EMC) Considerations*

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7821LLS device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.2.3 Application Curve

Figure 30 shows a typical eye diagram of the ISO7821LLS device which indicates low jitter and a wide-open eye at the maximum data rate of 150 Mbps.

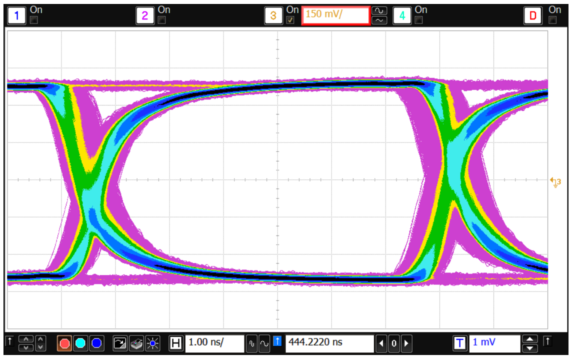


Figure 30. Eye Diagram at 150 Mbps PRBS, 3.3 V and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505. For such applications, detailed power supply design and transformer selection recommendations are available in the following data sheets: *SN6501 Transformer Driver for Isolated Power Supplies* (SLLSEA0) and *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* (SLLSEP9).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 31). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- While routing differential traces on a board, TI recommends that the distance between two differential pairs be much higher (at least 2x) than the distance between the traces in a differential pair. This distance minimizes crosstalk between the two differential pairs.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

The ISO7821LLS device requires no special layout considerations to mitigate electromagnetic emissions.

For detailed layout recommendations, see the application note, *Digital Isolator Design Guide* (SLLA284).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps (or rise and fall times higher than 1 ns) and trace lengths of up to 10 inches, use standard FR–4 UL94V-0 epoxy-glass as PCB material. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

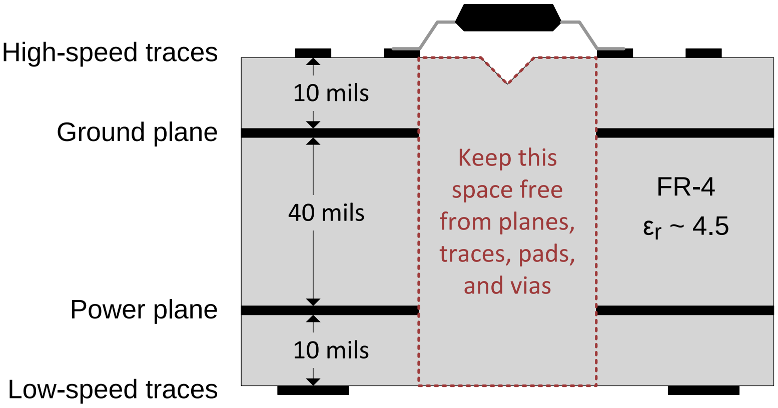


Figure 31. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《数字隔离器设计指南》*（文献编号：SLLA284）
- *《ISO782xLLx 隔离式双 LVDS 缓冲器评估模块》*（文献编号：SLLU240）
- *《隔离相关术语》*（文献编号：SLLA353）
- *《LVDS 所有者手册》*（文献编号：SNLA187）
- *《SN6501 适用于隔离式电源的变压器驱动器》*（文献编号：SLLSEA0）
- *《SN6505 适用于隔离式电源的低噪声 1A 变压器驱动器》*（文献编号：SLLSEP9）

12.2 接收文档更新通知

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12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7821LLSDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821LLS	Samples
ISO7821LLSDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7821LLS	Samples
ISO7821LLSDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821LLS	Samples
ISO7821LLSDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO7821LLS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

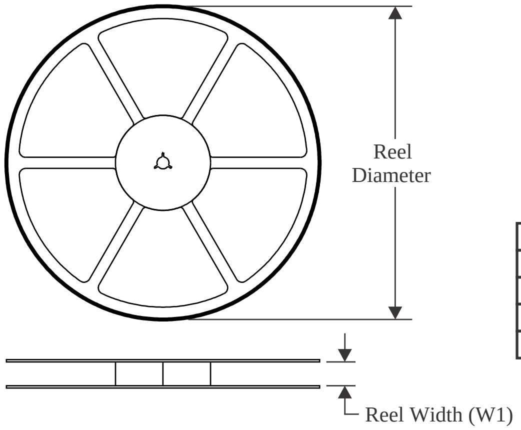
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

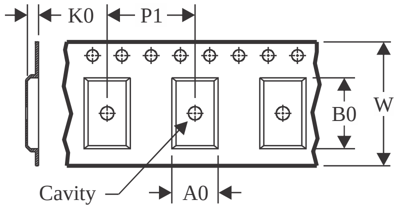
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

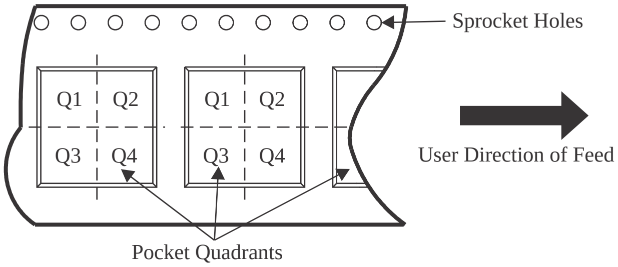


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

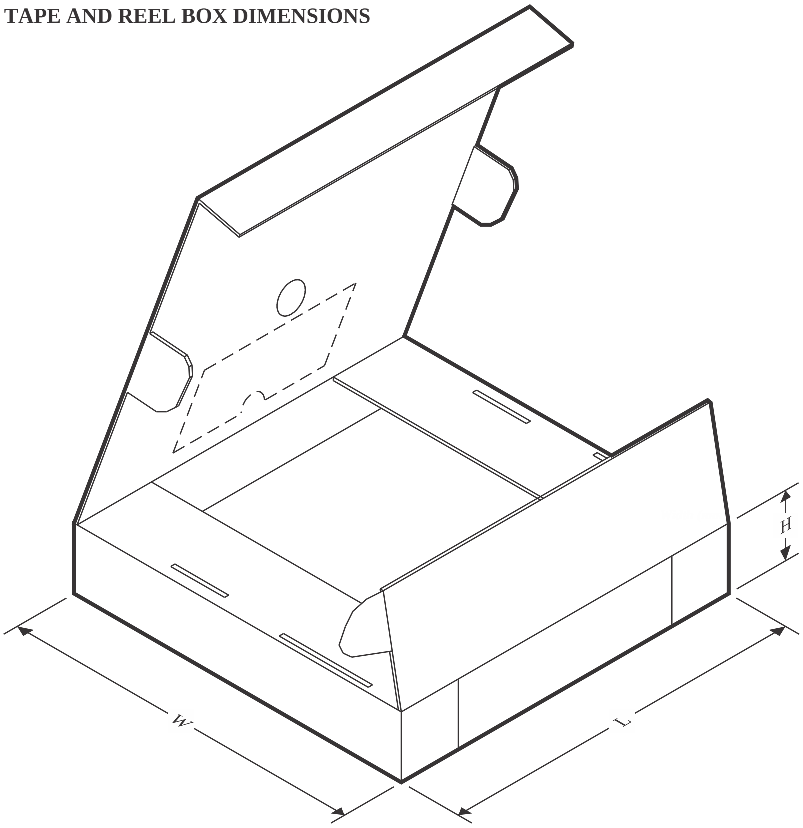
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7821LLSDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7821LLSDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

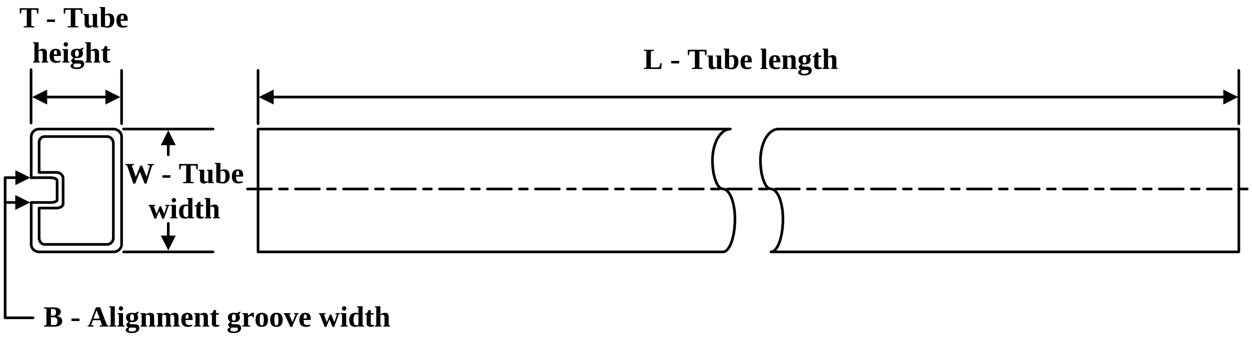
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7821LLSDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7821LLSDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7821LLSDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7821LLSDWW	DWW	SOIC	16	45	507	20	5000	9

GENERIC PACKAGE VIEW

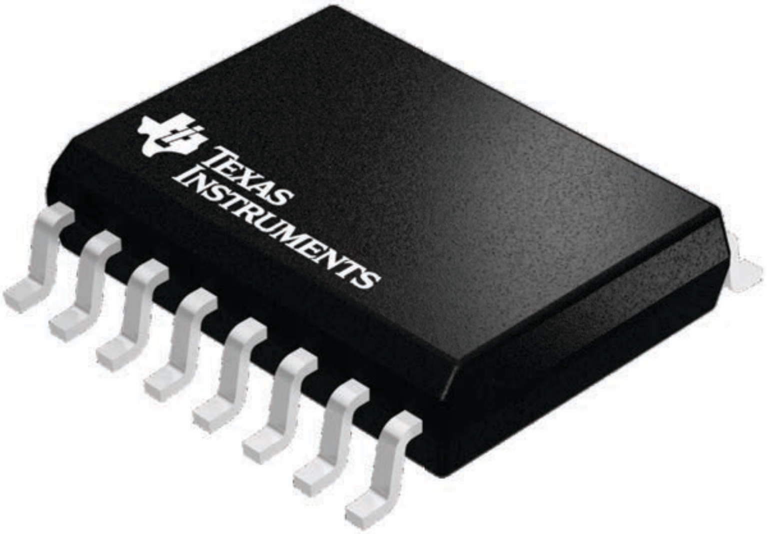
DW 16

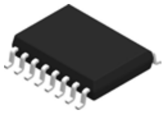
SOIC - 2.65 mm max height

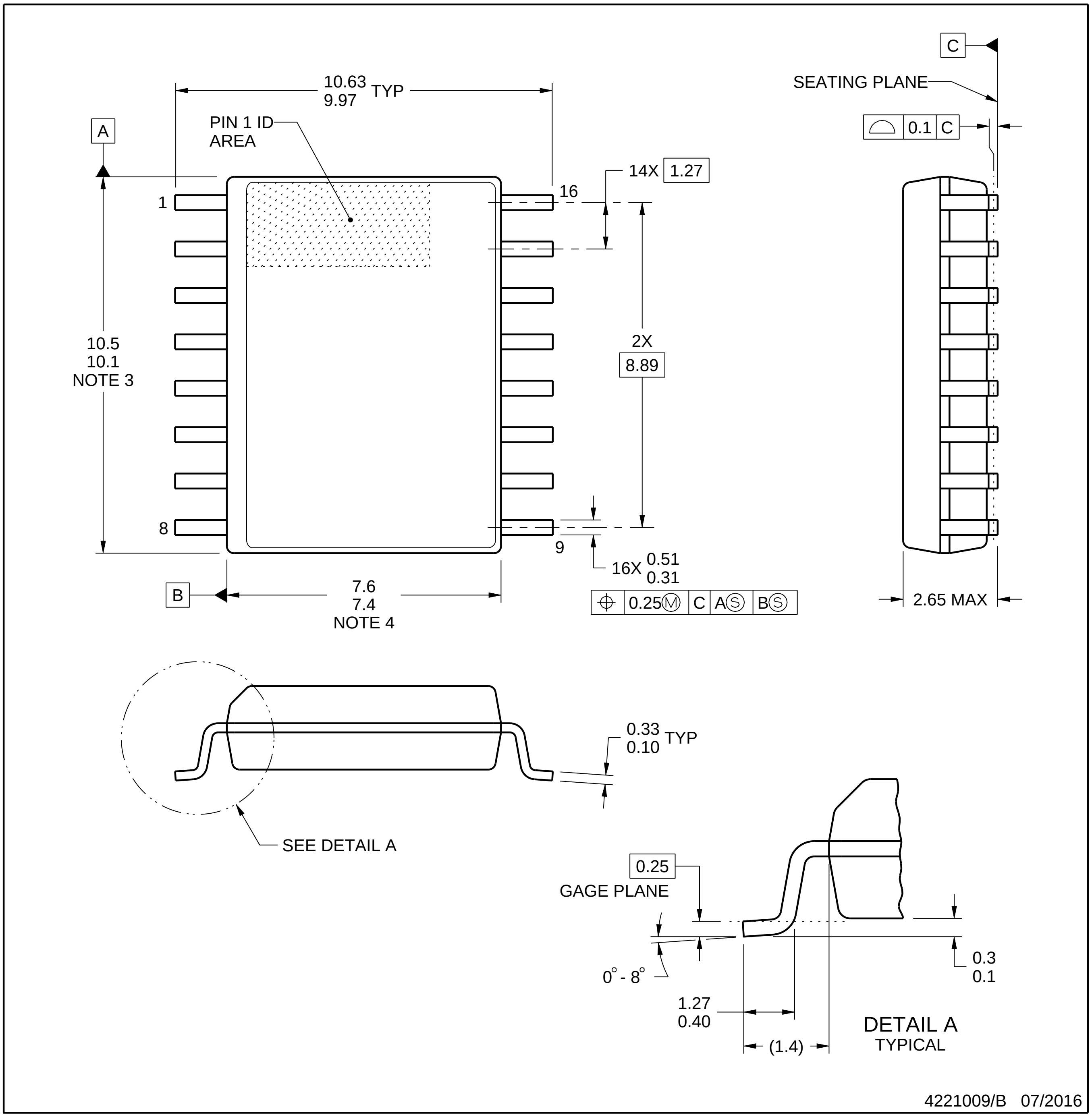
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



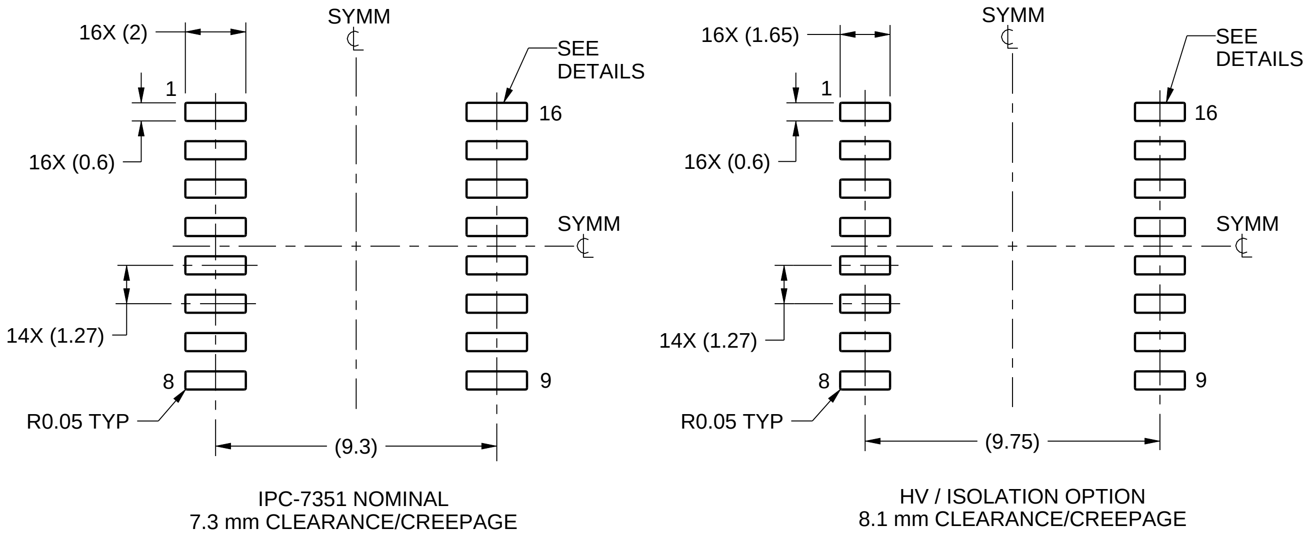




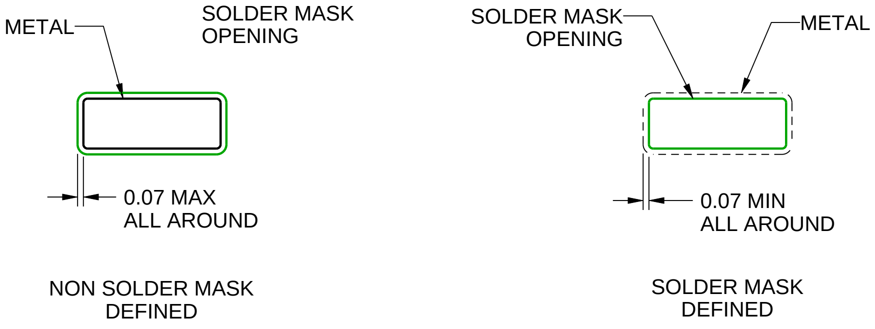
4221009/B 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X

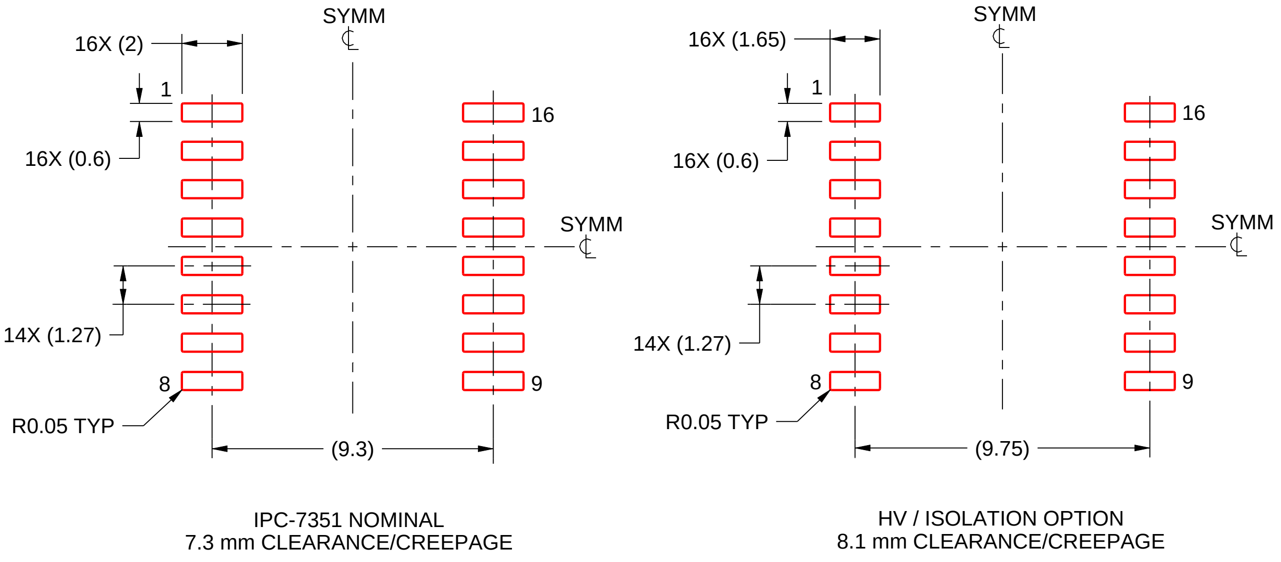


SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

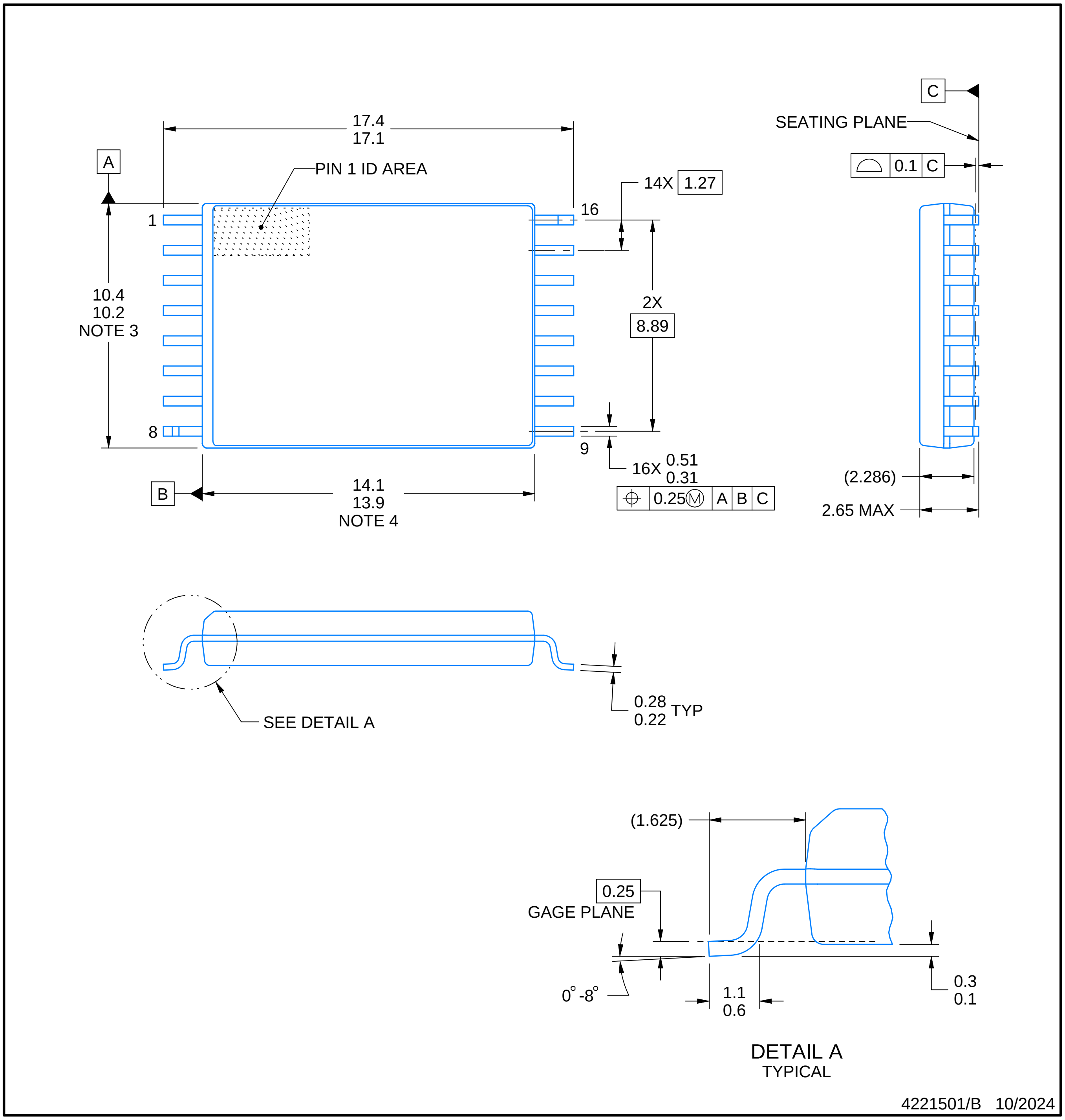
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DWW0016A

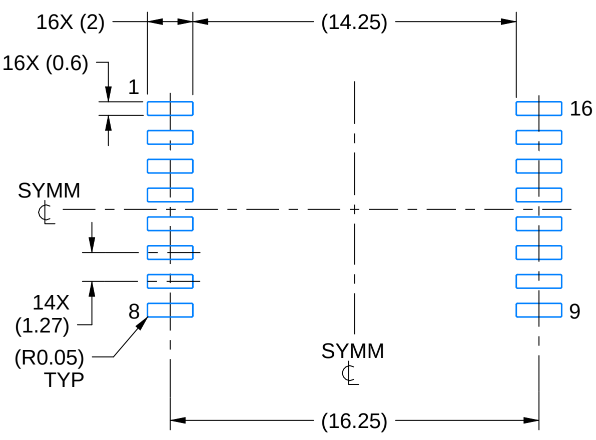
SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

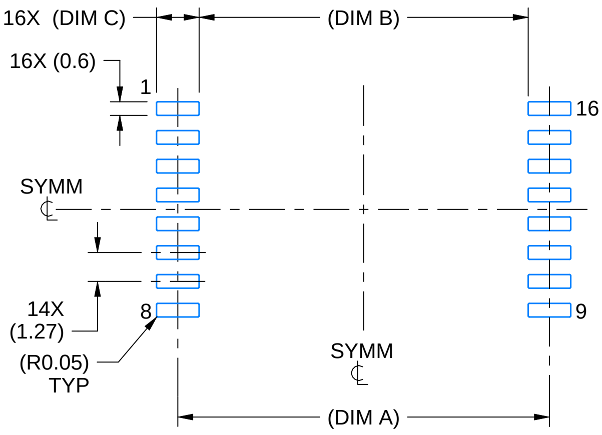


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

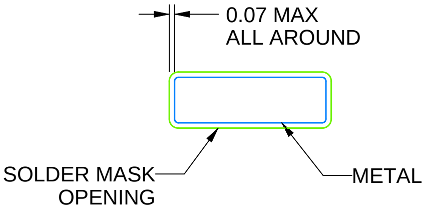


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

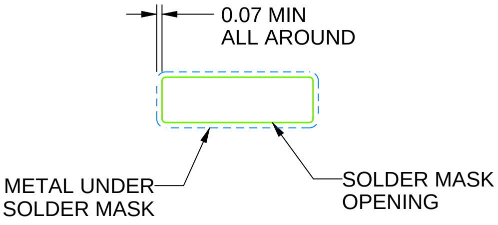


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)

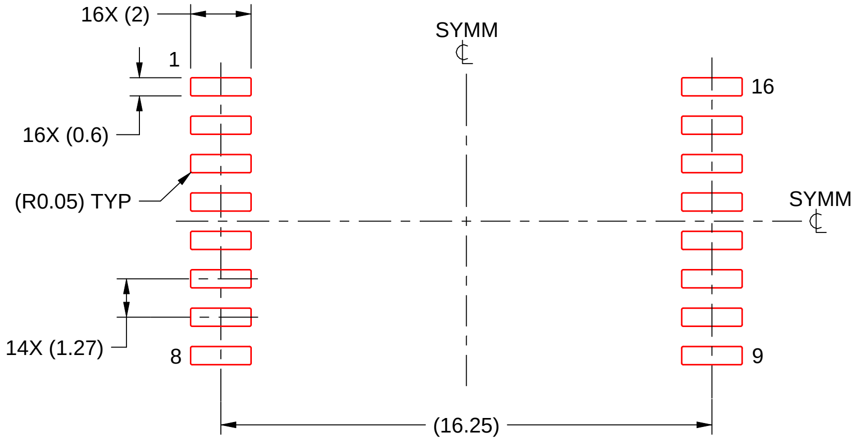


SOLDER MASK
DEFINED

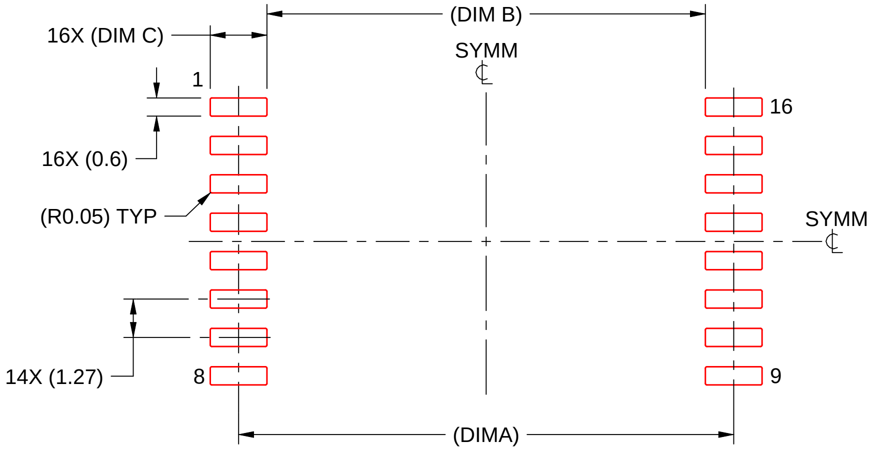
SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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