ISO7830 高性能 8000 V_{PK} 增强型三通道数字隔离器

1 特性

- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 至 5.5V 电平转换
- 宽温度范围：–55°C 至 125°C
- 低功耗，每通道电流典型值为 2.4mA（1Mbps 时）
- 低传播延迟：典型值 11ns（5V 电源供电时）
- 行业领先的 CMTI：±100kV/μs
- 优异的电磁兼容性 (EMC)
- 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
- 低辐射
- 隔离隔栅寿命：> 25 年
- 宽体小外形尺寸集成电路 (SOIC)-16 封装
- 安全及管理批准:
  - 8000 V_{PK} V_{IOTM} 和 2121 V_{PK} V_{IORM} 增强型隔离，符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准
  - 符合 UL 1577 标准且长达 1 分钟的 5.7kV_{RMS} 隔离
  - CSA 组件接受通知 5A，IEC 60950-1、IEC 60601-1 和 IEC 61010-1 终端设备标准
  - 通过 GB4943.1-2011 CQC 认证

2 应用范围

- 工业自动化
- 电机控制
- 电源
- 太阳能逆变器
- 医疗设备
- 混合动力电动汽车

3 说明

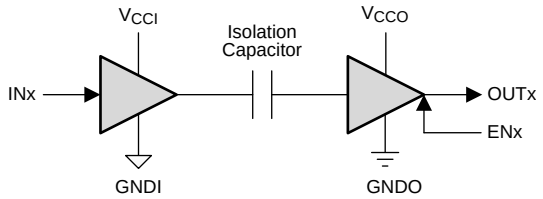
ISO7830 是一款高性能三通道数字隔离器，隔离电压高达 8000 V_{PK}。 该器件已通过符合 VDE、CSA 和 CQC 标准的增强型隔离认证。 在隔离 CMOS 或者 LVCMOS 数字 I/O 时，该隔离器可提供高电磁抗扰度和低辐射，且具有低功耗特性。 每个隔离通道的逻辑输入和输出缓冲器均由二氧化硅 (SiO_2) 绝缘隔栅分离开来。 该器件配有使能引脚，可用于将多个主驱动应用中的相应输出置于高阻态，也可用于降低功耗。 ISO7830 具有三个正向通道，没有反向通道。 如果出现输入功率或信号丢失，ISO7830 器件默认输出“高”电平，ISO7830F 器件默认输出“低”电平。 更多详细信息，请参见*器件功能模式*。 与隔离式电源一起使用时，此器件可防止数据总线或者其他电路上的噪声电流进入本地接地，以及干扰或损坏敏感电路。 凭借创新的芯片设计和布线技术，ISO7830 的电磁兼容性得到了显著增强，从而可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。 ISO7830 采用 16 引脚小外形尺寸集成电路 (SOIC) 宽体 (DW) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7830 ISO7830F	SOIC，DW (16)	10.30mm x 7.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



(1) V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

(2) V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接。

目录

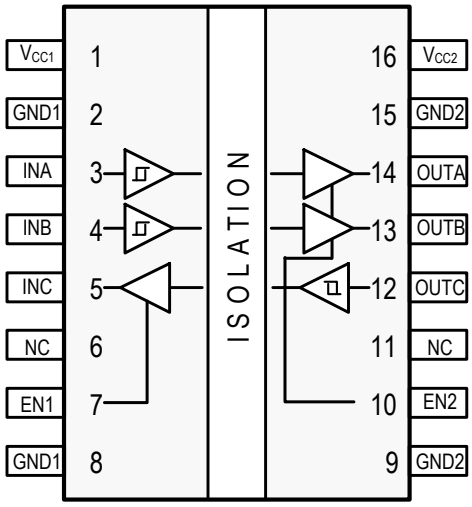
4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2015) to Revision A	Page
• 已从“单页产品预览”更改为“量产”数据表	1

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
NC	6, 11	—	Not connected
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)		–0.5	6	V
	Voltage	INx	–0.5	V_{CCX} + 0.5(3)	V
		OUTx			
		ENx			
I_O	Output current		–15	15	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO}(1) = 5 V	–4			mA
		V_{CCO}(1) = 3.3 V	–2			
		V_{CCO}(1) = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO}(1) = 5 V			4	mA
		V_{CCO}(1) = 3.3 V			2	
		V_{CCO}(1) = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI} (1)		V_{CCI} (1)	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}(1)	V
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature(2)		–55		150	°C
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) To maintain the recommended operating conditions for T_J, see *Thermal Information*.

6.4 Thermal Information

THERMAL METRIC(1)		DW (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	
ψ_{JT}	Junction-to-top characterization parameter	15.5	
ψ_{JB}	Junction-to-board characterization parameter	43.1	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Rating

			VALUE	UNIT
P_D	Maximum power dissipation by ISO7830	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave	150	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7830		40	
P_{D2}	Maximum power dissipation by side-2 of ISO7830		110	

6.6 Electrical Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 7		V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V; see Figure 10		70	100		kV/µs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	1.8	mA
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		0.4	0.6	
I_{CC1}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.6	
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		0.4	0.6	
I_{CC1}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	2	
I_{CC2}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.7	2.7	
I_{CC1}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.8	
I_{CC2}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		1.9	2.8	
I_{CC1}		1 Mbps	AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.8	4.4	
I_{CC2}		1 Mbps			1.9	3.0	
I_{CC1}		10 Mbps			2.9	4.4	
I_{CC2}		10 Mbps			3.3	4.6	
I_{CC1}		100 Mbps			3.9	4.9	
I_{CC2}		100 Mbps			17.5	20.8	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.7 Electrical Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 7		V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V; see Figure 10		70	100		kV/µs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	1.8	mA
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		0.3	0.6	
I_{CC1}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.6	
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		0.3	0.6	
I_{CC1}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	2	
I_{CC2}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.7	2.6	
I_{CC1}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.8	
I_{CC2}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		1.9	2.8	
I_{CC1}		1 Mbps	AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.8	4.4	
I_{CC2}		1 Mbps			1.9	2.9	
I_{CC1}		10 Mbps			2.9	4.4	
I_{CC2}		10 Mbps			2.9	4.1	
I_{CC1}		100 Mbps			3.5	4.8	
I_{CC2}		100 Mbps			13.2	16	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.8 Electrical Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 7		V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V; see Figure 10		70	100		kV/µs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	1.8	mA
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		0.3	0.6	
I_{CC1}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.6	
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		0.3	0.6	
I_{CC1}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.1	2.0	
I_{CC2}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.7	2.6	
I_{CC1}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		4.6	6.8	
I_{CC2}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		1.8	2.8	
I_{CC1}		1 Mbps	AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.8	4.4	
I_{CC2}		1 Mbps			1.8	2.9	
I_{CC1}		10 Mbps			2.9	4.4	
I_{CC2}		10 Mbps			2.6	3.7	
I_{CC1}		100 Mbps			3.4	4.7	
I_{CC2}		100 Mbps			10.3	12.7	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.9 Switching Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	11	16	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.55	4.1	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			2.5	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 7		1.7	3.9	
t_f	Output signal fall time			1.9	3.9	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		12	20	
t_{PLZ}	Disable propagation delay, low-to-high impedance output			12	20	
t_{PZH}	Enable propagation delay, high impedance-to-high output			10	20	ns
	Enable propagation delay, high impedance-to-high output			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output			2	2.5	µs
	Enable propagation delay, high impedance-to-low output			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.10 Switching Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	10.8	16	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.7	4.2	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			2.2	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 7		0.8	3	
t_f	Output signal fall time			0.8	3	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		17	32	
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	32	
t_{PZH}	Enable propagation delay, high impedance-to-high output			17	32	ns
	Enable propagation delay, high impedance-to-high output			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output			2	2.5	µs
	Enable propagation delay, high impedance-to-low output			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	7.5	11.7	17.5	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$	See Figure 7		0.66	4.2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 7		1	3.5	ns
t_f	Output signal fall time	See Figure 7		1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output	See Figure 8		22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		18	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.12 Typical Characteristics

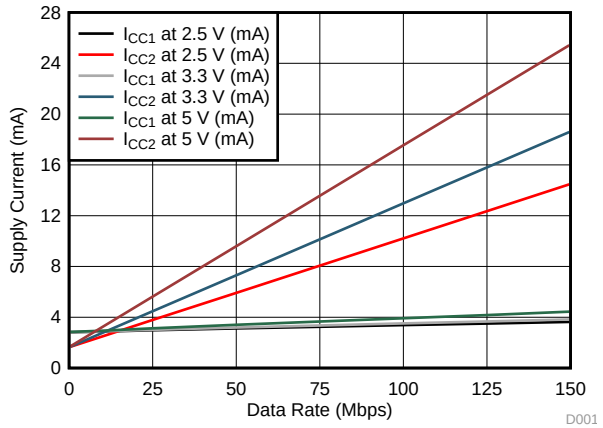


Figure 1. Supply Current vs Data Rate (With 15-pF Load)

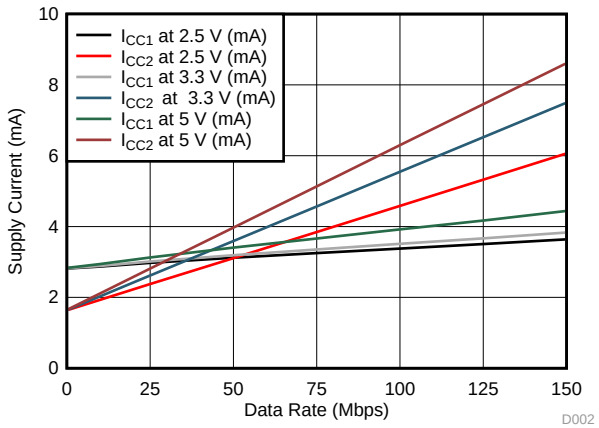


Figure 2. Supply Current vs Data Rate (With No Load)

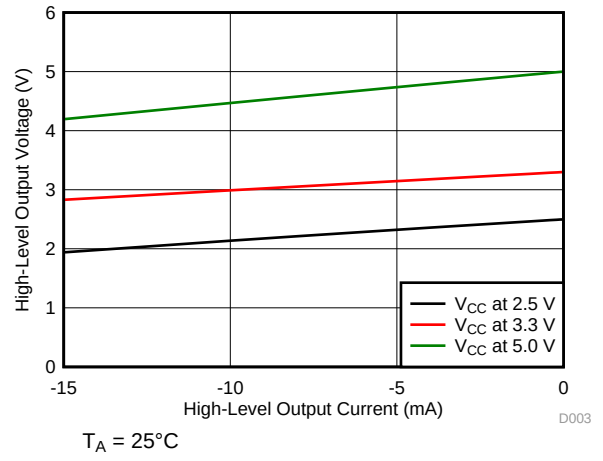


Figure 3. High-Level Output Voltage vs High-level Output Current

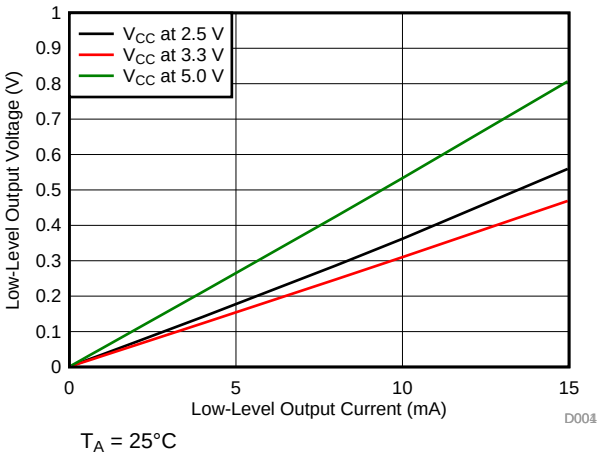


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

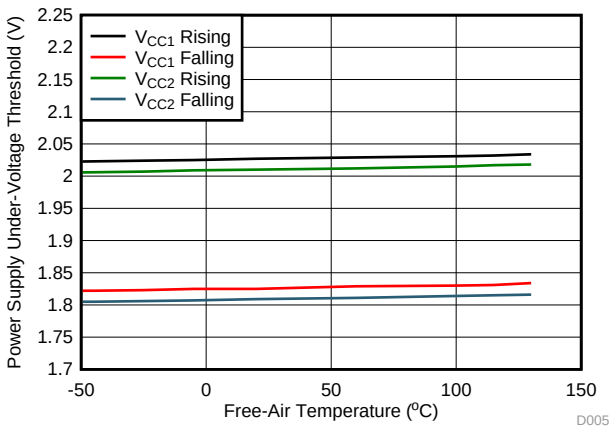


Figure 5. Power Supply Undervoltage Threshold vs Free-Air Temperature

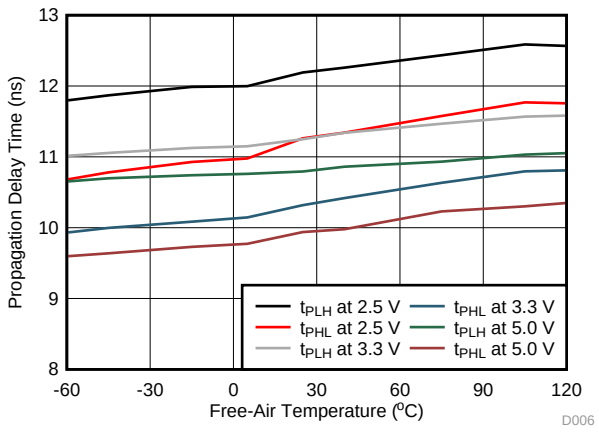
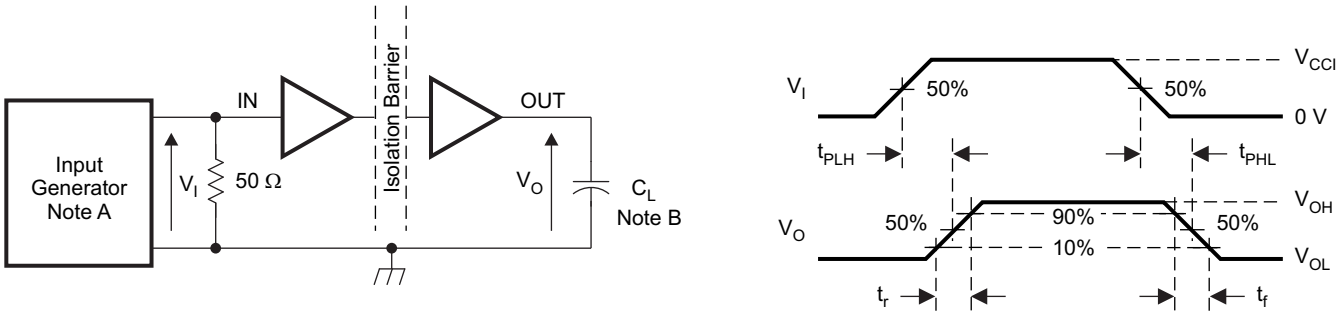


Figure 6. Propagation Delay Time vs Free-Air Temperature

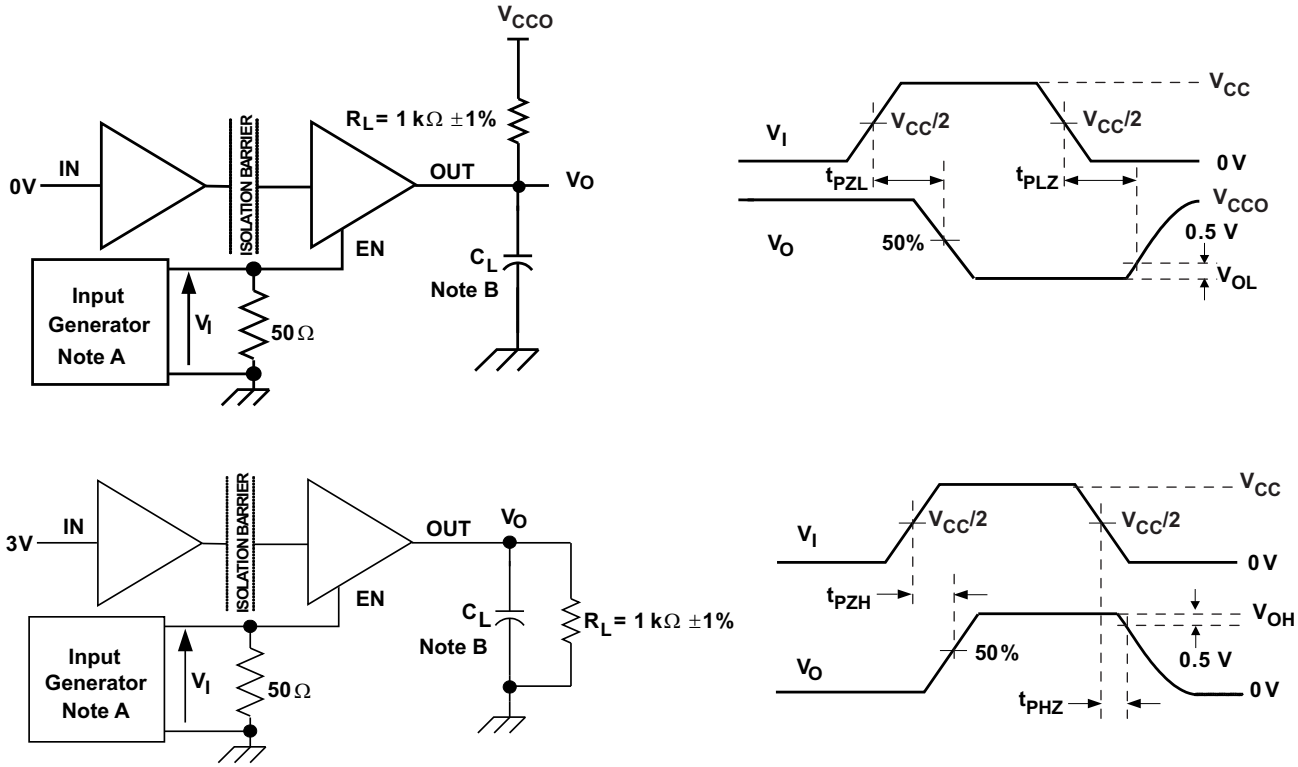
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7. Switching Characteristics Test Circuit and Voltage Waveforms

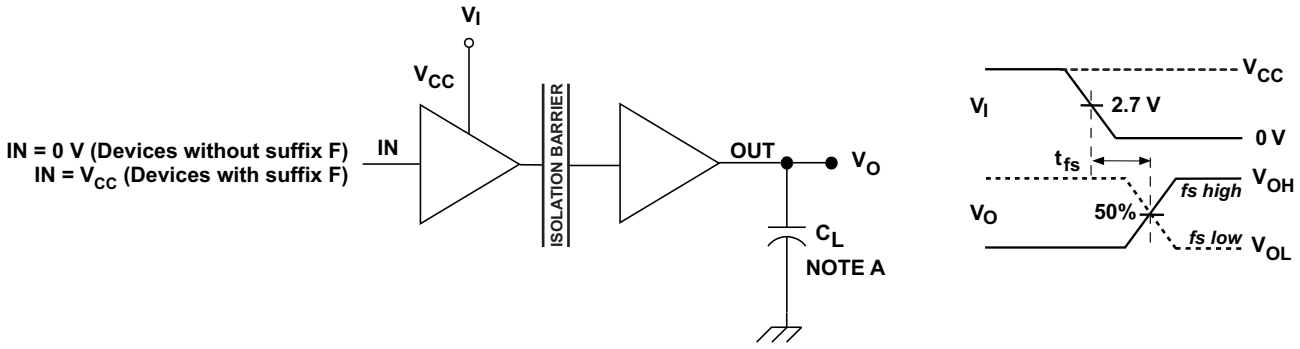


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

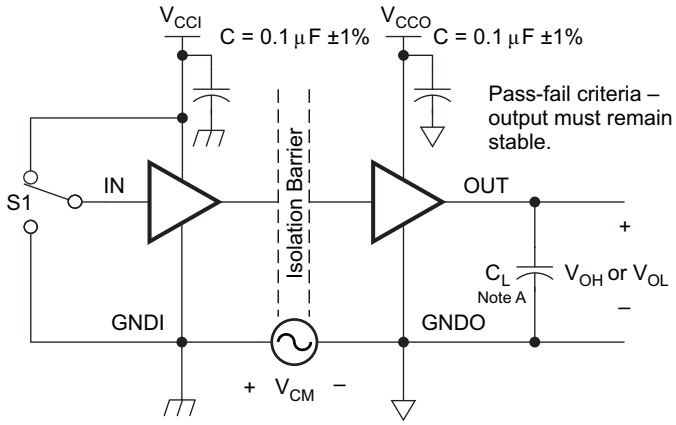
Figure 8. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

ISO7830 employs an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. ISO7830 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 11, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

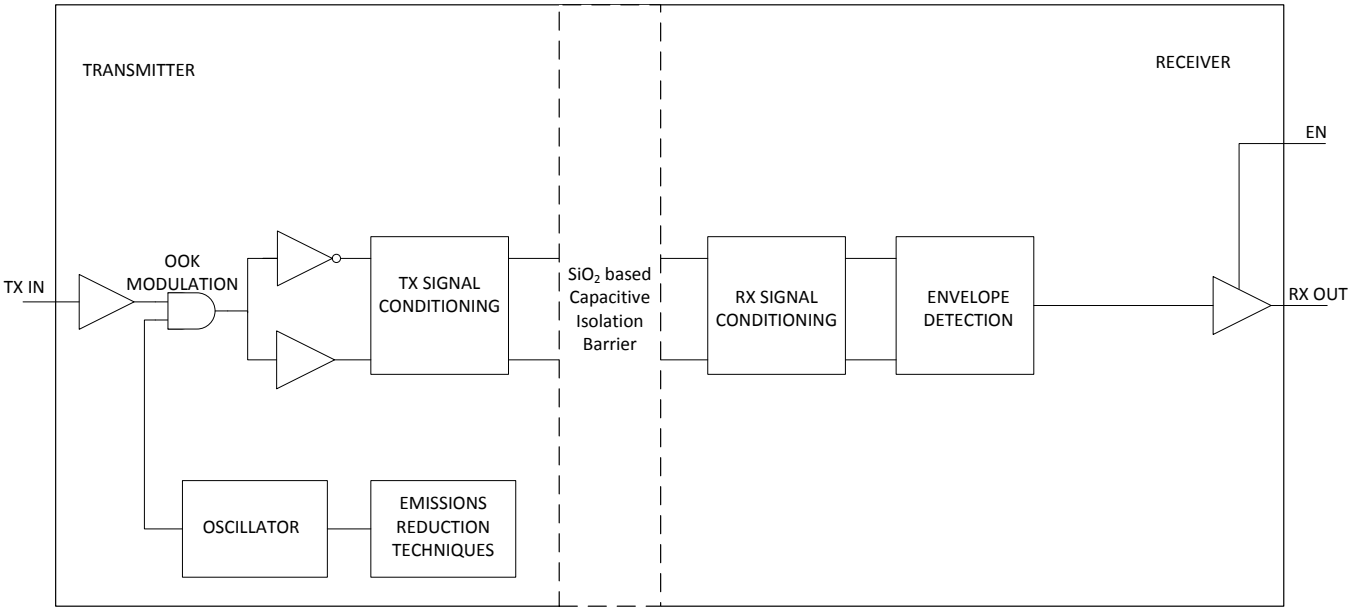


Figure 11. Conceptual Block Diagram of a Digital Capacitive Isolator

Also a conceptual detail of how the ON/OFF Keying scheme works is shown in Figure 12.

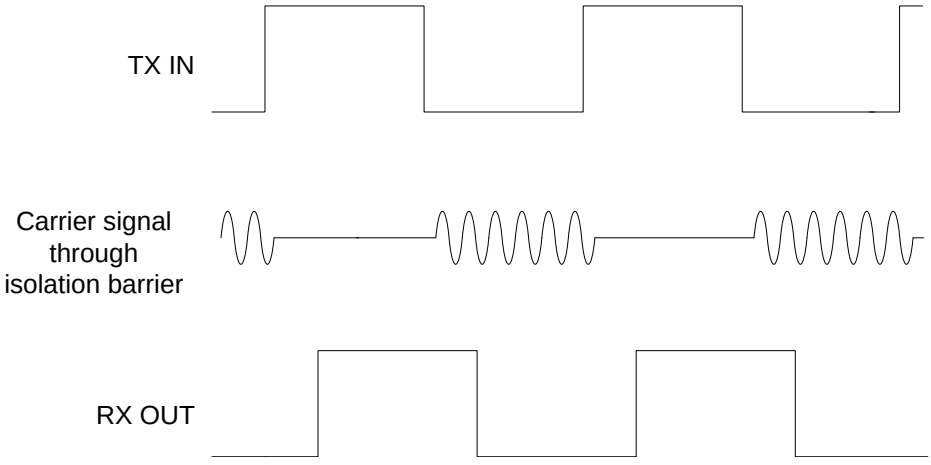


Figure 12. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7830	3 Forward	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7830	3 Forward	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See *Regulatory Information* for detailed isolation ratings.

8.3.1 High Voltage Feature Description

8.3.1.1 Package Insulation and Safety-Related Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	DW-16	8			mm
L(I02) (1)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	DW-16	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		600			V
R_{IO}	Isolation resistance, input to output (2)	V_{IO} = 500 V, T_A = 25°C		10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		10^{11}			Ω
C_{IO}	Barrier capacitance, input to output (2)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz			2		pF
C_I	Input capacitance (3)	V_I = V_{CC}/2 + 0.4 x sin (2πft), f = 1 MHz, V_{CC} = 5 V			2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	µm
V_{IOWM}	Maximum isolation working voltage	Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
			2121	V_{DC}
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
V_{IORM}	Maximum repetitive peak isolation voltage		2121	V_{PK}
V_{PR}	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	2545	V_{PK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial Discharge < 5 pC	3394	
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 sec (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 sec (100% production)	5700	V_{RMS}

(1) Climatic Classification 55/125/21

8.3.1.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	I
Installation classification	Rated mains voltage ≤ 600 V_{RMS}	I–IV
	Rated mains voltage ≤ 1000 V_{RMS}	I–III

8.3.1.4 Regulatory Information

DW package certifications are complete.

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed., 300 V_{RMS} max working voltage; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage	Single protection, 5700 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

(1) Production tested ≥ 6840 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current for DW-16 Package	$R_{\theta JA}$ = 78.9°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			288	mA
		$R_{\theta JA}$ = 78.9°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			440	
		$R_{\theta JA}$ = 78.9°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			576	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 78.9°C/W, T_J = 150°C, T_A = 25°C			1584	mW
T_S	Maximum case temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a High-K test board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance

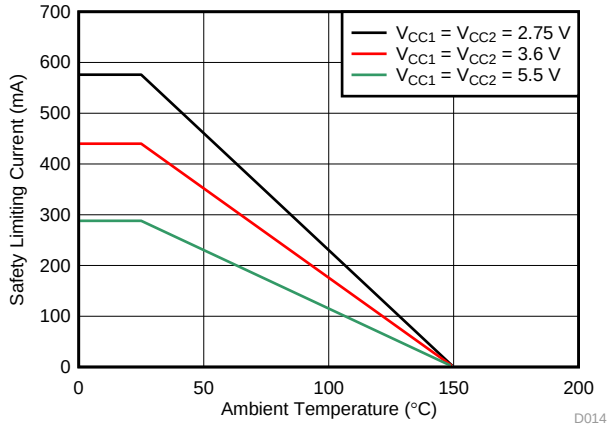


Figure 13. Thermal Derating Curve per VDE for DW-16 Package

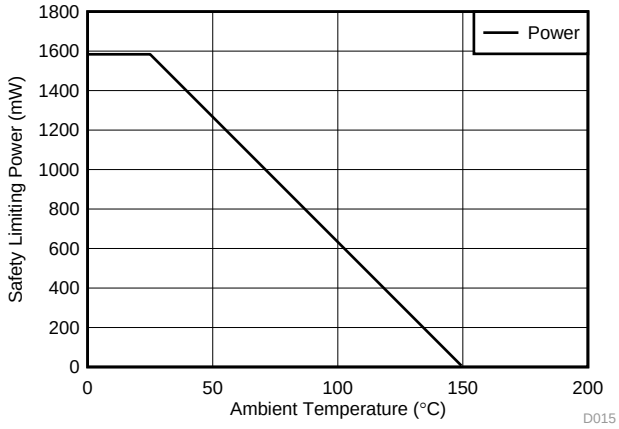


Figure 14. Thermal Derating Curve for Safety Limiting Power per VDE

8.4 Device Functional Modes

ISO7830 functional modes are shown in Table 1.

Table 1. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default= High for ISO7830 and Low for ISO7830F
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for ISO7830 and Low for ISO7830F When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

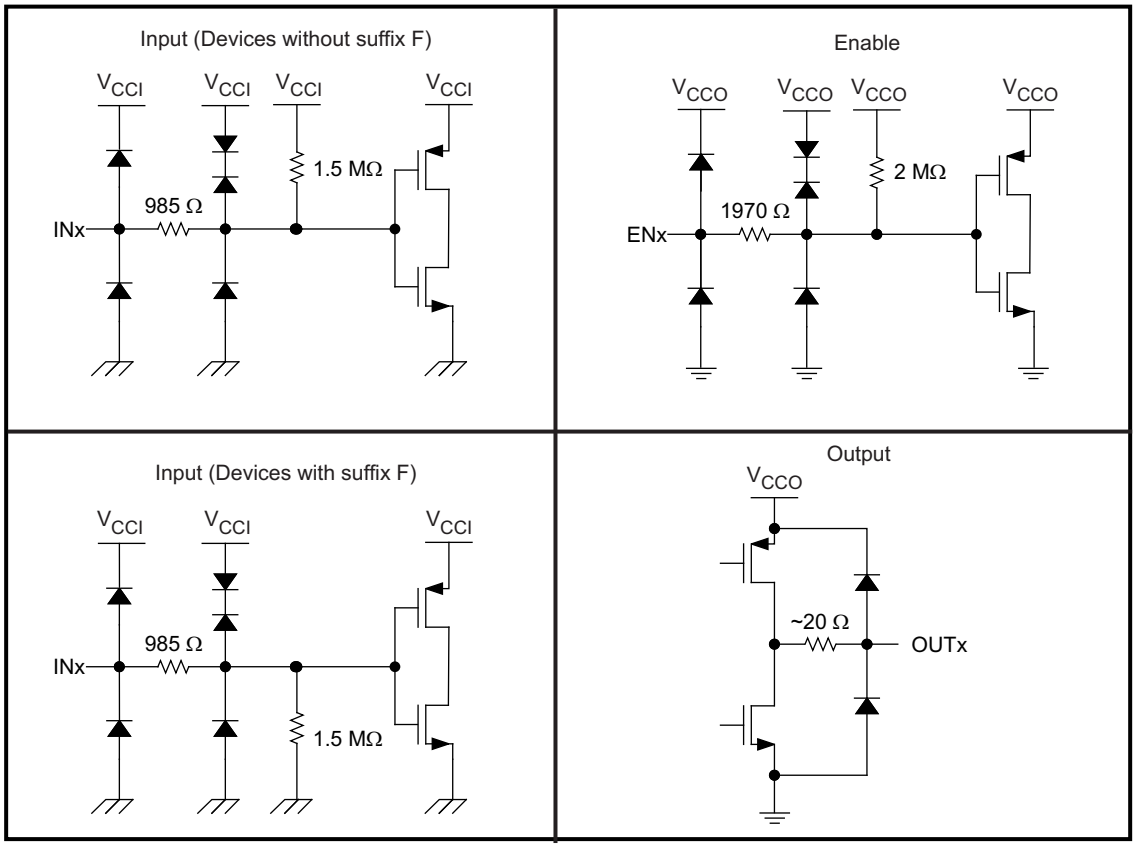


Figure 15. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7831 is a high-performance, quad-channel digital isolator with 5.7 kV_{RMS} isolation voltage. The device comes with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. ISO7831 uses single-ended CMOS-logic switching technology. Its supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The Isolated SPI Interface is shown in Figure 16.

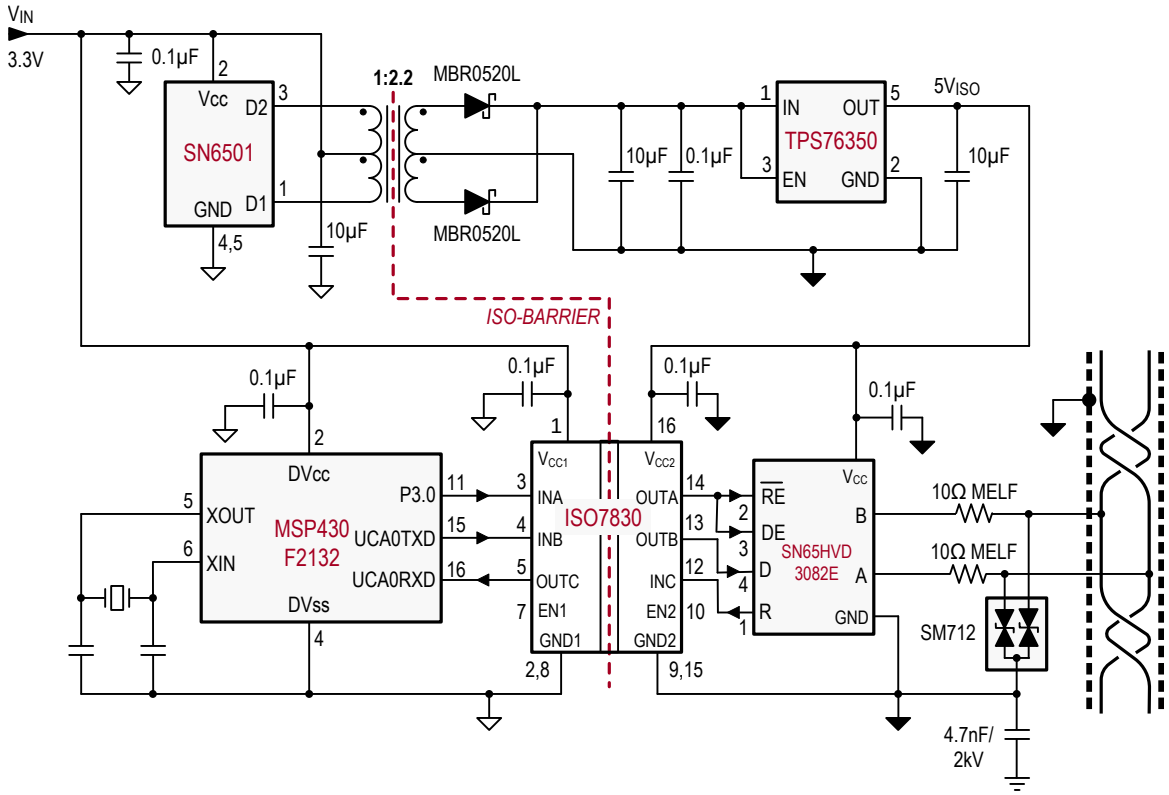


Figure 16. Isolated SPI Interface for an Analog Input Module With 16 Input

Typical Application (continued)

9.2.1 Design Requirements

For ISO7831, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO7831 only needs two external bypass capacitors to operate.

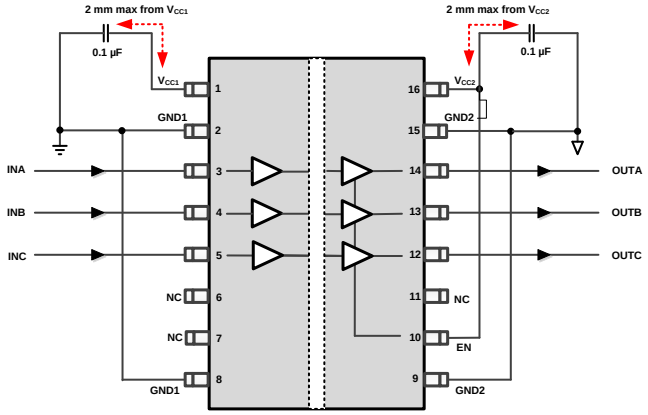


Figure 17. Typical ISO7830 Circuit Hook-up

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7830 incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.2.3 Application Curve

Typical eye diagram of ISO7830 indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

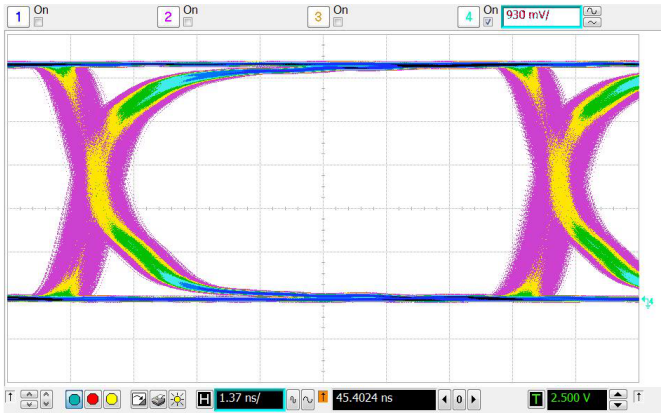


Figure 18. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 19). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see application note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (flame retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

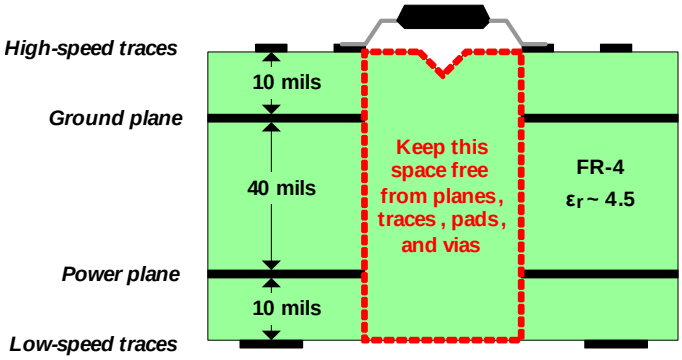


Figure 19. Layout Example Schematic

12 器件和文档支持

12.1 文档支持

《SN6501 用于隔离电源的变压器驱动器》，SLLSEA0

《数字隔离器设计指南》，SLLA284

12.1.1 相关文档

请参见*隔离术语表* (SLLA353)

12.2 相关链接

下面的表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

表 **3.** 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ISO7830	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7830F	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7830DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830	Samples
ISO7830DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830	Samples
ISO7830DWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830	Samples
ISO7830DWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830	Samples
ISO7830FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F	Samples
ISO7830FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F	Samples
ISO7830FDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F	Samples
ISO7830FDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7830F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

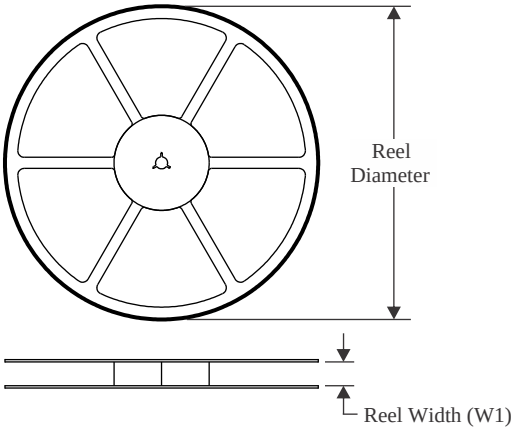
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

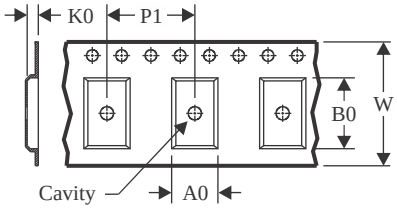
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

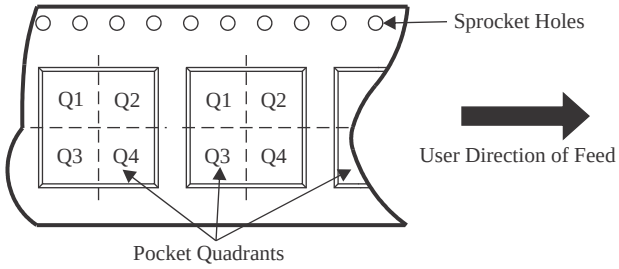


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

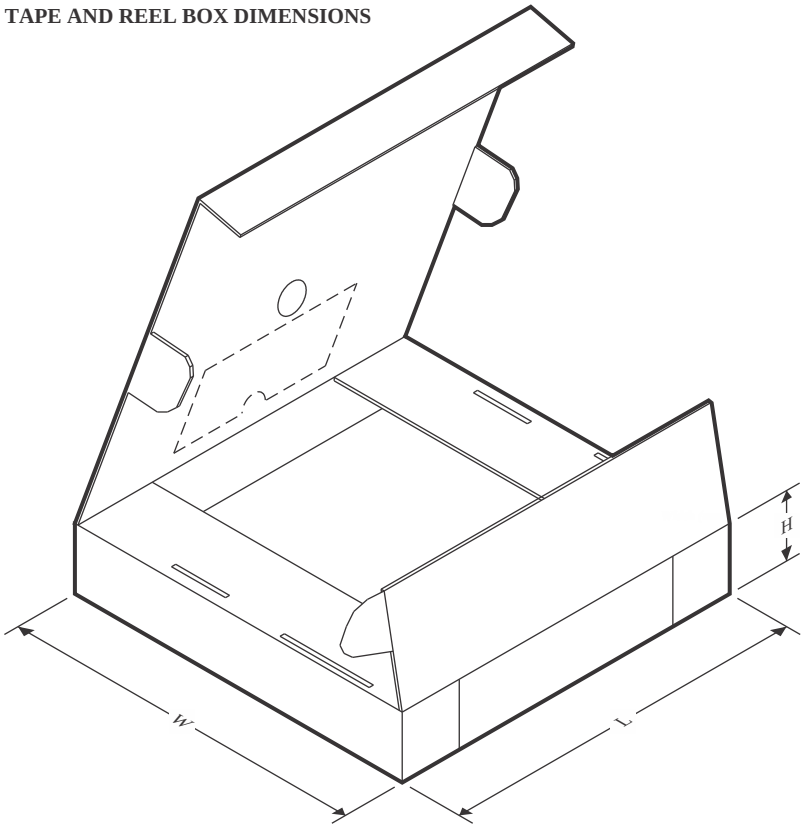
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7830DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7830DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7830FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7830FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

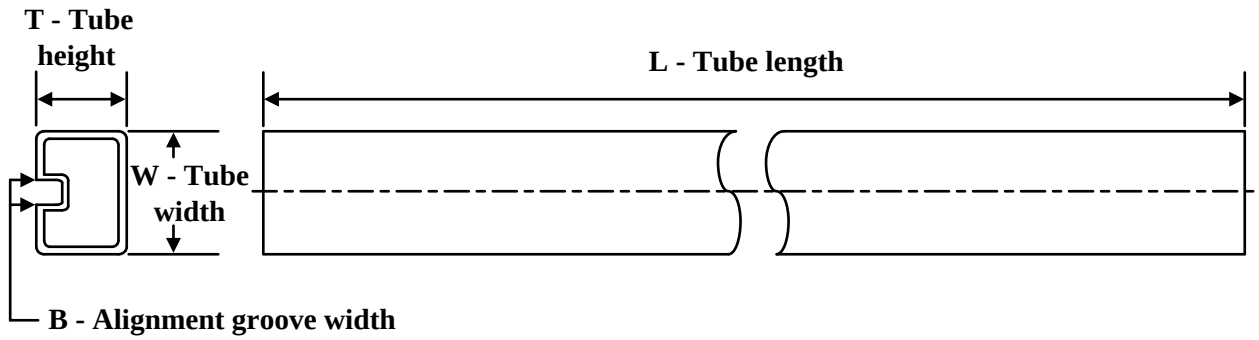
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7830DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7830DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7830FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7830FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7830DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7830FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7830FDWW	DWW	SOIC	16	45	507	20	5000	9

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