LM2735-Q1 520kHz 和 1.6MHz 高空间利用率升压和 SEPIC 直流/直流稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：-40°C 至 +125°C 运行环境温度范围
- 输入电压范围：2.7V 至 5.5V
- 输出电压范围：3V 至 24V
- 在整个温度范围内具有 2.1A 的开关电流
- 电流模式控制
- 逻辑高电平使能引脚
- 在关断模式下具有 80nA 的超低静态电流
- 170mΩ NMOS 开关
- ±2% 反馈电压精度
- 易于使用的小型解决方案总尺寸
  - 内部软启动
  - 内部补偿
  - 两种开关频率
  - 520kHz (LM2735-Y)
  - 1.6MHz (LM2735-X)
  - 使用小型表面贴装电感器和片式电容器
  - 微型 SOT-23 和 WSON 封装
- 使用 LM2735-Q1 及 WEBENCH® 电源设计器创建定制设计

2 应用

- 汽车信息娱乐系统与组合仪表
- 高级驾驶辅助系统 (ADAS)
- 网关
- 汽车 TFT LCD 偏置

3 说明

LM2735-Q1 器件是一款易于使用的高空间利用率 2.1A 低侧开关稳压器，非常适合升压和 SEPIC 直流/直流调节。该器件可提供所有有效功能，从而通过最小的 PCB 面积提供具有快速瞬变响应和精确调节功能的本地直流/直流转换。开关频率在内部设置为 520kHz 或 1.6MHz，从而允许使用极小的表面贴装电感器和片式电容器，同时提供高达 90% 的效率。该器件可用于进行后升压，即对主汽车系统 3.3V 电源轨进行升压，从而为需要 5V 电压的 CAN 收发器和其他电路供电。LM2735-Q1 可提供 24V 输出电压，因此还可为音频放大器、天线、同轴电缆供电 (PoC) 和汽车音频总线 (A2B) 器件供电。

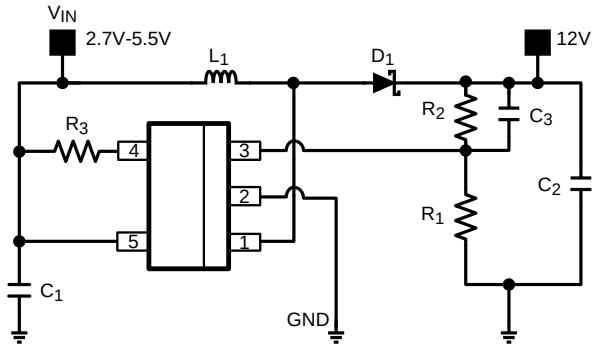
电流模式控制和内部补偿可在各种工作条件下提供易于使用、组件数最少且性能很高的调节。外部关断 具有 80nA 的超低待机电流，非常适合便携式 应用的需求。微型 SOT-23 和 WSON 封装可节省空间。其他 特性包括内部软启动、用于减小浪涌电流的电路、逐脉冲电流限制和热关断。

器件信息(1)

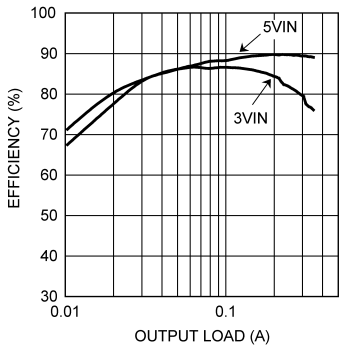
器件编号	封装	封装尺寸（标称值）
LM2735-Q1	WSON (6)	3.00mm × 3.00mm
	SOT-23 (5)	1.60mm × 2.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型的升压应用电路



效率与负载电流间的关系（V_O = 12V）



目录

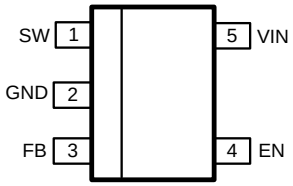
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

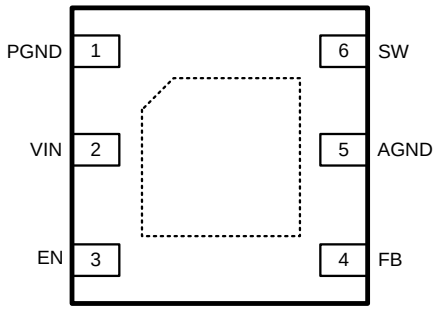
日期	修订版本	说明
2018 年 9 月	*	从 2007 年 6 月开始使用的综合数据表 SNVS485 商用和汽车数据表中，将 LM2735-Q1 分离出来。此文档，即 SNVSB73，对汽车用 LM2735-Q1 做了详细说明，并为 WEBENCH® 电源设计器添加了 ulink。
		将 SOT-23 和 WSON 封装的 V_{FB} 反馈测试条件从“T_J = –40°C 至 125°C”更改成了“T_J = 0°C 至 125°C”。

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



NGG Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
AGND	—	5	PWR	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to this pin and pin 4.
EN	4	3	I	Shutdown control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
FB	3	4	I	Feedback pin. Connect FB to external resistor-divider to set output voltage.
GND	2	DAP	PWR	Signal and power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin. For WSON, connect to pin 1 and pin 5 on top layer. Place 4-6 vias from DAP to bottom layer GND plane.
NC	—	—	—	No Connect
PGND	—	1	PWR	Power ground pin. Place PGND and output capacitor GND close together.
SW	1	6	O	Output switch. Connect to the inductor, output diode.
VIN	5	2	PWR	Supply voltage for power stage, and input supply voltage.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
V_{IN}	–0.5	7	V
SW voltage	–0.5	26.5	V
FB voltage	–0.5	3	V
EN voltage	–0.5	7	V
Junction temperature (3)		150	°C
Soldering information, infrared/convection reflow (15 s)		220	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}		2.7		5.5	V
V_{SW}		3		24	V
V_{EN} (1)		0		V_{IN}	V
Junction temperature		–40		125	°C
Power dissipation	(Internal) SOT-23			400	mW

(1) Do not allow this pin to float or be greater than V_{IN} + 0.3 V.

6.4 Thermal Information

THERMAL METRIC[1]		LM2735-Q1		UNIT
		NGG (WSON)	DBV (SOT-23)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	54.9	164.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[2]	50.9	115.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	27	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.4	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics application report*.
(2) Applies for packages soldered directly onto a 3-inch × 3-inch PC board with 2-oz. copper on 4 layers in still air.

6.5 Electrical Characteristics

Limits are for T_J = 25°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 5 V unless otherwise indicated under the Conditions column.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage	–40°C ≤ to T_J ≤ 125°C (SOT-23)	T_J = 25°C		1.255		V
			T_J = –40°C to 125°C	1.23		1.28	
		0°C ≤ to T_J ≤ 125°C (SOT-23)	T_J = 25°C		1.255		
			T_J = 0°C to 125°C	1.236		1.274	
		–40°C ≤ to T_J ≤ 125°C (WSON)	T_J = 25°C		1.255		
			T_J = –40°C to 125°C	1.225		1.285	
		0°C ≤ to T_J ≤ 125°C (WSON)	T_J = 25°C		1.255		
			T_J = 0°C to 125°C	1.229		1.281	
$\Delta V_{FB}/V_{IN}$	Feedback voltage line regulation	V_{IN} = 2.7 V to 5.5 V			0.06		%/V
I_{FB}	Feedback input bias current	T_J = 25°C			0.1		µA
		T_J = –40°C to 125°C				1	
F_{SW}	Switching frequency	LM2735-Q1-X	T_J = 25°C		1600		kHz
			T_J = –40°C to 125°C	1200		2000	
		LM2735-Q1-Y	T_J = 25°C		520		
			T_J = –40°C to 125°C	360		680	
D_{MAX}	Maximum duty cycle	LM2735-Q1-X	T_J = 25°C		96%		
			T_J = –40°C to 125°C	88%			
		LM2735-Q1-Y	T_J = 25°C		99%		
			T_J = –40°C to 125°C	91%			
D_{MIN}	Minimum duty cycle	LM2735-Q1-X			5%		
		LM2735-Q1-Y			2%		
$R_{DS(ON)}$	Switch ON-resistance	SOT-23	T_J = 25°C		170		mΩ
			T_J = –40°C to 125°C			330	
		WSON	T_J = 25°C		190		
			T_J = –40°C to 125°C			350	
I_{CL}	Switch current limit	T_J = 25°C			3		A
		T_J = –40°C to 125°C		2.1			
SS	Soft start				4		ms

Electrical Characteristics (continued)

Limits are for T_J = 25°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{IN} = 5 V unless otherwise indicated under the Conditions column.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current (switching)	LM2735-Q1-X	T_J = 25°C		7		mA
			T_J = –40°C to 125°C			11	
		LM2735-Q1-Y	T_J = 25°C		3.4		
			T_J = –40°C to 125°C			7	
	Quiescent current (shutdown)	All options V_{EN} = 0 V			80		nA
UVLO	Undervoltage lockout	VIN rising	T_J = 25°C		2.3		V
			T_J = –40°C to 125°C			2.65	
		VIN falling	T_J = 25°C		1.9		
			T_J = –40°C to 125°C	1.7			
V_{EN_TH}	Shutdown threshold voltage	See(1), T_J = –40°C to 125°C				0.4	V
	Enable threshold voltage	See(1), T_J = –40°C to 125°C		1.8			
I_{-SW}	Switch leakage	V_{SW} = 24 V			1		µA
I_{-EN}	Enable pin current	Sink/source			100		nA
T_{SD}	Thermal shutdown temperature(2)				160		°C
	Thermal shutdown hysteresis				10		

(1) Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
(2) Thermal shutdown occurs if the junction temperature exceeds the maximum junction temperature of the device.

6.6 Typical Characteristics

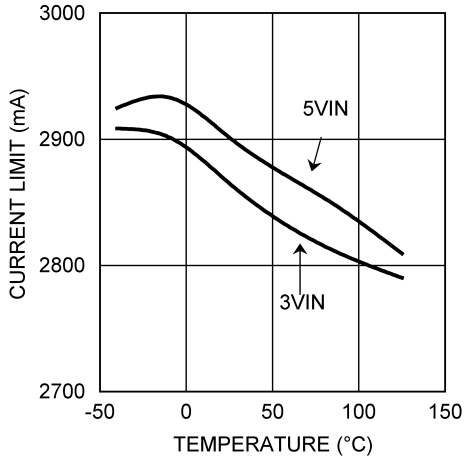


Figure 1. Current Limit vs Temperature

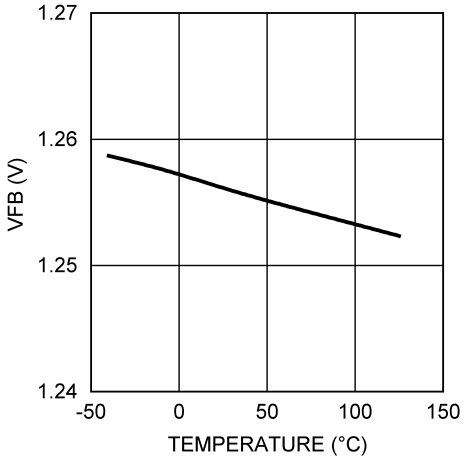


Figure 2. FB Pin Voltage vs Temperature

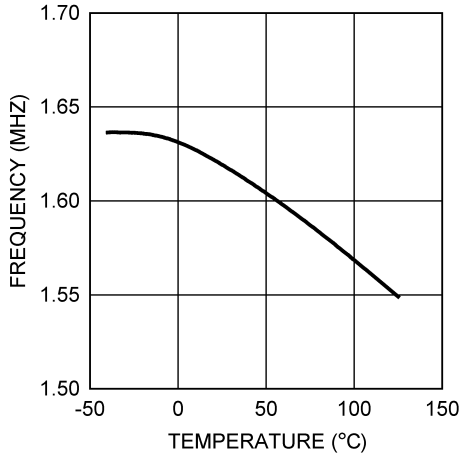


Figure 3. Oscillator Frequency vs Temperature - "X"

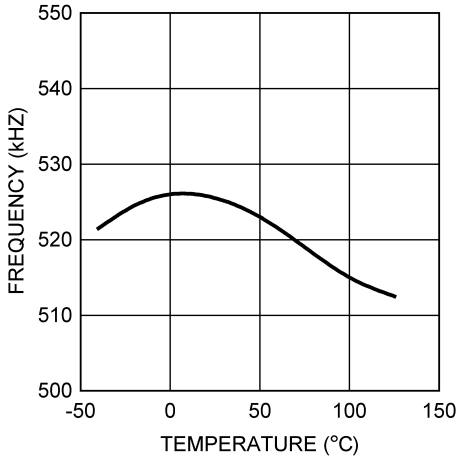


Figure 4. Oscillator Frequency vs Temperature - "Y"

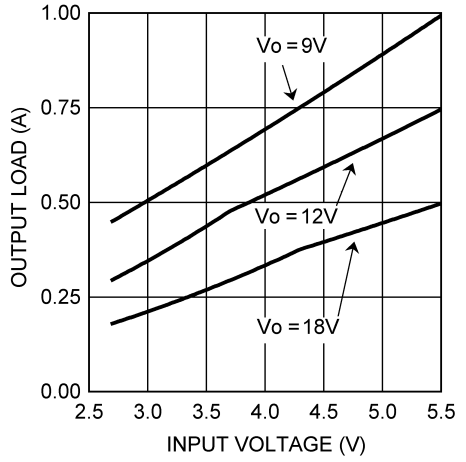


Figure 5. Typical Maximum Output Current vs V_{IN}

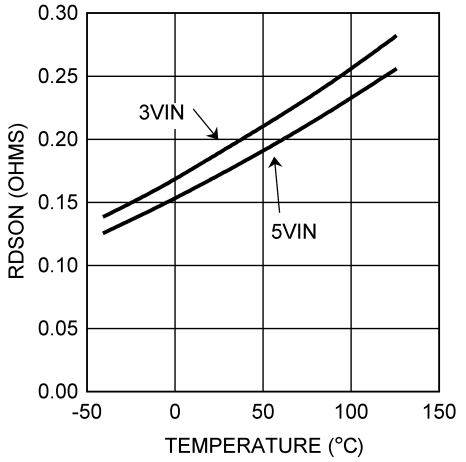
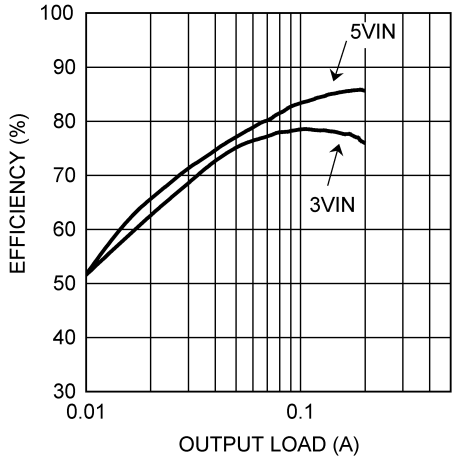


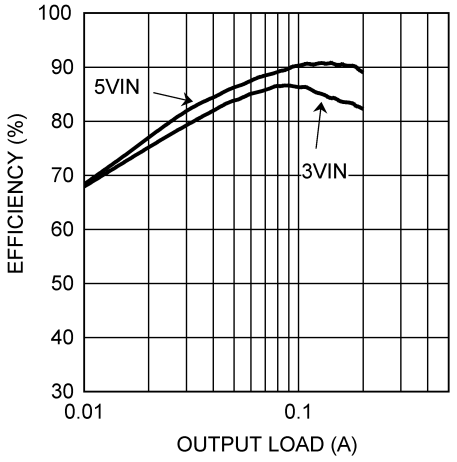
Figure 6. R_{DSON} vs Temperature

Typical Characteristics (continued)



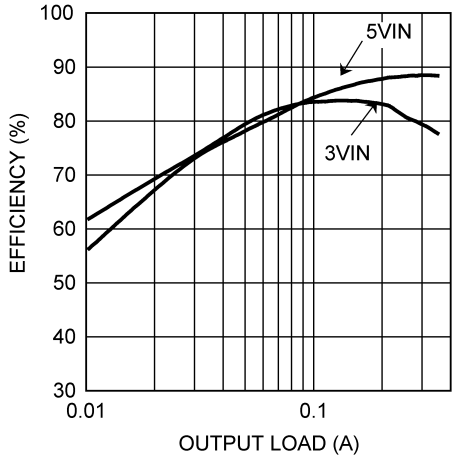
V_O = 20 V

Figure 7. LM2735-Q1X Efficiency vs Load Current



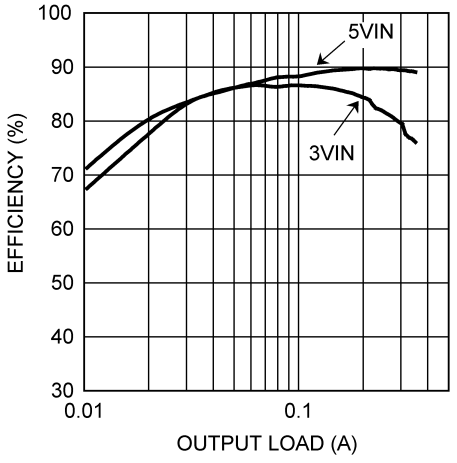
V_O = 20 V

Figure 8. LM2735-Q1Y Efficiency vs Load Current



V_O = 12 V

Figure 9. LM2735-Q1X Efficiency vs Load Current



V_O = 12 V

Figure 10. LM2735-Q1Y Efficiency vs Load Current

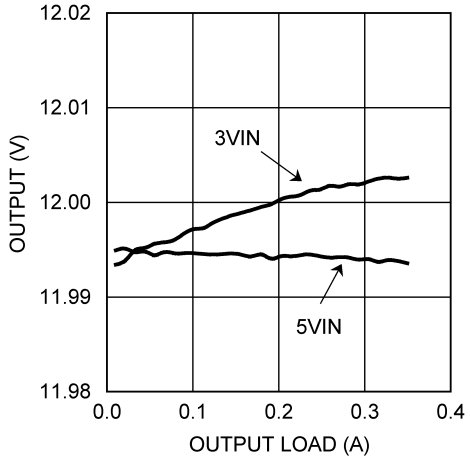


Figure 11. Output Voltage Load Regulation

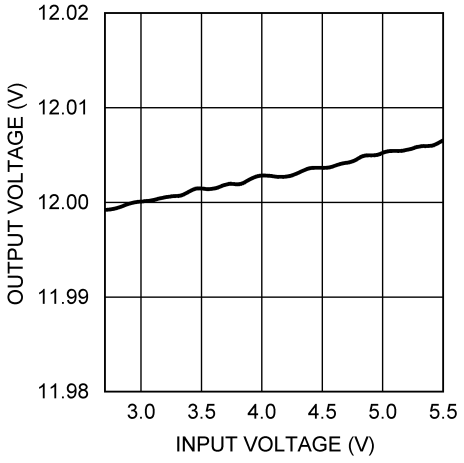


Figure 12. Output Voltage Line Regulation

7 Detailed Description

7.1 Overview

The LM2735-Q1 device is highly efficient and easy-to-use switching regulator for boost and SEPIC applications. The device provides regulated DC output with fast transient response. Device architecture (current mode control) and internal compensation enable solutions with minimum number of external components. Additionally high switching frequency allows for use of small external passive components (chip capacitors, SMD inductors) and enables power solutions with very small PCB area. LM2735-Q1 also provides features such as soft start, pulse-by-pulse current-limit, and thermal shutdown.

7.1.1 Theory of Operation

The LM2735-Q1 is a constant-frequency PWM boost regulator IC that delivers a minimum of 2.1 A peak switch current. The regulator has a preset switching frequency of either 520 kHz or 1.6 MHz. This high frequency allows the device to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LM2735-Q1 is internally compensated, so it is simple to use, and requires few external components. The device uses current-mode control to regulate the output voltage. The following operating description of the LM2735-Q1 refers to the simplified internal block diagram (*Functional Block Diagram*), the simplified schematic (Figure 13), and its associated waveforms (Figure 14). The LM2735-Q1 supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on-time, the SW pin voltage (V_{SW}) decreases to approximately GND, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sensed signal is summed with the corrective ramp of the regulator and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through diode D1, which forces the SW pin to swing to the output voltage plus the forward voltage (V_D) of the diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage .

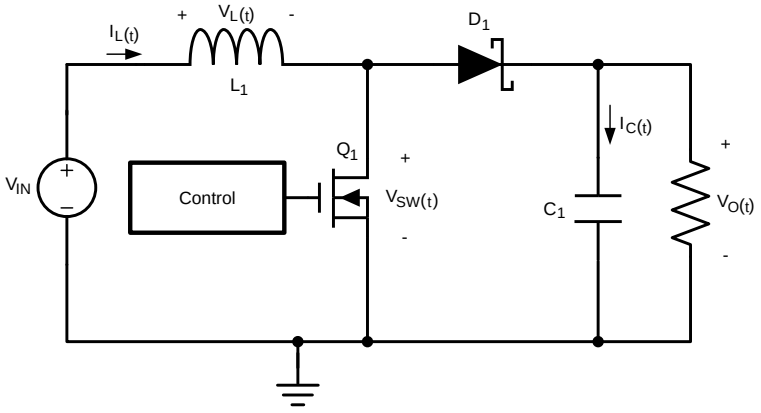


Figure 13. Simplified Schematic

Overview (continued)

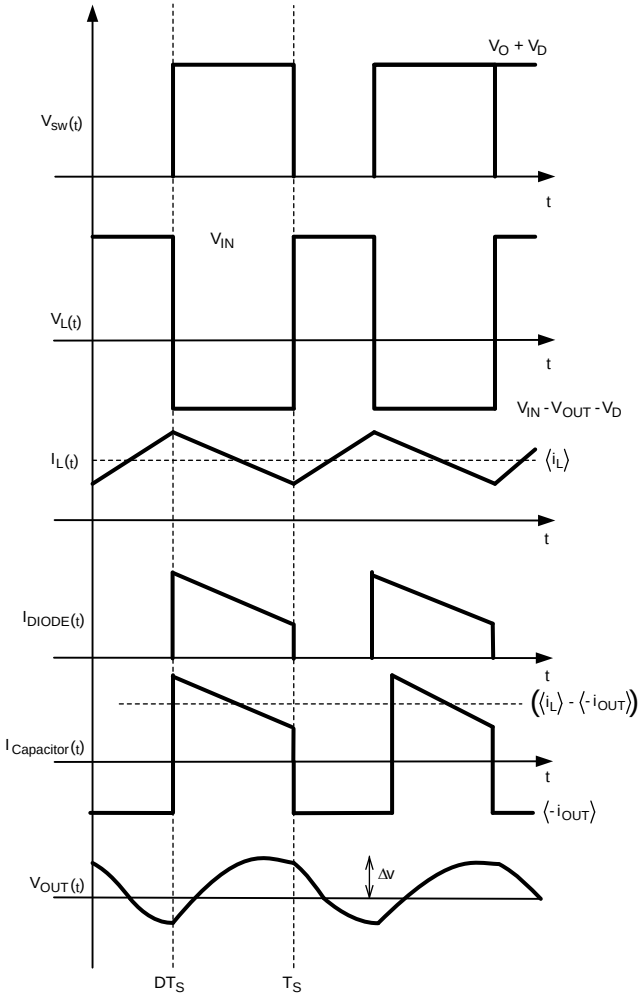
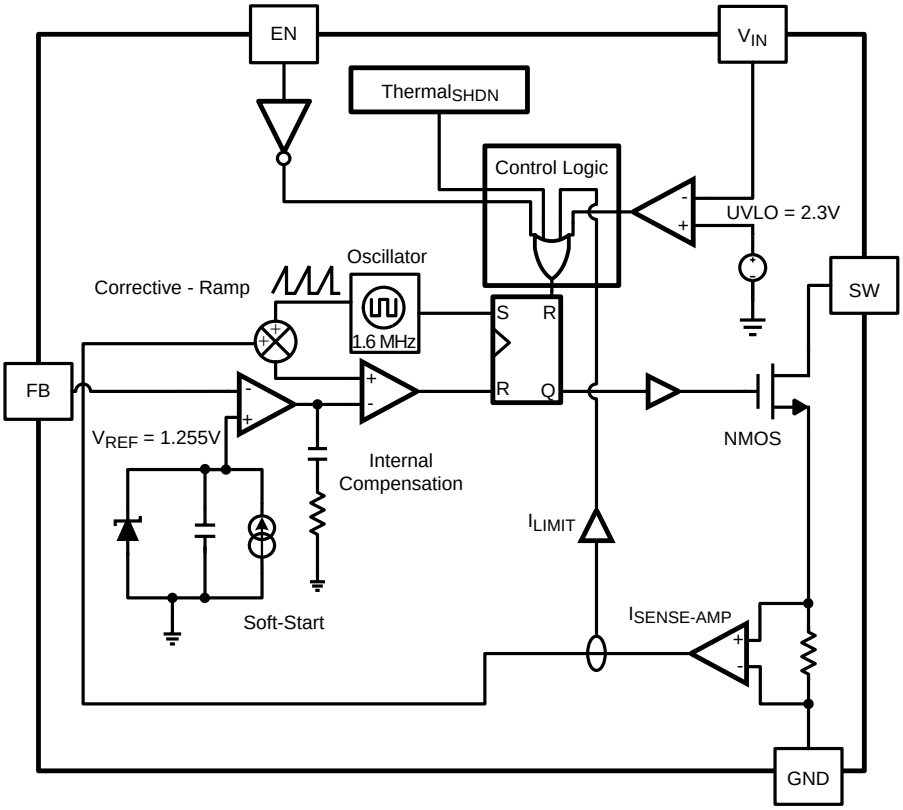


Figure 14. Typical Waveforms

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Limit

The LM2735-Q1 uses cycle-by-cycle current limiting to protect the internal NMOS switch. It is important to note that this current limit will not protect the output from excessive current during an output short circuit. The input supply is connected to the output by the series connection of an inductor and a diode. If a short circuit is placed on the output, excessive current can damage both the inductor and diode.

7.3.2 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 160°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 150°C.

7.3.3 Soft Start

This function forces V_{OUT} to increase at a controlled rate during start-up. During soft start, the reference voltage of the error amplifier ramps to its nominal value of 1.255 V in approximately 4 ms. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce inrush current.

7.3.4 Compensation

The LM2735-Q1 uses constant-frequency peak current mode control. This mode of control allows for a simple external compensation scheme that can be optimized for each application. A complicated mathematical analysis can be completed to fully explain the internal and external compensation of the LM2735-Q1, but for simplicity, a graphical approach with simple equations will be used. Below is a Gain and Phase plot of a LM2735-Q1 that produces a 12-V output from a 5-V input voltage. The Bode plot shows the total loop Gain and Phase without external compensation.

Feature Description (continued)

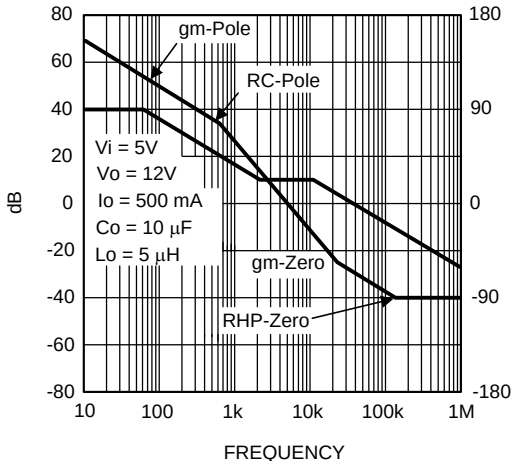


Figure 15. LM2735-Q1 Without External Compensation

One can see that the crossover frequency is fine, but the phase margin at 0 dB is very low (22°). A zero can be placed just above the crossover frequency so that the phase margin will be bumped up to a minimum of 45°. Below is the same application with a zero added at 8 kHz.

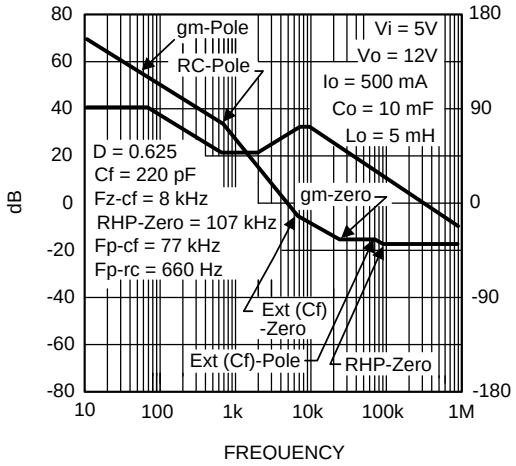


Figure 16. LM2735-Q1 With External Compensation

The simplest method to determine the compensation component value is as follows.

Set the output voltage with Equation 1.

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_1 \tag{1}$$

where

- R1 is the bottom resistor and R2 is the resistor tied to the output voltage.

The next step is to calculate the value of C3. The internal compensation has been designed so that when a zero is added from 5 kHz to 10 kHz, the converter will have good transient response with plenty of phase margin for all input and output voltage combinations.

$$F_{ZERO-CF} = \frac{1}{2\pi(R_2 \times C_f)} = 5\ \text{kHz} \rightarrow 10\ \text{kHz} \tag{2}$$

Feature Description (continued)

Lower output voltages will have the zero set closer to 10 kHz, and higher output voltages will usually have the zero set closer to 5 kHz. TI recommends obtaining a gain and phase plot for your actual application. See *Application and Implementation* to obtain examples of working applications and the associated component values.

Pole at origin due to internal GM amplifier:

$$F_{P\text{-}ORIGIN} \tag{3}$$

Pole due to output load and capacitor:

$$F_{P\text{-}RC} = \frac{1}{2\pi(R_{Load}C_{OUT})} \tag{4}$$

Equation 4 only determines the frequency of the pole for perfect current mode control (CMC). That is, it doesn't take into account the additional internal artificial ramp that is added to the current signal for stability reasons. Adding artificial ramp begins to move away from CMC to voltage mode control (VMC). The artifact is that the pole due to the output load, and output capacitor is actually slightly higher in frequency than calculated. In this example, it is calculated at 650 Hz, but in reality, it is around 1 kHz.

The zero created with capacitor C3 and resistor R2:

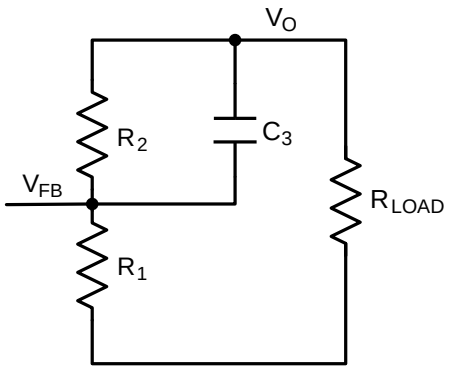


Figure 17. Setting External Pole-Zero

$$F_{ZERO\text{-}CF} = \frac{1}{2\pi(R_2 \times C_3)} \tag{5}$$

There is an associated pole with the zero that was created in Equation 5.

$$F_{POLE\text{-}CF} = \frac{1}{2\pi((R_1 \| R_2) \times C_3)} \tag{6}$$

It is always higher in frequency than the zero.

A right-half plane zero (RHPZ) is inherent to all boost converters. One must remember that the gain associated with a right-half plane zero increases at 20 dB per decade, but the phase decreases by 45° per decade. For most applications there is little concern with the RHPZ due to the fact that the frequency at which it shows up is well beyond crossover and has little to no effect on loop stability. One must be concerned with this condition for large inductor values and high output currents.

$$RHP_{ZERO} = \frac{(D')^2 R_{Load}}{2\pi \times L} \tag{7}$$

There are miscellaneous poles and zeros associated with parasitics internal to the LM2735-Q1, external components, and the PCB. They are located well over the crossover frequency, and for simplicity are not discussed.

7.4 Device Functional Modes

7.4.1 Enable Pin and Shutdown Mode

The LM2735-Q1 has a shutdown mode that is controlled by the Enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode and its quiescent current drops to typically 80 nA. Switch leakage adds up to another 1 µA from the input supply. The voltage at this pin should never exceed V_{IN} + 0.3 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device operates with input voltage in the range of 2.7 V to 5.5 V and provide regulated output voltage. This device is optimized for high-efficiency operation with minimum number of external components. For component selection, see *Detailed Design Procedure*.

8.2 Typical Applications

8.2.1 LM2735X-Q1 SOT-23 Design Example 1

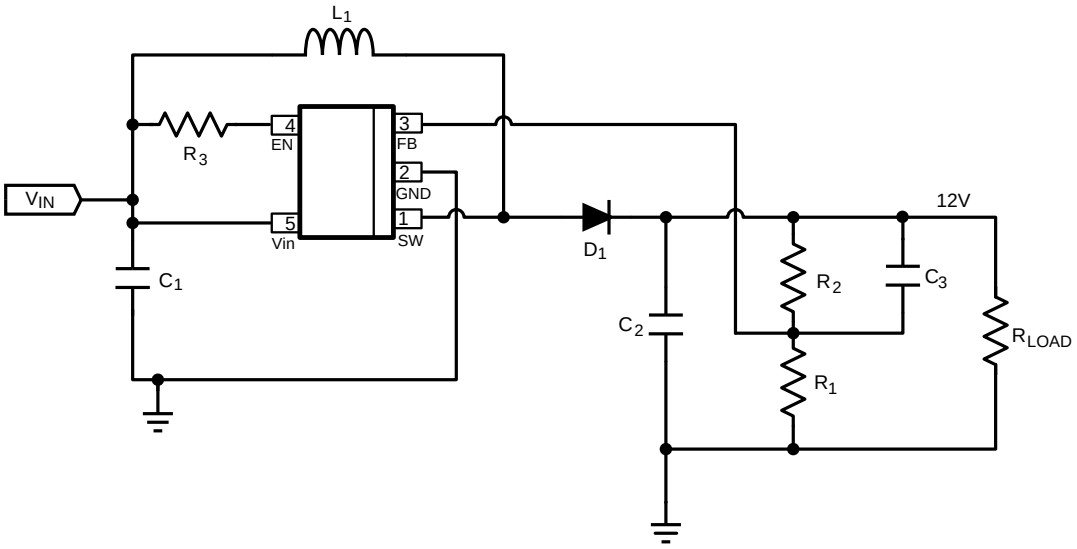


Figure 18. LM2735X-Q1 (1.6 MHz): V_{IN} = 5 V, V_{OUT} = 12 V at 350 mA

8.2.1.1 Design Requirements

The device must be able to operate at any voltage within input voltage range.

The load current needs to be defined in order to properly size the inductor, input capacitor, and output capacitor. The inductor must be able to handle full expected load current as well as the peak current generated during load transients and start-up. The inrush current at start-up depends on the output capacitor selection. More details are provided in *Detailed Design Procedure*.

The device has an enable pin (EN) that is used to enable and disable the device. This pin is active high and care should be taken that voltage on this pin does not exceed V_{IN} + 0.3 V.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM2735-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Table 1. Bill of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 Comp Capacitor	330 pF	TDK	C1608X5R1H331K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	15 µH 1.5 A	Coilcraft	MSS5131-153ML
R1	10.2 kΩ, 1%	Vishay	CRCW06031022F
R2	86.6 kΩ, 1%	Vishay	CRCW06038662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.1.2.2 Inductor Selection

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}):

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{1}{1-D}\right) = \frac{1}{D'} \tag{8}$$

Therefore:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{9}$$

Power losses due to the diode (D1) forward voltage drop, the voltage drop across the internal NMOS switch, the voltage drop across the inductor resistance (R_{DCR}), and switching losses must be included to calculate a more accurate duty cycle (see *Calculating Efficiency, and Junction Temperature* for a detailed explanation). A more accurate formula for calculating the conversion ratio is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\eta}{D'}$$

where

- η equals the efficiency of the LM2735-Q1 application. (10)

The inductor value determines the input ripple current. Lower inductor values decrease the size of the inductor, but increase the input ripple current. An increase in the inductor value decreases the input ripple current.

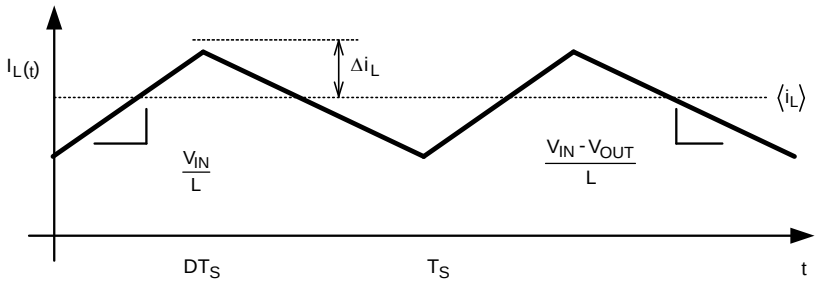


Figure 19. Inductor Current

$$\frac{2\Delta i_L}{DT_S} = \left(\frac{V_{IN}}{L}\right)$$

$$\Delta i_L = \left(\frac{V_{IN}}{2L}\right) x\, DT_S \tag{11}$$

A good design practice is to design the inductor to produce 10% to 30% ripple of maximum load. From the previous equations, the inductor value is then obtained.

$$L = \left(\frac{V_{IN}}{2 \times \Delta i_L}\right) x\, DT_S$$

where

- $1/T_S = F_{SW}$ = switching frequency (12)

Ensure that the minimum current limit (2.1 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$IL_{pk} = I_{IN} + \Delta I_L \tag{13}$$

or

$$IL_{pk} = I_{OUT} / D' + \Delta I_L \tag{14}$$

When selecting an inductor, make sure that it is capable of supporting the peak input current without saturating. Inductor saturation results in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum input current. For example, if the designed maximum input current is 1.5 A and the peak current is 1.75 A, then the inductor should be specified with a saturation current limit of >1.75 A. There is no need to specify the saturation or peak current of the inductor at the 3-A typical switch current-limit.

Because of the operating frequency of the LM2735-Q1, ferrite based inductors are preferred to minimize core losses. This presents little restriction since the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (DCR) provides better operating efficiency. For recommended inductors, see the following design examples.

8.2.1.2.3 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and equivalent series inductance (ESL). The recommended input capacitance is 10 µF to 44 µF, depending on the application. The capacitor manufacturer specifically states the input voltage rating. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. At the operating frequencies of the LM2735-Q1, certain capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) is higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Multilayer ceramic capacitors (MLCC) are good choices for both input and output capacitors and have very low ESL. For MLCCs, TI recommends using X7R or X5R dielectrics. Consult capacitor manufacturer datasheet to see how rated capacitance varies over operating conditions.

8.2.1.2.4 Output Capacitor

The LM2735-Q1 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output impedance therefore determines the maximum voltage perturbation. The output ripple of the converter is a function of the reactance of the capacitor and its equivalent series resistance (ESR):

$$\Delta V_{OUT} = \Delta I_L \times R_{ESR} + \left(\frac{V_{OUT} \times D}{2 \times F_{SW} \times R_{Load} \times C_{OUT}} \right) \quad (15)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action.

Given the availability and quality of MLCCs and the expected output voltage of designs using the LM2735-Q1, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high-frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasses this noise while a tantalum does not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications require a minimum at 4.7 µF of output capacitance. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

8.2.1.2.5 Setting the Output Voltage

The output voltage is set using the following equation where R1 is connected between the FB pin and GND, and R2 is connected between V_{OUT} and the FB pin.

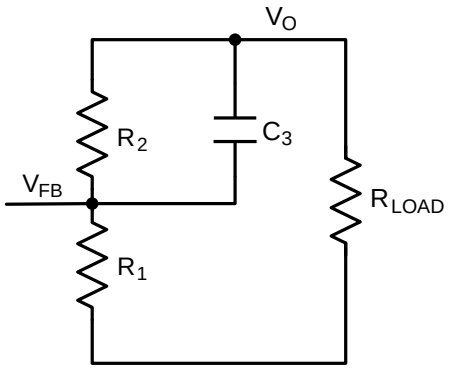
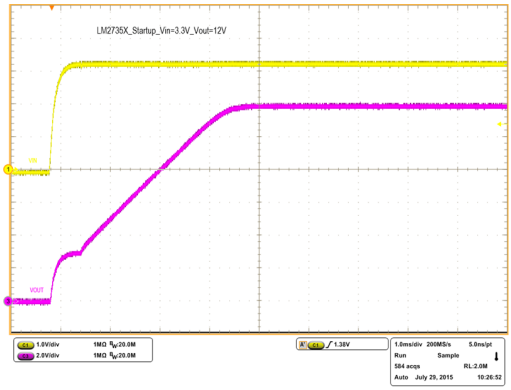


Figure 20. Setting V_{OUT}

A good value for R1 is 10 kΩ.

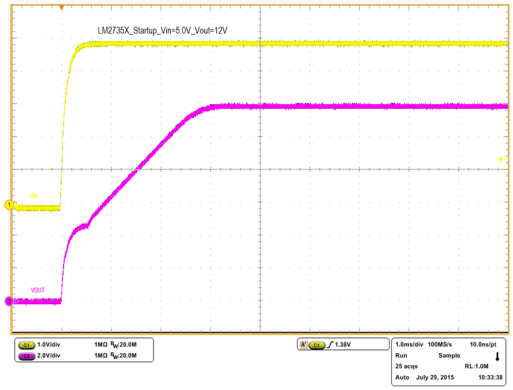
$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_1 \quad (16)$$

8.2.1.3 Application Curves



V_{IN} = 3.3 V V_{OUT} = 12 V

Figure 21. LM2735X-Q1 Typical Start-up Waveform



V_{IN} = 5 V V_{OUT} = 12 V

Figure 22. LM2735X-Q1 Typical Start-up Waveform

8.2.2 LM2735Y-Q1 SOT-23 Design Example 2

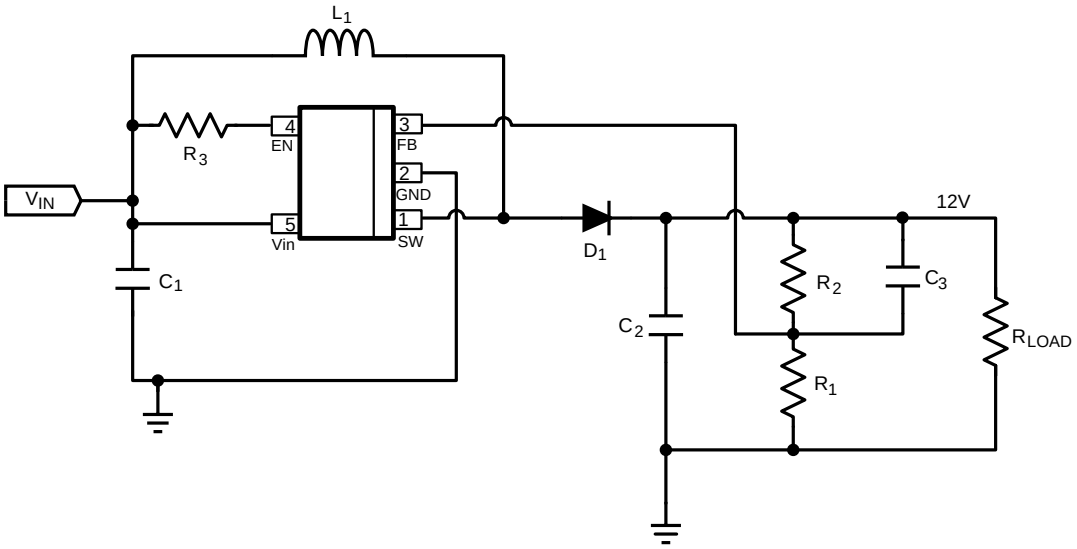


Figure 23. LM2735Y-Q1 (520 kHz): V_{IN} = 5 V, V_{OUT} = 12 V at 350 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YMF
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 Comp Capacitor	330 pF	TDK	C1608X5R1H331K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	33 µH 1.5 A	Coilcraft	DS3316P-333ML
R1	10.2 kΩ, 1%	Vishay	CRCW06031022F
R2	86.6 kΩ, 1%	Vishay	CRCW06038662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.3 LM2735X-Q1 WSON Design Example 3

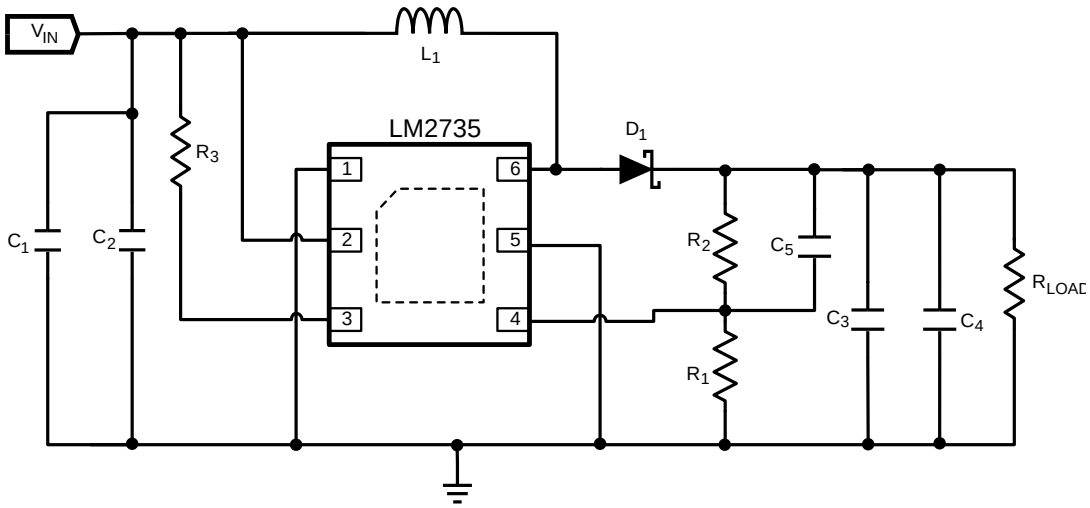


Figure 24. LM2735X-Q1 (1.6 MHz): V_{IN} = 3.3 V, V_{OUT} = 12 V at 350 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XSD
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Input Capacitor	No Load		
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C4 Output Capacitor	No Load		
C5 Comp Capacitor	330 pF	TDK	C1608X5R1H331K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	6.8 µH 2 A	Coilcraft	DO1813H-682ML
R1	10.2 kΩ, 1%	Vishay	CRCW06031022F
R2	86.6 kΩ, 1%	Vishay	CRCW06038662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.4 LM2735Y-Q1 WSON Design Example 4

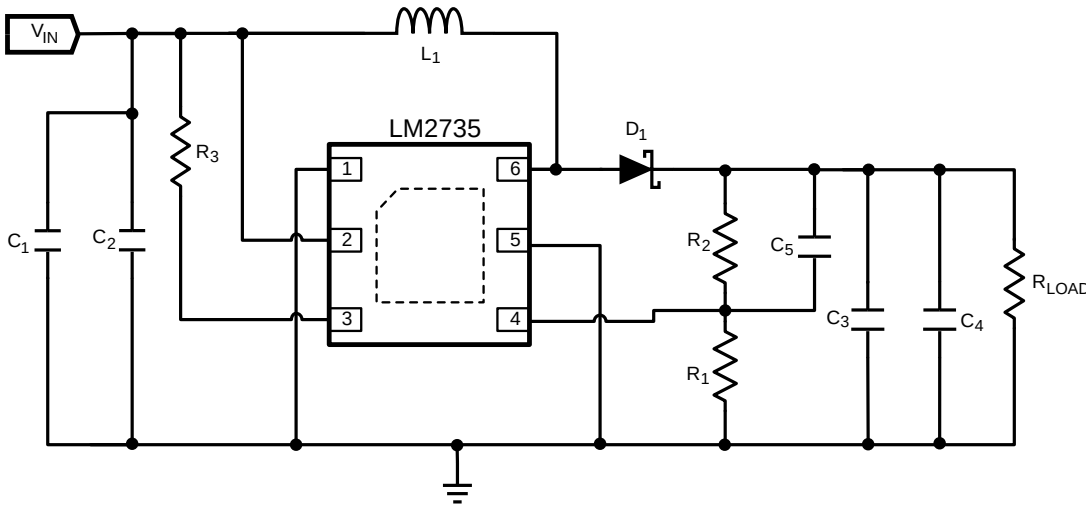


Figure 25. LM2735Y-Q1 (520 kHz): V_{IN} = 3.3 V, V_{OUT} = 12 V at 350 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YSD
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Input Capacitor	No Load		
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C4 Output Capacitor	No Load		
C5 Comp Capacitor	330 pF	TDK	C1608X5R1H331K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	15 µH 2 A	Coilcraft	MSS5131-153ML
R1	10.2 kΩ, 1%	Vishay	CRCW06031022F
R2	86.6 kΩ, 1%	Vishay	CRCW06038662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.5 LM2735X-Q1 SOT-23 Design Example 6

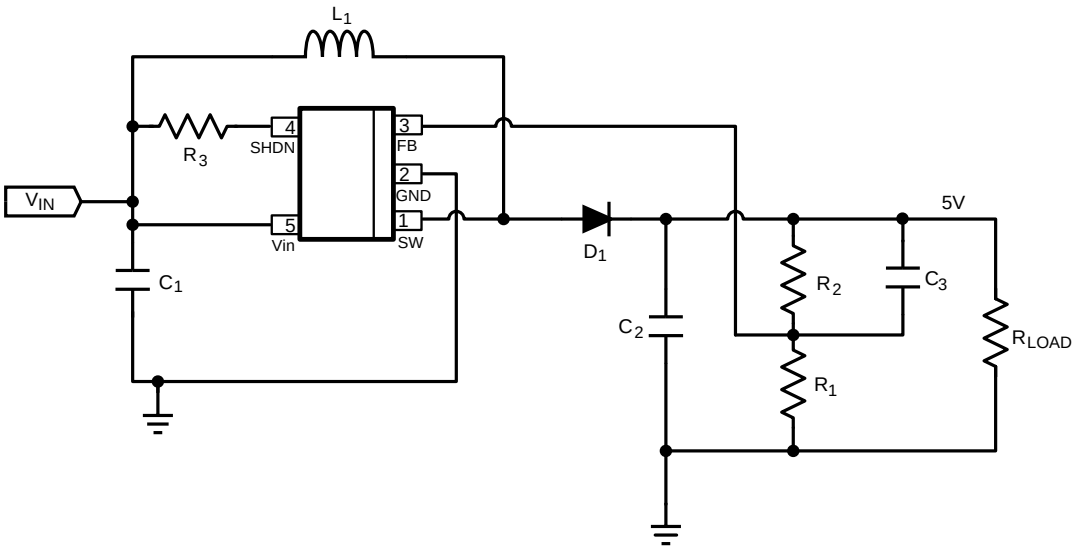


Figure 26. LM2735-Q1X (1.6 MHz): V_{IN} = 3 V, V_{OUT} = 5 V at 500 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1, Input Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C2, Output Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C3 Comp Capacitor	1000 pF	TDK	C1608X5R1H102K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	10 µH 1.2 A	Coilcraft	DO1608C-103ML
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F
R2	30.1 kΩ, 1%	Vishay	CRCW08053012F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.6 LM2735Y-Q1 SOT-23 Design Example 7

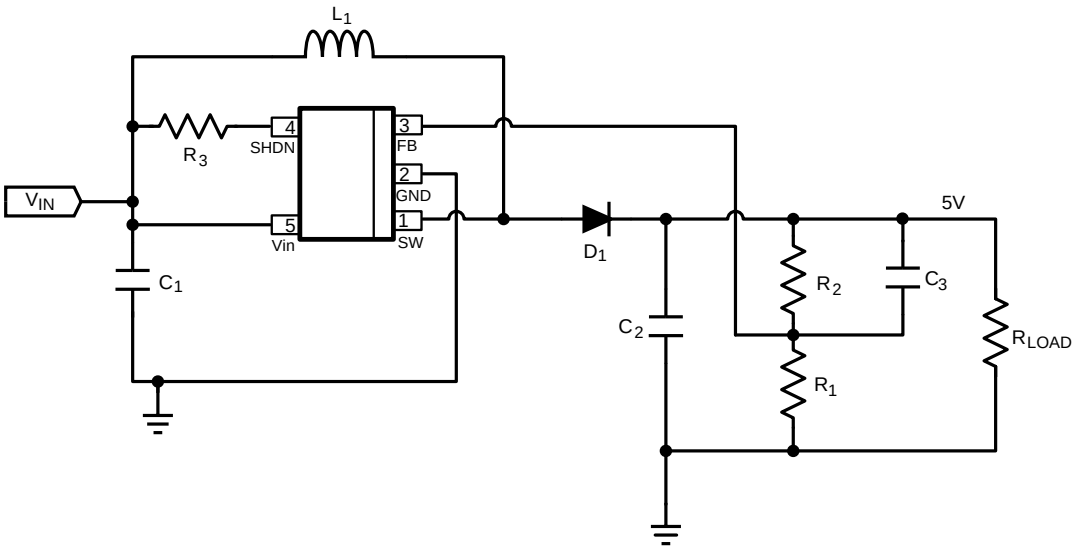


Figure 27. LM2735Y-Q1 (520 kHz): V_{IN} = 3 V, V_{OUT} = 5 V at 750 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YMF
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C3 Comp Capacitor	1000 pF	TDK	C1608X5R1H102K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	22 µH 1.2 A	Coilcraft	MSS5131-223ML
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F
R2	30.1 kΩ, 1%	Vishay	CRCW08053012F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.7 LM2735X-Q1 SOT-23 Design Example 8

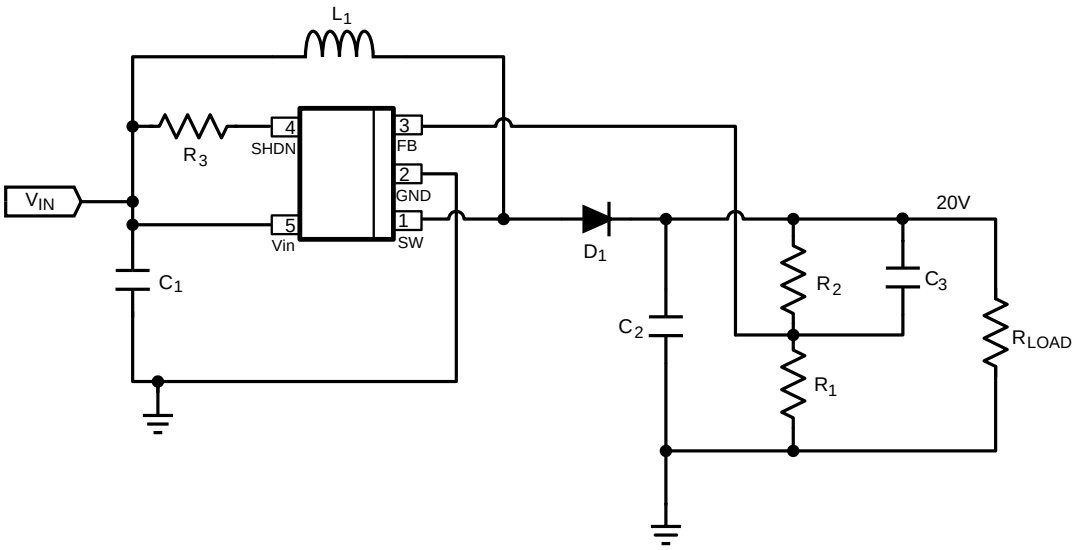


Figure 28. LM2735X-Q1 (1.6 MHz): V_{IN} = 3.3 V, V_{out} = 20 V at 100 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1, Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2, Output Capacitor	4.7 µF, 25 V, X5R	TDK	C3216X5R1E475K
C3 Comp Capacitor	470 pF	TDK	C1608X5R1H471K
D1, Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
L1	10 µH 1.2 A	Coilcraft	DO1608C-103ML
R1	10.0 kΩ, 1%	Vishay	CRCW06031002F
R2	150 kΩ, 1%	Vishay	CRCW06031503F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.8 LM2735Y-Q1 SOT-23 Design Example 9

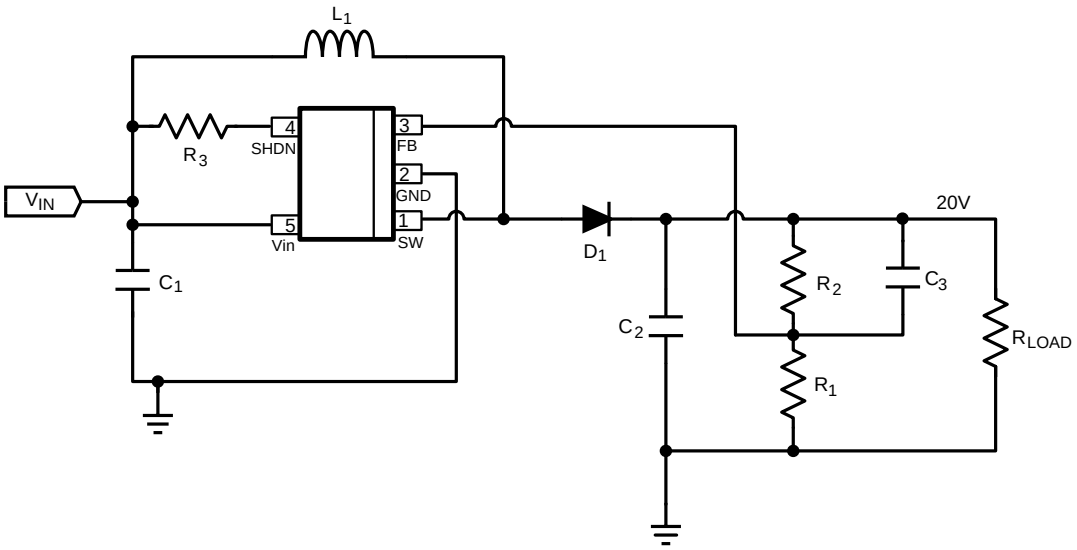


Figure 29. LM2735Y-Q1 (520 kHz): V_{IN} = 3.3 V, V_{OUT} = 20 V at 100 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YMF
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 Comp Capacitor	470 pF	TDK	C1608X5R1H471K
D1, Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
L1	33 µH 1.5 A	Coilcraft	DS3316P-333ML
R1	10.0 kΩ, 1%	Vishay	CRCW06031002F
R2	150.0 kΩ, 1%	Vishay	CRCW06031503F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.9 LM2735X-Q1 WSON Design Example 10

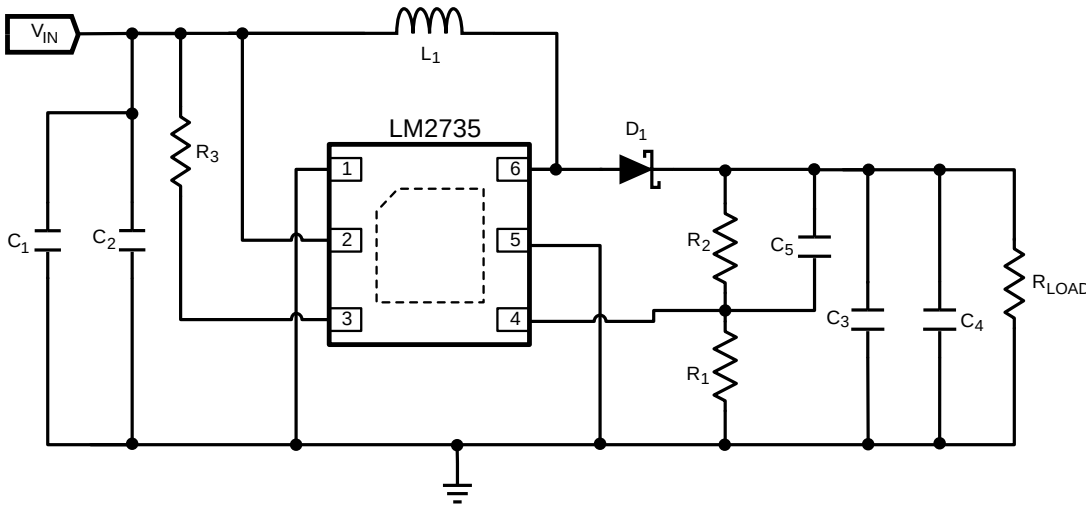


Figure 30. LM2735X-Q1 (1.6 MHz): V_{IN} = 3.3 V, V_{OUT} = 20 V at 150 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XSD
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C4 Output Capacitor	No Load		
C5 Comp Capacitor	470 pF	TDK	C1608X5R1H471K
D1, Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
L1	8.2 µH 2 A	Coilcraft	DO1813H-822ML
R1	10.0 kΩ, 1%	Vishay	CRCW06031002F
R2	150 kΩ, 1%	Vishay	CRCW06031503F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.10 LM2735Y-Q1 WSON Design Example 11

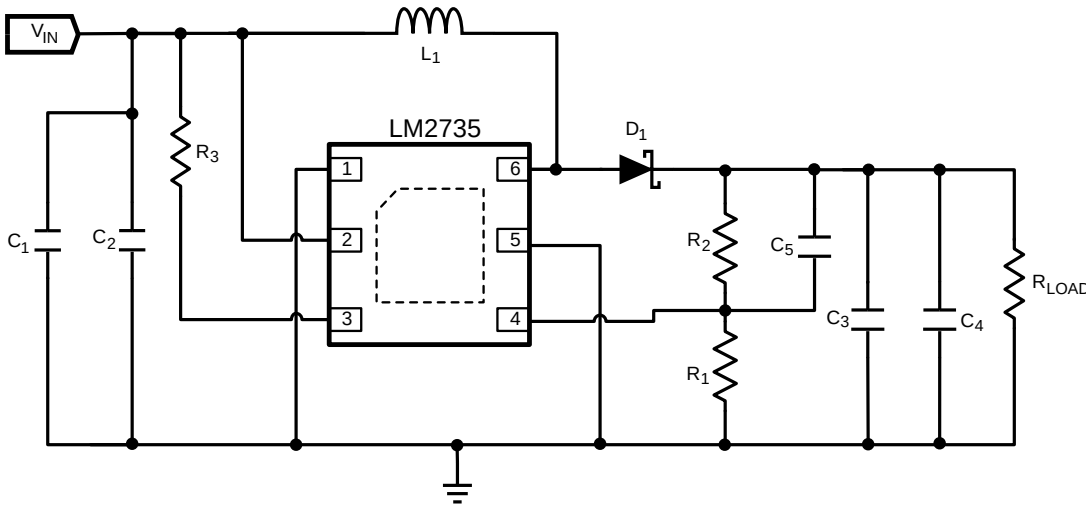


Figure 31. LM2735Y-Q1 (520 kHz): V_{IN} = 3.3 V, V_{OUT} = 20 V at 150 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YSD
C1 Input Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C2 Input Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C4 Output Capacitor	No Load		
C5 Comp Capacitor	470 pF	TDK	C1608X5R1H471K
D1, Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
L1	22 µH 1.5 A	Coilcraft	DS3316P-223ML
R1	10.0 kΩ, 1%	Vishay	CRCW06031002F
R2	150 kΩ, 1%	Vishay	CRCW06031503F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.11 LM2735X-Q1 WSON SEPIC Design Example 12

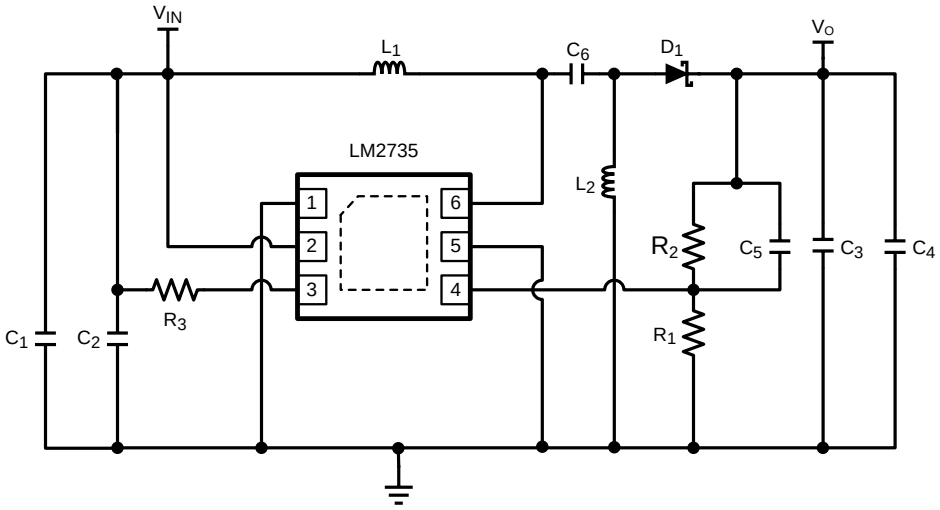


Figure 32. LM2735X-Q1 (1.6 MHz): V_{IN} = 2.7 V - 5 V, V_{OUT} = 3.3 V at 500 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XSD
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Input Capacitor	No Load		
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C4 Output Capacitor	No Load		
C5 Comp Capacitor	2200 pF	TDK	C1608X5R1H222K
C6	2.2 µF 16 V	TDK	C2012X5R1C225K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	6.8 µH	Coilcraft	DO1608C-682ML
L2	6.8 µH	Coilcraft	DO1608C-682ML
R1	10.2 kΩ, 1%	Vishay	CRCW06031002F
R2	16.5 kΩ, 1%	Vishay	CRCW06031652F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.12 LM2735X-Q1 SOT-23 LED Design Example 14

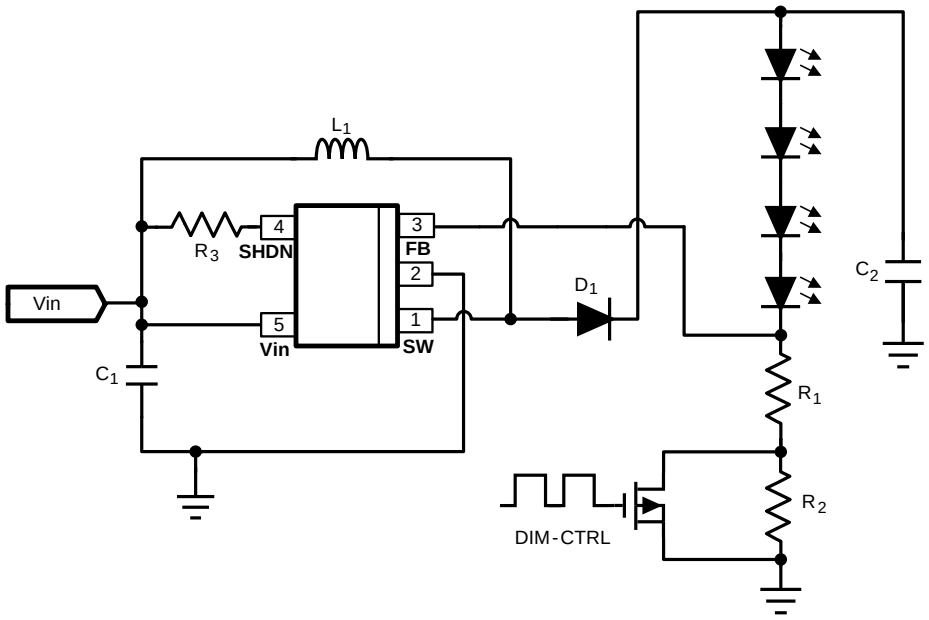


Figure 33. LM2735X-Q1 (1.6 MHz): V_{IN} = 2.7 V - 5 V, V_{OUT} = 20 V at 50 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	4.7 µF, 25 V, X5R	TDK	C3216JB1E475K
D1, Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
L1	15 µH 1.5 A	Coilcraft	MSS5131-153ML
R1	25.5 Ω, 1%	Vishay	CRCW080525R5F
R2	100 Ω, 1%	Vishay	CRCW08051000F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.13 LM2735Y-Q1 WSON FlyBack Design Example 15

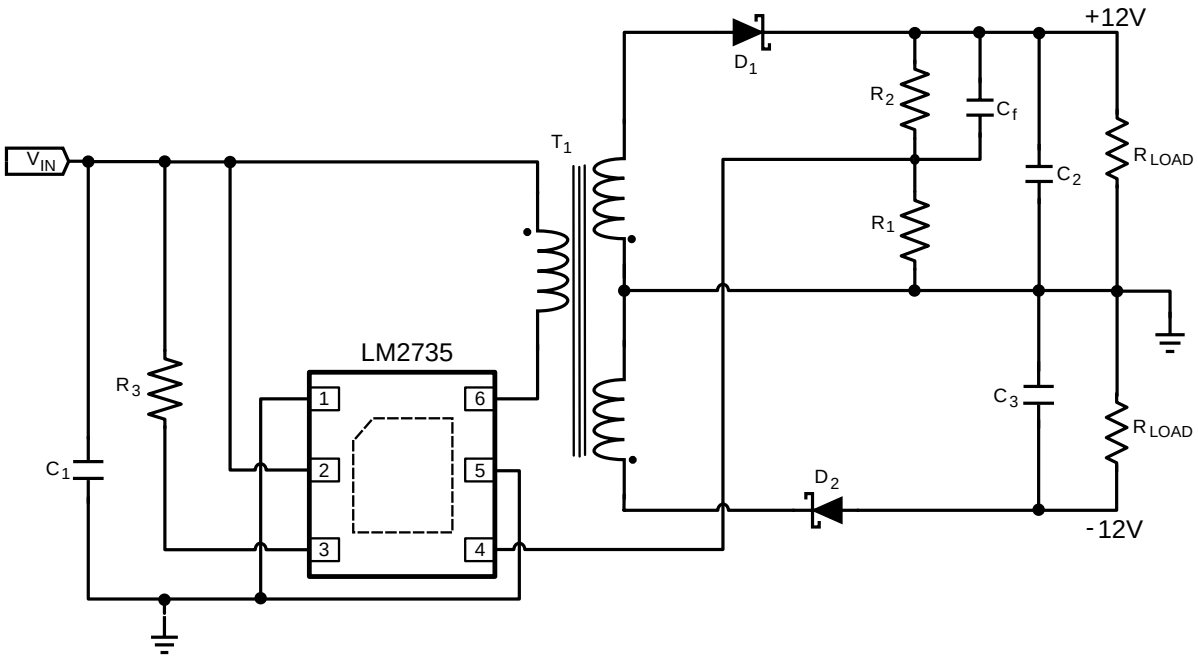


Figure 34. LM2735Y-Q1 (520 kHz): V_{IN} = 5 V, V_{OUT} = ±12 V 150 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1YSD
C1 Input Capacitor	22 µF, 6.3 V, X5R	TDK	C2012X5R0J226M
C2 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
Cf Comp Capacitor	330 pF	TDK	C1608X5R1H331K
D1, D2 Catch Diode	0.4 V_f Schottky 500 mA, 30 V_R	Vishay	MBR0530
T1			
R1	10.0 kΩ, 1%	Vishay	CRCW06031002F
R2	86.6 kΩ, 1%	Vishay	CRCW06038662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.14 LM2735X-Q1 SOT-23 LED Design Example 16 V_{RAIL} > 5.5 V Application

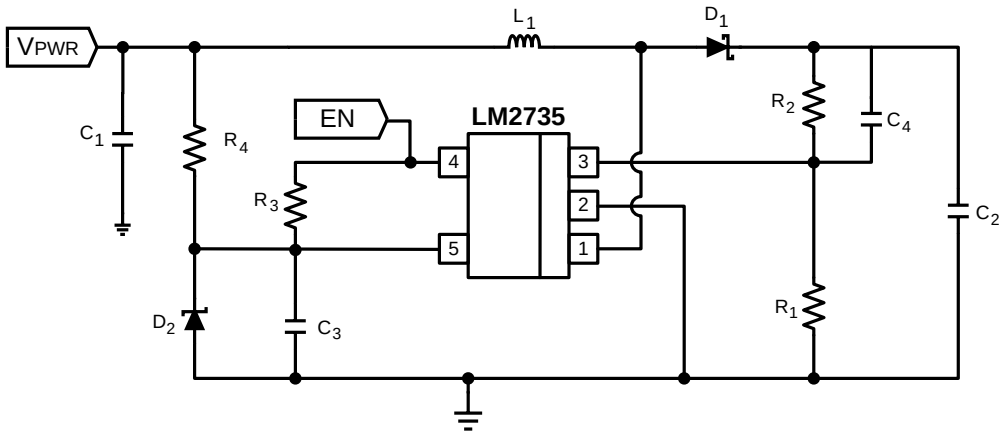


Figure 35. LM2735X-Q1 (1.6 MHz): V_{PWR} = 9 V, V_{OUT} = 12 V at 500 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1, Input Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C2, Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 V_{IN} Cap	0.1 µF, 6.3 V, X5R	TDK	C2012X5R0J104K
C4 Comp Capacitor	1000 pF	TDK	C1608X5R1H102K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
D2	3.3-V Zener, SOT-23	Diodes Inc	BZX84C3V3
L1	6.8 µH 2 A	Coilcraft	DO1813H-682ML
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F
R2	86.6 kΩ, 1%	Vishay	CRCW08058662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F
R4	499 Ω, 1%	Vishay	CRCW06034991F

8.2.15 LM2735X-Q1 SOT-23 LED Design Example 17 Two-Input Voltage Rail Application

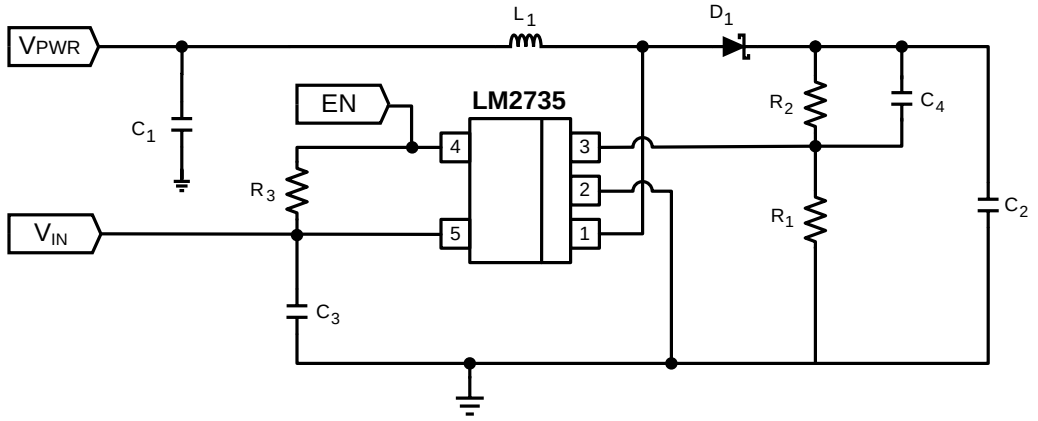


Figure 36. LM2735X-Q1 (1.6 MHz): V_{PWR} = 9 V_{IN}= 2.7 V - 5.5 V, V_{OUT} = 12 V at 500 mA

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2.1-A Boost Regulator	TI	LM2735-Q1XMF
C1, Input Capacitor	10 µF, 6.3 V, X5R	TDK	C2012X5R0J106K
C2, Output Capacitor	10 µF, 25 V, X5R	TDK	C3216X5R1E106M
C3 V_{IN} Capacitor	0.1 µF, 6.3 V, X5R	TDK	C2012X5R0J104K
C4 Comp Capacitor	1000 pF	TDK	C1608X5R1H102K
D1, Catch Diode	0.4 V_f Schottky 1 A, 20 V_R	ST	STPS120M
L1	6.8 µH 2 A	Coilcraft	DO1813H-682ML
R1	10.0 kΩ, 1%	Vishay	CRCW08051002F
R2	86.6 kΩ, 1%	Vishay	CRCW08058662F
R3	100 kΩ, 1%	Vishay	CRCW06031003F

8.2.16 SEPIC Converter

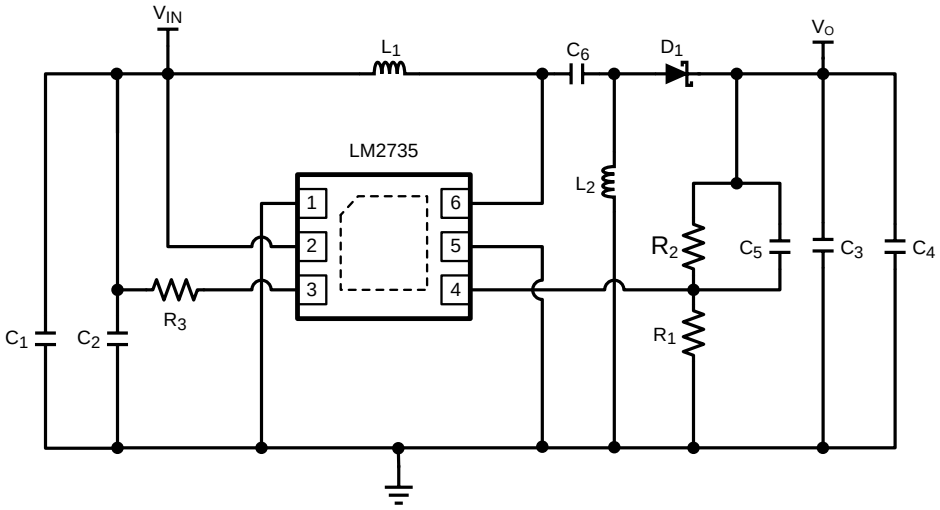


Figure 37. SEPIC Converter Schematic

8.2.16.1 Detailed Design Procedure

The LM2735-Q1 can easily be converted into a SEPIC converter. A SEPIC converter has the ability to regulate an output voltage that is either larger or smaller in magnitude than the input voltage. Other converters have this ability as well (CUK and buck-boost), but usually create an output voltage that is opposite in polarity to the input voltage. This topology is a perfect fit for Lithium Ion battery applications where the input voltage for a single-cell Li-Ion battery varies from 3 V to 4.5 V, and the output voltage is somewhere in between. Most of the analysis of the LM2735-Q1 boost converter is applicable to the LM2735-Q1 SEPIC converter.

8.2.16.1.1 SEPIC Design Guide

SEPIC Conversion ratio without loss elements:

$$\frac{V_o}{V_{IN}} = \frac{D}{D'} \tag{17}$$

Therefore:

$$D = \frac{V_O}{V_O + V_{IN}} \tag{18}$$

8.2.16.1.2 Small Ripple Approximation

In a well-designed SEPIC converter, the output voltage, input voltage ripple, and inductor ripple is small in comparison to the DC magnitude. Therefore, it is a safe approximation to assume a DC value for these components. The main objective of the Steady State Analysis is to determine the steady state duty-cycle, voltage and current stresses on all components, and proper values for all components.

In a steady-state converter, the net volt-seconds across an inductor after one cycle equals zero. Also, the charge into a capacitor equals the charge out of a capacitor in one cycle.

Therefore:

$$I_{L2} = \left(\frac{D}{D'}\right) \times I_{L1}$$

and

$$I_{L1} = \left(\frac{D}{D'}\right) X \left(\frac{V_O}{R}\right) \tag{19}$$

Substituting I_{L1} into I_{L2}

$$I_{L2} = \frac{V_O}{R} \tag{20}$$

The average inductor current of L2 is the average output load.

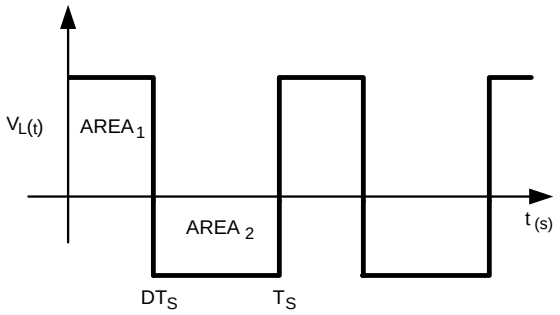


Figure 38. Inductor Volt-Sec Balance Waveform

Applying charge balance on C1:

$$V_{C1} = \frac{D^{'}(V_0)}{D} \tag{21}$$

Since there are no DC voltages across either inductor, and capacitor C6 is connected to V_{IN} through L1 at one end, or to ground through L2 on the other end, we can say that

$$V_{C1} = V_{IN} \tag{22}$$

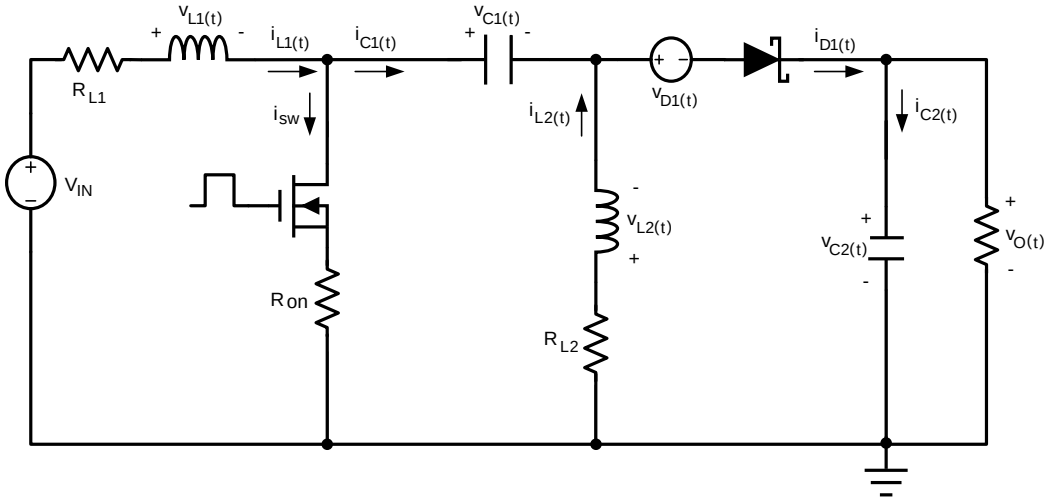
Therefore:

$$V_{IN} = \frac{D^{'}(V_0)}{D} \tag{23}$$

This verifies the original conversion ratio equation.

It is important to remember that the internal switch current is equal to I_{L1} and I_{L2}. During the D interval. Design the converter so that the minimum specified peak switch current limit (2.1 A) is not exceeded.

8.2.16.1.3 Steady State Analysis With Loss Elements



Using inductor volt-second balance and capacitor charge balance, the following equations are derived:

$$I_{L2} = \left(\frac{V_O}{R}\right)$$

and

$$I_{L1} = \left(\frac{V_O}{R}\right) X \left(\frac{D}{D'}\right) \quad (24)$$

$$\frac{V_o}{V_{IN}} = \left(\frac{D}{D'}\right)\left(\frac{1}{\left(1+\frac{V_D}{V_O}+\frac{R_{L2}}{R}\right)+\left(\frac{D}{D'^2}\right)\left(\frac{R_{ON}}{R}\right)+\left(\frac{D^2}{D'^2}\right)\left(\frac{R_{L1}}{R}\right)}\right) \quad (25)$$

Therefore:

$$\eta = \left(\frac{1}{\left(1+\frac{V_D}{V_O}+\frac{R_{L2}}{R}\right)+\left(\frac{D}{D'^2}\right)\left(\frac{R_{ON}}{R}\right)+\left(\frac{D^2}{D'^2}\right)\left(\frac{R_{L1}}{R}\right)}\right) \quad (26)$$

One can see that all variables are known except for the duty cycle (D). A quadratic equation is needed to solve for D. A less accurate method of determining the duty cycle is to assume efficiency, and calculate the duty cycle.

$$\frac{V_O}{V_{IN}} = \left(\frac{D}{1 - D}\right) x\, \eta \quad (27)$$

$$D = \left(\frac{V_O}{(V_{IN} x\, \eta) + V_O}\right) \quad (28)$$

Vin	2.7V
Vo	3.1V
Iin	770 mA
Io	500 mA
η	75%

Vin	3.3V
Vo	3.1V
Iin	600 mA
Io	500 mA
η	80%

Vin	5V
Vo	3.1V
Iin	375 mA
Io	500 mA
η	83%

Figure 39. Efficiencies for Typical SEPIC Application

9 Power Supply Recommendations

The LM2735-Q1 device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 2.7 V. In case where input supply is located farther away (more than a few inches) from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

When planning layout, there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing a boost converter layout is the close coupling of the GND connections of the C_{OUT} capacitor and the LM2735-Q1 PGND pin. The GND ends should be close to one another and be connected to the GND plane with at least two through-holes. There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. Place the feedback resistors as close as possible to the IC, with the AGND of R1 placed as close as possible to the GND (pin 5 for the WSON) of the IC. The V_{OUT} trace to R2 should be routed away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components should also be placed as close as possible to the IC. See Application Note *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines*for further considerations and the LM2735-Q1 demo board as an example of a 4-layer layout.

Below is an example of a good thermal and electrical PCB design. This is very similar to TI's LM2735-Q1 demonstration boards that are obtainable through the TI website. The demonstration board consists of a 2-layer PCB with a common input and output voltage application. Most of the routing is on the top layer, with the bottom layer consisting of a large ground plane. The placement of the external components satisfies the electrical considerations, and the thermal performance has been improved by adding thermal vias and a top layer *Dog-Bone*.

10.1.1 WSON Package

The LM2735-Q1 packaged in the 6–pin WSON:

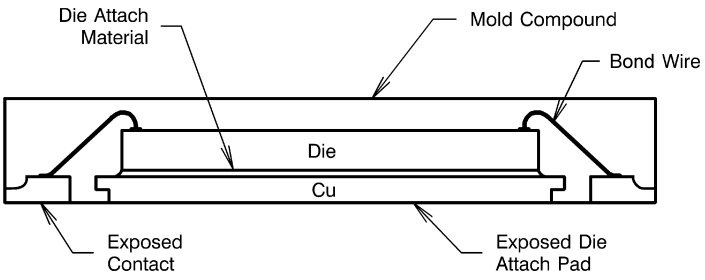


Figure 40. Internal WSON Connection

For certain high power applications, the PCB land may be modified to a *dog bone* shape (see Figure 41). Increasing the size of ground plane, and adding thermal vias can reduce the $R_{\theta JA}$ for the application.

Layout Guidelines (continued)

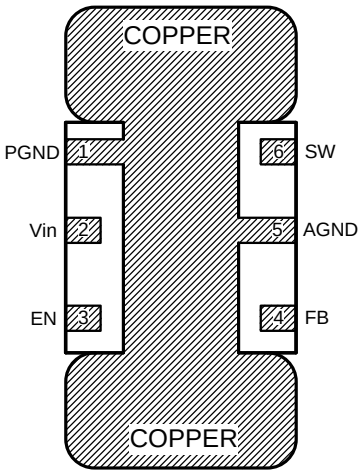


Figure 41. PCB Dog Bone Layout

10.2 Layout Examples

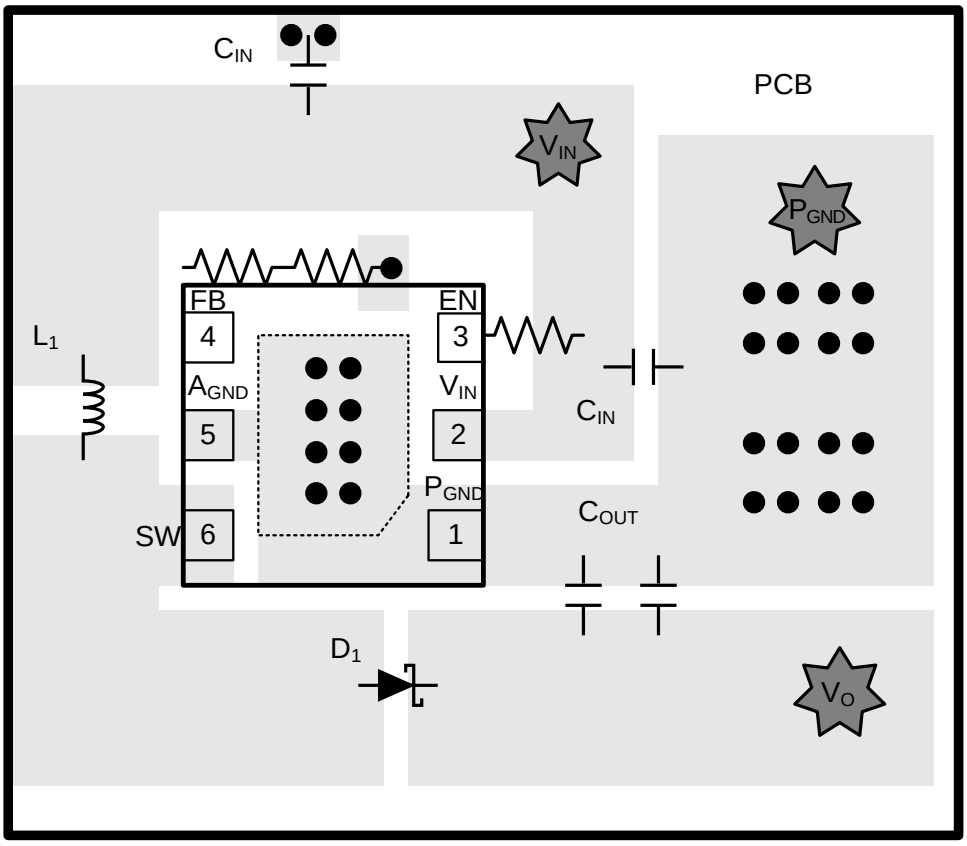


Figure 42. Example of Proper PCB Layout

Layout Examples (continued)

The layout guidelines described for the LM2735-Q1 Boost-Converter are applicable to the SEPIC Converter. Figure 43 shows a proper PCB layout for a SEPIC Converter.

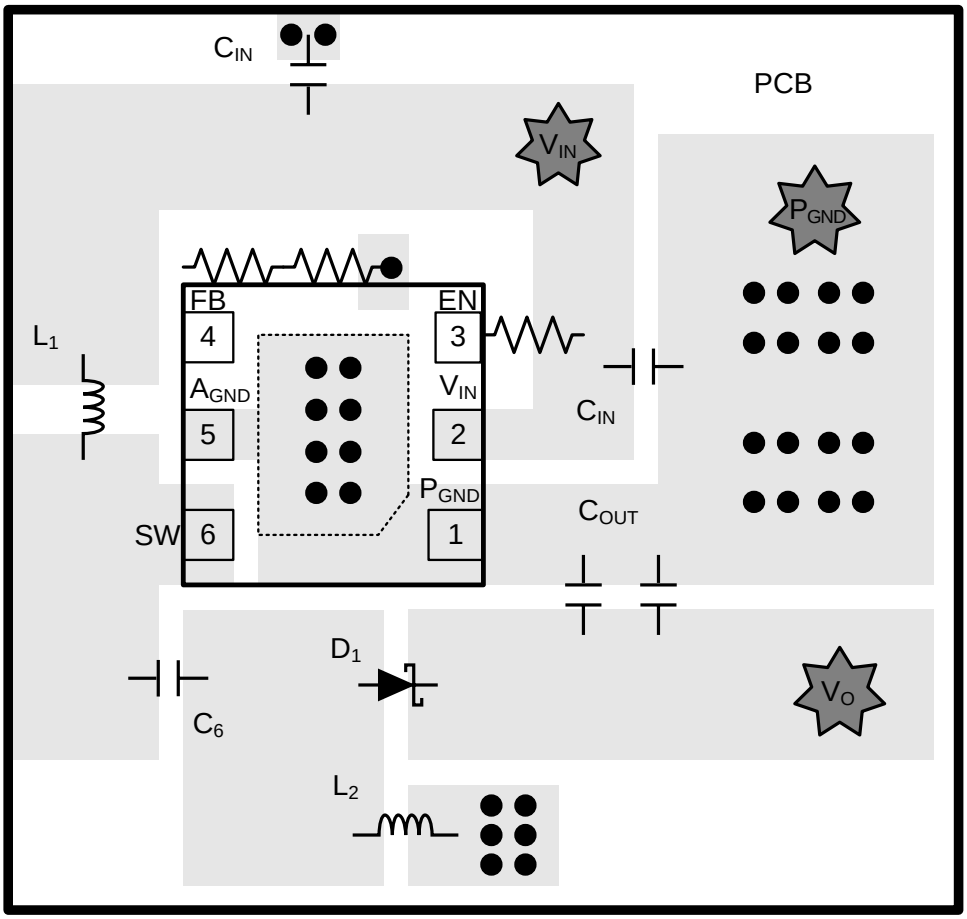


Figure 43. SEPIC PCB Layout

10.3 Thermal Considerations

When designing for thermal performance, one must consider many variables:

- Ambient temperature: The surrounding maximum air temperature is fairly explanatory. As the temperature increases, the junction temperature increases. This may not be linear though. As the surrounding air temperature increases, resistances of semiconductors, wires and traces increase. This decreases the efficiency of the application, and more power is converted into heat, increasing the silicon junction temperatures further.
- Forced airflow: Forced air can drastically reduce the device junction temperature. Air flow reduces the hot spots within a design. Warm airflow is often much better than a lower ambient temperature with no airflow.
- External components: Choose components that are efficient, and you can reduce the mutual heating between devices.

Thermal Considerations (continued)

10.3.1 Definitions

Heat energy is transferred from regions of high temperature to regions of low temperature through three basic mechanisms: radiation, conduction and convection.

Radiation Electromagnetic transfer of heat between masses at different temperatures.

Conduction Transfer of heat through a solid medium.

Convection Transfer of heat through the medium of a fluid; typically air.

Conduction & Convection will be the dominant heat transfer mechanism in most applications.

$R_{\theta JC}$ Thermal impedance from silicon junction to device case temperature.

$R_{\theta JA}$ Thermal impedance from silicon junction to ambient air temperature.

$C_{\theta JC}$ Thermal Delay from silicon junction to device case temperature.

$C_{\theta CA}$ Thermal Delay from device case to ambient air temperature.

$R_{\theta JA}$ & $R_{\theta JC}$ These two symbols represent thermal impedances, and most data sheets contain associated values for these two symbols. The units of measurement are °C/Watt.

$R_{\theta JA}$is the sum of smaller thermal impedances (see Figure 44). The capacitors represent delays that are present from the time that power and its associated heat is increased or decreased from steady state in one medium until the time that the heat increase or decrease reaches steady state on the another medium.

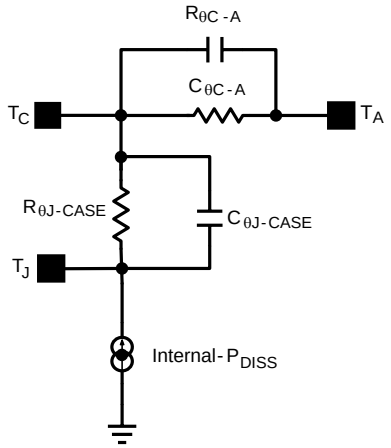


Figure 44. Simplified Thermal Impedance Model

The datasheet values for these symbols are given so that one might compare the thermal performance of one package against another. In order to achieve a comparison between packages, all other variables must be held constant in the comparison (PCB size, copper weight, thermal vias, power dissipation, V_{IN}, V_{OUT}, Load Current, and so forth). This does shed light on the package performance, but it would be a mistake to use these values to calculate the actual junction temperature in your application.

$$R_{\theta JA} = \frac{T_J - T_A}{P_{Dissipation}} \tag{29}$$

Calculation of the variables of Equation 29 is discussed later, as well as how to eventually calculate a proper junction temperature with relative certainty. The following defines the process of calculating the junction temperature and clarify some common misconceptions.

Thermal Considerations (continued)

$R_{\theta JA}$ [Variables]:

- Input voltage, output voltage, output current, RDSon.
- Ambient temperature and air flow.
- Internal and external components power dissipation.
- Package thermal limitations.
- PCB variables (copper weight, thermal vias, layers component placement).

It is incorrect to assume that the top case temperature is the proper temperature when calculating $R_{\theta JC}$ value. The $R_{\theta JC}$ value represents the thermal impedance of all six sides of a package, not just the top side. This document refers to a thermal impedance called $R_{\psi JC}$. $R_{\psi JC}$ represents a thermal impedance associated with just the top case temperature. This allows calculation of the junction temperature with a thermal sensor connected to the top case.

10.3.2 PCB Design With Thermal Performance in Mind

The PCB design is a very important step in the thermal design procedure. The LM2735-Q1 is available in 2 package options (5-pin SOT-23 and 6-pin WSON). The options are electrically the same, but difference between the packages is size and thermal performance. The WSON has thermal die attach pads (DAP) attached to the bottom of the packages, and are therefore capable of dissipating more heat than the SOT-23 package. It is important that the correct package for the application is chosen. A detailed thermal design procedure has been included in this data sheet. This procedure helps determine which package is correct, and common applications are analyzed.

There is one significant thermal PCB layout design consideration that contradicts a proper electrical PCB layout design consideration. This contradiction is the placement of external components that dissipate heat. The greatest external heat contributor is the external Schottky diode. It would be ideal to be able to separate by distance the LM2735-Q1 from the Schottky diode, and thereby reducing the mutual heating effect, however, this creates electrical performance issues. It is important to keep the LM2735-Q1, the output capacitor, and Schottky diode physically close to each other (see Figure 42). The electrical design considerations outweigh the thermal considerations. Other factors that influence thermal performance are thermal vias, copper weight, and number of board layers.

10.3.3 LM2735-Q1 Thermal Models

Heat is dissipated from the LM2735-Q1 and other devices. The external loss elements include the Schottky diode, inductor, and loads. All loss elements mutually increase the heat on the PCB, and therefore increase each other's temperatures.

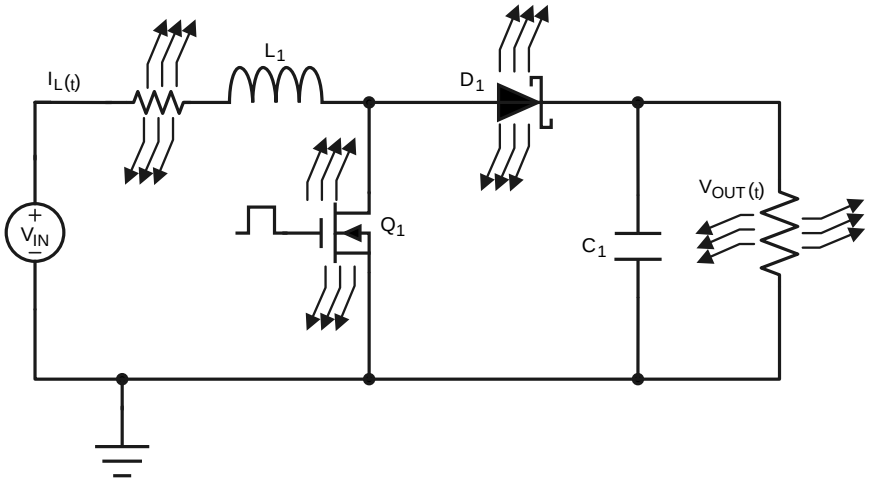


Figure 45. Thermal Schematic

Thermal Considerations (continued)

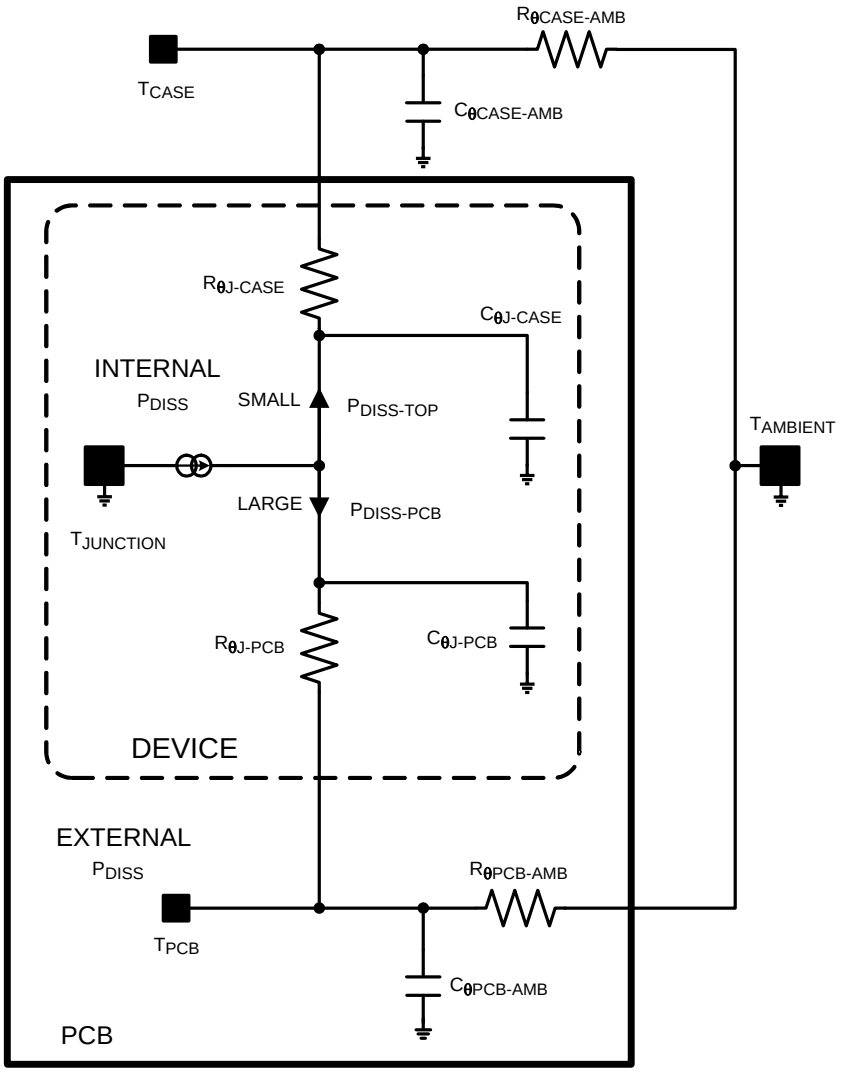


Figure 46. Associated Thermal Model

10.3.4 Calculating Efficiency, and Junction Temperature

The complete LM2735-Q1 DC/DC converter efficiency (η) can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}}$$

or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (30)$$

Power loss (P_{LOSS}) is the sum of two types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads.

Losses in the LM2735-Q1 device:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (31)$$

Thermal Considerations (continued)

Conversion ratio of the boost converter with conduction loss elements inserted:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{D'}\left(1 - \frac{D' \times V_D}{V_{IN}}\right)\left(\frac{1}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}}\right) \quad (32)$$

If the loss elements are reduced to zero, the conversion ratio simplifies to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{D'} \quad (33)$$

And this is known:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\eta}{D'} \quad (34)$$

Therefore:

$$\eta = D' \frac{V_{OUT}}{V_{IN}} = \left(\frac{1 - \frac{D' \times V_D}{V_{IN}}}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}}\right) \quad (35)$$

Calculations for determining the most significant power losses are discussed below. Other losses totaling less than 2% are not discussed.

A simple efficiency calculation that takes into account the conduction losses is shown below:

$$\eta \approx \left(\frac{1 - \frac{D' \times V_D}{V_{IN}}}{1 + \frac{R_{DCR} + (D \times R_{DSON})}{D'^2 R_{OUT}}}\right) \quad (36)$$

The diode, NMOS switch, and inductor DCR losses are included in this calculation. Setting any loss element to zero simplifies the equation.

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the manufacturer's *Electrical Characteristics* section of the data sheet.

The conduction losses in the diode are calculated as follows:

$$P_{DIODE} = V_D \times I_O \quad (37)$$

Depending on the duty cycle, this can be the single most significant power loss in the circuit. Take care to choose a diode that has a low forward voltage drop. Another concern with diode selection is reverse leakage current. Depending on the ambient temperature and the reverse voltage across the diode, the current being drawn from the output to the NMOS switch during time D could be significant, this may increase losses internal to the LM2735-Q1 and reduce the overall efficiency of the application. See the data sheets of the Schottky diode manufacturer for reverse leakage specifications; and, typical applications within this data sheet for diode selections.

Another significant external power loss is the conduction loss in the input inductor. The power loss within the inductor can be simplified to:

$$P_{IND} = I_{IN}^2 R_{DCR} \quad (38)$$

$$P_{IND} = \left(\frac{I_O^2 R_{DCR}}{D'}\right) \quad (39)$$

Thermal Considerations (continued)

The LM2735-Q1 conduction loss is mainly associated with the internal NFET:

$$P_{COND\text{-}NFET} = I^2_{SW\text{-}rms} \times R_{DSON} \times D \quad (40)$$

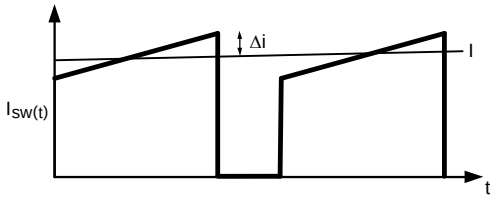


Figure 47. LM2735-Q1 Switch Current

$$Isw\text{-}rms = I_{IND}\sqrt{D} \times \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I_{IND}}\right)^2} \approx I_{IND}\sqrt{D}$$

$$P_{IND} = I_{IN}^2 \times R_{IND\text{-}DCR}$$

(small ripple approximation) (41)

$$P_{COND\text{-}NFET} = I_{IN}^2 \times R_{DSON} \times D \quad (42)$$

$$P_{COND\text{-}NFET} = \left(\frac{I_O}{D'}\right)^2 \times R_{DSON} \times D \quad (43)$$

The value for should be equal to the resistance at the junction temperature you wish to analyze. As an example, at 125°C and V_{IN} = 5 V, R_{DSON} = 250 mΩ (see *Typical Characteristics* for value).

Switching losses are also associated with the internal NMOS switch. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss.

The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node:

$$P_{SWR} = 1/2(V_{OUT} \times I_{IN} \times F_{SW} \times T_{RISE}) \quad (44)$$

$$P_{SWF} = 1/2(V_{OUT} \times I_{IN} \times F_{SW} \times T_{FALL}) \quad (45)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (46)$$

Table 2. Typical Switch-Node Rise and Fall Times

V_{IN}	V_{OUT}	T_{RISE}	T_{FALL}
3 V	5 V	6 nS	4 nS
5 V	12 V	6 nS	5 nS
3 V	12 V	7 nS	5 nS
5 V	18 V	7 nS	5 nS

Quiescent power losses: I_Q is the quiescent operating current, and is typically around 4 mA

$$P_Q = I_Q \times V_{IN} \quad (47)$$

10.3.4.1 Example Efficiency Calculation

Table 3. Operating Conditions

PARAMETER	VALUE
V_{IN}	5 V
V_{OUT}	12 V
I_{OUT}	500 mA
V_D	0.4 V
F_{SW}	1.60 MHz
I_Q	4 mA
T_{RISE}	6 nS
T_{FALL}	5 nS
R_{DSon}	250 mΩ
R_{DCR}	50 mΩ
D	0.64
I_{IN}	1.4 A

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS} \quad (48)$$

Quiescent Power Losses:

$$P_Q = I_Q \times V_{IN} = 20 \text{ mW} \quad (49)$$

Switching Power Losses:

$$P_{SWR} = 1/2(V_{OUT} \times I_{IN} \times F_{SW} \times T_{RISE}) \cong 6 \text{ ns} \cong 80 \text{ mW} \quad (50)$$

$$P_{SWF} = 1/2(V_{OUT} \times I_{IN} \times F_{SW} \times T_{FALL}) \cong 5 \text{ ns} \cong 70 \text{ mW} \quad (51)$$

$$P_{SW} = P_{SWR} + P_{SWF} = 150 \text{ mW} \quad (52)$$

Internal NFET Power Losses:

$$R_{DSON} = 250 \text{ m}\Omega \quad (53)$$

$$P_{CONDUCTION} = I_{IN}^2 \times D \times R_{DSON} \times 305 \text{ mW} \quad (54)$$

Diode Losses:

$$V_D = 0.45 \text{ V} \quad (55)$$

$$P_{DIODE} = V_D \times I_{IN}(1–D) = 236 \text{ mW} \quad (56)$$

Inductor Power Losses:

$$R_{DCR} = 75 \text{ m}\Omega \quad (57)$$

$$P_{IND} = I_{IN}^2 \times R_{DCR} = 145 \text{ mW} \quad (58)$$

Total Power Losses are:

Table 4. Power Loss Tabulation

PARAMETER	VALUE	PARAMETER	VALUE
V_{IN}	5 V		
V_{OUT}	12 V		
I_{OUT}	500 mA	**POUT**	6 W
V_D	0.4 V	**PDIODE**	236 mW
F_{SW}	1.6 MHz		
T_{RISE}	6 nS	**PSWR**	80 mW
T_{FALL}	5 nS	**PSWF**	70 mW
I_Q	4 mA	**PQ**	20 mW
R_{DSon}	250 mΩ	**PCOND**	305 mW
R_{DCR}	75 mΩ	**PIND**	145 mW
D	0.623		
η	86%	**PLOSS**	856 mW

$$P_{INTERNAL} = P_{COND} + P_{SW} = 475 \text{ mW} \quad (59)$$

10.3.5 Calculating $R_{\theta JA}$ and $R_{\Psi JC}$

$$R_{\theta JA} = \frac{T_J - T_A}{P_{Dissipation}}$$

and

$$R_{\Psi JC} = \frac{T_J - T_{CASE}}{P_{Dissipation}} \quad (60)$$

Now the internal power dissipation is known, and the junction temperature is attempted to be kept at or below 125°C. The next step is to calculate the value for $R_{\theta JA}$ and/or $R_{\psi JC}$. This is actually very simple to accomplish, and necessary if marginality is a possibility in regards to thermals or determining what package option is correct.

The LM2735-Q1 has a thermal shutdown comparator. When the silicon reaches a temperature of 160°C, the device shuts down until the temperature reduces to 150°C. Knowing this, the $R_{\theta JA}$ or the $R_{\psi JC}$ of a specific application can be calculated. Because the junction-to-top case thermal impedance is much lower than the thermal impedance of junction to ambient air, the error in calculating $R_{\psi JC}$ is lower than for $R_{\theta JA}$. However, a small thermocouple must be attached onto the top case of the LM2735-Q1 to obtain the $R_{\psi JC}$ value.

Knowing the temperature of the silicon when the device shuts down allows three of the four variables to be known. Once the thermal impedance is calculated, work backwards with the junction temperature set to 125°C to determine what maximum ambient air temperature keeps the silicon below the 125°C temperature.

10.3.5.1 Procedure

Place the application into a thermal chamber. Sufficient power must be dissipated in the device so that a good thermal impedance value may be obtained.

Raise the ambient air temperature until the device goes into thermal shutdown. Record the temperatures of the ambient air and/or the top case temperature of the LM2735-Q1. Calculate the thermal impedances.

10.3.5.2 Example From Previous Calculations

$P_{Dissipation}$ = 475 mW

T_A at Shutdown = 139°C

$T_{Case\text{-}Top}$ at Shutdown = 155°C

$$R_{\theta JA} = \frac{T_J - T_A}{P_{Dissipation}} : R_{\Psi JC} = \frac{T_J - T_{Case\text{-}Top}}{P_{Dissipation}} \quad (61)$$

$R_{\theta JA}$ WSON = 55°C/W

$R_{\psi JC}$ WSON = 21°C/W

WSON typical application produces $R_{\theta JA}$ numbers in the range of 50°C/W to 65°C/W, and $R_{\psi JC}$ varies from 18°C/W to 28°C/W. These values are for PCBs with two and four layer boards with 0.5-oz copper, and 4 to 6 thermal vias to bottom side ground plane under the DAP.

For 5-pin SOT-23 package typical applications, $R_{\theta JA}$ numbers range from 80°C/W to 110°C/W, and $R_{\psi JC}$ varies from 50°C/W to 65°C/W. These values are for PCBs with 2- and 4-layer boards with 0.5-oz copper, with 2 to 4 thermal vias from GND pin to bottom layer.

For typical thermal impedances and an ambient temperature maximum of 75°C: if the design requires more than 400 mW internal to the LM2735-Q1 be dissipated, or there is 750 mW of total power loss in the application, TI recommends using the 6-pin WSON package.

NOTE

To use these procedures, it is important to dissipate an amount of power within the device to indicate a true thermal impedance value. If a very small internal dissipated value is used, it can be determined that the thermal impedance calculated is abnormally high, and subject to error. Figure 48 shows the nonlinear relationship of internal power dissipation vs $R_{\theta JA}$.

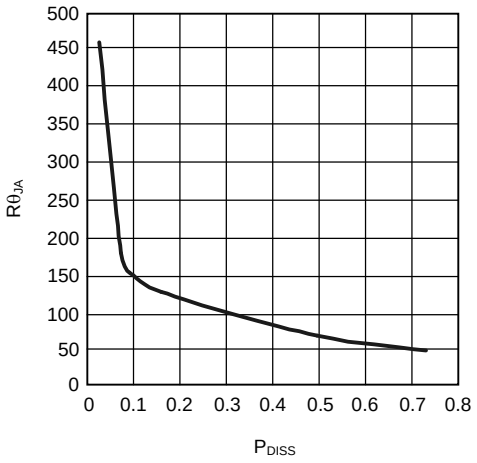


Figure 48. $R_{\theta JA}$ vs Internal Dissipation for the WSON

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.2 使用 WEBENCH® 工具创建定制设计方案

请单击此处，使用 LM2735-Q1 器件及 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.3 文档支持

11.3.1 相关文档

请参阅如下相关文档：

《AN-1229 SIMPLE SWITCHER ® PCB 布局指南》

11.4 接收文档更新通知

要接收文档更新通知，请转至 TI.com.cn 上的器件产品文件夹进行设置。单击右上角的*通知我* 即可接收产品信息更改每周摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

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11.7 静电放电警告

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11.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2735XQMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SVDB	Samples
LM2735XQMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SVDB	Samples
LM2735YQMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SXUB	Samples
LM2735YQSD/NOPB	ACTIVE	WSON	NGG	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L283B	Samples
LM2735YQSDX/NOPB	ACTIVE	WSON	NGG	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L283B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

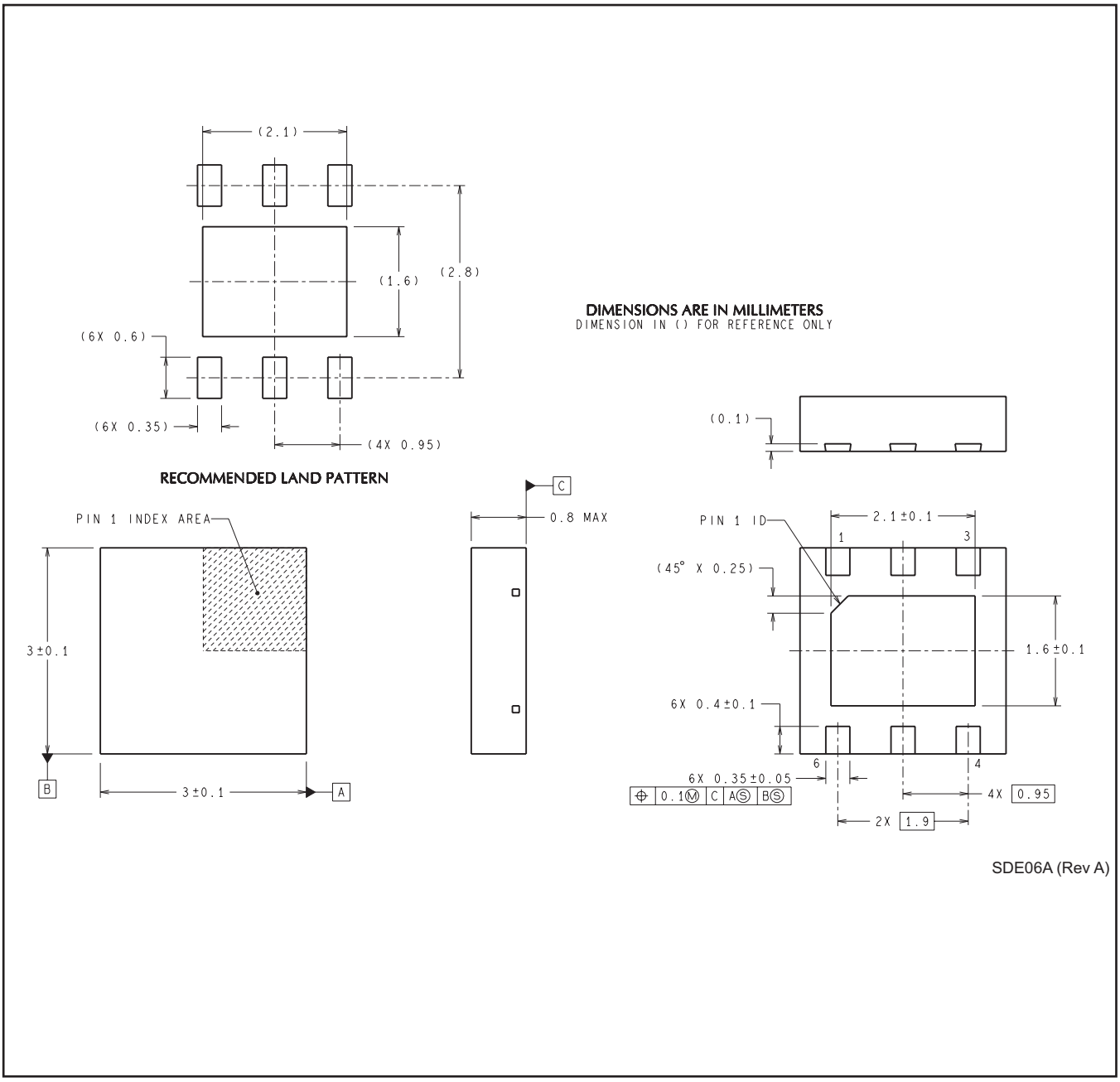
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

NGG0006A



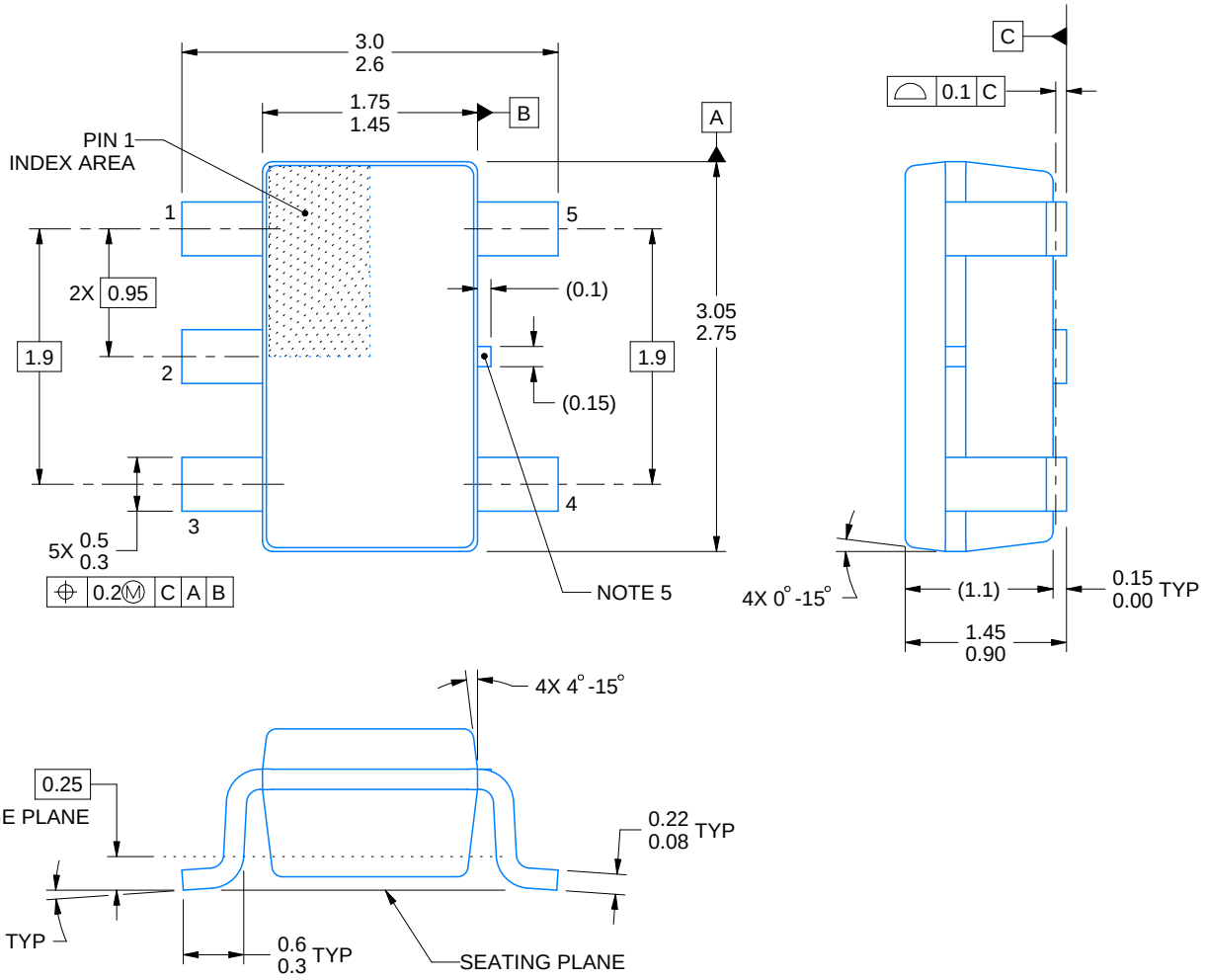
SDE06A (Rev A)

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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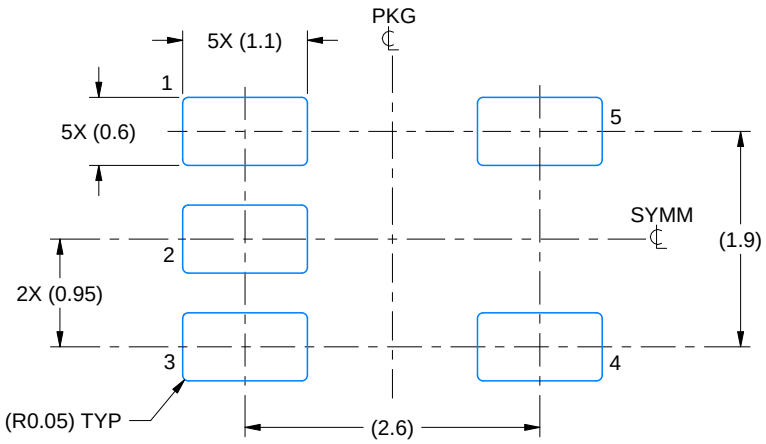
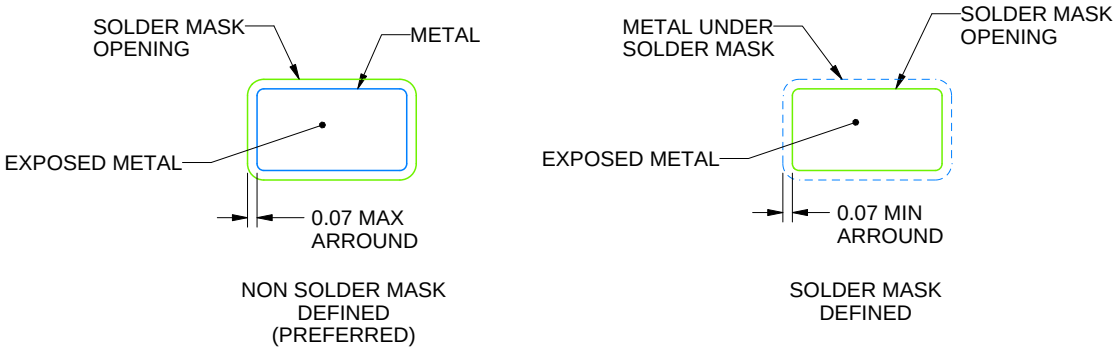
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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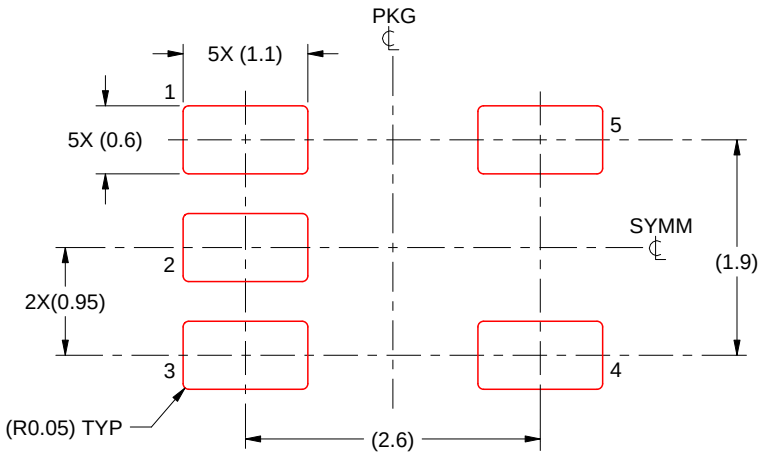
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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