LM73-Q1 具有双线制接口的 2.7V、SOT-23、11 位至 14 位数字温度传感器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果
  - LM73-Q1 温度等级 1：-40°C 至 125°C
  - LM73-Q1 超出人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - LM73-Q1 带电器件模型 (CDM) ESD 分类等级 C6
- 通过一个地址引脚可为每个版本选择三个可选地址中的任一地址，共有 6 个可用地址。
- 兼容 SMBus 和 I^2C 的双线制接口
- 支持 400kHz 工作频率
- 关断模式具有单次触发功能，可实现极低的平均功耗
- 11 位至 14 位的可编程数字温度分辨率
- 快速转换速率适用于快速上电和测量快速充电温度
- 开漏 $\overline{\text{ALERT}}$ 输出引脚在温度超过编程的温度限制时激活
- 非常稳定的低噪声数字量输出
- UL 认证器件
- 温度精度：±1.45°C（最大值）
- 温度范围：-40°C 至 125°C
- 转换时间
  - 11 位 (0.25°C)：14ms（最大值）
  - 14 位 (0.03125°C)：112ms（最大值）
- 工作电源电流：320µA（典型值）
- 关断电源电流：1.9µA（典型值）
- 分辨率：0.25°C 至 0.03125°C

2 应用

- 汽车空调
- 高级驾驶员辅助系统 (ADAS)
- 空气流量传感器
- 信息娱乐处理器管理
- 仪表板系统
- UREA 传感器
- HID 灯

3 说明

LM73-Q1 是一款集成有增量式 Δ-Σ ADC 的数字量输出温度传感器。LM73-Q1 通过兼容 SMBus 和 I^2C 接口的双线制接口进行通信，主机可随时查询 LM73-Q1 从而读取温度。

LM73-Q1 可在较宽的温度范围（–40°C 至 125°C）下运行，温度范围为 -10°C 至 80°C 时精度可达 ±1.45°C。LM73-Q1 包括四种可选分辨率选项，可用于调整温度转换时间和灵敏度，从而实现最优性能。LM73-Q1 默认采用 11 位模式 (0.25°C/LSB)，可在 14ms 的最长时间内测量温度，这非常适用于需要在上电后快速获取温度数据的 应用 。在分辨率最高的 14 位模式 (0.03125°C/LSB) 下，LM73-Q1 经过优化，可感测非常小的温度变化。

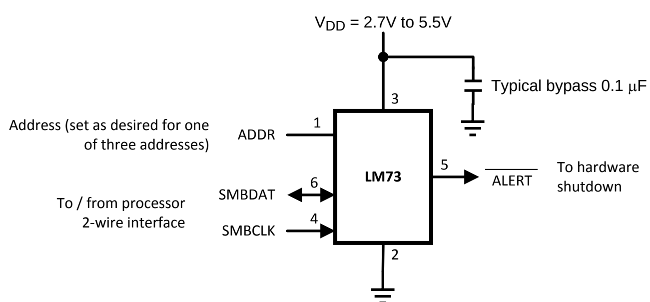
可通过单个多级地址线选择三个独特设备地址中的任一个地址。开漏 $\overline{\text{ALERT}}$ 输出在温度超过可编程限制时激活。数据和时钟线均经过滤波，可实现优异的噪声容差和可靠通信。此外，LM73-Q1 具有超时特性，若时钟和数据线保持低电平超过一段时间，这种特性会将这些线路自动复位。这可在不需要主机处理器干预的情况下防止出现总线锁定状态。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
LM73-Q1	SOT (6)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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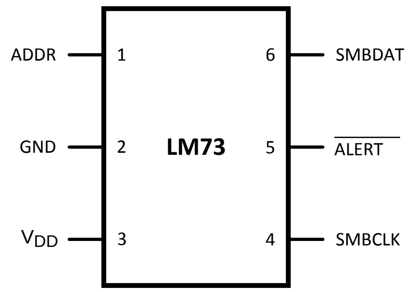
4 修订历史记录

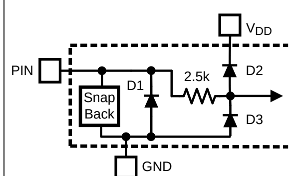
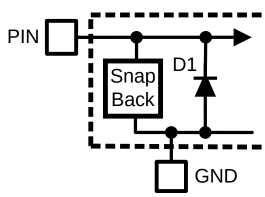
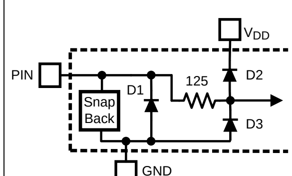
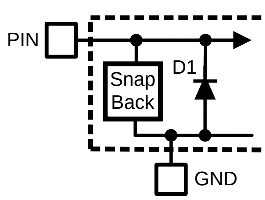
日期	修订版本	注释
2016 年 12 月	*	最初发布版本。

5 Pin Configuration and Functions

**DDC Package
6-Pin (SOT-23)
Top View**



Pin Functions

PIN		TYPE	EQUIVALENT CIRCUIT	FUNCTION
NO.	NAME			
1	ADDR	CMOS Logic Input (three levels)		Address Select Input: One of three device addresses is selected by connecting to ground, left floating, or connecting to V_{DD}.
2	GND	Ground		Ground
3	V_{DD}	Power		Supply Voltage
4	SMBCLK	CMOS Logic Input		Serial Clock: SMBus clock signal. Operates up to 400 kHz. Low-pass filtered.
5	$\overline{\text{ALERT}}$	Open-Drain Output		Digital output which goes active whenever the measured temperature exceeds a programmable temperature limit.
6	SMBDAT	Open-Drain Input/Output		Serial Data: SMBus bi-directional data signal used to transfer serial data synchronous to the SMBCLK. Low-pass filtered.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
Supply Voltage	−0.3		V to 6	V
Voltage at SMBCLK and SMBDAT pins	−0.3 V to V		6	V
Voltage at All Other Pins	−0.3	(V_{DD} + 0.5)	6	V
Input Current at Any Pin(3)			±5	mA
Storage Temperature, T_{stg}	−65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.. Reflow temperature profiles are different for lead-free and non-lead-free packages.
(3) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > V_{DD}), the current at that pin should be limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
LM73-Q1	–40	125	°C
Supply Voltage Range (V_{DD})	2.7	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		LM73-Q1 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	
$R_{\theta JA}$	Junction-to-board thermal resistance	25	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	21	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 2.7 V to 5.5 V. All limits T_A = T_J = 25°C, unless otherwise noted. T_A is the ambient temperature. T_J is the junction temperature.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Accuracy (1)	V_{DD} = 3.3V	T_A = −40°C to -25°C	–1.85		1.85	°C
		T_A = −25°C to –10°C	–1.65		1.65	°C
		T_A = −10°C to 80°C	–1.45		1.45	°C
		T_A = 80°C to 115°C	–1.65		1.65	°C
		T_A = 115°C to 125°C	-1.8		1.8	°C
	V_{DD} = 2.7V to V_{DD} = 4.5V	T_A = −40°C to -25°C	-2.1		2.1	°C
		T_A = −25°C to –10°C	–1.75		1.75	°C
		T_A = −10°C to 80°C	-1.65		1.65	°C
		T_A = 80°C to 115°C	-1.8		1.8	°C
		T_A = 115°C to 125°C	-2		2	°C
	V_{DD} > 4.5V to V_{DD} = 5.5V	T_A = −40°C to -25°C	-2.4		2.4	°C
		T_A = −25°C to -10°C	-2.2		2.2	°C
		T_A = −10°C to 80°C	–1.9		1.9	°C
		T_A = 80°C to 115°C	-1.8		1.8	°C
		T_A = 115°C to 125°C	-2		2	°C
Resolution	RES1 Bit = 0, RES0 Bit = 0			11		Bits
				0.25		°C/LSB
	RES1 Bit = 0, RES0 Bit = 1			12		Bits
				0.125		°C/LSB
	RES1 Bit = 1, RES0 Bit = 0			13		Bits
				0.0625		°C/LSB
	RES1 Bit = 1, RES0 Bit = 1			14		Bits
				0.03125		°C/LSB
Temperature Conversion Time (2)	RES1 Bit = 0, RES0 Bit = 0			10.1		ms
		T_A = T_J = T_{MIN} to T_{MAX}			14	
	RES1 Bit = 0, RES0 Bit = 1			20.2		ms
		T_A = T_J = T_{MIN} to T_{MAX}			28	
	RES1 Bit = 1, RES0 Bit = 0			40.4		ms
		T_A = T_J = T_{MIN} to T_{MAX}			56	
	RES1 Bit = 1, RES0 Bit = 1			80.8		ms
		T_A = T_J = T_{MIN} to T_{MAX}			112	
Quiescent Current	Continuous Conversion Mode, SMBus inactive			320		µA
		T_A = T_J = T_{MIN} to T_{MAX}			495	
	Shutdown, bus-idle timers on			120		µA
		T_A = T_J = T_{MIN} to T_{MAX}			175	
	Shutdown, bus-idle timers off			1.9		µA
		T_A = T_J = T_{MIN} to T_{MAX}			8	
Power-On Reset Threshold	Measured on V_{DD} input, falling edge	T_A = T_J = T_{MIN} to T_{MAX}	0.9			V

(1) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM73-Q1 and the thermal resistance.
(2) This specification is provided only to indicate how often temperature data is updated. The LM73-Q1 can be read at any time without regard to conversion state (and will yield last conversion result).

6.6 Logic Electrical Characteristics- Digital DC Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 2.7 V to 5.5 V. All limits $T_A = T_J$ = 25°C, unless otherwise noted. T_A is the ambient temperature. T_J is the junction temperature.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SMBDAT, SMBCLK INPUTS							
V_{IH}	Logical 1 Input Voltage	$T_A = T_J = T_{MIN}$ to T_{MAX}		0.7 × V_{DD}			V
V_{IL}	Logical 0 Input Voltage	$T_A = T_J = T_{MIN}$ to T_{MAX}				0.3 × V_{DD}	V
$V_{IN;HYST}$	SMBDAT and SMBCLK Digital Input Hysteresis				0.07 × V_{DD}		V
I_{IH}	Logical 1 Input Current	$V_{IN} = V_{DD}$			0.01		µA
			$T_A = T_J = T_{MIN}$ to T_{MAX}			2	
I_{IL}	Logical 0 Input Current	V_{IN} = 0 V			–0.01		µA
			$T_A = T_J = T_{MIN}$ to T_{MAX}			–2	
C_{IN}	Input Capacitance				5		pF
SMBDAT, ALERT OUTPUTS							
I_{OH}	High Level Output Current	$V_{OH} = V_{DD}$			0.01		µA
			$T_A = T_J = T_{MIN}$ to T_{MAX}			2	
V_{OL}	SMBus Low Level Output Voltage	I_{OL} = 3 mA	$T_A = T_J = T_{MIN}$ to T_{MAX}			0.4	V
ADDRESS INPUT							
$V_{IH;ADDRESS}$	Address Pin High Input Voltage	$T_A = T_J = T_{MIN}$ to T_{MAX}		V_{DD} – 0.100			V
$V_{IL;ADDRESS}$	Address Pin Low Input Voltage	$T_A = T_J = T_{MIN}$ to T_{MAX}				0.100	V
$I_{IH;ADDRESS}$	Address Pin High Input Current	$V_{IN} = V_{DD}$			0.01		µA
			$T_A = T_J = T_{MIN}$ to T_{MAX}			2	
$I_{IL;ADDRESS}$	Address Pin Low Input Current	V_{IN} = 0 V			–0.01		µA
			$T_A = T_J = T_{MIN}$ to T_{MAX}			–2	

6.7 SMBus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 2.7 V to 5.5 V, C_L (load capacitance) on output lines = 400 pF. All limits $T_A = T_J$ = 25°C, unless otherwise noted. See Figure 1.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{SMB}	SMBus Clock Frequency	No minimum clock frequency if Time-Out feature is disabled.	$T_A = T_J = T_{MIN}$ to T_{MAX}			400	kHz
t_{LOW}	SMBus Clock Low Time	$T_A = T_J = T_{MIN}$ to T_{MAX}		300			ns
t_{HIGH}	SMBus Clock High Time	$T_A = T_J = T_{MIN}$ to T_{MAX}		300			ns
$t_{F;SMBO}$	Output Fall Time (1)	C_L = 400 pF $I_{PULL-UP}$ ≤ 3 mA	$T_A = T_J = T_{MIN}$ to T_{MAX}			250	ns
$t_{TIMEOUT}$	SMBDAT and SMBCLK Time Low for Reset of Serial Interface (2)	$T_A = T_J = T_{MIN}$ to T_{MAX}		15		45	ms
$t_{SU;DAT}$	Data In Setup Time to SMBCLK High	$T_A = T_J = T_{MIN}$ to T_{MAX}		100			ns
$t_{HD;DATI}$	Data Hold Time: Data In Stable after SMBCLK Low	$T_A = T_J = T_{MIN}$ to T_{MAX}		0			ns
$t_{HD;DATO}$	Data Hold Time: Data Out Stable after SMBCLK Low	$T_A = T_J = T_{MIN}$ to T_{MAX}		30			ns
$t_{HD;STA}$	Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first clock falling edge)	$T_A = T_J = T_{MIN}$ to T_{MAX}		60			ns
$t_{SU;STO}$	Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup)	$T_A = T_J = T_{MIN}$ to T_{MAX}		50			ns
$t_{SU;STA}$	SMBus Repeated Start-Condition Setup Time, SMBCLK High to SMBDAT Low	$T_A = T_J = T_{MIN}$ to T_{MAX}		50			ns
t_{BUF}	SMBus Free Time Between Stop and Start Conditions	$T_A = T_J = T_{MIN}$ to T_{MAX}		1.2			µs
t_{POR}	Power-On Reset Time (3)	$T_A = T_J = T_{MIN}$ to T_{MAX}			1		ms

(1) The output fall time is measured from ($V_{IH;MIN}$ + 0.15V) to ($V_{IL;MAX}$ - 0.15V).
(2) Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the LM73-Q1's SMBus state machine, setting SMBDAT and SMBCLK pins to a high impedance state.
(3) Represents the time from V_{DD} reaching the power-on-reset level to the LM73-Q1 communications being functional. After an additional time equal to one temperature conversion time, valid temperature is available in the *Temperature Data Register* .

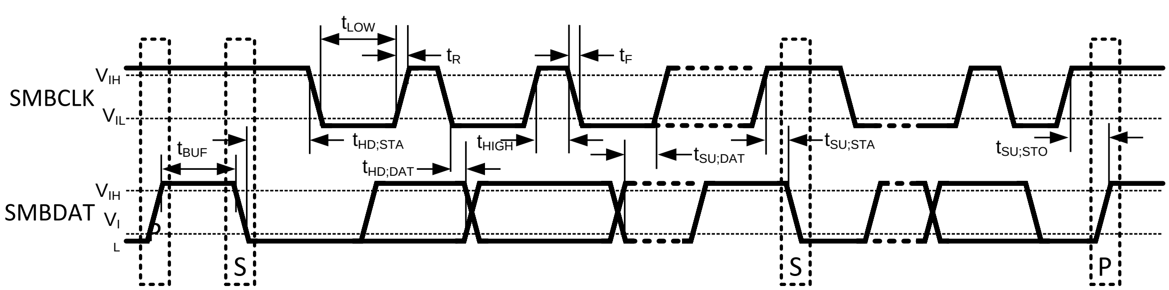


Figure 1. SMBus Communication

6.8 Typical Characteristics

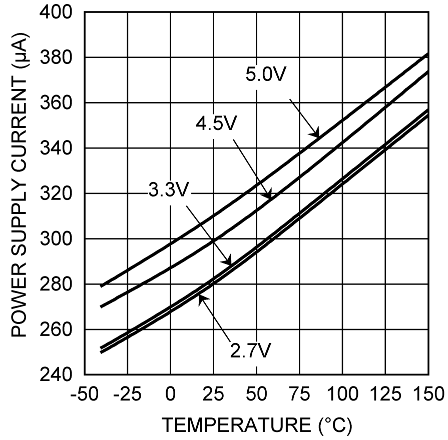


Figure 2. Operating Current vs. Temperature

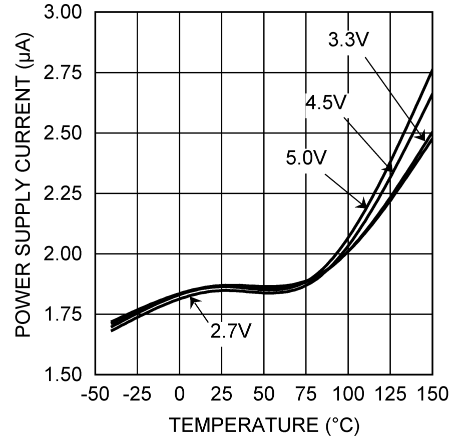


Figure 3. Shutdown Current vs.Temperature

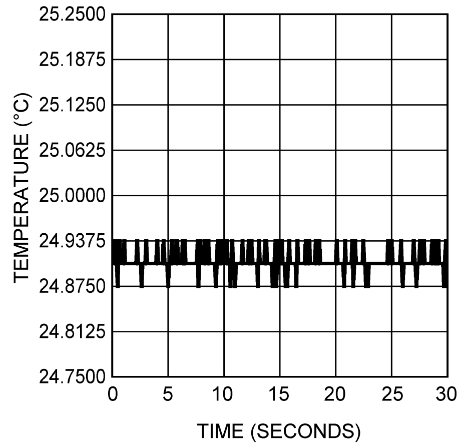


Figure 4. Typical Output Noise

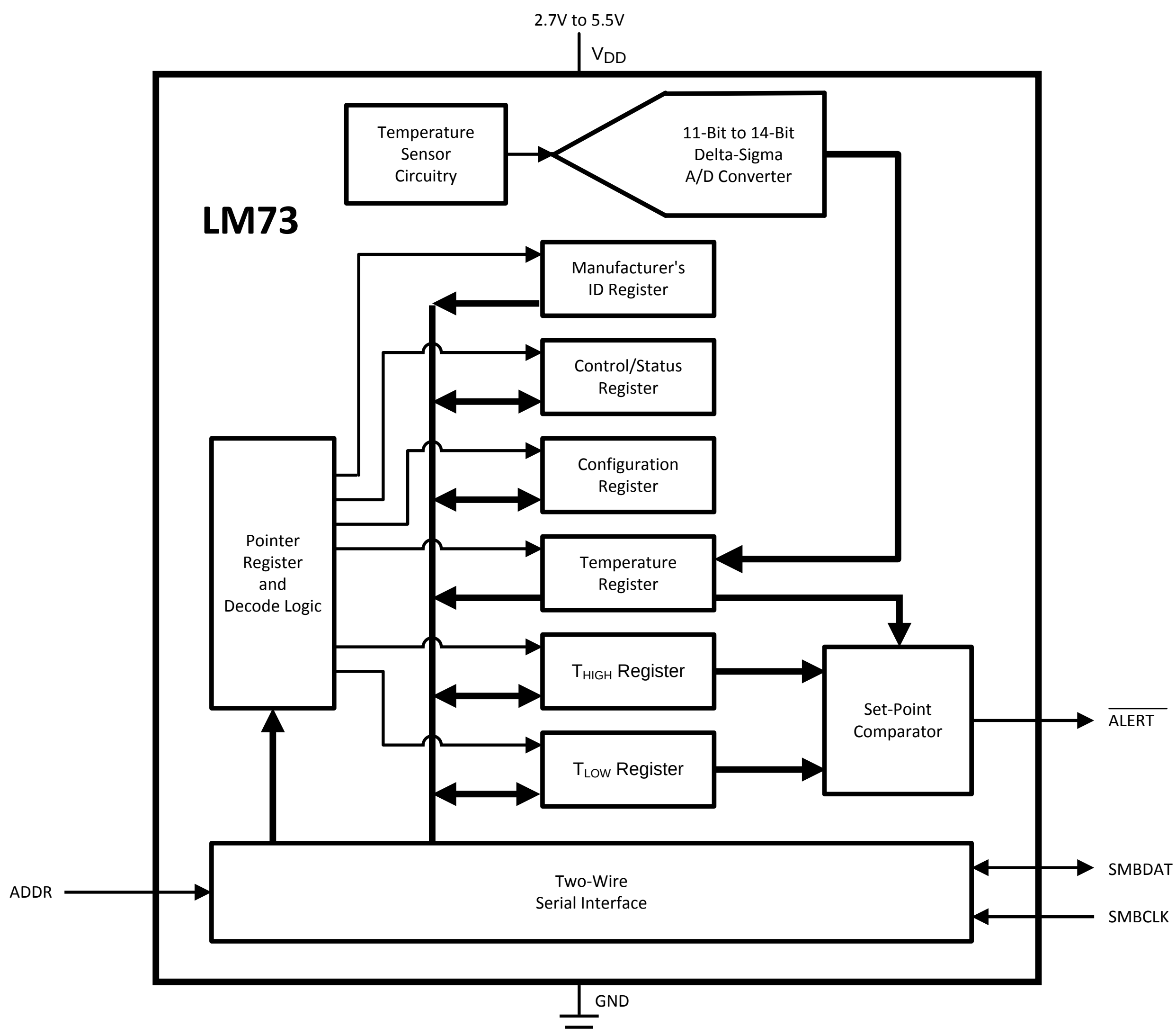
7 Detailed Description

7.1 Overview

The LM73-Q1 is a digital temperature sensor that senses the temperature of its die using a sigma-delta analog-to-digital converter and stores the temperature in the Temperature Register. The LM73-Q1's 2-wire serial interface is compatible with SMBus 2.0 and I^2C. Please see the SMBus 2.0 specification for a detailed description of the differences between the I^2C bus and SMBus.

The temperature resolution is programmable, allowing the host system to select the optimal configuration between sensitivity and conversion time. The LM73-Q1 can be placed in shutdown to minimize power consumption when temperature data is not required. While in shutdown, a 1-shot conversion mode allows system control of the conversion rate for ultimate flexibility.

7.2 Functional Block Diagram



7.3 Feature Description

The LM73-Q1 features the following registers. See *LM73-Q1 Registers* for a complete list of the pointer address, content, and reset state of each register.

- Pointer Register

Feature Description (continued)

- Temperature Register
- Configuration Register
- T_{HIGH} Register
- T_{LOW} Register
- Control/Status Register
- Identification Register

7.3.1 Power-On Reset

The power-on reset (POR) state is the point at which the supply voltage rises above the power-on reset threshold (specified in the *Electrical Characteristics*), generating an internal reset. Each of the registers contains a defined value upon POR and this data remains there until any of the following occurs:

- The first temperature conversion is completed, causing the Temperature Register and various status bits to be updated internally, depending on the value of the measured temperature.
- The master writes different data to any Read/Write (R/W) bits, or
- The LM73-Q1 is powered down.

7.3.2 One-Shot Conversion

The LM73-Q1 features a one-shot conversion bit, which is used to initiate a single conversion and comparison cycle when the LM73-Q1 is in shutdown mode. While the LM73-Q1 is in shutdown mode, writing a 1 to the One-Shot bit in the Configuration Register will cause the LM73-Q1 to perform a single temperature conversion and update the Temperature Register and the affected status bits. Operating the LM73-Q1 in this one-shot mode allows for extremely low average-power consumption, making it ideal for low-power applications.

When the One-Shot bit is set, the LM73-Q1 initiates a temperature conversion. After this initiation, but before the completion of the conversion and resultant register updates, the LM73-Q1 is in a "one-shot" state. During this state, the Data Available (DAV) flag in the Control/Status register is 0 and the Temperature Register contains the value 8000h (-256°C). All other registers contain the data that was present before initiating the one-shot conversion. After the temperature measurement is complete, the DAV flag will be set to 1 and the temperature register will contain the resultant measured temperature.

7.3.3 Temperature Data Format

The resolution of the temperature data and the size of the data word are user-selectable through bits RES1 and RES0 in the *Control/Status Register*. By default, the LM73-Q1 temperature stores the measured temperature in an 11-bit (10 bits plus sign) word with one least significant bit (LSB) equal to 0.25°C. The maximum word size is 14 bits (13-bits plus sign) with a resolution of 0.03125 °C/LSB.

CONTROL BIT		DATA FORMAT	
RES1	RES0	WORD SIZE	RESOLUTION
0	0	11 bits	0.25 °C/LSB
0	1	12 bits	0.125 °C/LSB
1	0	13 bits	0.0625 °C/LSB
1	1	14 bits	0.03125 °C/LSB

The temperature data is reported in 2's complement format. The word is stored in the 16-bit Temperature Register and is left justified in this register. Unused temperature-data bits are always reported as 0.

Table 1. 11-Bit (10-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
150°C	0100 1011 0000 0000	4B00h
25°C	0000 1100 1000 0000	0C80h
1°C	0000 0000 1000 0000	0080h
0.25°C	0000 0000 0010 0000	0020h

Table 1. 11-Bit (10-Bit Plus Sign) (continued)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
0°C	0000 0000 0000 0000	0000h
−0.25°C	1111 1111 1110 0000	FFE0h
−1°C	1111 1111 1000 0000	FF80h
−25°C	1111 0011 1000 0000	F380h
−40°C	1110 1100 0000 0000	EC00h

Table 2. 12-Bit (11-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
150°C	0100 1011 0000 0000	4B00h
25°C	0000 1100 1000 0000	0C80h
1°C	0000 0000 1000 0000	0080h
0.125°C	0000 0000 0001 0000	0010h
0°C	0000 0000 0000 0000	0000h
−0.125°C	1111 1111 1111 0000	FFF0h
−1°C	1111 1111 1000 0000	FF80h
−25°C	1111 0011 1000 0000	F380h
−40°C	1110 1100 0000 0000	EC00h

Table 3. 13-Bit (12-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
150°C	0100 1011 0000 0000	4B00h
25°C	0000 1100 1000 0000	0C80h
1°C	0000 0000 1000 0000	0080h
0.0625°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
−0.0625°C	1111 1111 1111 1000	FFF8h
−1°C	1111 1111 1000 0000	FF80h
−25°C	1111 0011 1000 0000	F380h
−40°C	1110 1100 0000 0000	EC00h

Table 4. 14-Bit (13-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
150°C	0100 1011 0000 0000	4B00h
25°C	0000 1100 1000 0000	0C80h
1°C	0000 0000 1000 0000	0080h
0.03125°C	0000 0000 0000 0100	0004h
0°C	0000 0000 0000 0000	0000h
−0.03125°C	1111 1111 1111 1100	FFFCh
−1°C	1111 1111 1000 0000	FF80h
−25°C	1111 0011 1000 0000	F380h
−40°C	1110 1100 0000 0000	EC00h

7.3.4 SMBus Interface

The LM73-Q1 operates as a slave on the SMBus. The SMBDAT line is bidirectional. The SMBCLK line is an input only. The LM73-Q1 never drives the SMBCLK line and it does not support clock stretching.

The LM73-Q1 uses a 7-bit slave address. It is available in two versions. Each version can be configured for one of three unique slave addresses, for a total of six unique address.

PART NUMBER	ADDRESS PIN	DEVICE ADDRESS
LM73C0-Q1	Float Ground V_{DD}	1001 000 1001 001 1001 010
LM73C1-Q1	Float Ground V_{DD}	1001 100 1001 101 1001 110

The SMBDAT output is an open-drain output and does not have internal pull-ups. A “high” level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible without effecting the SMBus desired data rate. This will minimize any internal temperature reading errors due to internal heating of the LM73-Q1.

The LM73-Q1 features an integrated low-pass filter on both the SMBCLK and the SMBDAT line. These filters increase communications reliability in noisy environments.

If either the SMBCLK or SMBDAT line is held low for a time greater than $t_{TIMEOUT}$ (see *Logic Electrical Characteristics* for the value of $t_{TIMEOUT}$), the LM73-Q1 state machine will reset to the SMBus idle state, releasing the data line. Once the SMBDAT is released high, the master may initiate an SMBus start.

7.3.5 ALERT Function

The $\overline{\text{ALERT}}$ output is an over-temperature indicator. At the end of every temperature conversion, the measured temperature is compared to the value in the T_{HIGH} Register. If the measured temperature exceeds the value stored in T_{HIGH}, the $\overline{\text{ALERT}}$ output goes active (see Figure 5). This over-temperature condition will also cause the ALRT_STAT bit in the Control/Status Register to change value (this bit mirrors the logic level of the $\overline{\text{ALERT}}$ pin).

The $\overline{\text{ALERT}}$ pin and the ALRT_STAT bit are cleared when any of the following occur:

- The measured temperature falls below the value stored in the T_{LOW} Register
- A 1 is written to the $\overline{\text{ALERT}}$ Reset bit in the Configuration Register
- The master resets it through an SMBus Alert Response Address (ARA) procedure

If $\overline{\text{ALERT}}$ has been cleared by the master writing a 1 to the $\overline{\text{ALERT}}$ Reset bit, while the measured temperature still exceeds the T_{HIGH} setpoint, $\overline{\text{ALERT}}$ will go active again after the completion of the next temperature conversion.

Each temperature reading is associated with a Temperature High (THI) and a Temperature Low (TLOW) flag in the Control/Status Register. A digital comparison determines whether that reading is above the T_{HIGH} setpoint or below the T_{LOW} setpoint. If so, the corresponding flag is set. All digital comparisons to the T_{HIGH}, and T_{LOW} values are based on an 11-bit temperature comparison. Regardless of the resolution setting of the LM73-Q1, the lower three temperature LSBs will not affect the state of the $\overline{\text{ALERT}}$ output, THI flag, and TLOW flag.

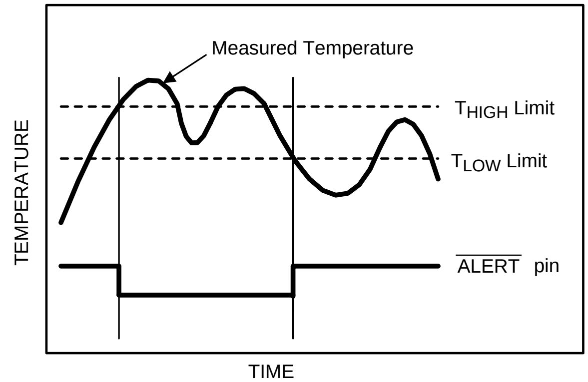


Figure 5. ALERT Temperature Response Cleared When Temperature Crosses T_{LOW}

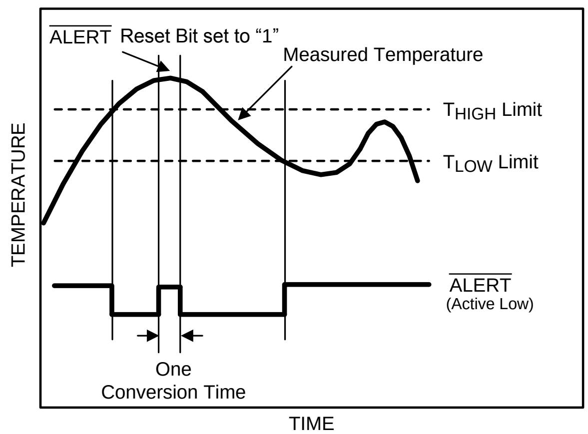


Figure 6. ALERT Temperature Response Cleared by Writing a 1 to the ALERT Reset Bit.

7.3.6 Communicating With the LM73-Q1

The data registers in the LM73-Q1 are selected by the Pointer Register. At power-up the Pointer Register is set to 00h, the location for the Temperature Register. The Pointer Register latches the last location it was set to. Note that all Pointer Register bits are decoded; any incorrect pointer values will not be acknowledged and will not be stored in the Pointer Register.

NOTE

A write to an invalid pointer address is not allowed. If the master writes an invalid address to the Pointer Register, the LM73-Q1 will not acknowledge the address and the Pointer Register will continue to contain the last value stored in it.

A **Write** to the LM73-Q1 will always include the address byte and the pointer byte.

A **Read** from the LM73-Q1 can occur in either of the following ways:

- If the location latched in the Pointer Register is correct (that is, the Pointer Register is pre-set prior to the read), then the read can simply consist of an address byte, followed by retrieving the data byte. Most of the time it is expected that the Pointer Register will point to Temperature Registers because that will be the data most frequently read from the LM73-Q1.
- If the Pointer Register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The data byte is read out of the LM73-Q1 by the most significant bit first. At the end of a read, the LM73-Q1 can accept either an Acknowledge or No Acknowledge bit from the Master. No Acknowledge is typically used as a signal to the slave that the Master has read its last byte.

7.3.6.1 Reading from the LM73-Q1

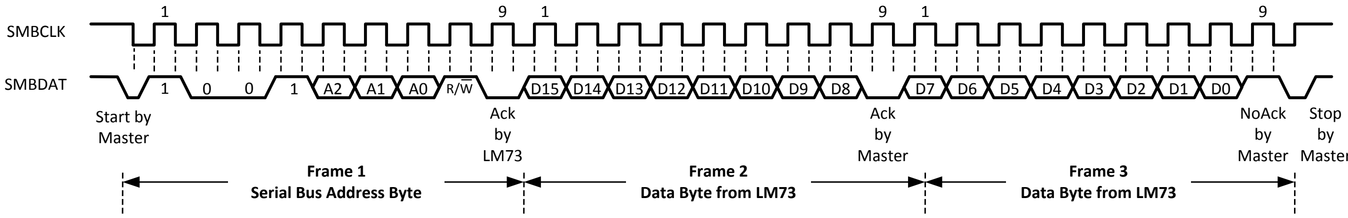


Figure 7. Typical Read from a 2-Byte Register with Preset Pointer

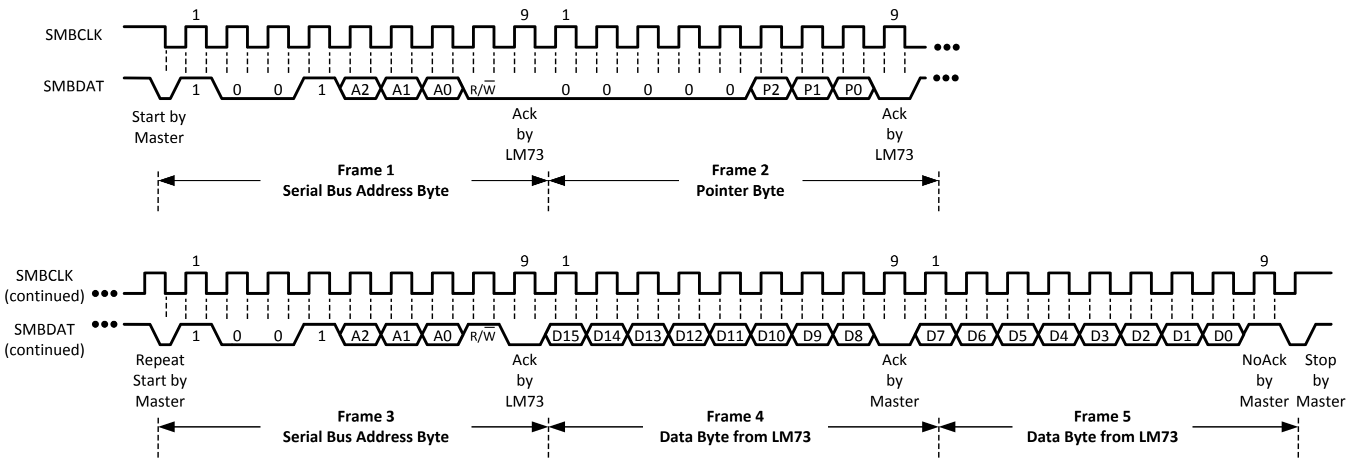


Figure 8. Typical Pointer Set Followed by Immediate Read of a 2-Byte Register

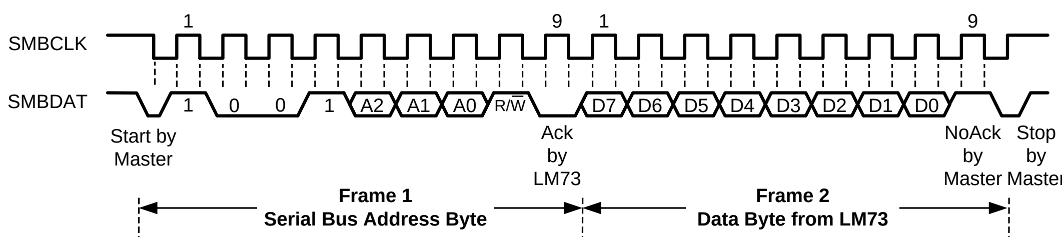


Figure 9. Typical Read from a 1-Byte Register with Preset Pointer

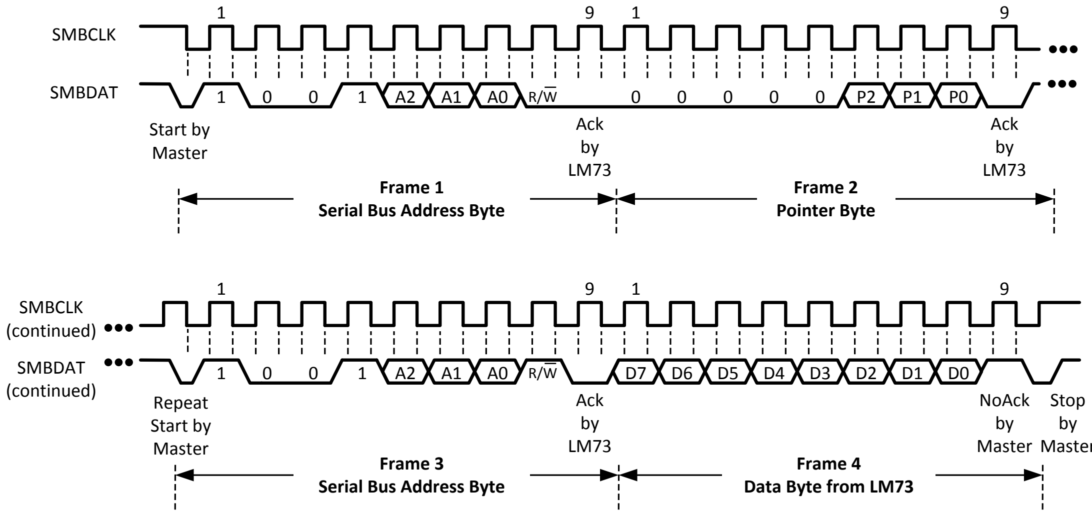


Figure 10. Typical Pointer Set Followed by Immediate Read of a 1-Byte Register

7.3.6.2 Writing to the LM73-Q1

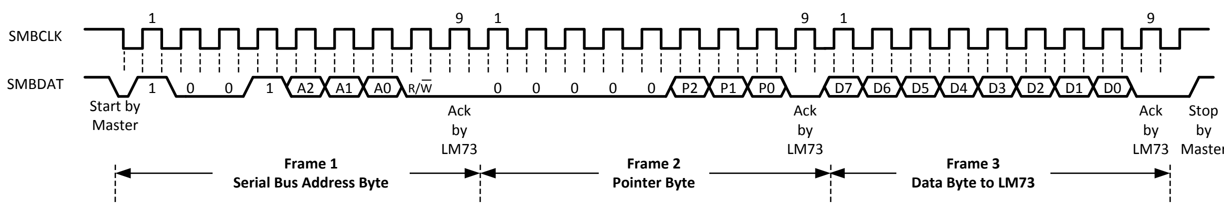


Figure 11. Typical 1-Byte Write

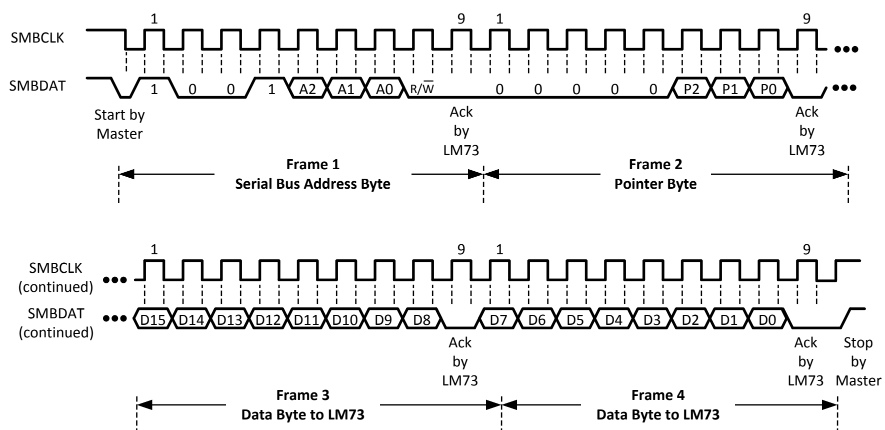


Figure 12. Typical 2-Byte Write

7.4 Device Functional Modes

7.4.1 Shutdown Mode

Shutdown Mode is enabled by writing a “1” to the Full Power Down Bit, Bit 7 of the Configuration Register, and holding it high for at least the specified maximum conversion time at the existing temperature resolution setting. (see Temperature Conversion Time specifications under the *Temperature-to-Digital Converter Characteristics*). For example, if the LM73-Q1 is set for 12-bit resolution before shutdown, then Bit 7 of the Configuration register must go high and stay high for the specified maximum conversion time for 12-bits resolution.

Device Functional Modes (continued)

The LM73-Q1 will always finish a temperature conversion and update the temperature registers before shutting down.

Writing a “0” to the Full Power Down Bit restores the LM73-Q1 to normal mode. The user should wait at least the specified maximum conversion time, at the existing resolution setting, before accurate data appears in the temperature register.

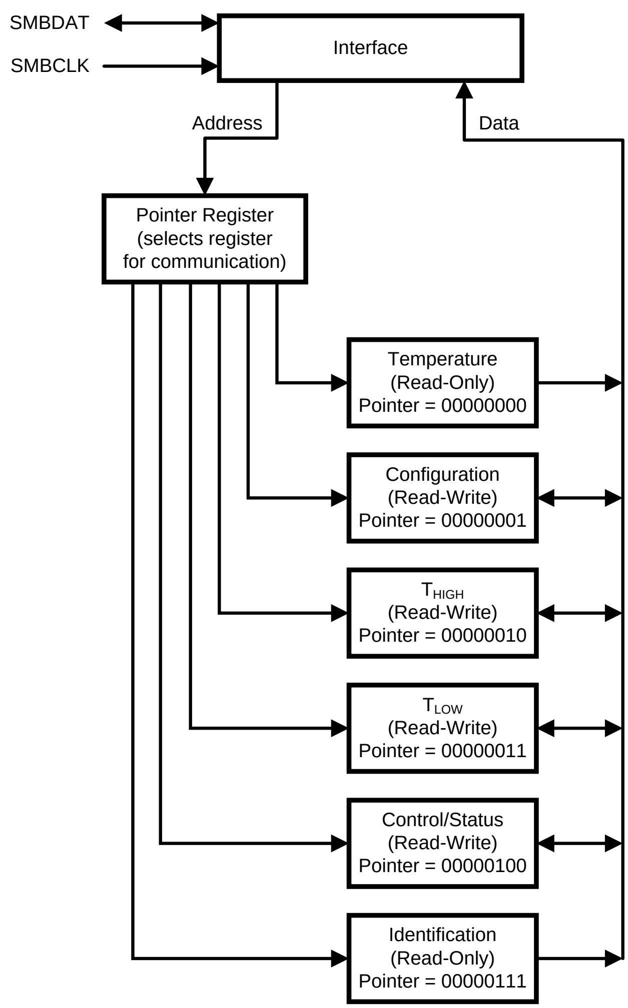
7.5 Register Map

7.5.1 LM73-Q1 Registers

The LM73-Q1's internal registers are selected by the Pointer register. The Pointer register latches the last location that it was set to. The pointer register and all internal registers are described below. All registers reset at device power up.

7.5.1.1 Pointer Register

The diagram below shows the Pointer Register, the six internal registers to which it points, and their associated pointer addresses.



P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

Bits	Name	Description
7:3	Not Used	Must write zeros only.
2:0	Register Select	Pointer address. Points to desired register. See table below.

P2	P1	P0	REGISTER (1)
0	0	0	Temperature
0	0	1	Configuration
0	1	0	T_{HIGH}
0	1	1	T_{LOW}
1	0	0	Control / Status
1	1	1	Identification

(1) A write to an invalid pointer address is not allowed. If the master writes an invalid address to the Pointer Register,
(a) the LM73-Q1 will not acknowledge the address and
(b) the Pointer Register will continue to contain the last value stored in it.

7.5.1.2 Temperature Data Register

Pointer Address 00h (Read Only)

Reset State: 7FFCh (+255.96875°C)

One-Shot State: 8000h (-256°C)

D15	D14	D13	D12	D11	D10	D9	D8
SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C

D7	D6	D5	D4	D3	D2	D1	D0
1°C	0.5°C	0.25°C	0.125°C	0.0625°C	0.03125°C	reserved	reserved

Bits	Name	Description
15:2	Temperature Data	Represents the temperature that was measured by the most recent temperature conversion. On Power-up, this data is invalid until the Data Available (DAV) bit in the Control/Status register is high (after the completion of the first temperature conversion). The resolution is user-programable from 11-bit resolution (0.25°C/LSB) through 14-bit resolution (0.03125°C/LSB). The desired resolution is programmed with bits 5 and 6 of the Control/Status register.
1:0	Not Used	Return zeros upon read.

7.5.1.3 Configuration Register

Pointer Address 01h (R/W)

Reset State: 40h

D7	D6	D5	D4	D3	D2	D1	D0
PD	reserved	$\overline{\text{ALRT EN}}$	ALRT POL	ALRT RST	ONE SHOT	reserved	

Bits	Name	Description
7	Full Power Down	Writing a 1 to this bit and holding it high for at least the specified maximum conversion time, at the existing temperature resolution setting, puts the LM73-Q1 in shutdown mode for power conservation. Writing a 0 to this bit restores the LM73-Q1 to normal mode. Waiting one specified maximum conversion time for the existing resolution setting assures accurate data in the temperature register.
6	reserved	User must write only a 1 to this bit
5	$\overline{\text{ALERT}}$ Enable	A 0 in this location enables the $\overline{\text{ALERT}}$ output. A 1 disables it. This bit also controls the $\overline{\text{ALERT}}$ Status bit (the Control/Status Register, Bit 3) since that bit reflects the state of the Alert pin.
4	$\overline{\text{ALERT}}$ Polarity	When set to 1, the $\overline{\text{ALERT}}$ pin and $\overline{\text{ALERT}}$ Status bit are active-high. When 0, it is active-low.
3	$\overline{\text{ALERT}}$ Reset	Writing a 1 to this bit resets the $\overline{\text{ALERT}}$ pin and the $\overline{\text{ALERT}}$ Status bit. It will always be 0 when read.
2	One Shot	When in shutdown mode (Bit 7 is 1), initiates a single temperature conversion and update of the temperature register with new temperature data. Has no effect when in continuous conversion mode (i.e., when Bit 7 is 0). Always returns a 0 when read.
1:0	Reserved	User must write only a 0 to these bits.

7.5.1.4 T_{HIGH} Upper-Limit Register

Pointer Address 02h (R/W)

Reset State: 7FE0h (+255.75°C)

D15	D14	D13	D12	D11	D10	D9	D8
SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C

D7	D6	D5	D4	D3	D2	D1	D0
1°C	0.5°C	0.25°C	reserved				

Bits	Name	Description
15:5	Upper-Limit Temperature	If the measured temperature that is stored in this register exceeds this user-programmable upper temperature limit, the $\overline{\text{ALERT}}$ pin will go active and the THIGH flag in the Control/Status register will be set to 1. Two's complement format.
4:0	Reserved	Returns zeros upon read. Recommend writing zeros only in these bits.

7.5.1.5 T_{LOW} Lower-Limit Register

Pointer Address 03h (R/W)

Reset State: 8000h (–256°C)

D15	D14	D13	D12	D11	D10	D9	D8
SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C

D7	D6	D5	D4	D3	D2	D1	D0
1°C	0.5°C	0.25°C	reserved				

Bits	Name	Description
15:5	Lower-Limit Temperature	If the measured temperature that is stored in the temperature register falls below this user-programmable lower temperature limit, the $\overline{\text{ALERT}}$ pin will be deactivated and the T_{LOW} flag in the Control/Status register will be set to 1. Two's complement format.
4:0	Reserved	Returns zeros upon read. Recommend writing zeros only in these bits.

7.5.1.6 Control/Status Register

Pointer Address 04h (R/W)

Reset State: 08h

D7	D6	D5	D4	D3	D2	D1	D0
TO_DIS	RES1	RES0	reserved	ALRT_STAT	THI	TLOW	DAV

BITS	NAME	DESCRIPTION
7	Time-Out Disable	Disable the time-out feature on the SMBDAT and SMBCLK lines if set to 1. Setting this bit turns off the bus-idle timers, enabling the LM73-Q1 to operate at lowest shutdown current.
6:5	Temperature Resolution	Selects one of four user-programmable temperature data resolutions 00: 0.25°C/LSB, 11-bit word (10 bits plus Sign) 01: 0.125°C/LSB, 12-bit word (11 bits plus Sign) 10: 0.0625°C/LSB, 13-bit word (12 bits plus Sign) 11: 0.03125°C/LSB, 14-bit word (13 bits plus Sign)
4	reserved	Always returns zero when read. Recommend customer write zero only.
3	$\overline{\text{ALERT}}$ Pin Status	Value is 0 when $\overline{\text{ALERT}}$ output pin is low. Value is 1 when $\overline{\text{ALERT}}$ output pin is high. The $\overline{\text{ALERT}}$ output pin is reset under any of the following conditions: (1) Cleared by writing a 1 to the $\overline{\text{ALERT}}$ Reset bit in the configuration register, (2) Measured temperature falls below the T_{LOW} limit, or (3) cleared via the ARA sequence. Recommend customer write zero only.
2	Temperature High Flag	Bit is set to 1 when the measured temperature exceeds the T_{HIGH} limit stored in the programmable T_{HIGH} register. Flag is reset to 0 when both of the following conditions are met: (1) measured temperature no longer exceeds the programmed T_{HIGH} limit *and* (2) upon reading the Control/Status register. If the temperature is not longer above the T_{HIGH} limit, this status bit remains set until it is read by the master so that the system can check the history of what caused the $\overline{\text{ALERT}}$ output to go active. This bit is not cleared after every read if the measured temperature is still above the T_{HIGH} limit.
1	Temperature Low Flag	Bit is set to 1 when the measured temperature falls below the T_{LOW} limit stored in the programmable T_{LOW} register. Flag is reset to 0 when both of the following conditions are met: (1) measured temperature is no longer below the programmed T_{LOW} limit *and* (2) upon reading the Control/Status register. If the temperature is no longer below the T_{LOW} limit, the status bit remains set until it is read by the master so that the system can check the history of what cause the $\overline{\text{ALERT}}$ output to go active. This bit is not cleared after every read if temperature is still below T_{LOW} limit.
0	Data Available Flag	This bit is 0 when the LM73-Q1 is in the process of converting a new temperature. It is 1 when the conversion is done. After initiating a temperature conversion while operating in the one-shot mode, this status bit can be monitored to indicate when the conversion is done. After triggering the one-shot conversion, the data in the temperature register is invalid until this bit is high (that is, after completion of the conversion). On power-up, the LM73-Q1 is in continuous conversion mode; while in continuous conversion mode (the default mode after power-on reset) this bit will always be high. Recommend customer write zero only.

7.5.1.7 Identification Register

Pointer Address 07h (Read Only)

Reset State: 0190h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0

BITS	NAME	DESCRIPTION
15:8	Manufacturer Identification Byte	Always returns 01h to uniquely identify the manufacturer as Texas Instruments.
7:4	Product Identification Nibble	Always returns 9h to uniquely identify this part as the LM73-Q1 Temperature Sensor.
3:0	Die Revision Step Nibble	Always returns 0h to uniquely identify the revision as level zero.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Thermal Path Considerations

To get the expected results when measuring temperature with an integrated circuit temperature sensor like the LM73-Q1, it is important to understand that the sensor measures its own die temperature. For the LM73-Q1, the best thermal path between the die and the outside world is through the LM73-Q1's pins. In the SOT23 package, all the pins on the LM73-Q1 will have an equal effect on the die temperature. Because the pins represent a good thermal path to the LM73-Q1 die, the LM73-Q1 will provide an accurate measurement of the temperature of the printed circuit board on which it is mounted. There is a less efficient thermal path between the plastic package and the LM73-Q1 die. If the ambient air temperature is significantly different from the printed circuit board temperature, it will have a small effect on the measured temperature.

8.1.2 Output Considerations: Tight Accuracy, Resolution and Low Noise

The LM73-Q1 is well suited for applications that require tight temperature measurement accuracy. In many applications, the low temperature error can mean better system performance and, by eliminating a system calibration step, lower production cost.

With digital resolution as fine as 0.03125 °C/LSB, the LM73-Q1 senses and reports very small changes in its temperature, making it ideal for applications where temperature sensitivity is important. For example, the LM73-Q1 enables the system to quickly identify the direction of temperature change, allowing the processor to take compensating action before the system reaches a critical temperature.

The LM73-Q1 has very low output noise, typically 0.015°C rms, which makes it ideal for applications where stable thermal compensation is a priority. For example, in a temperature-compensated oscillator application, the very small deviation in successive temperature readings translates to a stable frequency output from the oscillator.

8.2 Typical Application

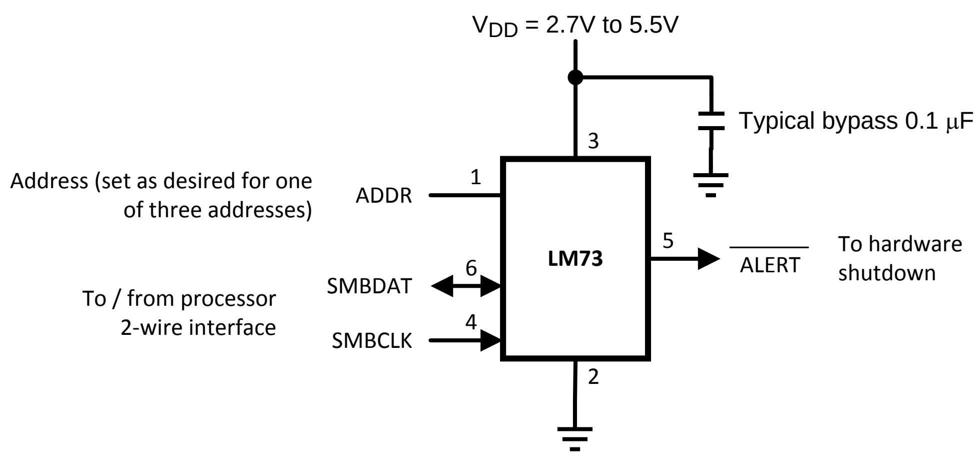


Figure 13. Digital Temperature Sensing

8.2.1 Design Requirements

The LM73-Q1 requires positive supply voltage of 2.7 V to 5.5 V to be applied between $+V_{DD}$ and GND. For best results, bypass capacitors of 100 nF and 10 μF are recommended.

Typical Application (continued)

8.2.2 Detailed Design Procedure

The temperature resolution is programmable, allowing the host system to select the optimal configuration between sensitivity and conversion time. The LM73-Q1 can be placed in shutdown to minimize power consumption when temperature data is not required. While in shutdown, a 1-shot conversion mode allows system control of the conversion rate for ultimate flexibility.

8.2.3 Application Curve

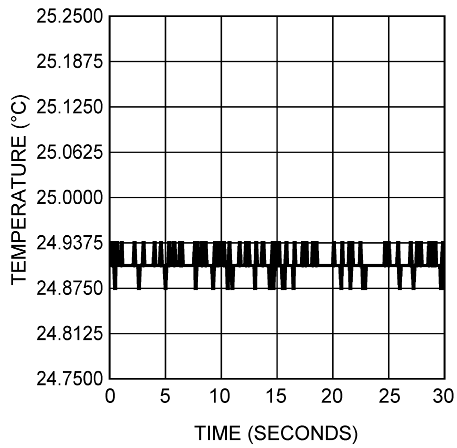


Figure 14. Typical Performance

9 Power Supply Recommendations

In systems where there is a large amount of capacitance on the VDD node, the LM73-Q1 power supply ramp-up time can become excessively long. Slow power-supply ramp times may result in abnormal temperature readings. A linear power-on-ramp of less than 0.7 V/msec and an exponential ramp with an RC time constant of more than 1.25 msec is categorized as a slow power-supply ramp. To avoid errors, use the power up sequence described below.

The software reset sequence is as follows:

1. Allow V_{DD} to reach the specified minimum operating voltage, as specified in the *Recommended Operating Conditions* section.
2. Write a 1 to the Full Power Down bit, Bit 7 of the Configuration Register, and hold it high for the specified maximum conversion time for the initial default of 11-bits resolution. This ensures that a complete reset operation has occurred. See the Temperature Conversion Time specifications within the *Temperature-to-Digital Converter Characteristics* for more details.
3. Write a 0 to the Full Power Down bit to restore the LM73-Q1 to normal mode.

10 Layout

10.1 Layout Guidelines

To achieve the expected results when measuring temperature with an integrated circuit temperature sensor like the LM73-Q1, it is important to understand that the sensor measures its own die temperature. For the LM73-Q1, the best thermal path between the die and the outside world is through the LM73-Q1's pins. In the SOT-23 package, all the pins on the LM73-Q1 will have an equal effect on the die temperature. Because the pins represent a good thermal path to the LM73-Q1 die, the LM73-Q1 will provide an accurate measurement of the temperature of the printed circuit board on which it is mounted.

10.2 Layout Example

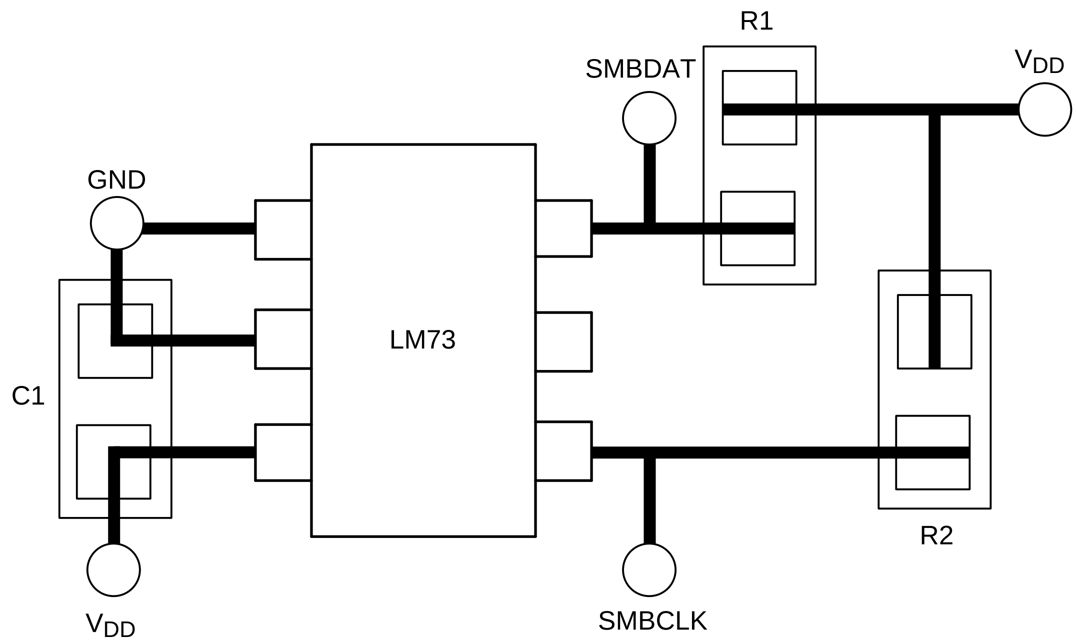


Figure 15. PBC Layout

11 器件和文档支持

11.1 相关文档

相关文档如下：

半导体和集成电路 (IC) 封装热度量

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM73C0QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	730Q	Samples
LM73C1QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	731Q	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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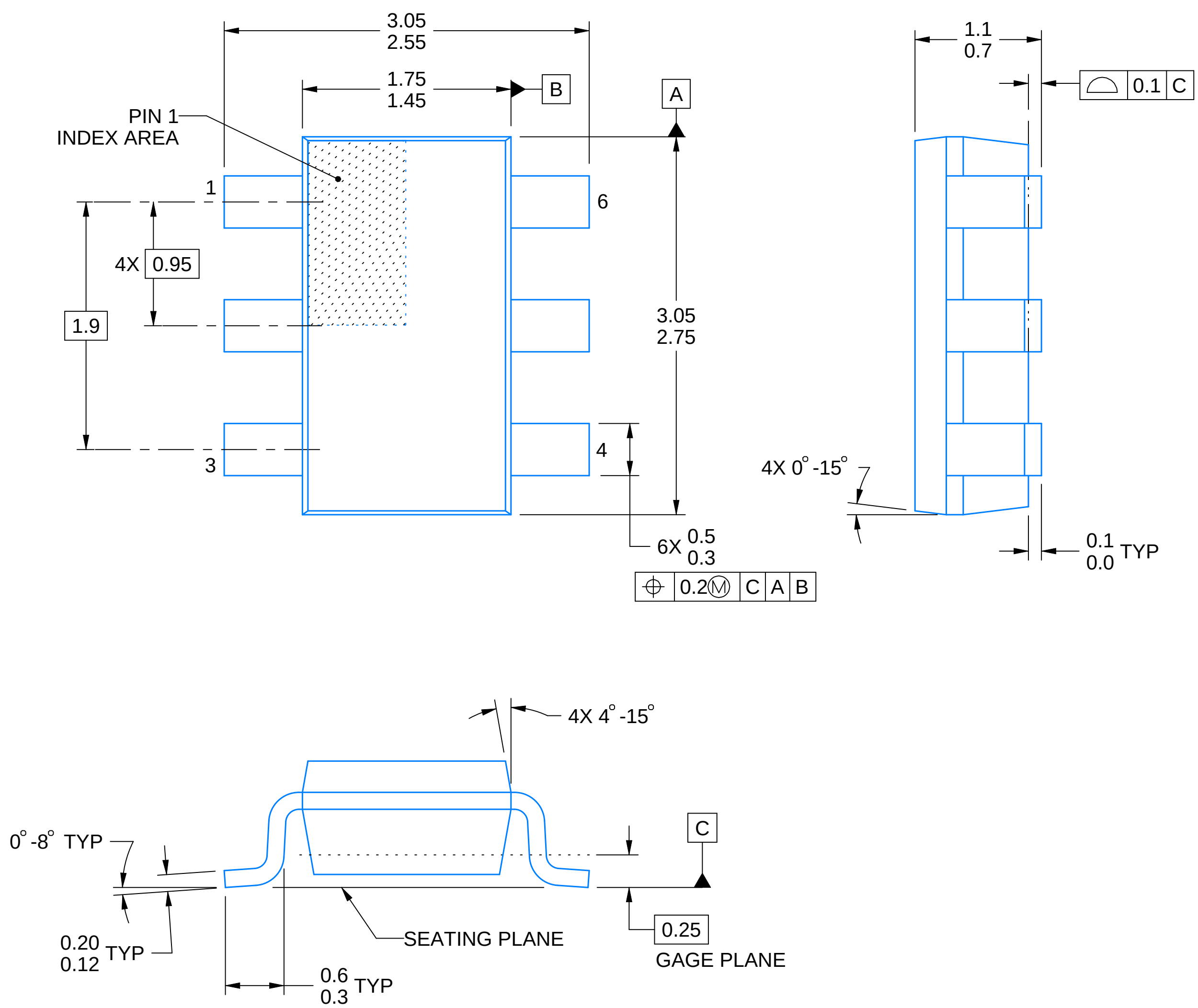

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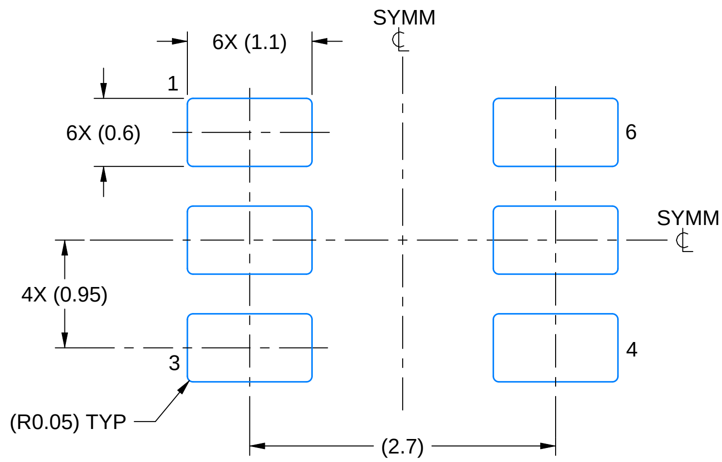
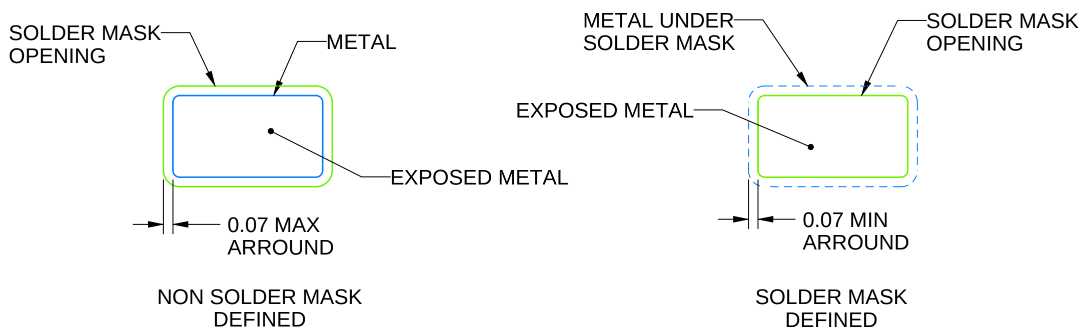
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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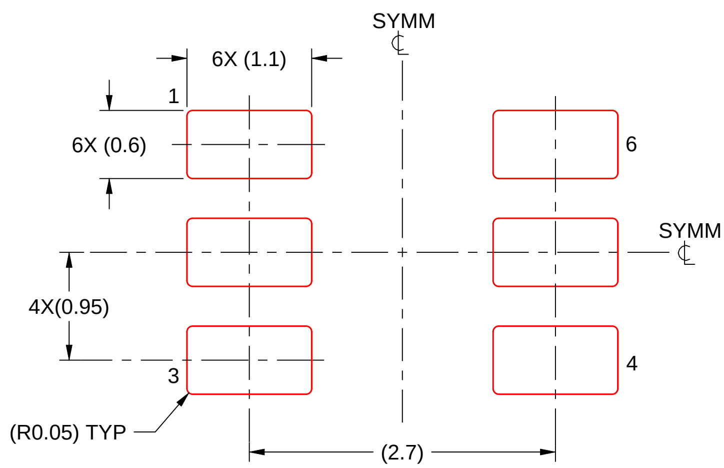
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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