LMK62XX 高性能低抖动振荡器

1 特性

- 低噪声、高性能
  - 抖动：150fs RMS 典型值 Fout > 100MHz
  - PSRR：–60dBc，具有强大的抗电源噪声能力
- 支持的输出格式：
  - 低压正发射极耦合逻辑 (LVPECL)、低压差分信令 (LVDS) 和高速收发器逻辑 (HCSL) 高达 400MHz
- 总频率容差：±50ppm (LMK62X2) 和 ±25ppm (LMK62X0)
- 3.3V 工作电压
- 工业温度范围：–40°C 至 +85°C
- 5mm × 3.2mm 6 引脚封装，与业界通用 5032 XO 封装引脚兼容

2 应用

- 晶体振荡器、SAW 振荡器或芯片振荡器的高性能替代产品
- 开关、路由器、网卡、基带装置 (BBU)、服务器、存储/SAN
- 测试和测量
- 医疗成像
- FPGA、处理器连接

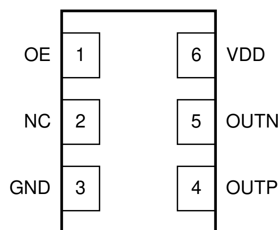
3 说明

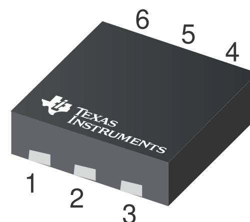
LMK62XX 器件是一款低抖动振荡器，可生成常用参考时钟。该器件在工厂预编程，可支持任何参考时钟频率；支持的输出格式是 LVPECL、LVDS 和 HCSL（最高 400MHz）。内部电源调节功能提供出色的电源纹波抑制 (PSRR)，降低了供电网络的成本和复杂性。该器件由单个 3.3V ± 5% 电源供电。

器件信息

器件型号	输出频率 (MHz) 及格式	总频率稳定性 (ppm)	封装尺寸[(1)] [(2)]
LMK62E2-100M	100 LVPECL	±50	SIA（QFM，6）5.00mm × 3.20mm
LMK62E2-156M	156.25 LVPECL	±50	
LMK62E0-156M	156.25 LVPECL	±25	
LMK62A2-100M	100 LVDS	±50	
LMK62A2-150M	150 LVDS	±50	
LMK62A2-156M	156.25 LVDS	±50	
LMK62A2-200M	200 LVDS	±50	
LMK62A2-266M	266.66 LVDS	±50	
LMK62I0-100M	100 HCSL	±25	
LMK62I0-156M	156.25 HCSL	±25	

(1) 有关所有可用封装，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。





引脚分配

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

English Data Sheet: SNAS691

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4 Pin Configuration and Functions

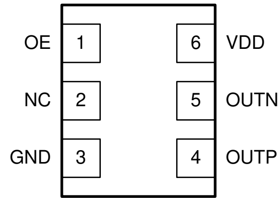

图 4-1. SIA Package 6-pin QFM Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device ground
VDD	6	Analog	3.3-V power supply
OUTPUT BLOCK			
OUTP	4	Universal	Differential output pair (LVPECL, LVDS or HCSL).
OUTN	5		
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No connect
OE	1	LVCMOS	Output enable (internal pulldown). When set to low, output pair is disabled and set at high impedance. The recommended external pullup resistor value is 10 kΩ.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			105	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

5.4 Thermal Information

THERMAL METRIC(1)		LMK62XX (2) (3) (4)	UNIT
		SIA (QFM)	
		6 PINS	
		Airflow (LFM) 0	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4-layer JEDEC board.
(3) Connected to GND with 2 thermal vias (0.3-mm diameter).
(4) ψ_{JB} (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

5.5 Electrical Characteristics - Power Supply

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL(2)		95	110	mA
		LVDS		85	100	
		HCSL(3)		90	105	
IDD-PD	Device current consumption when output is disabled	OE = GND		70		mA

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150-Ω termination resistors, from total power dissipation.
(3) Excludes load current.

5.6 LVPECL Output Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)				400	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(2)		700	950	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\lvert V_{OD}\rvert$		V
V_{OS}	Output common-mode voltage			VDD – 1.45		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			260	350	ps
ODC	Output duty cycle(3)		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.

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(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

5.7 LVDS Output Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency[(1)]				400	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})[(1)]		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 x $\lvert V_{OD}\rvert$		V
V_{OS}	Output common-mode voltage		1.125	1.2	1.375	V
t_R / t_F	Output rise/fall time (20% to 80%)[(2)]			260	350	ps
ODC	Output duty cycle[(2)]		45%		55%	
R_{OUT}	Differential output impedance			107		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

5.8 HCSL Output Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency				400	MHz
V_{OH}	Output high voltage		660		900	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage[(2) (3)]		250		475	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} [(2) (3)]		0		140	mV
dV/dt	Slew rate[(4)]		1		3	V/ns
ODC	Output duty cycle[(4)]		45%		55%	

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

5.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

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5.10 Frequency Tolerance Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	LMK62X2: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	–50		50	ppm
		LMK62X0: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	–25		25	ppm

(1) Ensured by characterization.

5.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage[(1)]		2.85		3	V
V_{DROOP}	Allowable voltage droop[(2)]				0.1	V
$t_{STARTUP}$	Start-up time [(1)]	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time[(2)]	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time[(2)]	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Ensured by characterization.
(2) Ensured by design.

5.12 PSRR Characteristics

VDD = 3.3 V, T_A = 25°C[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple[(2)] [(3)] at 156.25-MHz output, all output types	Sine wave at 50 kHz		–60		dBc
		Sine wave at 100 kHz		–60		
		Sine wave at 500 kHz		–60		
		Sine wave at 1 MHz		–60		

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π *f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

5.13 PLL Clock Output Jitter Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C[(1)] [(3)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter[(2)] (12 kHz – 20 MHz)	$f_{OUT} \geq$ 100 MHz, all output types		150	250	fs RMS

(1) See *Parameter Measurement Information* for relevant test conditions.
(2) Ensured by characterization.
(3) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

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5.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6 Parameter Measurement Information

6.1 Device Output Configurations

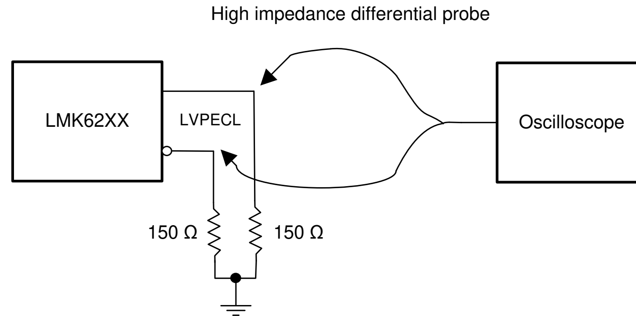

图 6-1. LVPECL Output DC Configuration During Device Test

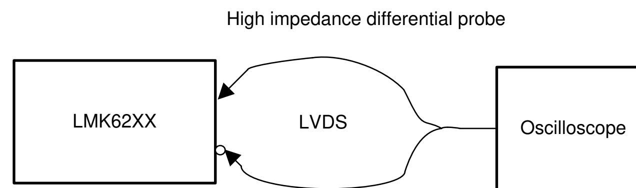

图 6-2. LVDS Output DC Configuration During Device Test

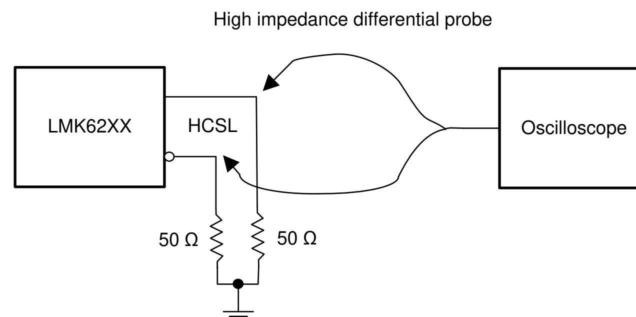

图 6-3. HCSL Output DC Configuration During Device Test [1]

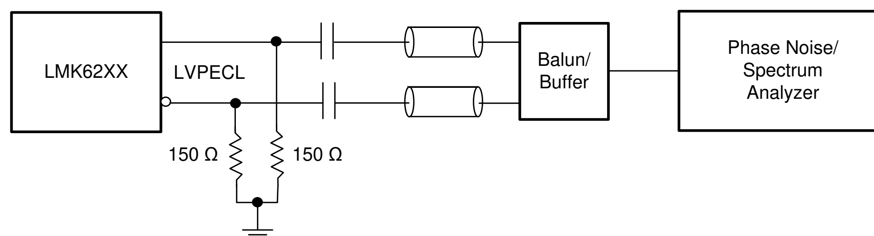

图 6-4. LVPECL Output AC Configuration During Device Test

[1] Also compatible with 85 Ω termination

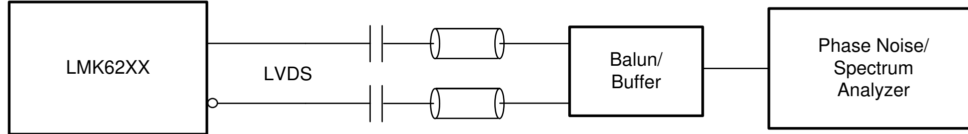

图 6-5. LVDS Output AC Configuration During Device Test

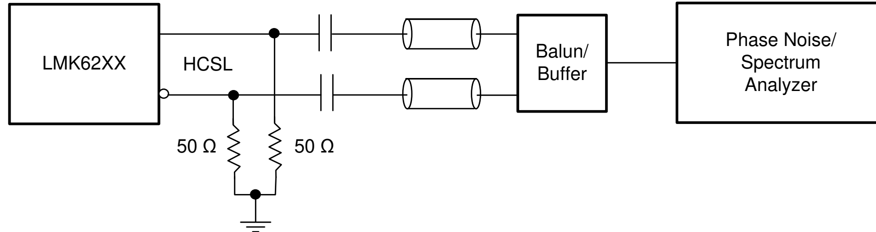

图 6-6. HCSL Output AC Configuration During Device Test

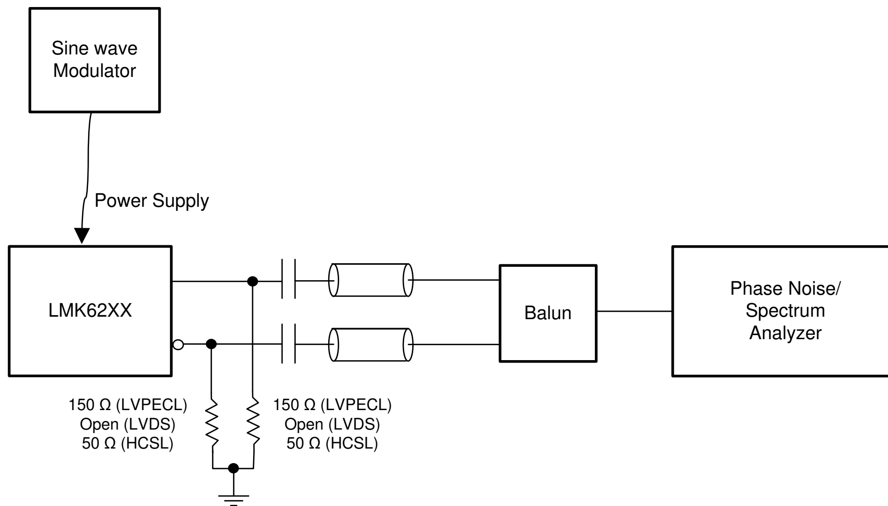

图 6-7. PSRR Test Setup

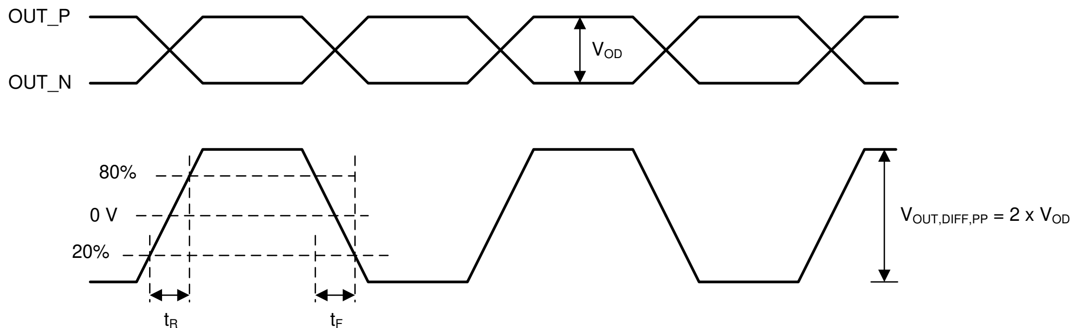

图 6-8. Differential Output Voltage and Rise/Fall Time

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

For best electrical performance of LMK62XX, TI recommends using a combination of 10 µF, 1 µF, and 0.1 µF on the power-supply bypass network of the device. TI also recommends using component side mounting of the power-supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. 图 7-1 shows the layout recommendation for power supply decoupling of LMK62XX.

7.2 Layout

7.2.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK62XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

7.2.1.1 Ensuring Thermal Reliability

The LMK62XX is a high-performance device. Therefore, pay careful attention to the device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in 图 7-1, to maximize thermal dissipation out of the package.

方程式 1 shows the relationship between the PCB temperature around the LMK62XX and the junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \qquad (1)$$

where

- T_B: PCB temperature around the LMK62XX
- T_J: Junction temperature of LMK62XX
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK62XX (64.1°C/W without airflow)
- P: On-chip power dissipation of LMK62XX

To ensure that the maximum junction temperature of LMK62XX is below 105°C, it can be calculated that the maximum PCB temperature without airflow should be at 81°C or below when the device is optimized for best performance, resulting in maximum on-chip power dissipation of 0.36 W.

7.2.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK62XX, TI recommends routing vias into decoupling capacitors and then into the LMK62XX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. 图 7-1 shows the layout recommendation for LMK62XX.

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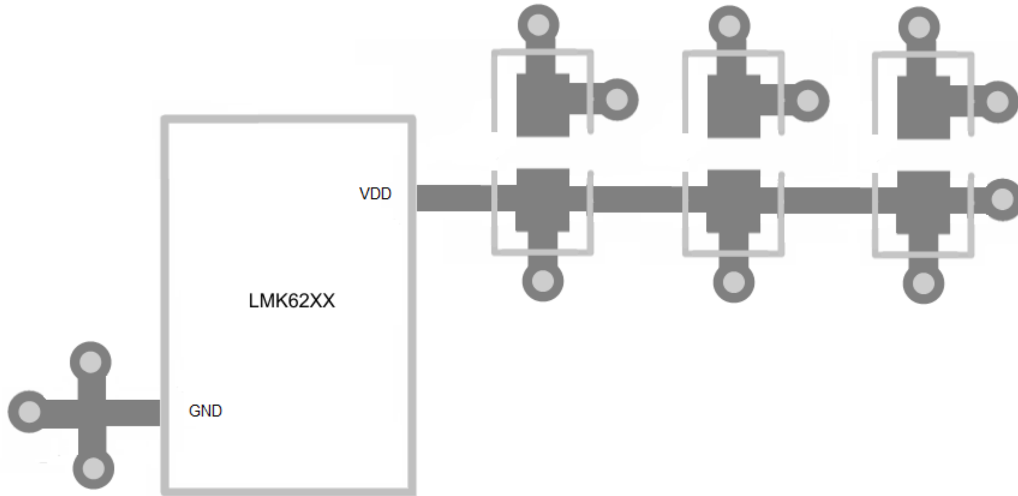

图 7-1. LMK62XX Layout Recommendation for Power Supply and Ground

7.2.1.3 Recommended Solder Reflow Profile

TI recommends following the recommendations set by the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing LMK62XX with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferred. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well as the recommended soldering profile from the manufacturer, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

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8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

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8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (July 2018) to Revision E (December 2023) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式......1
- 更改了*器件信息* 表......1
- Changed the OE pin description in the *Pin Functions* table......3

Changes from Revision C (December 2017) to Revision D (July 2018) — **Page**

- Added V_{OS} minimum and maximum values to the *LVDS Output Characteristics* table......5

Changes from Revision B (June 2017) to Revision C (December 2017) — **Page**

- 在器件列表中增加了 LMK62E2-100M、LMK62I0-100M 和 LMK62I0-156M......1

Changes from Revision A (April 2017) to Revision B (June 2017) — **Page**

- 在器件列表中增加了 LMK62E0-156M、LMK62A2-100M、LMK62A2-150M、LMK62A2-156M、LMK62A2-200M 和 LMK62A2-266M......1

Changes from Revision * (December 2016) to Revision A (April 2017) — **Page**

- 将预告信息数据表更改为量产数据......1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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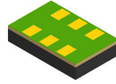

PACKAGE OUTLINE

SIA0006B

QFM - 1.1 mm max height

QUAD FLAT MODULE

B
3.3
3.1
A
PIN 1 INDEX AREA
5.1
4.9
1.1 MAX
C
SEATING PLANE
0.1 C
2.1
6X (0.1)
3
4
2X
2.54
4X
1.27
SYMM
1
6
6X 0.67
0.61
0.1Ⓜ C A B
0.05Ⓜ C
SYMM
6X 0.93
0.87

4223058/A 06/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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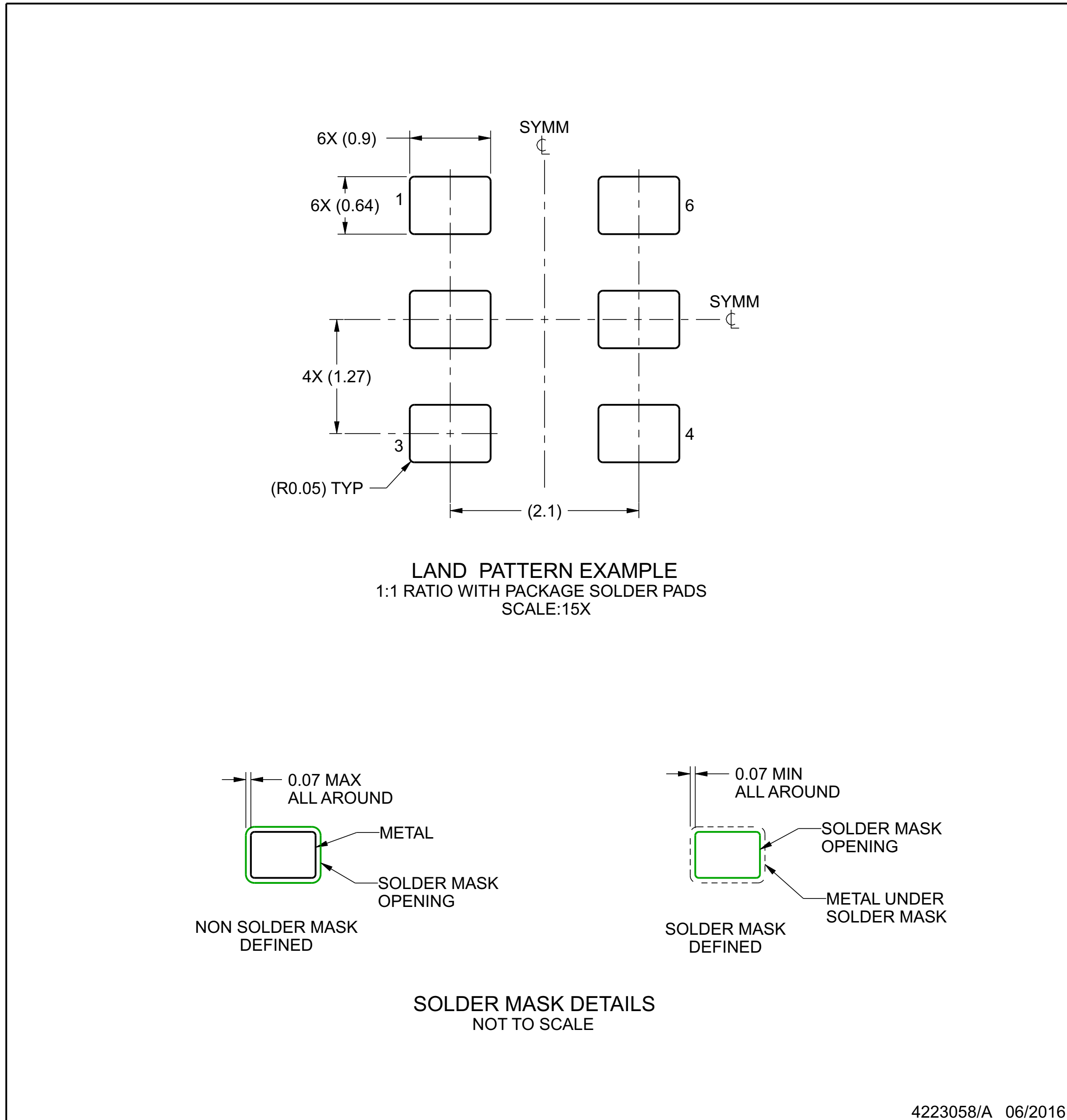
EXAMPLE BOARD LAYOUT

SIA0006B

QFM - 1.1 mm max height

QUAD FLAT MODULE



NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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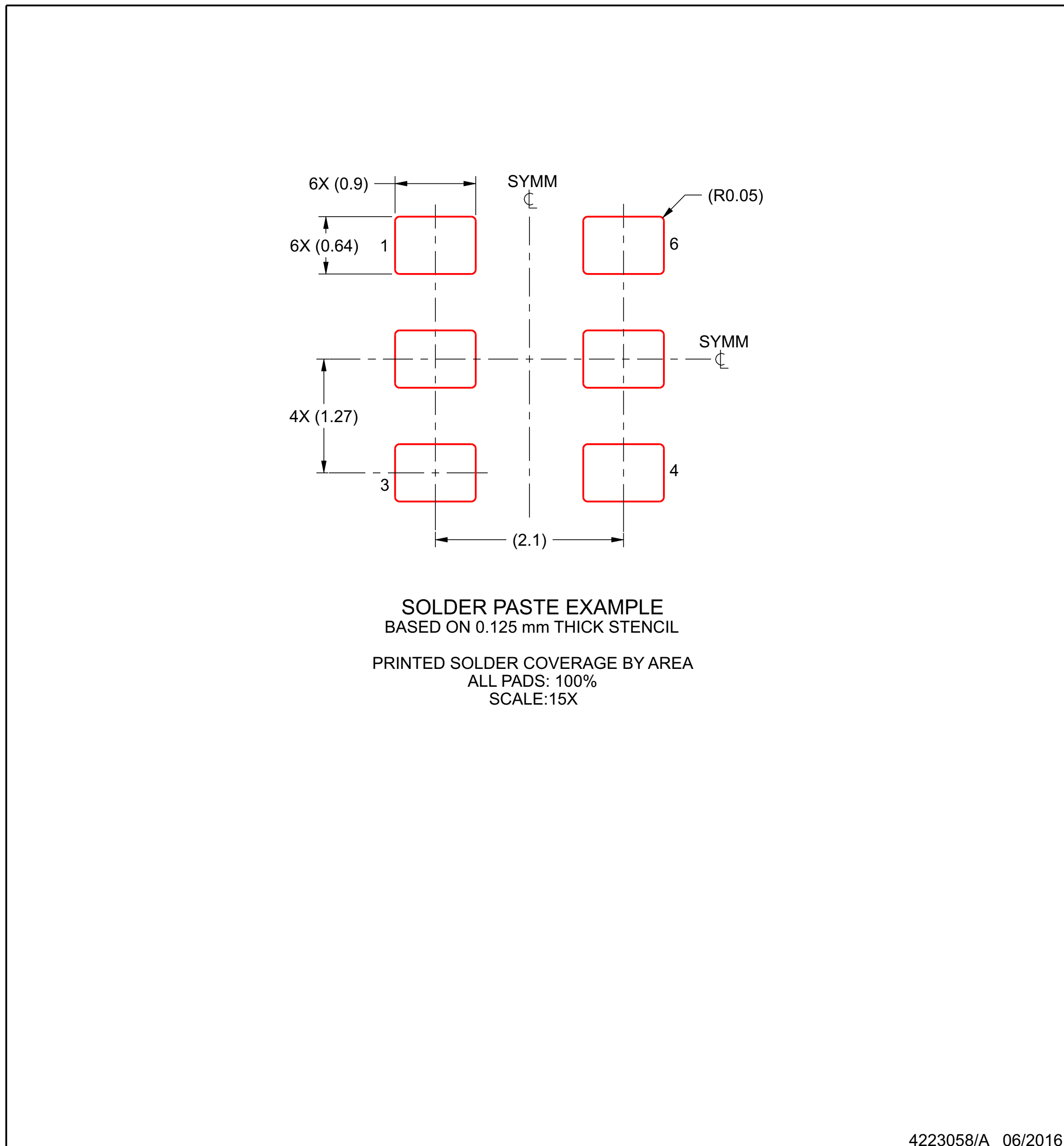
EXAMPLE STENCIL DESIGN

SIA0006B

QFM - 1.1 mm max height

QUAD FLAT MODULE



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK62A2-100M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 10000	
LMK62A2-100M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 10000	
LMK62A2-150M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 15000	
LMK62A2-150M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 15000	
LMK62A2-156M25SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 15625	
LMK62A2-156M25SIAT	NRND	QFM	SIA	6	250	RoHS (In Work) & Green (In Work)	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 15625	
LMK62A2-200M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 20000	
LMK62A2-200M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 20000	
LMK62A2-266M66SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 26666	Samples
LMK62A2-266M66SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62A2 26666	
LMK62E0-156M25SIAR	NRND	QFM	SIA	6	2500	RoHS (In Work) & Green (In Work)	NIAU	Level-3-260C-168 HR	-40 to 85	62E0 15625	
LMK62E0-156M25SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62E0 15625	
LMK62E2-100M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62E2 10000	
LMK62E2-100M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62E2 10000	
LMK62E2-156M25SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62E2 15625	
LMK62E2-156M25SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62E2 15625	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK62I0-100M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62I0 10000	
LMK62I0-100M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62I0 10000	
LMK62I0-156M25SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62I0 15625	
LMK62I0-156M25SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	62I0 15625	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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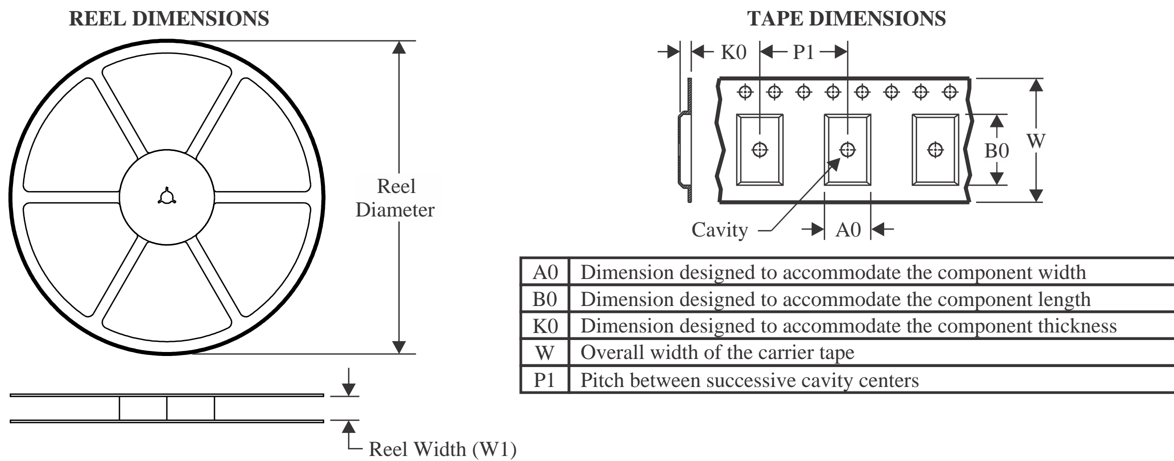
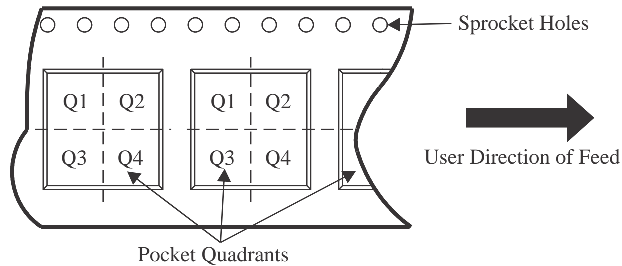
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

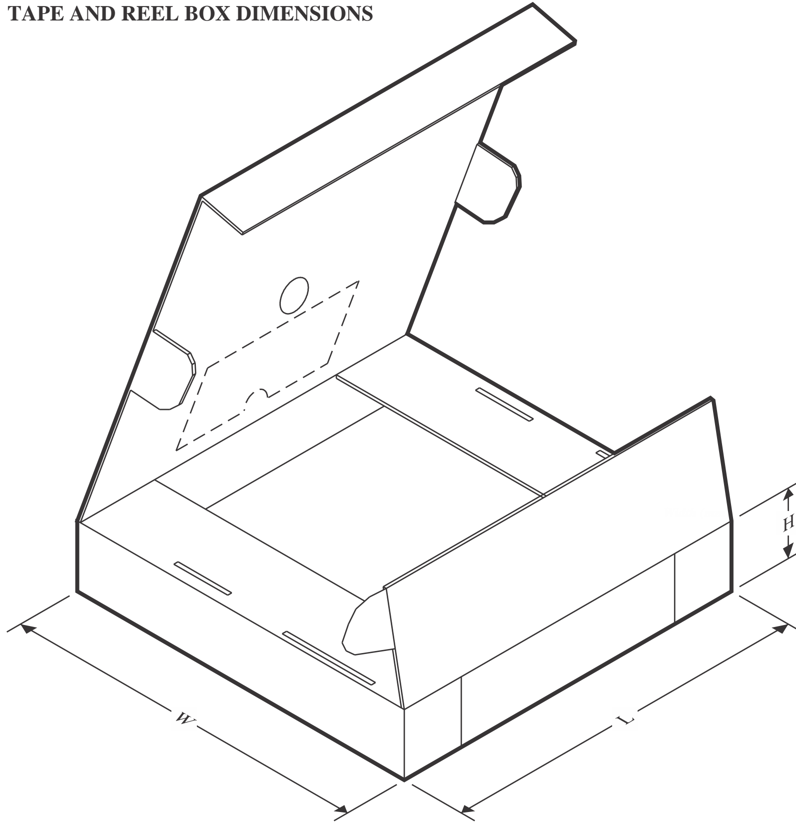


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK62A2-100M00SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-100M00SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-150M00SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-150M00SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-156M25SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-156M25SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-200M00SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-200M00SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-266M66SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62A2-266M66SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E0-156M25SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E0-156M25SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E2-100M00SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E2-100M00SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E2-156M25SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62E2-156M25SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK62I0-100M00SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62I0-100M00SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62I0-156M25SIAR	QFM	SIA	6	2500	330.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1
LMK62I0-156M25SIAT	QFM	SIA	6	250	180.0	12.4	3.5	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK62A2-100M00SIAR	QFM	SIA	6	2500	367.0	367.0	35.0
LMK62A2-100M00SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62A2-150M00SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62A2-150M00SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62A2-156M25SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62A2-156M25SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62A2-200M00SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62A2-200M00SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62A2-266M66SIAR	QFM	SIA	6	2500	367.0	367.0	35.0
LMK62A2-266M66SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62E0-156M25SIAR	QFM	SIA	6	2500	367.0	367.0	35.0
LMK62E0-156M25SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62E2-100M00SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62E2-100M00SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62E2-156M25SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62E2-156M25SIAT	QFM	SIA	6	250	210.0	185.0	35.0
LMK62I0-100M00SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62I0-100M00SIAT	QFM	SIA	6	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK62I0-156M25SIAR	QFM	SIA	6	2500	346.0	346.0	33.0
LMK62I0-156M25SIAT	QFM	SIA	6	250	210.0	185.0	35.0

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