1.5A、24V、17MHz 功率运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
- 高输出电流：1.5A
- 宽电源电压范围：
  - 单电源：7V 至 24V
  - 双电源：±3.5V 至 ±12V
- 大输出摆幅：$20V_{PP}$（1.5A 时）
- 全面保护：
  - 热关断
  - 可调电流限制
- 诊断标志：
  - 过流
  - 热关断
- 输出使能和关断 (E/$\overline{S}$) 控制
- 高速：
  - 增益带宽积：17MHz
  - 全功率带宽（$10V_{PP}$ 时）：1.3MHz
  - 压摆率：40V/μs
- 用于结温监控的二极管
- HSOIC-20 PowerPAD™ 集成电路封装

2 应用

- 电力线通信
- 旋转变压器驱动器
- 阀和致动器驱动器
- V_{COM} 驱动器
- 电机驱动器
- 音频功率放大器
- 电源输出放大器
- 测试设备放大器
- 传感器激励
- 激光二极管驱动器
- 通用线性电源升压器

3 说明

OPA564-Q1 是一款低成本、高电流运算放大器，非常适合用于将高达 1.5A 电流驱动至无功负载。高压摆率可提供 1.3MHz 的全功率带宽和出色的线性度。这些单片集成电路可以在要求严格的电力线通信和电机控制应用中提供高可靠性。

OPA564-Q1 可由 7V 至 24V 的单电源或者 ±3.5V 至 ±12V 的双电源供电。在单电源操作中，输入共模范围可扩展至负电源。在最大输出电流下，宽输出摆幅能够以标称 24V 的电源电压提供 $20V_{PP}$ (I_{OUT} = 1.5A) 性能。

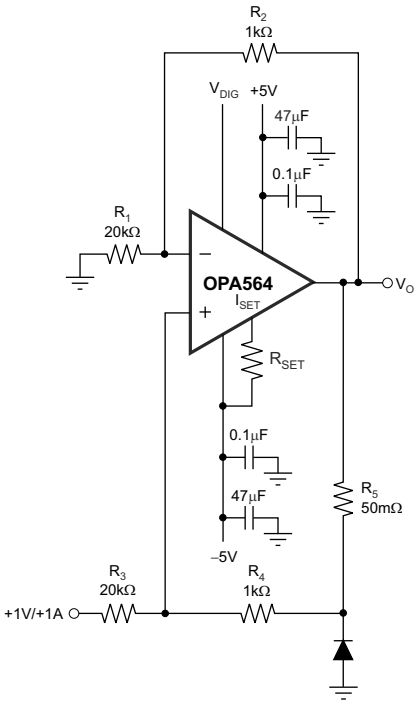
OPA564-Q1 在过热条件下以及电流过载时会受到内部保护。该器件可提供准确的用户自选的电流限制。提供的两个标志输出：一个表示电流限制，另一个显示过热情况。该器件还具有使能和关断 (E/$\overline{S}$) 引脚，该引脚可强制为低电平以关闭输出，从而有效地断开负载。

OPA564-Q1 采用热增强型、表面贴装 PowerPAD 集成电路封装 (HSOIC-20)。

封装信息

器件型号(1)	封装(2)	封装尺寸(3)
OPA564-Q1	DWP（HSOIC，20）	12.825mm × 10.405mm

(1) 请参阅节 4。
(2) 如需更多信息，请参阅节 11。
(3) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



改进型 Howland 电流泵

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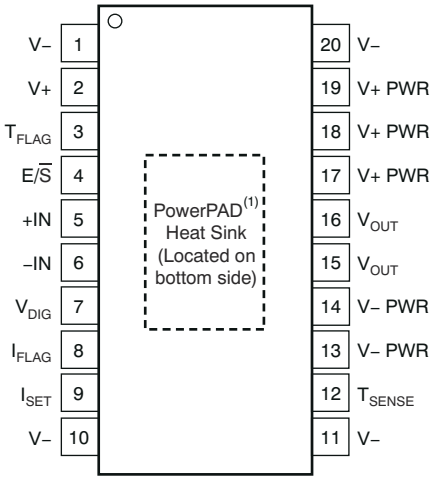
4 Device Comparison Table

DEVICE	DESCRIPTION
TMP141-Q1	Automotive Grade, ±1°C Remote and Local Temperature Sensor With N-Factor and Series-R Correction
OPA333-Q1	Automotive, microPower, 1.8V, 17µA Zero-Drift CMOS Precision Operational Amplifier
TLE427-Q1	Automotive 450mA, Off-Battery (42V), Low-Dropout Voltage Regulator With RESET With Delay
OPA561	Power Operational Amplifier, 1.2A, 15V, 17MHz, 50V/µs

5 Pin Configuration and Functions



(1) PowerPAD is internally connected to V–, Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.

图 5-1. DWP Package, 20-Pin HSOIC (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
E/$\overline{S}$	4	Input	Enable/$\overline{Shutdown}$ output stage; take E/$\overline{S}$ low to shut down output
I_{FLAG}	8	Output	Current limit flag; active high
I_{SET}	9	Input	Current limit set (see 节 8.1)
– IN	6	Input	Inverting op amp input
+IN	5	Input	Noninverting op amp input
T_{FLAG}	3	Output	Thermal overtemperature flag; flag is high when alarmed and device has gone into thermal shutdown
T_{SENSE}	12	Input/Output	Temperature sense pin for use with a remote junction temperature sensor
V –	1, 10, 11, 20	Ground	– Supply for amplifier, PWR Out, and thermal pad
V – PWR	13, 14	Ground	– Supply for power output stage
V+	2	Power	+Supply for signal amplifier
V+ PWR	17, 18, 19	Power	+Supply for power output stage
V_{DIG}	7	Power	+Supply for digital flag and E/$\overline{S}$ (referenced to V –). Valid range is (V –) + 3.0V ≤ V_{DIG} ≤ (V –) + 5.5V.
V_{OUT}	15, 16	Output	Output voltage; R_O is high impedance when shut down
Pad	Thermal Pad	—	Thermal pad. Connect to V –

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			26	V
	Signal input pins	Voltage(2)	(V–) – 0.4	(V+) + 0.4	V
		Current through ESD diodes(2)		±10	mA
		Maximum differential voltage across inputs(3)		0.5	V
	Signal output pins	Voltage	(V–) – 0.4	(V+) + 0.4	V
		Current(4)		±10	mA
	Output short-circuit(5)			Continuous	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	150	°C
	Latch-up per JESD78B			Class 1 Level B	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit signals that can swing more than 0.4V beyond the supply rails to 10mA or less.
(3) See 图 7-7 for information on input protection. See also 节 7.3.3.
(4) Output pins are diode-clamped to the power-supply rails. Current limit input signals forcing the output pin more than 0.4V beyond the supply rails to 10mA or less.
(5) Short-circuit to ground within SOA. See also 节 8.1.4.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	4000	V
		Charged device model (CDM), per AEC Q100-011	1000	
		Machine model (MM)	200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted

		MIN	NOM	MAX	UNIT
V_S	Supply voltage(1)	7		24	V
V_{DIG}	Digital supply voltage	(V–) + 3.0		(V–) + 5.5	V
T_A	Operating ambient temperature(2)	–40		125	°C

(1) Power-supply sequencing requirements must be observed; see also 节 8.3.
(2) The OPA564-Q1 typically goes into thermal shutdown at a junction temperature greater than 140°C.

6.4 Thermal Information

THERMAL METRIC(1)		OPA564-Q1 DWP (HSOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

at T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = 0V			±2	±20	mV
dV_{OS}/dT	vs temperature	T_A = –40°C to +125°C			±10		µV/°C
PSRR	vs power supply	V_{CM} = 0V, V_S = ±3.5V to ±13V			10	150	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)	V_{CM} = 0V			10	100	pA
	vs temperature	T_A = –40°C to +125°C			See 图 6-10		
I_{OS}	Input offset current(1)				10	100	pA
NOISE							
e_n	Input voltage noise density	f = 1kHz			102.8		nV/√Hz
		f = 10kHz			20		nV/√Hz
		f = 100kHz			8		nV/√Hz
I_n	Input current noise	f = 1kHz			4		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage	Linear operation		(V–)		(V+) – 3	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) to (V+) – 3V		70	80		dB
		V_{CM} = (V–) to (V+) – 3V, T_A = –40°C to +125°C			See 图 6-9		
INPUT IMPEDANCE							
	Input impedance	Differential			10^{12} || 16		Ω || pF
		Common-mode			10^{12} || 9		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_{OUT} = $20V_{PP}$, R_{LOAD} = 1kΩ		80	108		dB
		V_{OUT} = $20V_{PP}$, R_{LOAD} = 10Ω			93		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product(1)	R_{LOAD} = 5Ω			17		MHz
SR	Slew rate	G = 1, 10V step			40		V/µs
	Full power bandwidth	G = +2, V_{OUT} = $10V_{PP}$			1.3		MHz
	Settling time	G = +1, 10V step, C_{LOAD} = 100pF	±0.1%		0.6		µs
			±0.01%		0.8		µs
THD+N	Total harmonic distortion + noise	f = 1kHz, R_{LOAD} = 5Ω, G = +1, V_{OUT} = $5V_P$			0.003		%

6.5 Electrical Characteristics（续）

at T_{CASE} = +25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_{OUT}	Voltage output	Positive	I_{OUT} = 0.5A	(V+) – 1	(V+) – 0.4		V
			I_{OUT} = 1.5A	(V+) – 2	(V+) – 1.5		V
		Negative	I_{OUT} = –0.5A	(V–) + 1	(V–) + 0.3		V
			I_{OUT} = –1.5A	(V–) + 2	(V–) + 1.1		V
I_{OUT}	Maximum continuous current, dc				1.5(2)		A
R_O	Output impedance, closed loop	f = 100kHz			10		Ω
Z_O	Output impedance, open loop	G = +2, f = 100kHz			See 图 6-24		
	Output current limit range(3)				±0.4 to ±1.9		A
I_{LIM}	Current limit equation				$I_{LIM} \cong 20k \times \left[\frac{1.2V}{5k\Omega + R_{SET}}\right]$ (4) (5)		A
		Solved for R_{SET} (current limit)			$R_{SET} \cong (24k\Omega / I_{LIM}) - 5k\Omega$		Ω
	Current limit accuracy	I_{LIM} = 1.5A			10		%
	Current limit overshoot(1) (6)	V_{IN} = 5V pulse (200ns t_r), G = +2			50		%
	Output impedance(7)	Output shutdown			6 || 120		GΩ || pF
C_{LOAD}	Capacitive load drive				See 图 6-6		
DIGITAL CONTROL							
	$V_{E/\overline{S}}$ high (output enabled)	V_{DIG} = 3.3V to 5.5V referenced to V–	E/$\overline{S}$ pin open or forced high	(V–) + 2		(V–) + V_{DIG}	V
	$V_{E/\overline{S}}$ Low (output shut down)		E/$\overline{S}$ pin forced low	(V–)		(V–) + 0.8	V
	$I_{E/\overline{S}}$ high (output enabled)		E/$\overline{S}$ pin indicates high		10		µA
	$I_{E/\overline{S}}$ low (output shut down)		E/$\overline{S}$ pin indicates low		1		µA
	Output shutdown time				1		µs
	Output enable time				3		µs
	Current limit flag output	Normal operation, sinking 10 µA			V–	(V–) + 0.8	V
		Current-limited operation, sourcing 20 µA		(V–) + 2	V_{DIG}		V
THERMAL SHUTDOWN							
	Normal operation	Sinking 200 µA			V–	(V–) + 0.8	V
	Thermal shutdown(8)	Sourcing 200 µA		(V–) + 2	V_{DIG}		V
	Junction temperature at shutdown(9)				140 to 157		°C
	Hysteresis(9)				15 to 19		°C
T_{SENSE}							
η	Diode ideality factor				1.033		
POWER SUPPLY(10)							
I_Q	Quiescent current(4)	I_{OUT} = 0A			39	50	mA
		I_{OUT} = 0A, T_A = –40°C to 125°C				50	mA
I_{QSD}	Quiescent current in shutdown mode					5	mA
I_{DIG}	Digital quiescent current	V_{DIG} = 5V			43	100	µA

(1) See 节 6.6.
(2) Under safe operating conditions; see also 节 8.1.4.
(3) Minimum current limit is 0.4A; see also 节 7.3.1.
(4) Quiescent current increases when the current limit is increased (see also 图 6-33).
(5) R_{SET} (current limit) ranges from 55kΩ (I_{OUT} = 400mA) to 10kΩ (I_{OUT} = 1.6A typical); see also 节 7.3.1.
(6) Transient load transition time must be ≥ 200ns.
(7) See also 节 7.3.2.
(8) When sourcing, the V_{DIG} supply must be able to supply the current.
(9) Characterized, but not production tested.
(10) Power-supply sequencing requirements must be observed. See 节 8.3 for more information.

6.6 Typical Characteristics

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

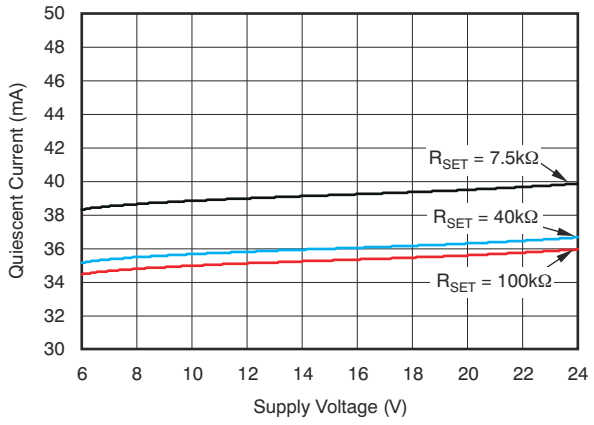


图 6-1. Quiescent Current vs Supply Voltage

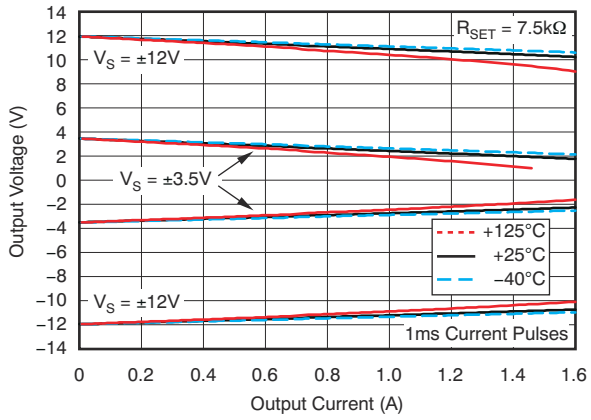
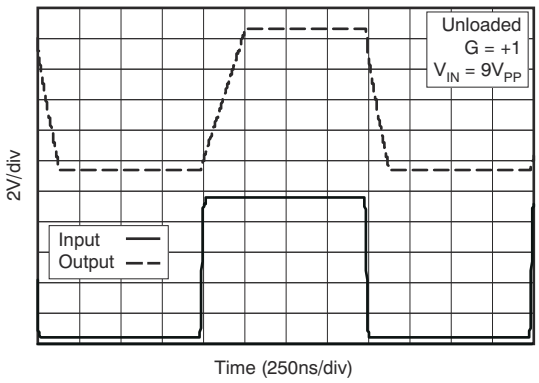


图 6-2. Output Voltage Swing vs Output Current



No load

图 6-3. Large−Signal Step Response

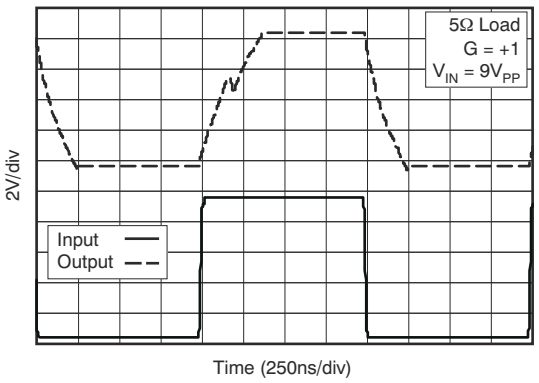


图 6-4. Large−Signal Step Response

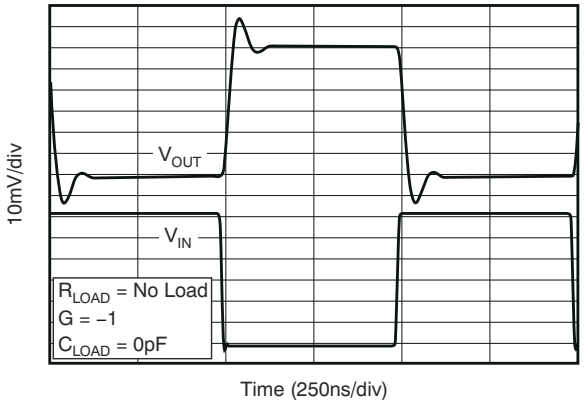


图 6-5. Small−Signal Step Response

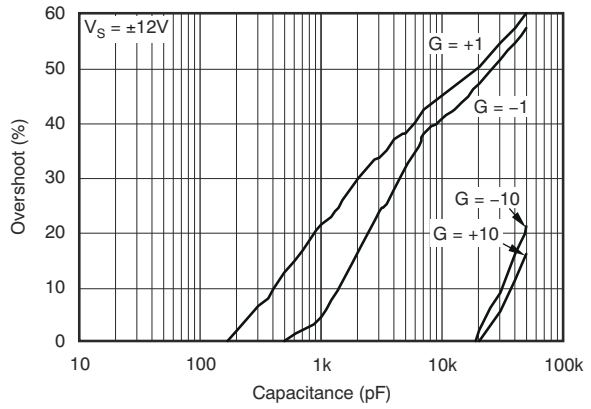


图 6-6. Small−Signal Overshoot vs Load Capacitance

6.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

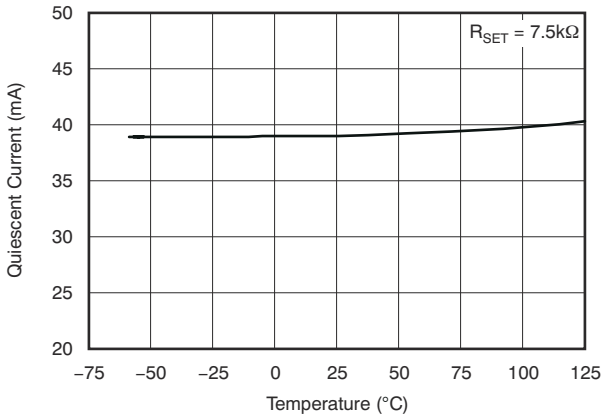


图 6-7. I_Q vs Temperature

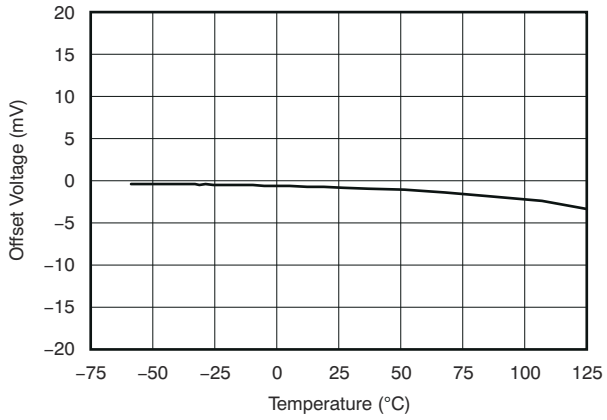


图 6-8. Offset Voltage vs Temperature

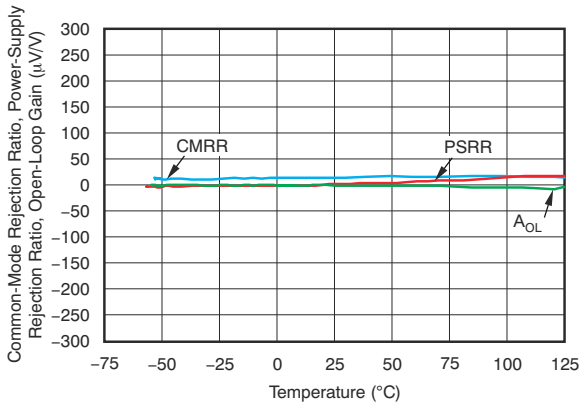


图 6-9. A_{OL}, PSRR, and CMRR vs Temperature

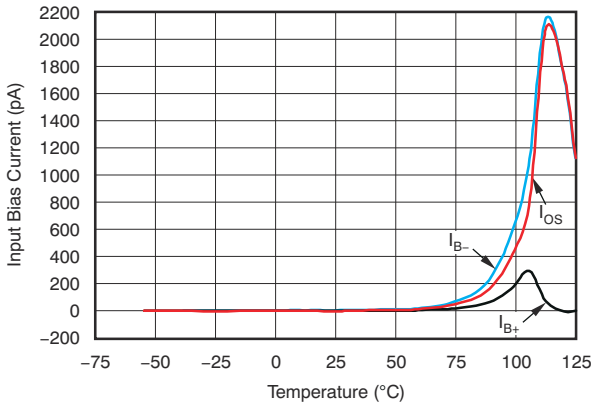


图 6-10. I_B vs Temperature

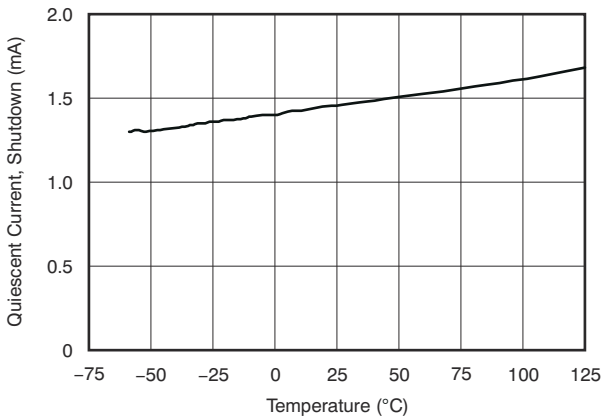


图 6-11. I_Q, Shutdown vs Temperature

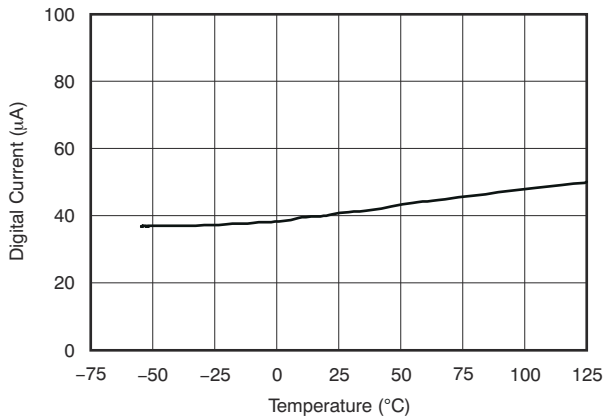


图 6-12. I_{DIG} vs Temperature

6.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

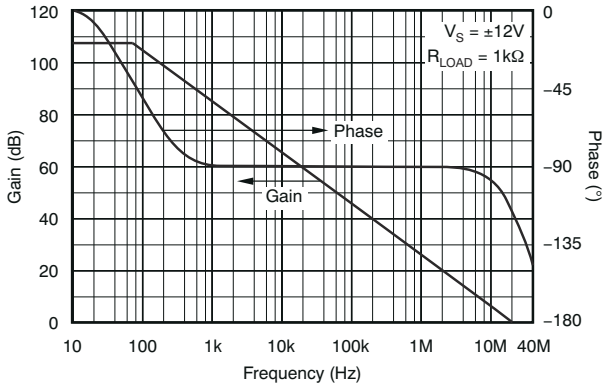


图 6-13. Gain and Phase vs Frequency

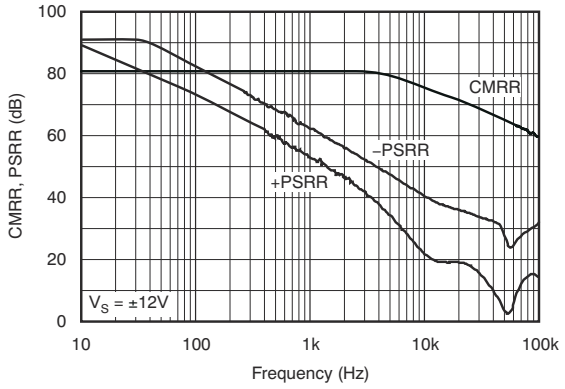


图 6-14. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

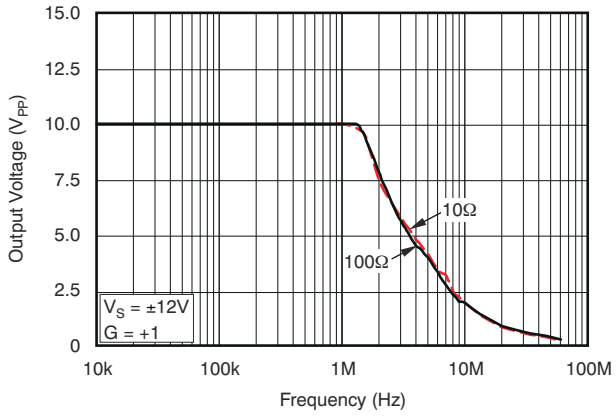


图 6-15. Output Voltage Swing vs Frequency

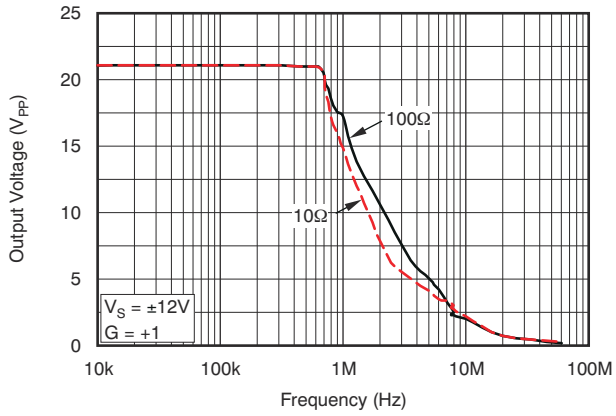


图 6-16. Output Voltage Swing vs Frequency

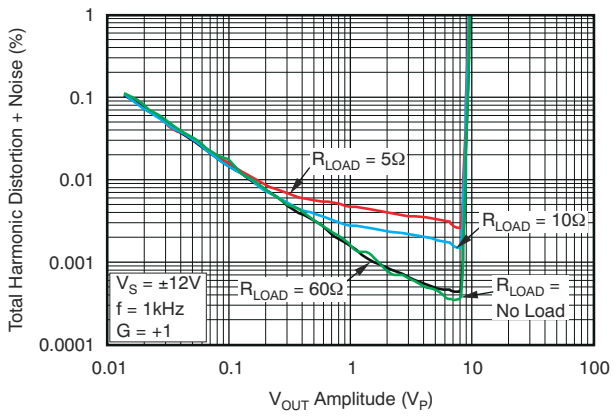


图 6-17. Total Harmonic Distortion + Noise vs Amplitude

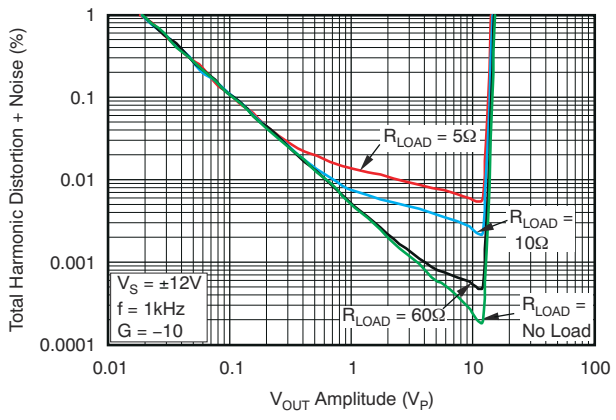


图 6-18. Total Harmonic Distortion + Noise vs Amplitude

6.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

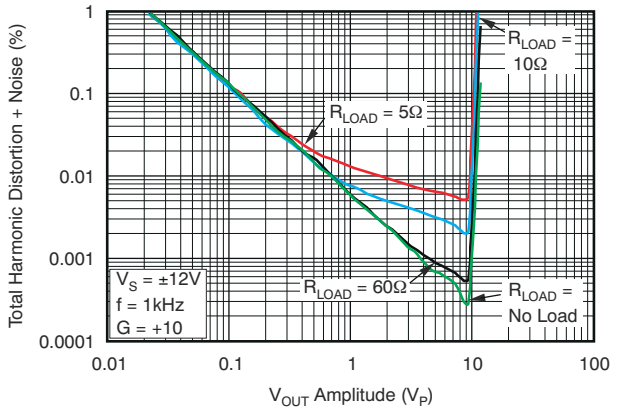


图 6-19. Total Harmonic Distortion + Noise vs Amplitude

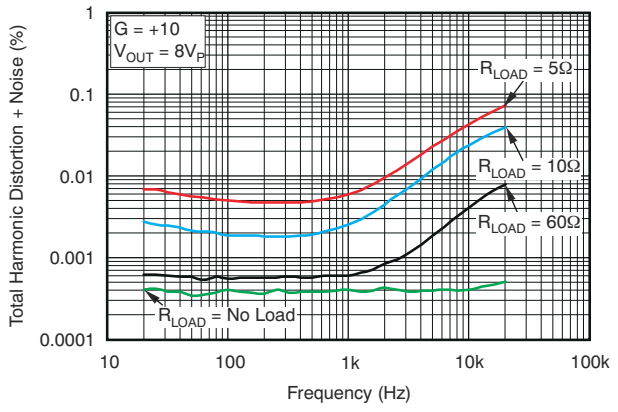


图 6-20. Total Harmonic Distortion + Noise vs Frequency

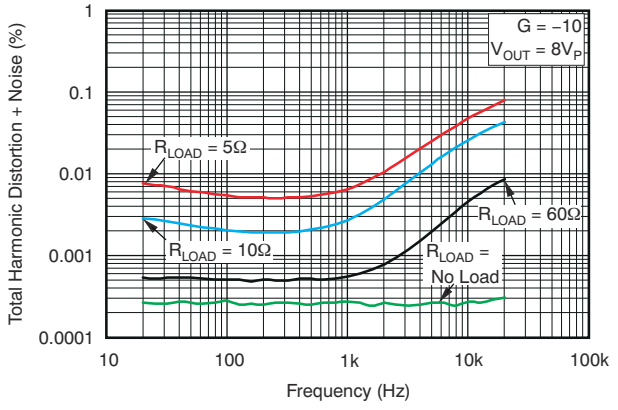


图 6-21. Total Harmonic Distortion + Noise vs Frequency

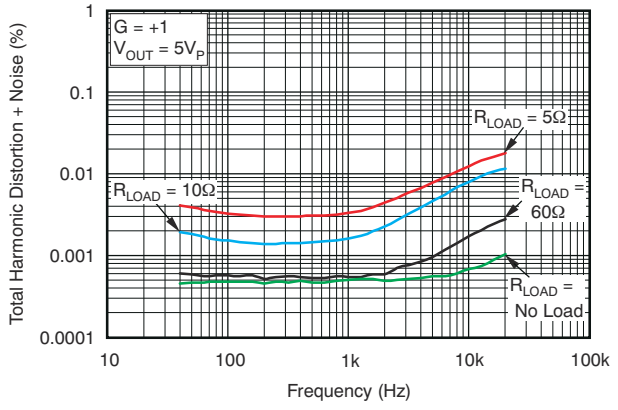


图 6-22. Total Harmonic Distortion + Noise vs Frequency

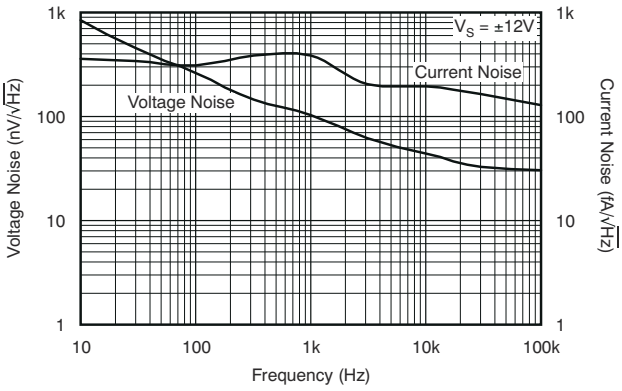
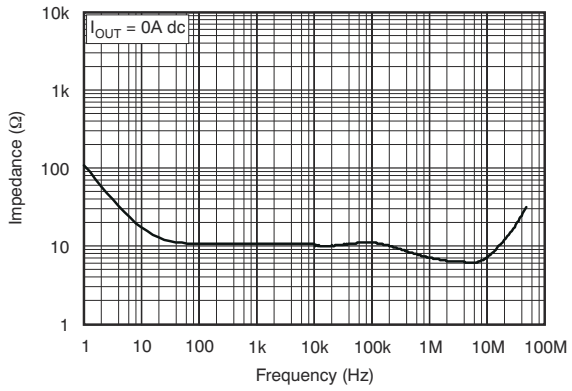


图 6-23. Input Voltage Spectral Noise and Current Noise vs Frequency

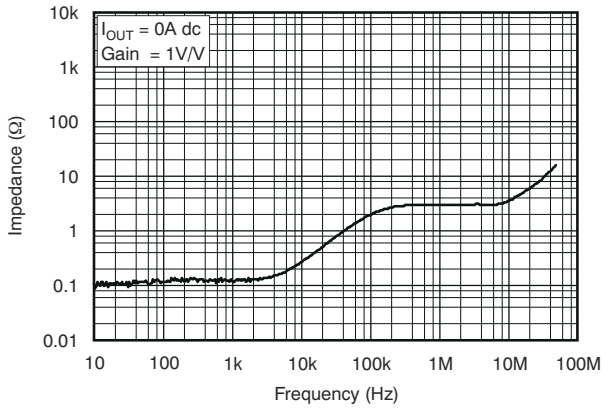


No load

图 6-24. Open-Loop Output Impedance

6.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)



No load

图 6-25. Closed-Loop Output Impedance

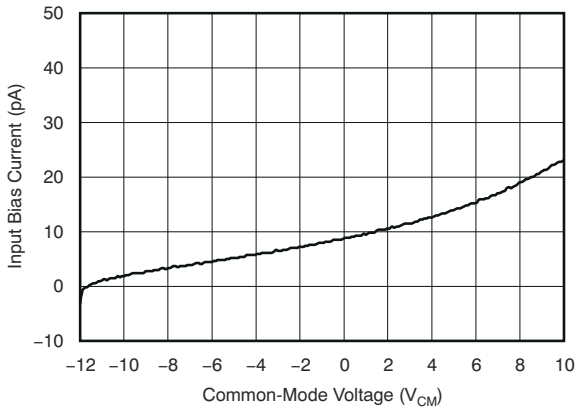
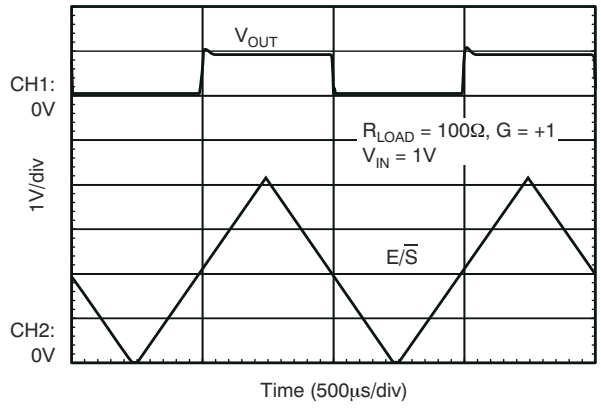


图 6-26. Input Bias Current vs Common-Mode Voltage



R_{LOAD} = 100Ω

图 6-27. Enable Response

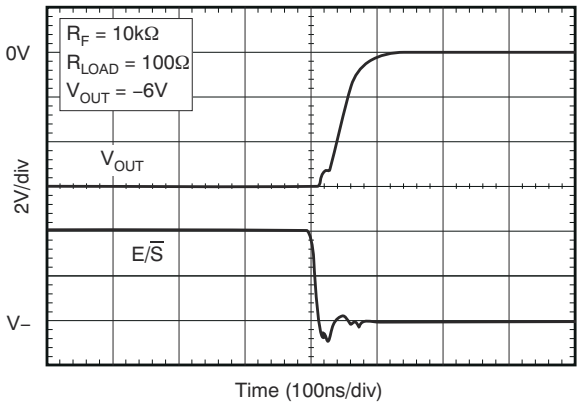


图 6-28. Shutdown Time (Inverting Configuration)

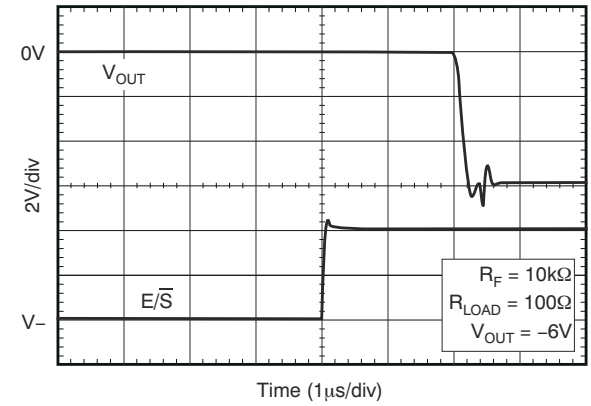


图 6-29. Enable Time (Inverting Configuration)

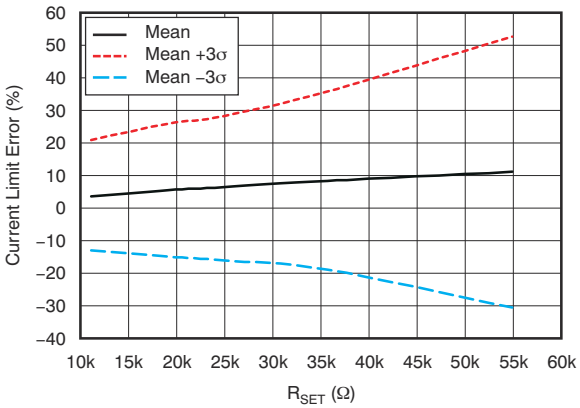


图 6-30. Current Limit Percent Error vs R_{SET}

6.6 Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±12V, R_{LOAD} = 20kΩ to GND, R_{SET} = 7.5kΩ, and E/$\overline{S}$ pin enabled (unless otherwise noted)

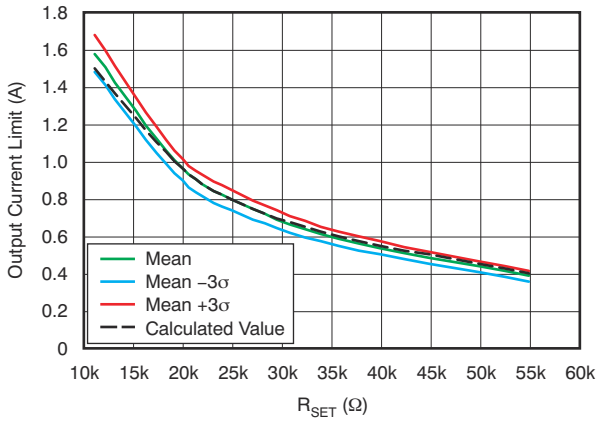


图 6-31. Output Current Limit vs R_{SET} (Sourcing Current)

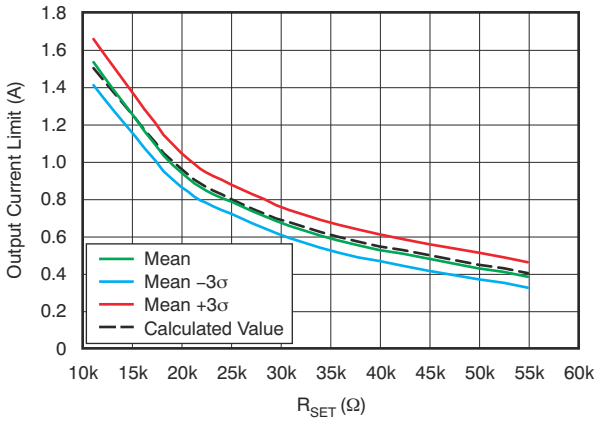


图 6-32. Output Current Limit vs R_{SET} (Sinking Current)

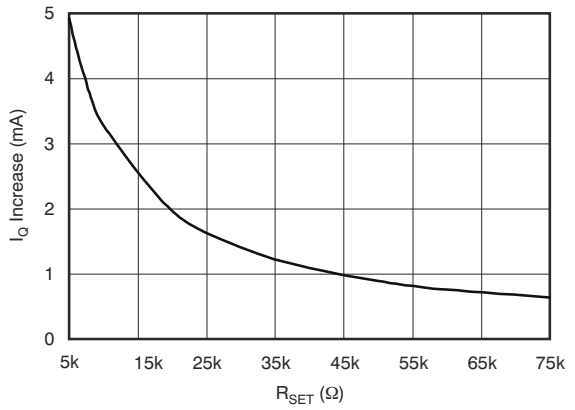


图 6-33. Quiescent Current Increase vs R_{SET}

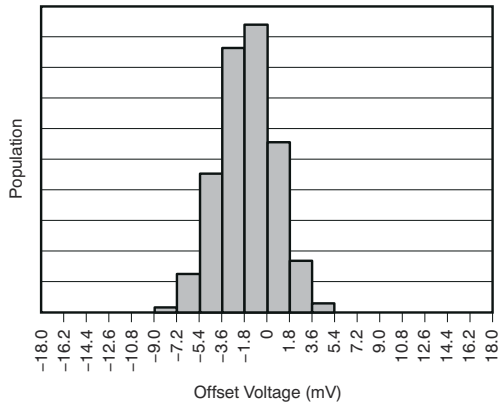


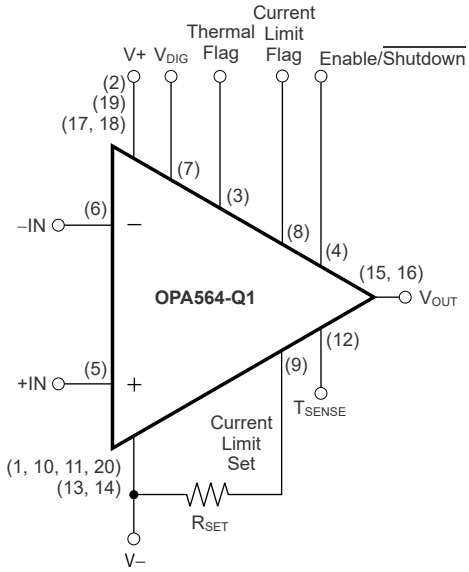
图 6-34. Offset Voltage Production Distribution

7 Detailed Description

7.1 Overview

The OPA564-Q1 is a low-cost, high-current op amp that is an excellent choice for driving up to 1.5A into reactive loads. The high slew rate provides 1.3MHz of full-power bandwidth and excellent linearity. These monolithic integrated circuits provide high reliability in demanding powerline communications and motor-control applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Current Limit

The OPA564-Q1 provides overcurrent protection to the load through an accurate, user-adjustable current limit (I_{SET} pin). The current limit value, I_{LIM}, can be set from 0.4A to 1.6A by controlling the current through the I_{SET} pin. Setting the current limit does not require special power resistors. The output current does not flow through the I_{SET} pin.

A simple resistor to the negative rail is sufficient for a general, coarse limit of the output current. 图 6-30 exhibits the percent of error in the transfer function between I_{SET} and I_{OUT} versus the current limit set resistor, R_{SET}. The ±3 sigma distribution is derived from one lot of material characterized at room temperature. As significant variation can occur from unit to unit and across operating conditions, do not use the adjustable current limit to set an exact output current, but rather, to protect the device. 图 6-31 and 图 6-32 show how this error translates to variation in I_{OUT} versus R_{SET}. The dotted line represents the ideal output current setting that is determined by the following equation:

$$I_{LIM} \cong 20k \times \left[\frac{1.2V}{5k\Omega + R_{SET}}\right] \quad (1)$$

The mismatch errors between the current-limit set mirror and the output stage are primarily a result of variations in the approximately 1.2V band-gap reference, an internal 5kΩ resistor, the mismatch between the current limit and the output stage mirror, and the tolerance and temperature coefficient of the R_{SET} resistor referenced to the negative rail. Additionally, an increase in junction temperature can induce added mismatch in accuracy between the I_{SET} and I_{OUT} mirror. See 图 8-7 for a method that can be used to dynamically change the current limit setting using a simple, zero-drift current source. This approach simplifies the current-limit equation to the following:

$$I_{LIM} \cong 20k \times I_{SET} \quad (2)$$

The current into the I_{SET} pin is determined by the NPN current source. Therefore, the errors contributed by the internal 1.2V band-gap reference and the 5kΩ resistor mismatch are eliminated, thus improving the overall accuracy of the transfer function. In this case, the primary source of error in I_{SET} is the R_{SET} resistor tolerance and the beta of the NPN transistor.

The primary intent of the current limit on the OPA564-Q1 is coarse protection of the output stage; therefore, exercise caution when attempting to control the output current by dynamically toggling the current-limit setting. Predictable performance is better achieved by controlling the output voltage through the feedback loop of the OPA564-Q1.

7.3.1.1 Setting the Current Limit

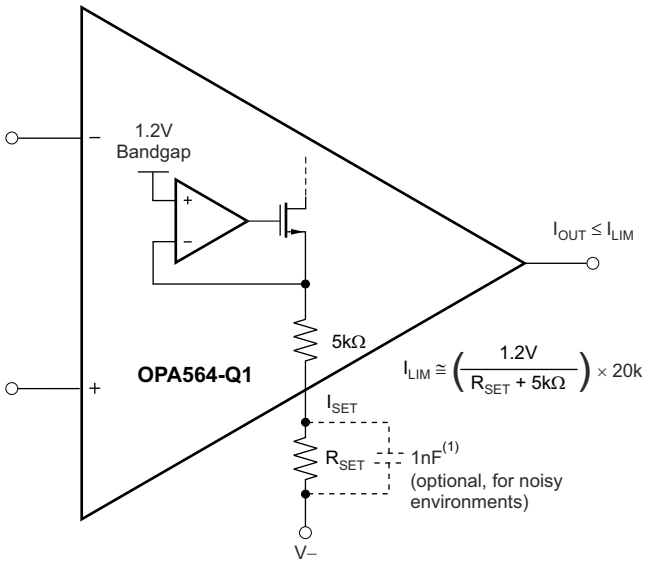
Leaving the I_{SET} pin unconnected damages the device. Connecting I_{SET} directly to V– is not recommended because direct connection programs the current limit far beyond the 1.5A capability of the device and causes excess power dissipation. The minimum recommended value for R_{SET} is 7.5kΩ, which programs the maximum current limit to approximately 1.9A. The maximum value for R_{SET} is 55kΩ, which programs the minimum current limit to approximately 0.4A. The simplest method for adjusting the current limit (I_{LIM}) uses a resistor or potentiometer connected between the I_{SET} pin and V–, according to 方程式 1.

If I_{LIM} has been defined, solve for R_{SET} by rearranging 方程式 1 into 方程式 3:

$$R_{SET} \cong \left[\frac{24k\Omega}{I_{LIM}}\right] - 5k\Omega \quad (3)$$

R_{SET} in combination with a 5kΩ internal resistor determines the magnitude of a small current that sets the desired output current limit.

图 7-1 shows a simplified schematic of the OPA564-Q1 current limit architecture.



1. At power-on, this capacitor is not charged. Therefore, the OPA564-Q1 is programmed for maximum output current. Capacitor values > 1nF are not recommended.

图 7-1. Adjustable Current Limit

7.3.2 Enable and Shutdown (E/$\overline{S}$) Pin

The output of the OPA564-Q1 shuts down when the E/$\overline{S}$ pin is forced low. For normal operation (output enabled), pull the E/$\overline{S}$ pin high (at least 2V greater than V–). To enable the OPA564-Q1 permanently, leave the the E/$\overline{S}$ pin unconnected. The E/$\overline{S}$ pin has an internal 100kΩ pullup resistor. When the output is shut down, the output impedance of the OPA564-Q1 is typically 6GΩ || 120pF. 图 7-6 shows the output shutdown output voltage versus output current. Although the output is high-impedance when shut down, there is still a path through the feedback network into the input stage to ground; see 图 7-7. To prevent damage to the OPA564-Q1, ensure that the voltage across input pins +IN and –IN does not exceed ±0.5V, and that the current flowing through the input pins does not exceed 10mA when operated beyond the supply rails, V– and V+; see also *Input Protection*.

7.3.3 Input Protection

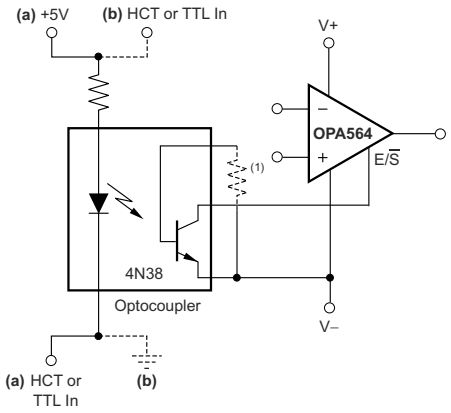
Electrostatic discharge (ESD) protection followed by back-to-back diodes and input resistors (see 图 7-7) are used for input protection on the OPA564-Q1. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes because of the finite slew rate of the amplifier. If the input current is not limited, the back-to-back diodes and the input devices can be destroyed. Sources of high input current can also cause subtle damage to the amplifier. Although the unit can still function, important parameters such as input offset voltage, drift, and noise can shift.

When using the OPA564-Q1 as a unity-gain buffer (follower), as an inverting amplifier, or in shutdown mode, limit the input voltage between the input terminals (+IN and –IN) so that the voltage does not exceed 0.5V. Maintain this condition across the entire common-mode range from V– to V+. If the inputs exceed either supply rail, limit the current to 10mA through the ESD protection diodes. During excursions past the rails, limit the voltage across the input terminals. If necessary, add external back-to-back diodes between +IN and –IN to maintain the 0.5V requirement between these connections.

7.3.4 Output Shutdown

The shutdown pin (E/$\overline{S}$) is referenced to the negative supply (V–). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications. In single-supply operation, V– typically equals common ground. Therefore, the shutdown logic signal and the OPA564-Q1 shutdown pin are referenced to the same potential. In this configuration, the logic pin and the OPA564-Q1 enable can simply be connected together. Shutdown occurs for voltage levels of less than 0.8V. The OPA564-Q1 is enabled at logic levels greater than 2V. In dual-supply operation, the logic pin remains referenced to a logic ground. However, the shutdown pin of the OPA564-Q1 continues to be referenced to V–.

Thus, in a dual-supply system, to shut down the OPA564-Q1 the voltage level of the logic signal must be level-shifted by some means. One way to shift the logic signal voltage level is by using an optocoupler, as 图 7-2 shows.



1. Optional; can be required to limit leakage current of optocoupler at high temperatures.

图 7-2. Shutdown Configuration for Dual Supplies (Using Optocoupler)

To shut down the output, the E/$\overline{S}$ pin is pulled low, no greater than 0.8V greater than V – . This function can be used to conserve power during idle periods. To return the output to an enabled state, pull the E/$\overline{S}$ pin to at least 2.0V greater than V – . 图 6-27 shows the typical enable and shutdown response times. Be aware that the E/$\overline{S}$ pin does not affect the internal thermal shutdown.

When the OPA564-Q1 is used in applications where the device shuts down, take special care with respect to input protection. Consider the following two examples.

图 7-3 shows the amplifier in a follower configuration. The load is connected midway between the supplies, V+ and V – .

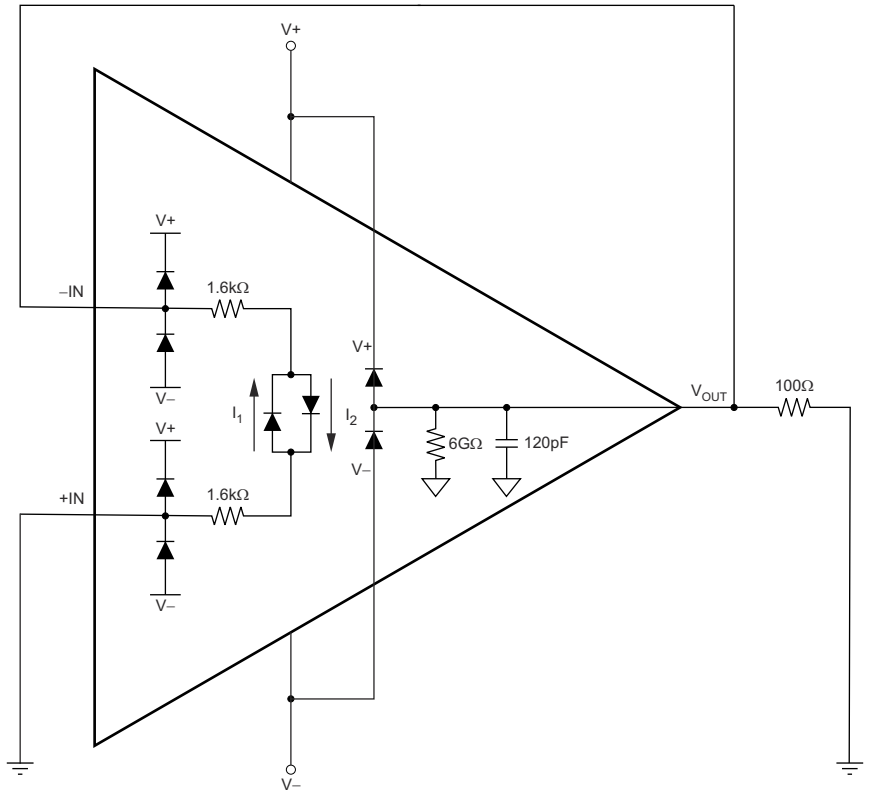


图 7-3. Shutdown Equivalent Circuit With Load Connected Midway Between Supplies

When the device shuts down in this situation, the load pulls V_{OUT} to ground. Little or no current then flows through the input of the OPA564-Q1.

Now consider 图 7-4. Here, the load is connected to V – . When the device shuts down, current flows from the positive input +IN through the first 1.6kΩ resistor through an input protection diode, then through the second 1.6kΩ resistor, and finally through the 100Ω resistor to V – .

小心
This configuration damages the device.

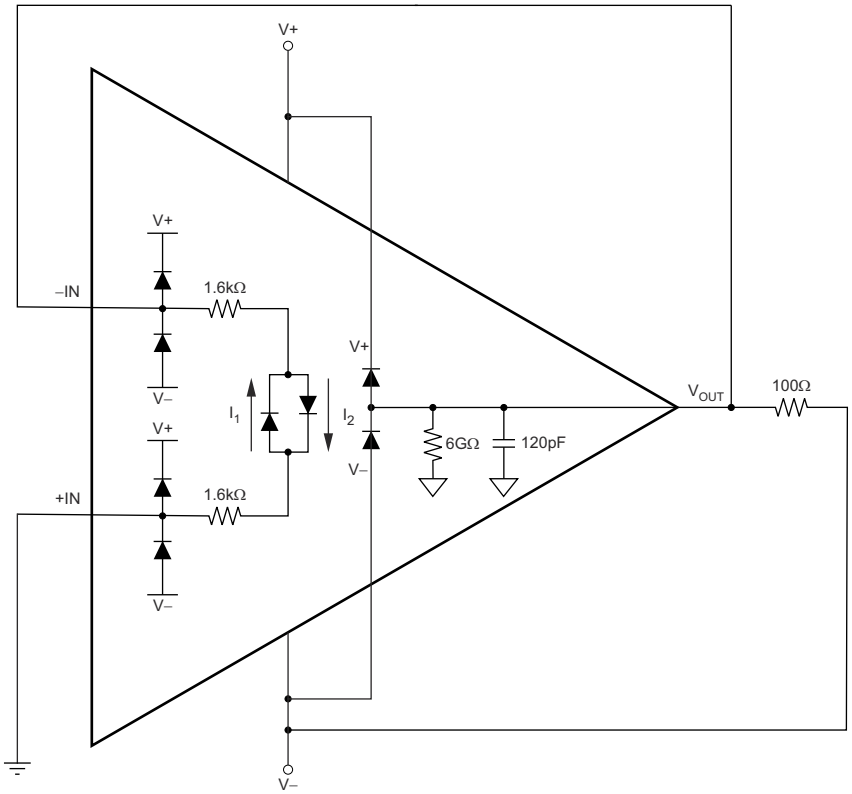


图 7-4. Shutdown Equivalent Circuit With Load Connected to V – : Voltage Across Inputs During Disable Exceeds Input Requirements

This current flow produces a voltage across the inputs that is much greater than 0.5V, which damages the OPA564-Q1. A similar problem occurs if the load is connected to the positive supply.

The solution is to place external protection diodes across the OPA564-Q1 input. 图 7-5 illustrates this configuration.

备注

This configuration protects the input during shutdown.

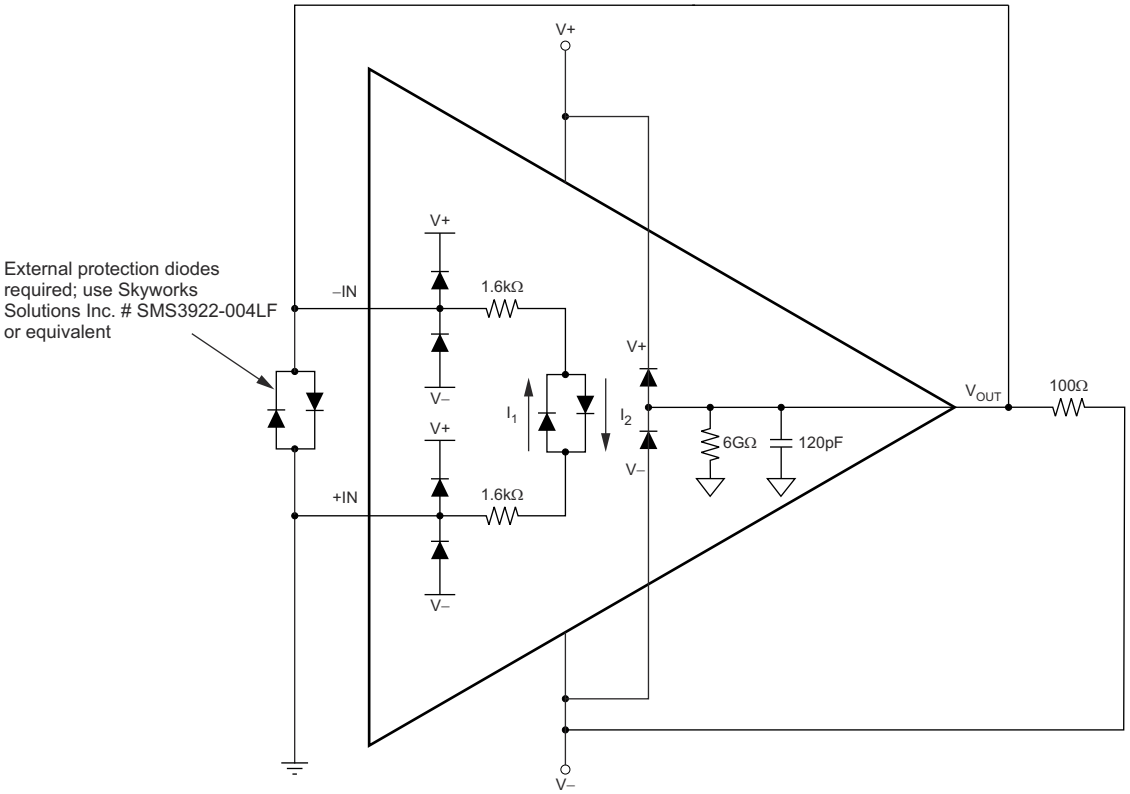


图 7-5. Shutdown Equivalent Circuit With Load Connected to V – : Protected Input Configuration

7.3.5 Microcontroller Compatibility

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic high levels while other models power up with logic low levels after reset. In the configuration of 图 7-2 **(a)**, the shutdown signal is applied on the cathode side of the photodiode within the optocoupler. A high logic level causes the OPA564-Q1 to be enabled, and a low logic level shuts the OPA564-Q1 down. In the configuration of 图 7-2 **(b)**, with the logic signal applied on the anode side, a high level causes the OPA564-Q1 to shut down, and a low level enables the op amp.

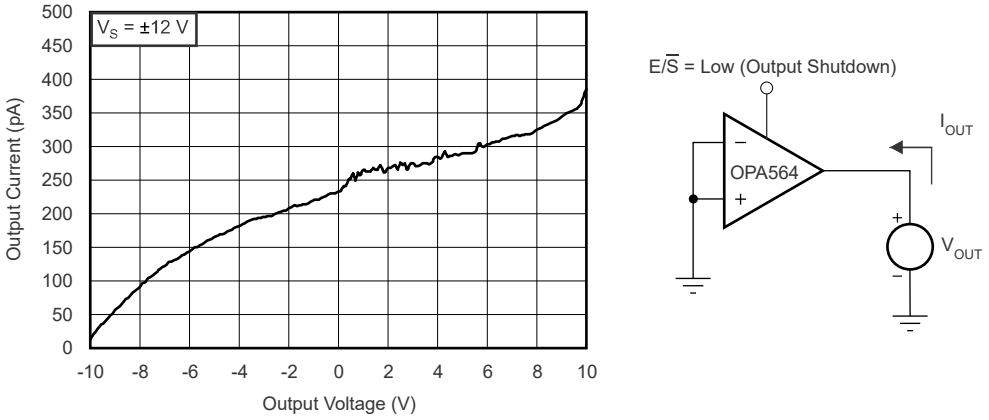


图 7-6. Output Shutdown Output Impedance

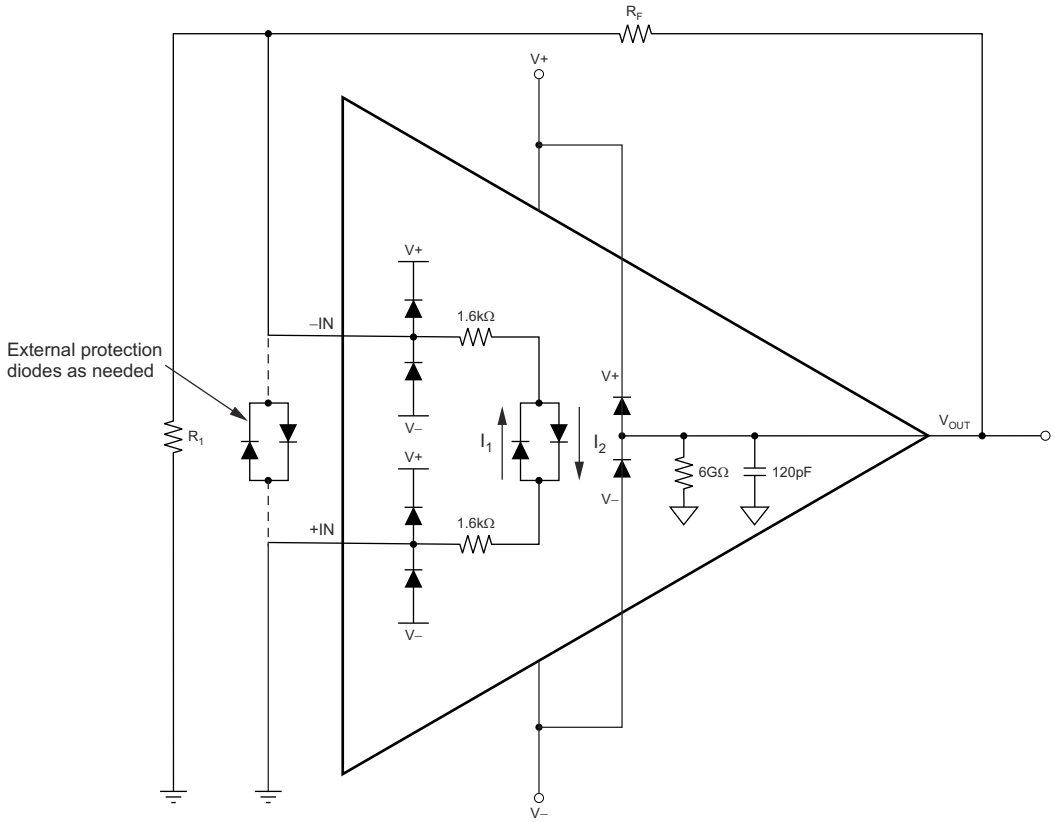


图 7-7. OPA564-Q1: Output Shutdown Equivalent Circuit (With External Feedback)

7.3.6 Current Limit Flag

The OPA564-Q1 features a current limit flag (I_{FLAG}) that can be monitored to determine if the load current is operating within or exceeding the current limit set by the user. The output signal of I_{FLAG} is compatible with standard CMOS logic and is referenced to the negative supply pin (V –). A voltage level of 0.8V or less with respect to V – indicates that the amplifier is operating within the limits set by the user. A voltage level of 2.0V or greater with respect to V – indicates that the OPA564-Q1 operation exceeds the current limit set by the user. See also 节 7.3.1.1. Either read the I_{FLAG} pin with a high-impedance digital I/O pin, or buffer the I_{FLAG} pin.

7.3.7 Thermal Protection

The OPA564-Q1 has thermal sensing circuitry that helps protect the amplifier from exceeding temperature limits. Power dissipated in the OPA564-Q1 causes the junction temperature to rise. Internal thermal shutdown circuitry disables the output when the die temperature reaches the thermal shutdown temperature limit. The OPA564-Q1 output remains shut down until the die has cooled sufficiently; see the *Electrical Characteristics*, *Thermal Shutdown* section. When the OPA564-Q1 is in thermal shutdown, the device asserts the T_{FLAG} pin high. The T_{FLAG} pin returns low when the device returns to normal operation. Read the T_{FLAG} pin with a high-impedance digital I/O pin, or buffer the T_{FLAG} pin.

Depending on load and signal conditions, the thermal protection circuit can cycle on and off. This cycling limits the amplifier dissipation, but can have undesirable effects on the load. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable, long-term, continuous operation, with I_{OUT} at the maximum output of 1.5A, limit the junction temperature to 85°C maximum. 图 7-8 shows the maximum output current versus junction temperature for dc and RMS signal outputs. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection triggers. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection triggers when the maximum expected ambient condition of the application is exceeded by 35°C.

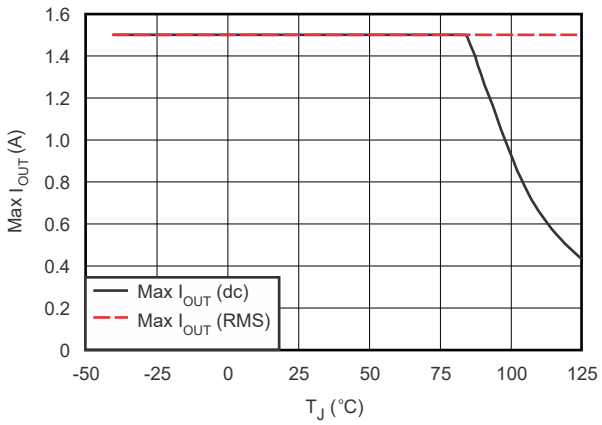


图 7-8. Maximum Output Current vs Junction Temperature

The internal protection circuitry of the OPA564-Q1 is designed to protect against overload conditions; this circuitry was not intended to replace a proper heat sink. Continuously running the OPA564-Q1 into thermal shutdown degrades reliability.

7.3.8 Junction Temperature Measurement Using T_{SENSE}

The OPA564-Q1 includes an internal diode for junction temperature monitoring. The η-factor of this diode is typically 1.033. To measure the OPA564-Q1 junction temperature, connect the T_{SENSE} pin to a remote-junction temperature sensor, such as the TMP411 (see 图 8-13).

7.4 Device Functional Modes

The device has two modes of operation: normal and low-power shutdown.

8 Application and Implementation

备注

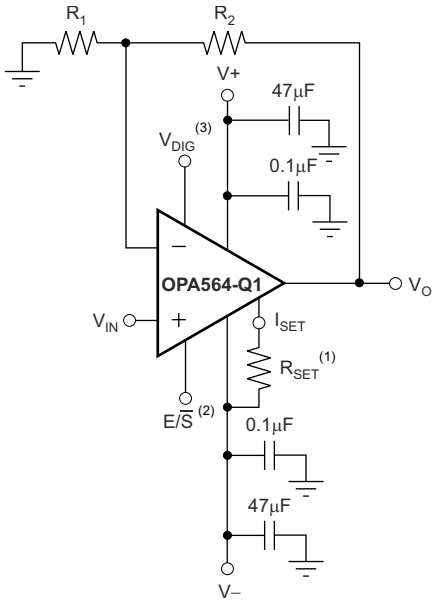
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Basic Configuration

图 8-1 shows the OPA564-Q1 connected as a basic noninverting amplifier. However, the OPA564-Q1 can be used in virtually any op-amp configuration.

Bypass power-supply pins with low series impedance capacitors. The technique of using ceramic and tantalum capacitors in parallel is recommended. Use power-supply wiring with a low series impedance.



1. R_{SET} sets the current limit value from 0.4A to 1.5A.
2. E/$\overline{S}$ pin forced low shuts down the output.
3. V_{DIG} must not exceed (V –) + 5.5V; see 图 8-12 for examples of generating a signal for V_{DIG}.

图 8-1. Basic Noninverting Amplifier

8.1.2 Output-Stage Compensation

The complex load impedances common in power op-amp applications can cause output-stage instability. For normal operation, output compensation circuitry is typically not required. However, if the OPA564-Q1 is intended to be driven into current limit, an R/C network (snubber) can be required. A snubber circuit, such as the one shown in 图 8-10 can also enhance stability when driving large capacitive loads (greater than 1000pF) or inductive loads (for example, motors or loads separated from the amplifier by long cables). Typically, 3Ω to 10Ω in series with 0.01 μF to 0.1 μF is adequate. Some variations in circuit value can be required with certain loads.

8.1.3 Output Protection

The output structure of the OPA564-Q1 includes ESD diodes (see 图 7-7). Do not allow the voltage at the OPA564-Q1 output to exceed 0.4V beyond either supply rail to avoid damage to the device. Reactive and electromagnetic field (EMF) generation loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. 图 8-10 and 图 8-11 illustrate how to avoid this damaging condition with clamping diodes from the output pin to the power supplies. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

8.1.4 Power Dissipation and Safe Operating Area

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of output current (I_{OUT}) and the voltage across the conducting output transistor [(V+) – V_{OUT} when sourcing; V_{OUT} – (V–) when sinking]. Dissipation with ac signals is lower. See the *Power Amplifier Stress and Power Handling Limitations* application bulletin, available for download from www.ti.com, for an explanation on how to calculate or measure power dissipation with unusual signals and loads.

图 8-2 shows the safe operating area at room temperature with various heat-sinking efforts. Note that the safe output current decreases as (V+) – V_{OUT} or V_{OUT} – (V–) increases. 图 8-3 shows the safe operating area at various temperatures with the thermal pad being soldered to a 2oz copper pad.

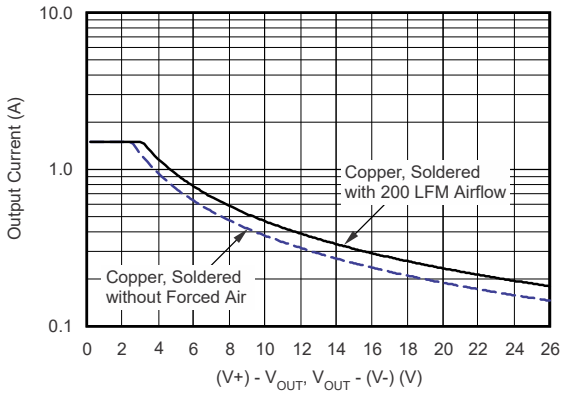
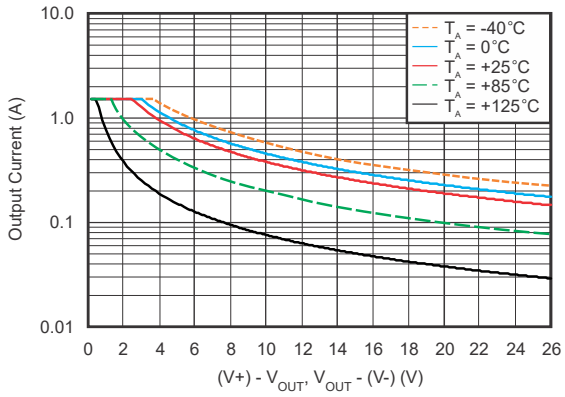


图 8-2. Safe Operating Area at Room Temperature



Note: Thermal pad soldered to a 2-oz copper pad.

图 8-3. Safe Operating Area at Various Ambient Temperatures

The power that can be safely dissipated in the package is related to the ambient temperature and the heat-sink design. The PowerPAD integrated circuit package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. See *节 8.4.1.1* section for further details.

The relationship between thermal resistance and power dissipation can be expressed as:

$$T_J = T_A + T_{JA} \quad (4)$$

$$T_{JA} = P_D \times \theta_{JA} \quad (5)$$

Combining these equations produces:

$$T_J = T_A + P_D \times \theta_{JA} \quad (6)$$

where:

- T_J = Junction temperature (°C)
- T_A = Ambient temperature (°C)
- θ_{JA} = Junction-to-ambient thermal resistance (°C/W)
- P_D = Power dissipation (W)

To determine the required heat-sink area, calculate the required power dissipation and consider the relationship between power dissipation and thermal resistance to minimize shutdown conditions and allow for proper long-term operation (junction temperature of 85°C or less).

After the heat-sink area has been selected, test for worst-case load conditions to maintain proper thermal protection.

For applications with limited board size, see 图 8-4 for the approximate thermal resistance relative to heat-sink area. Increasing heat-sink area beyond 2in^2 provides little improvement in thermal resistance. To achieve the 28.7°C/W shown in *Thermal Information*, a 2oz copper plane size of 3in^2 is used. The PowerPAD integrated circuit package is designed for continuous power levels from 2W to 4W, depending on ambient temperature and heat-sink area. The addition of airflow also influences maximum power dissipation, as 图 8-5 illustrates. Higher power levels can be achieved in applications with a low on and off duty cycle, such as remote meter reading.

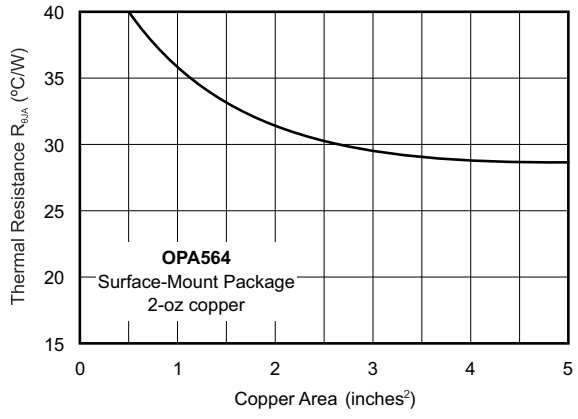


图 8-4. Thermal Resistance vs Circuit Board Copper Area

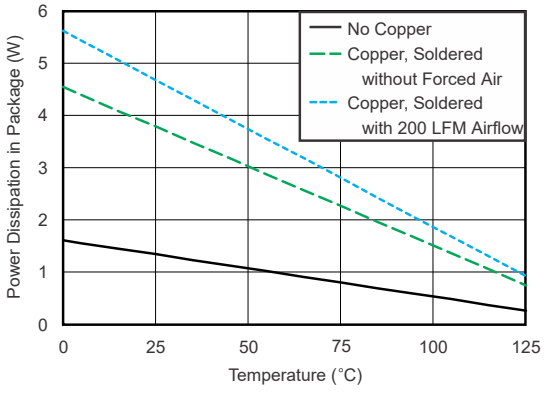


图 8-5. Maximum Power Dissipation vs Temperature

8.2 Typical Applications

8.2.1 Improved Howland Current Pump

The high output current and low supply of the OPA564-Q1 make this device a good candidate for driving laser diodes and thermoelectric coolers. 图 8-6 shows an improved Howland current pump circuit.

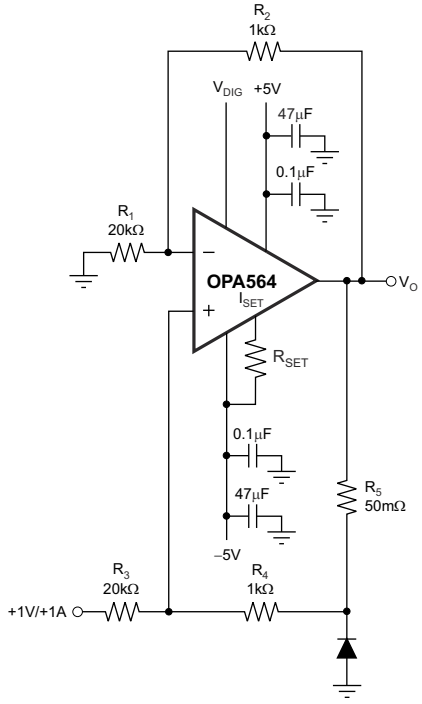


图 8-6. Improved Howland Current Pump

8.2.2 Programmable Power Supply

图 8-7 shows the how the OPA333 is used to control I_{SET} to adjust the current limit of the OPA564-Q1. Ensure that the ground used as the reference for V_{SET} and R_{SET} is approximately equal to V – .

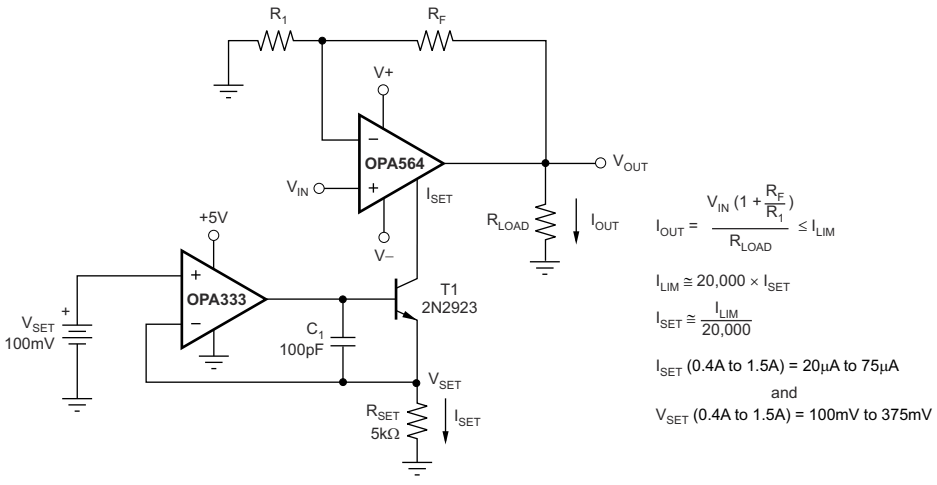
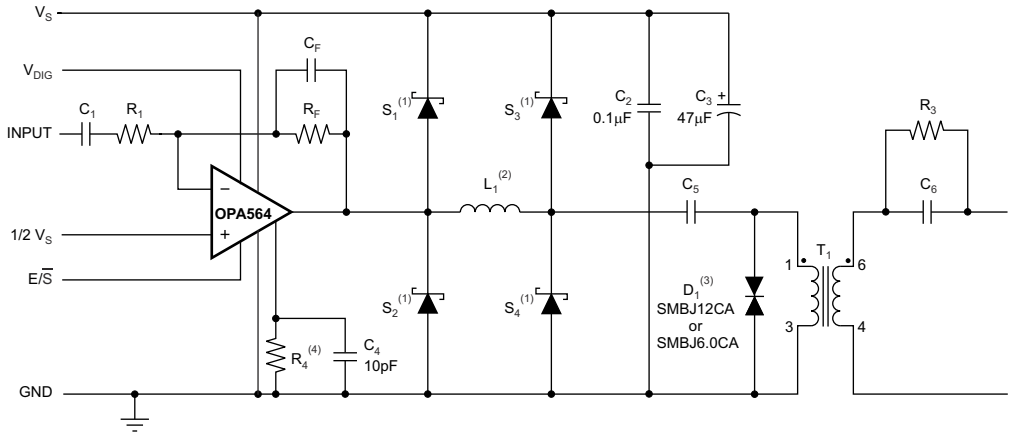


图 8-7. Programmable Current Limit Option

8.2.3 Powerline Communication

Powerline-communication (PLC) applications require some form of signal transmission over an existing ac power line. A common technique used to couple these modulated signals to the line is through a signal transformer. A power amplifier is often needed to provide adequate levels of current and voltage to drive the varying loads that exist on modern powerlines. 图 8-8 shows one such application. The OPA564-Q1 is used to drive signals used in frequency modulation schemes such as frequency-shift keying (FSK) or orthogonal frequency-division multiplexing (OFDM) to transmit digital information over the powerline. The power output capabilities of the OPA564-Q1 are needed to drive the current requirements of the transformer that is shown in the figure, coupled to the ac power line via a coupling capacitor. Circuit protection is often required to prevent excessive line voltages or current surges from damaging the active circuitry in the power amplifier and application circuitry.



1. S_1, S_2, S_3, and S_4 are Schottky diodes. S_1 and S_2 are B350 or equivalent. S_3 and S_4 are BAV99T or equivalent.
2. Ensure that L_1 is small enough so that L_1 does not interfere with the bandwidth of interest, but large enough to suppress transients that can damage the OPA564-Q1.
3. D_1 is a transient suppression diode. For 24V supplies, use SMBJ12CA. For 12V supplies, use SMBJ6.0CA. Ensure that the voltage rating of the transient voltage suppressor is half the supply rating or less.
4. The minimum recommended value for R_4 is 7.5kΩ.

图 8-8. Powerline Communication Line Coupling

图 8-9 illustrates a detailed powerline communication circuit.

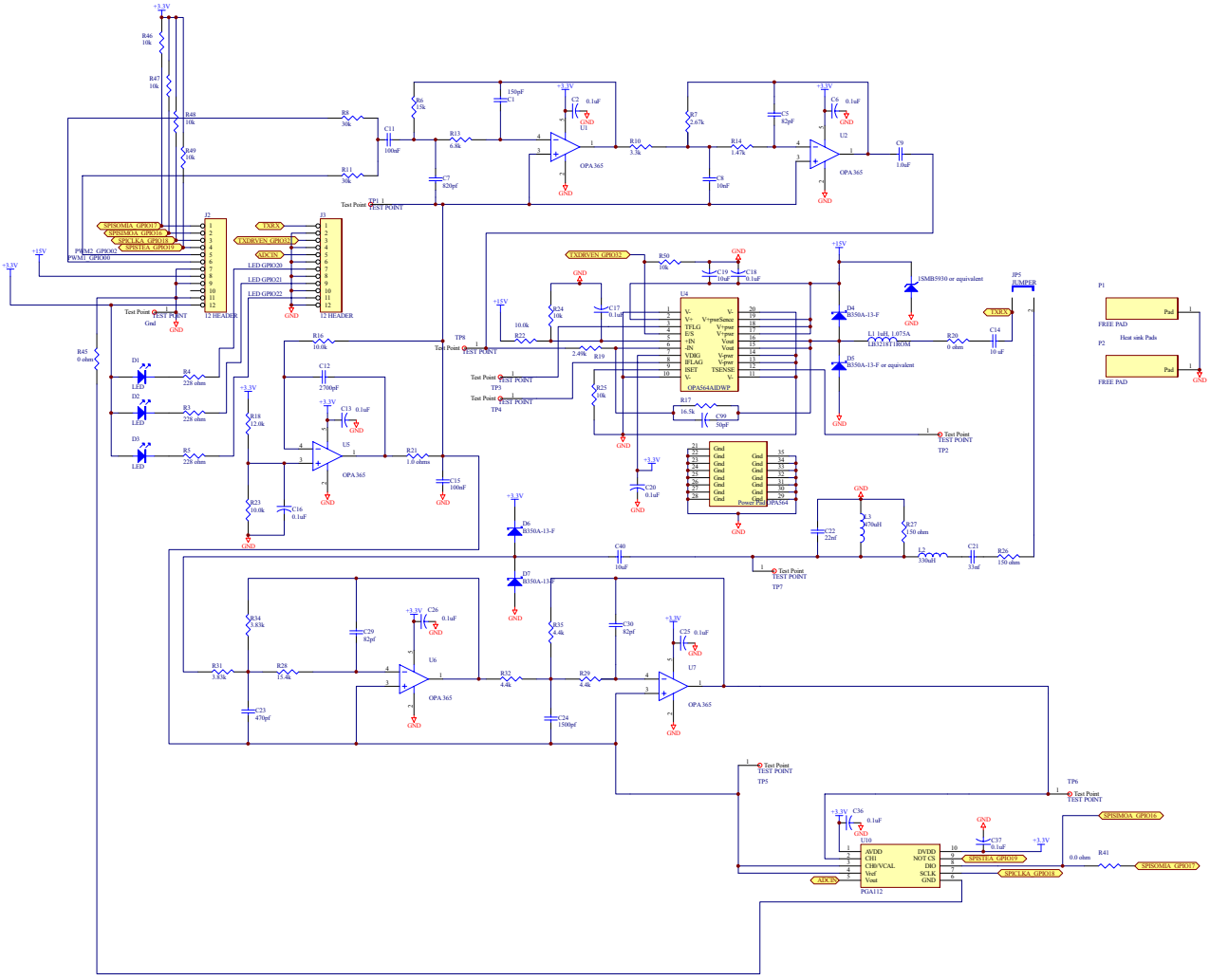
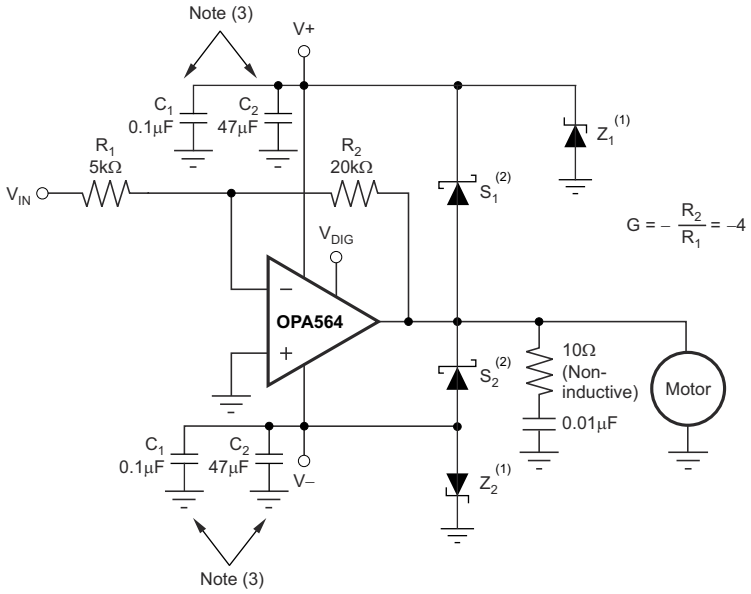


图 8-9. Detailed Powerline Communication Circuit

8.2.4 Motor-Drive Circuit

图 8-10 shows a basic motor-speed driver, but does not include any control over the motor speed.

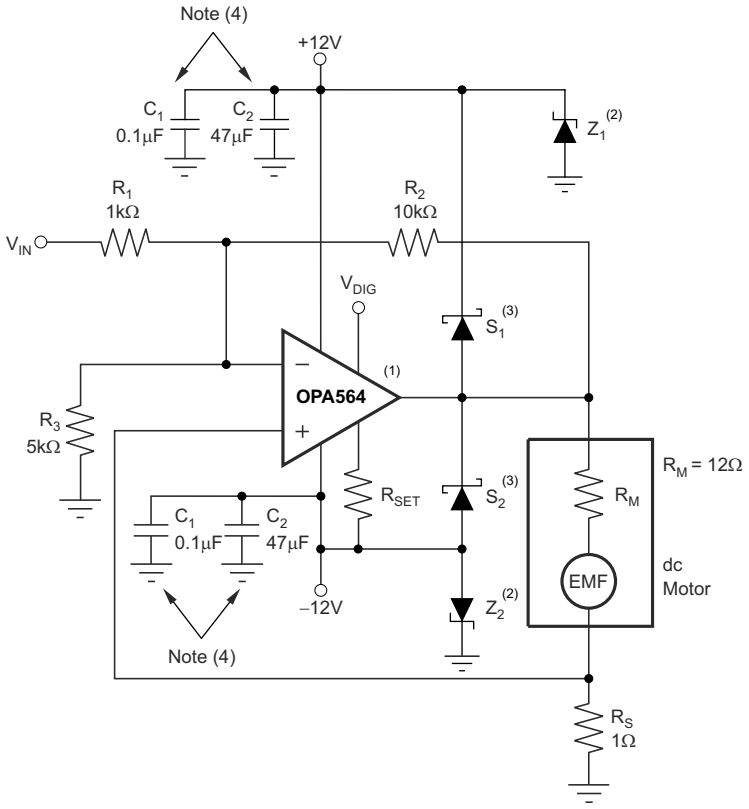


1. Z_1, Z_2 = zener diodes (IN5246 or equivalent). Select Z_1 and Z_2 diodes that are capable of the maximum anticipated surge current.
2. S_1, S_2 = Schottky diodes (STPS1L40 or equivalent).
3. C_1 = high-frequency bypass capacitors; C_2 = low-frequency bypass capacitors (minimum of 10 µ F for every 1A peak current)

图 8-10. Motor-Drive Circuit

8.2.5 DC Motor-Speed Controller (Without Tachometer)

For applications where good control of the speed of the motor is desired, but the precision of a tachometer control is not required, the circuit in 图 8-11 provides control by using feedback of the current consumption to adjust the motor drive.



1. I_{FLAG} and T_{FLAG} connections are not shown.
2. Z_1, Z_2 = zener diodes (IN5246 or equivalent). Select Z_1 and Z_2 diodes that are capable of the maximum anticipated surge current.
3. S_1, S_2 = Schottky diodes (STPS1L40 or equivalent).
4. C_1 = high-frequency bypass capacitors; C_2 = low-frequency bypass capacitors (minimum of 10 µ F for every 1A peak current).

图 8-11. DC Motor-Speed Controller (Without Tachometer)

For more information on this circuit, see the *DC Motor Speed Controller: Control a DC Motor without Tachometer Feedback* the application bulletin, available for download at www.ti.com.

8.2.6 Generating V_{DIG}

图 8-12 shows two examples of generating the signal for V_{DIG}. 图 8-12(a) uses an 1N4732A zener to bias the V_{DIG} to precisely 4.7V greater than V –. 图 8-12(b) uses a high-voltage subregulator to derive the V_{DIG} voltage. Ensure that any decoupling capacitance present on the VDIG pin does not cause a timing condition that violates the power-supply sequencing outlined in 节 8.3.

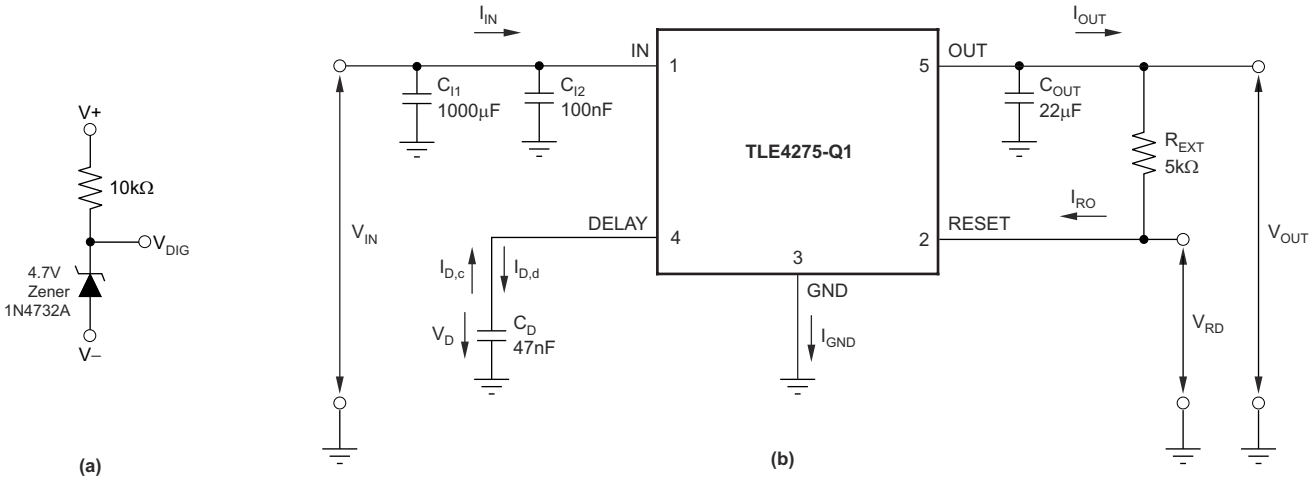


图 8-12. Circuits to Generate V_{DIG}

8.2.7 Temperature Measurement

The OPA564-Q1 includes an internal diode for junction temperature monitoring. The η-factor of this diode is typically 1.033. 图 8-13 shows that to measure the OPA564-Q1 junction temperature, connect the T_{SENSE} pin to a remote-junction temperature sensor, such as the TMP411.

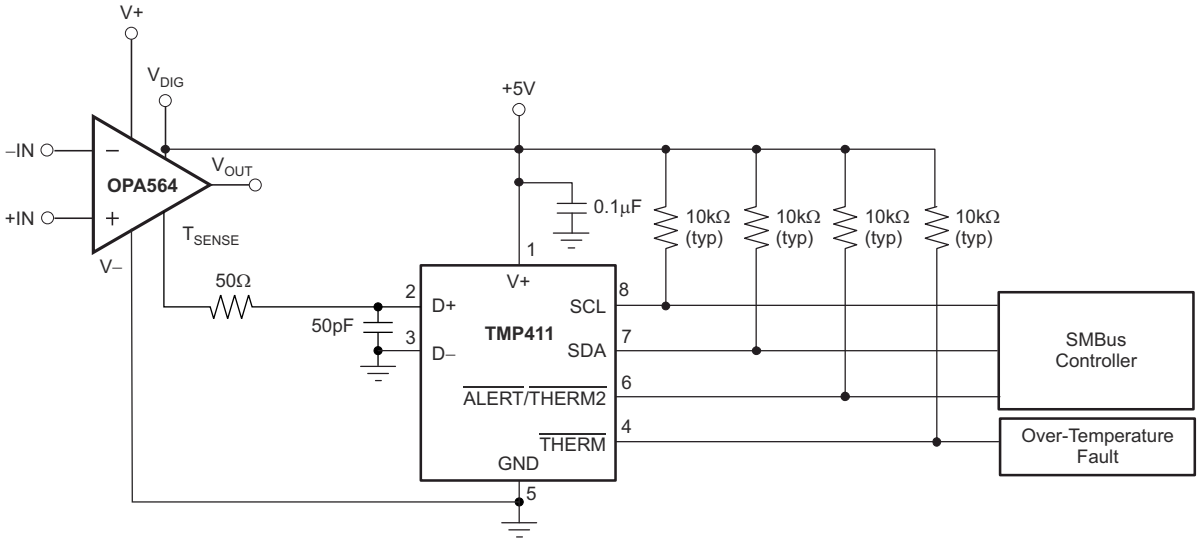
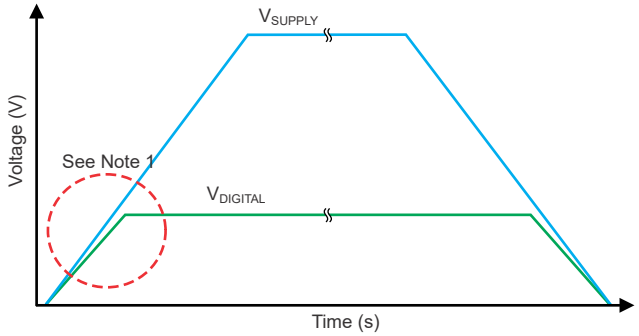


图 8-13. Temperature Measurement Using T_{SENSE} and the TMP411

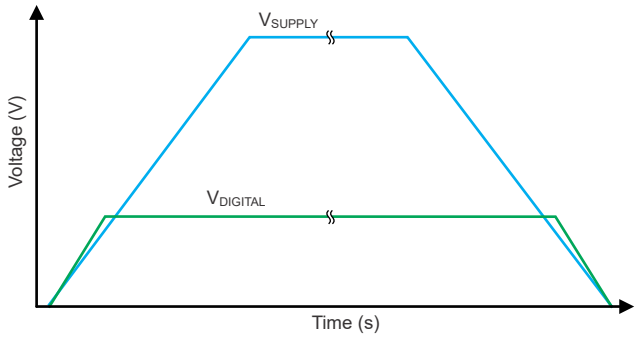
8.3 Power Supply Recommendations

The OPA564-Q1 operates with excellent performance from single (7V to 24V) or dual (±3.5V to ±12V) analog supplies and a digital supply of 3.3V to 5.5V (referenced to the V – pin). The analog power-supply voltages do not need to be symmetrical, as long as the total voltage remains less than 24V. For example, the positive supply can be set to 14V with the negative supply at –10V. Most behaviors remain constant across the operating voltage range. 节 6.6 shows the parameters that vary significantly with operating voltage.

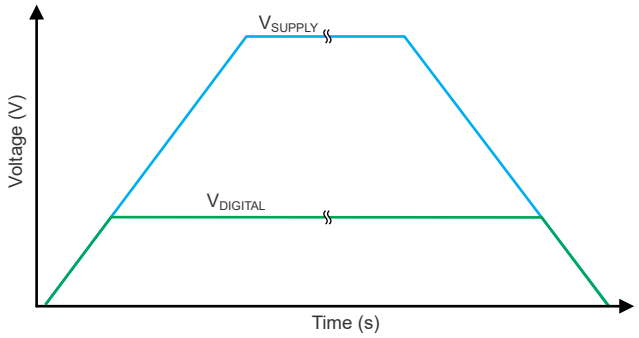
To prevent damage to the OPA564-Q1, ensure that the digital supply voltage (V_{DIG}) is applied before the supply voltage when sequencing power supplies. 图 8-14 shows acceptable versus unacceptable power-supply sequencing.



(A) Sequence not allowed(1)



(B) Sequence allowed



(C) Sequence allowed

(1) The power-supply sequence illustrated in (A) is not allowed because this power-supply sequence damages the device.

图 8-14. Power-Supply Sequencing

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Thermally Enhanced PowerPAD™ Integrated Circuit Package

The OPA564-Q1 uses the HSOIC-20 PowerPAD integrated circuit package (DWP), a thermally-enhanced, standard size integrated-circuit (IC) package. This package enhances power dissipation capability significantly. This package is easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

图 8-15 shows how DWP package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. The thermal pad provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package.

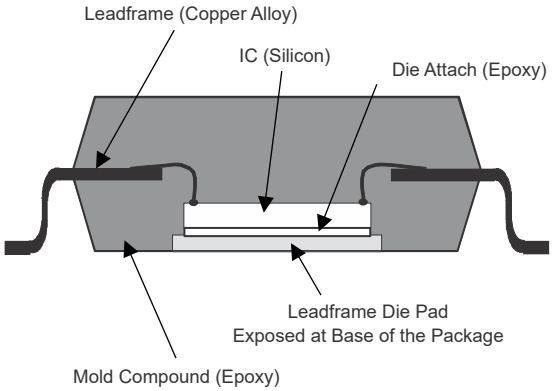


图 8-15. Cross-Section Views

The PowerPAD integrated circuit package with exposed pad down are designed to be soldered directly to the PCB, using the PCB as a heat sink. Texas Instruments does not recommend the use of the PowerPAD integrated circuit package without soldering the package to the PCB because of the risk of lower thermal performance and mechanical integrity. In addition, through the use of thermal vias, the bottom-side thermal pad can be directly connected to a power plane or special heat-sink structure designed into the PCB. Ensure that the thermal pad is at the same voltage potential as V – . Always solder the bottom-side thermal pad to the PCB, even with applications that have low power dissipation. The solder provides the necessary thermal and mechanical connection between the leadframe die and the PCB.

8.4.1.1.1 Bottom-Side Thermal Pad Assembly Process

1. The thermal pad must be connected to the most negative supply of the device, V – .
2. Prepare the PCB with a top-side etch pattern, as shown in the attached thermal land pattern mechanical drawing. Use etch for the leads as well as etch for the thermal land.
3. Place the recommended number of holes (or thermal vias) in the area of the thermal pad, as seen in the attached thermal land pattern mechanical drawing. These holes are 13 mils (0.013in, or 330.2 μm) in diameter. Keep the holes small so that solder wicking through the holes is not a problem during reflow.
4. For optimized performance, place a small number of the holes under the package and outside the thermal pad area. These holes provide an additional heat path between the copper land and ground plane and are 25 mils (0.025in, or 635 μm) in diameter. These holes can be larger because these holes are not in the area to be soldered; therefore, wicking is not a problem. This configuration is illustrated in the attached thermal land pattern mechanical drawing.
5. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal plane that is at the same voltage potential as V – .
6. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology (as 图 8-16 shows). Web connections have a high thermal resistance connection that is useful for slowing heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, connect the holes under the PowerPAD integrated circuit package to the internal plane with a complete connection around the entire circumference of the plated through-hole.
7. Leave the terminals of the package and the thermal pad area exposed through the top-side solder mask. Leave the 13-mil holes exposed through the thermal pad area. Cover the larger 25-mil holes outside the thermal pad area with solder mask.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.
9. With these preparatory steps completed, the PowerPAD integrated circuit package is simply placed in position and run through the solder-reflow operation as with any standard surface-mount component. This processing results in a device that is properly installed.

For detailed information on the PowerPAD integrated circuit package, including thermal modeling considerations and repair procedures, see the *PowerPAD Thermally Enhanced Package* technical brief, available at www.ti.com.

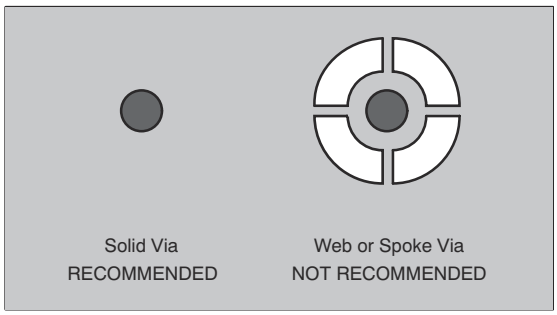


图 8-16. Via Connection Methods

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2011) to Revision A (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了*封装信息* 表以及*引脚配置和功能*、*规格*、*ESD 等级*、*建议运行条件*、*热性能信息*、*详细说明*、*概述*、*功能方框图*、*特性说明*、*器件功能模式*、*应用和实现*、*典型应用*、*电源相关建议*、*布局*、*器件和文档支持* 和*机械*、*封装和可订购信息* 部分	1
• 删除了预发布 DWD 封装和相关内容	1
• 将 HSOP 的实例更改为 HSOIC（拼写错误）	1
• 将首页图中的 20kΩ 电阻器标签从 R_4 更改为 R_3 (拼写错误)	1
• Updated *Related Products* table and renamed to *Device Comparison Table*	2
• Changed Operating Junction Temperature to Operating Ambient Temperature and moved to new *Recommended Operating Conditions*	4
• Updated format of *Electrical Characteristics*	5
• Changed Output current limit range typical value from "±0.4 to ±2.0" to "±0.4 to ±1.9"	5
• Changed current limit flag output typical value for normal operation from 0 to V –	5
• Changed Thermal Shutdown typical value for normal operation from 0 to V –	5
• Changed current limit value range from "0.4A to 1.5A" to "0.4A to 1.6A" in *Adjustable Current Limit*	13
• Added text regarding adjustable current limit used to protect the device in *Adjustable Current Limit*	13
• Updated equation terms for consistency	13
• Changed R_{CL} to R_{SET} in Figure 7-1, *Adjustable Current Limit*	14

- Added text regarding I_{FLAG} pin to last sentence of *Current Limit Flag* 21
- Added text regarding T_{FLAG} pin to first paragraph of *Thermal Protection* 21
- Added R_1 and R_2 resistor labels to Figure 8-1, *Basic Noninverting Amplifier* 23
- Changed copper plane size from $9in^2$ to $3in^2$ to match Figure 8-2 in *Power Dissipation and Safe Operating Area* 24
- Changed Figure 8-4, *Thermal Resistance vs Circuit Board Copper Area*, to align with *Thermal Information* .24
- Changed Figure 8-6, *Improved Howland Current Pump*, 20kΩ resistor from R_4 to R_3 (typo), and deleted footnote..... 26
- Added text to clarify application operation in *Programmable Power Supply* 26
- Moved misplaced junction dot to correct location in Figure 8-10, *Motor-Drive Circuit* 29

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA564AQDWPRQ1	ACTIVE	SO PowerPAD	DWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA564AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA564-Q1 :

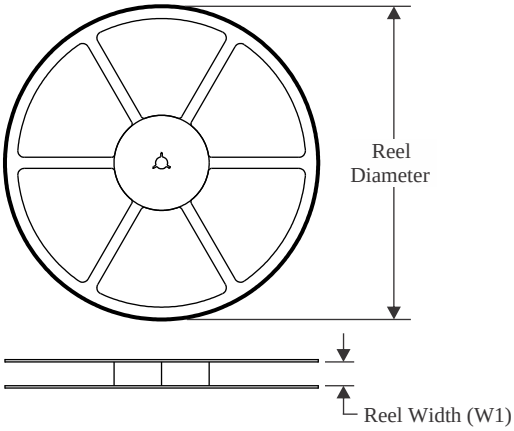
- Catalog : OPA564

NOTE: Qualified Version Definitions:

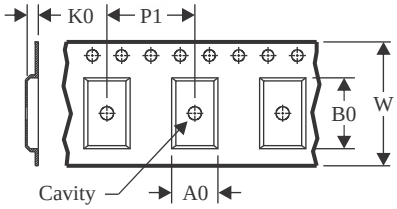
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

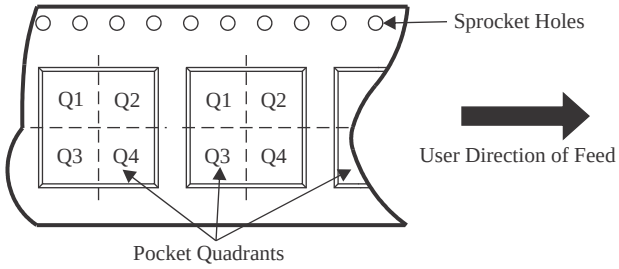


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

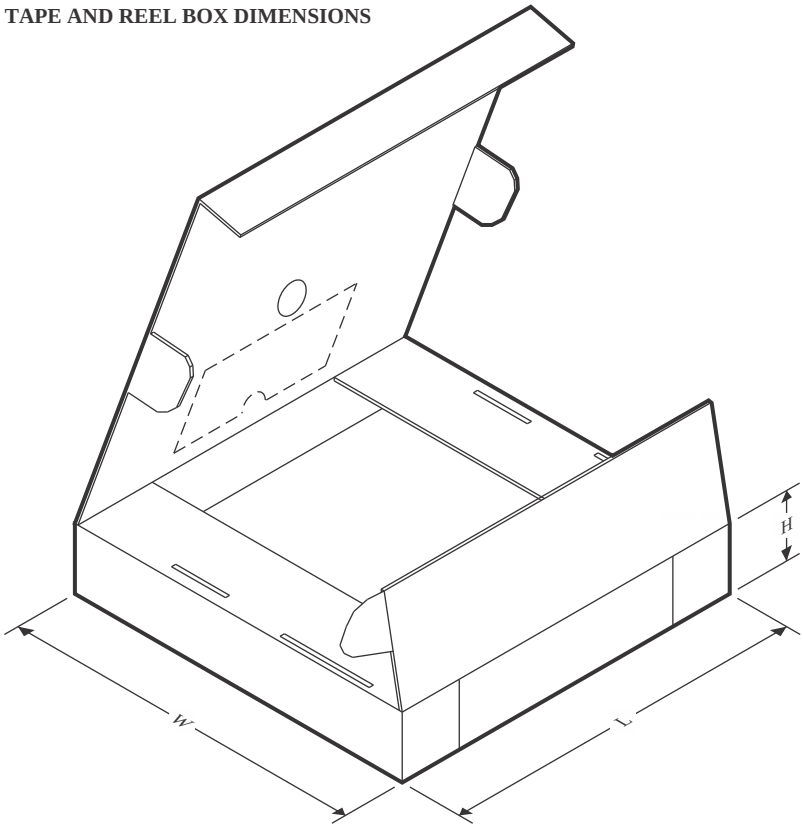
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA564AQDWPRQ1	SO PowerPAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

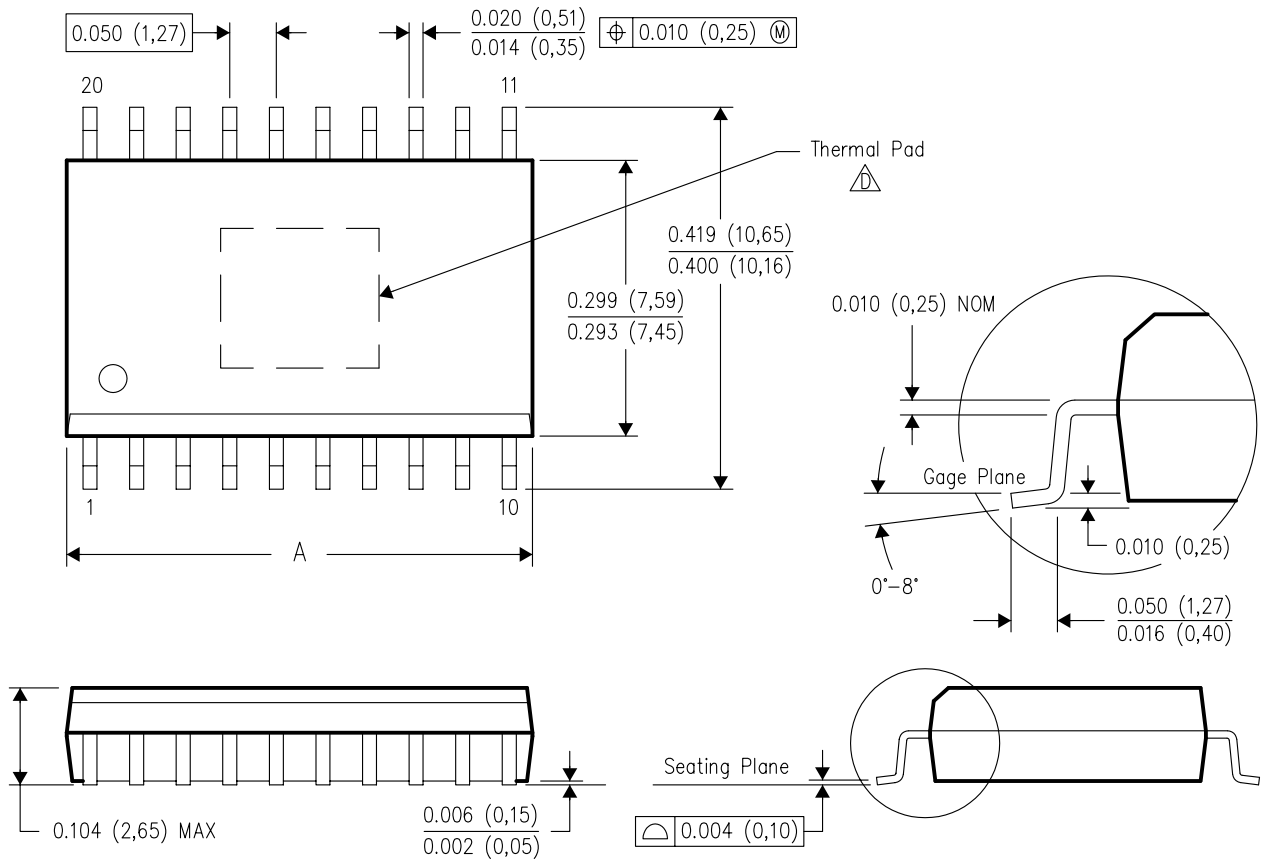


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA564AQDWPRQ1	SO PowerPAD	DWP	20	2000	350.0	350.0	43.0

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

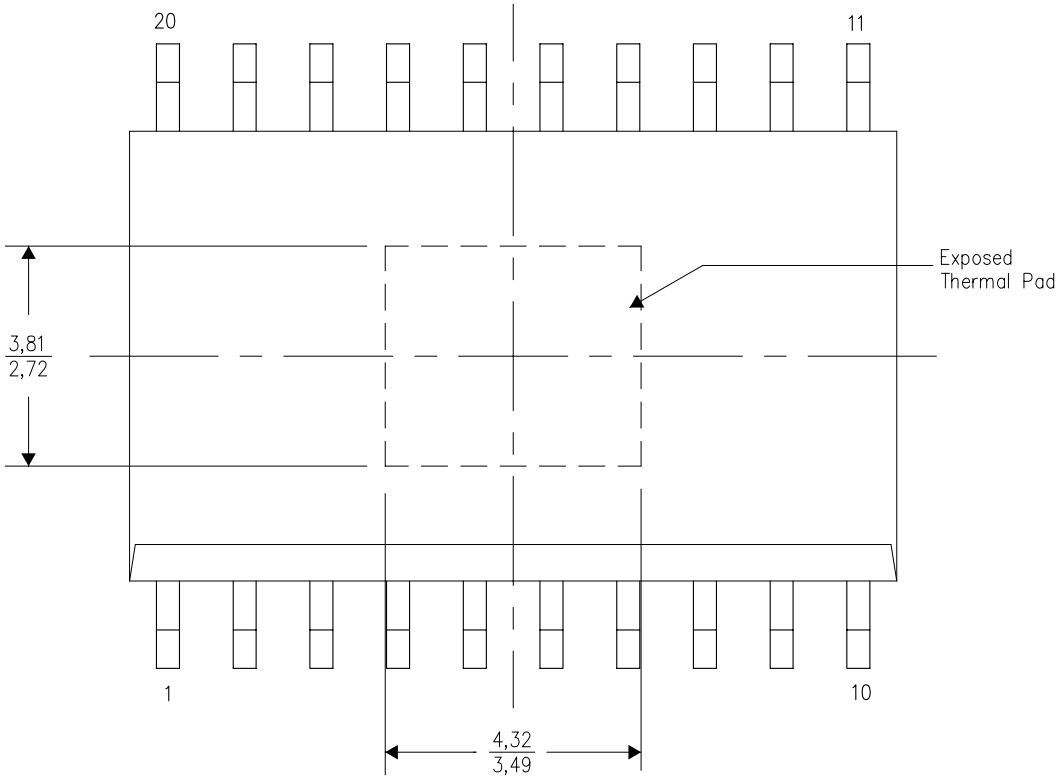
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206325–2/E 12/10

NOTE: A. All linear dimensions are in millimeters

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