

SNx4AHCT373 具有三态输出的八路透明 D 类锁存器

1 特性

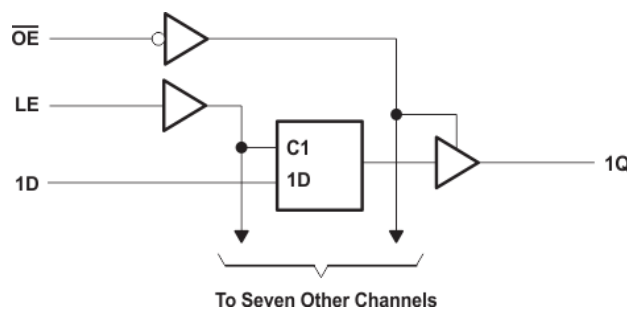
- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 说明

AHCT373 器件是八路透明 D 类锁存器。在锁存器使能 (LE) 输入为高电平时，Q 输出将跟随数据 (D) 输入。当 LE 为低电平时，Q 输出被锁存在 D 输入端的逻辑电平上。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN54AHCT373	J (CDIP , 20)	24.2mm x 7.62mm	24.2mm x 6.92mm
	W (CFP , 20)	13.09mm x 8.13mm	13.09mm x 6.92mm
	FK (LCCC , 20)	8.89mm x 8.89mm	8.89mm x 8.89mm
SN74AHCT373	DB (SSOP , 20)	7.2mm x 7.8mm	7.50mm x 5.30mm
	DW (SOIC , 20)	12.80mm x 10.3mm	12.8mm x 7.5mm
	NS (SOP , 20)	12.60mm x 7.8mm	12.6mm x 5.30mm
	N (PDIP , 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	PW (TSSOP , 20)	6.50mm x 6.4mm	6.50mm x 4.40mm



逻辑图 (正逻辑)



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3 Pin Configuration and Functions

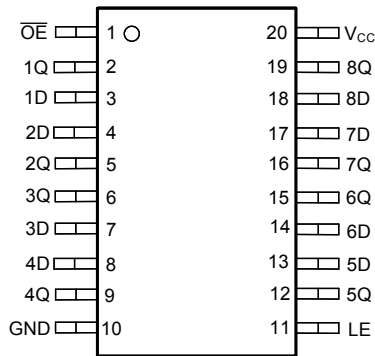


图 3-1. SN54AHCT373 J or W Package;
SN74AHCT373 DB, DGV, DW, N, NS, or PW
Package (Top View)

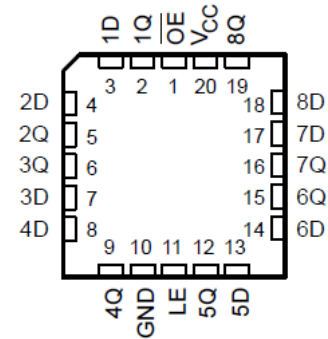


图 3-2. SN54AHCT373 FK Package (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OE	I	Output Enable
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground
11	LE	I	Latch Enable
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	V _{CC}	—	Power Pin

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	7	V
V _I	Input voltage range ⁽²⁾	- 0.5	7	V
V _O	Output voltage range ⁽²⁾	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	- 20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
Continuous current through V _{CC} or GND			±75	mA
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

		Value	UNIT
V _(ESD)	Electrostatic discharge	±2000	V
		±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		- 8		- 8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	- 55	125	- 40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHCT373						UNIT
	DW (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
	20 PINS						
R _{θJA} Junction-to-ambient thermal resistance	58	70	92	69	60	116.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT373		SN74AHCT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36			0.44		
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.25			± 2.5	μA	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			± 0.1			± 1 ⁽¹⁾	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4			40	μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35			1.5	mA	
C _i	V _I = V _{CC} or GND	5 V			4			10	pF	
C _o	V _O = V _{CC} or GND	5 V			9				pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

4.6 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		T _A = 25°C		SN54AHCT373		SN74AHCT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, \overline{LE} high	6.5		6.5		6.5		ns
t _{su}	Setup time, data before \overline{LE} ↓	1.5		1.5		1.5		ns
t _h	Hold time, data after \overline{LE} ↓	3.5		3.5		3.5		ns

4.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT373		SN74AHCT373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	$C_L = 15 \text{ pF}$		5.1 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	ns
t_{PHL}					5.1 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	9.5 ⁽¹⁾	1	9.5	
t_{PLH}	LE	Q	$C_L = 15 \text{ pF}$		7.7 ⁽¹⁾	12.3 ⁽¹⁾	1 ⁽¹⁾	13.5 ⁽¹⁾	1	13.5	ns
t_{PHL}					7.7 ⁽¹⁾	12.3 ⁽¹⁾	1 ⁽¹⁾	13.5 ⁽¹⁾	1	13.5	
t_{PZH}	$\overline{\text{OE}}$	Q	$C_L = 15 \text{ pF}$		6.3 ⁽¹⁾	10.9 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	ns
t_{PZL}					6.3 ⁽¹⁾	10.9 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	
t_{PHZ}	$\overline{\text{OE}}$	Q	$C_L = 15 \text{ pF}$		6 ⁽¹⁾	10.2 ⁽¹⁾	1 ⁽¹⁾	11 ⁽¹⁾	1	11	ns
t_{PLZ}					6 ⁽¹⁾	10.2 ⁽¹⁾	1 ⁽¹⁾	11 ⁽¹⁾	1	11	
t_{PLH}	D	Q	$C_L = 50 \text{ pF}$		5.9	9.5	1	10.5	1	10.5	ns
t_{PHL}					5.9	9.5	1	10.5	1	10.5	
t_{PLH}	LE	Q	$C_L = 50 \text{ pF}$		8.5	13.3	1	14.5	1	14.5	ns
t_{PHL}					8.5	13.3	1	14.5	1	14.5	
t_{PZH}	$\overline{\text{OE}}$	Q	$C_L = 50 \text{ pF}$		7.1	11.9	1	13.5	1	13.5	ns
t_{PZL}					7.1	11.9	1	13.5	1	13.5	
t_{PHZ}	$\overline{\text{OE}}$	Q	$C_L = 50 \text{ pF}$		6.8	11.2	1	12	1	12	ns
t_{PLZ}					6.8	11.2	1	12	1	12	
$t_{sk(o)}$			$C_L = 50 \text{ pF}$			1 ⁽²⁾			1	ns	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

4.8 Noise Characteristics

$V_{CC} = 5 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHCT373			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	1.2	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	-1.2	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

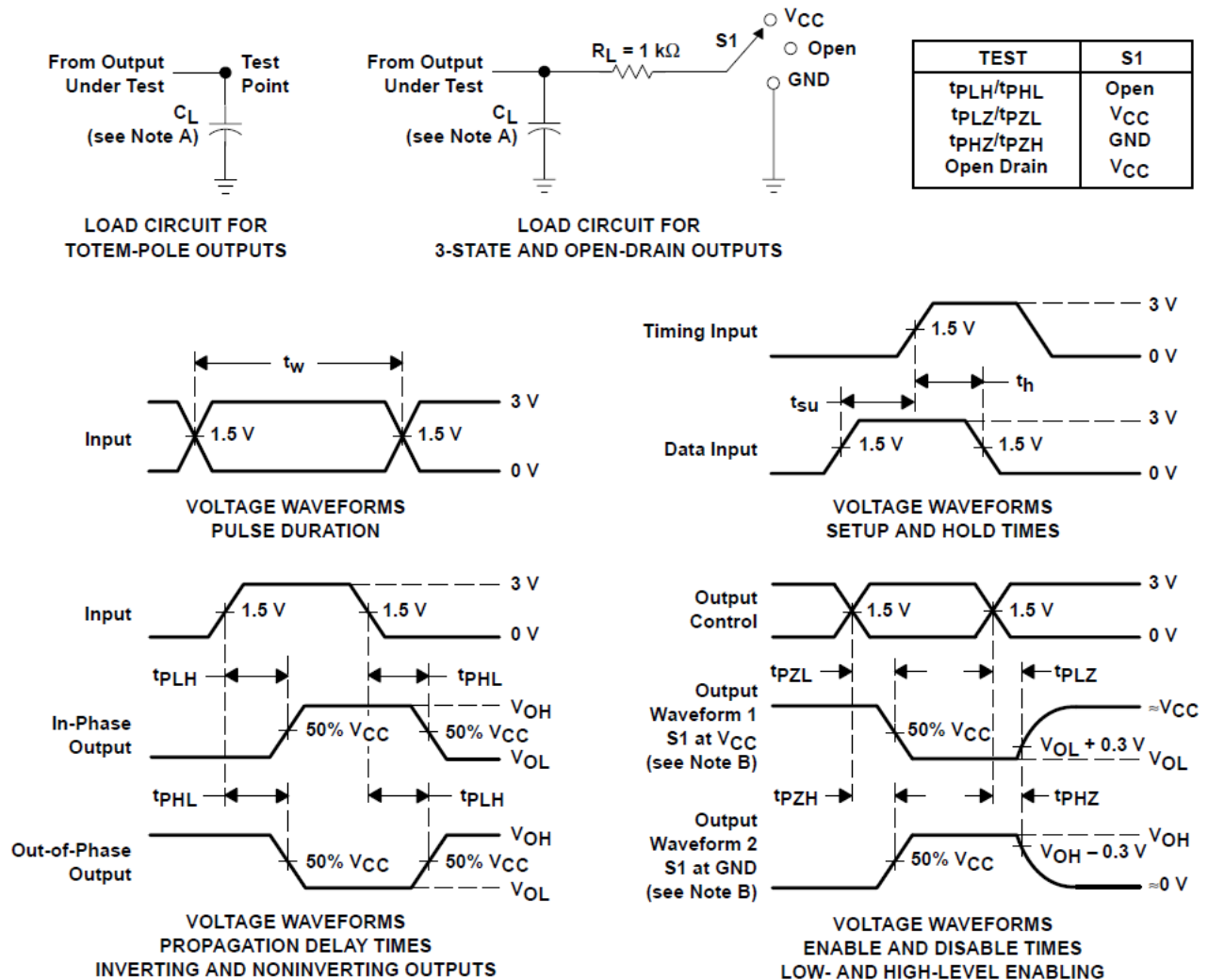
(1) Characteristics are for surface-mount packages only.

4.9 Operating Characteristics

$V_{CC} = 5 V$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance No load, $f = 1 \text{ MHz}$	17	pF

5 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram

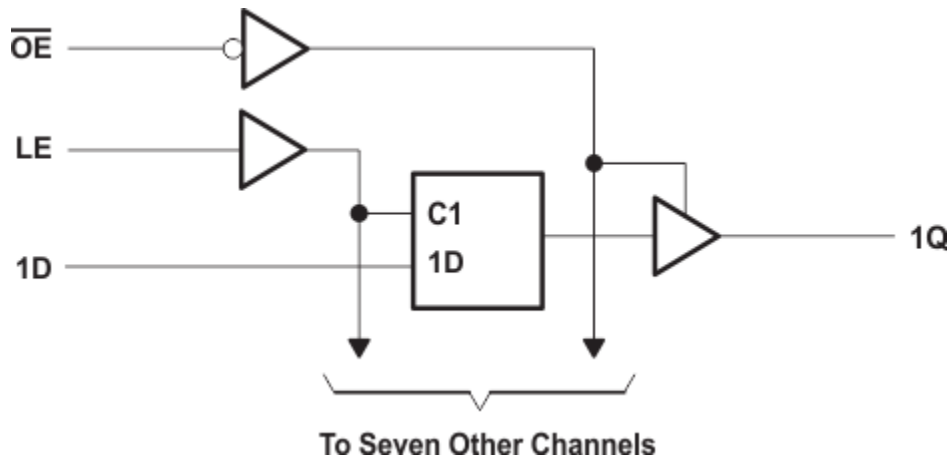


图 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table
(Each Latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

7 Application and Implementation

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, $0.1 \mu\text{f}$ is recommended; if there are multiple V_{CC} pins, then $0.01 \mu\text{f}$ or $0.022 \mu\text{f}$ is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A $0.1 \mu\text{f}$ and a $1 \mu\text{f}$ are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

7.2.2 Layout Example

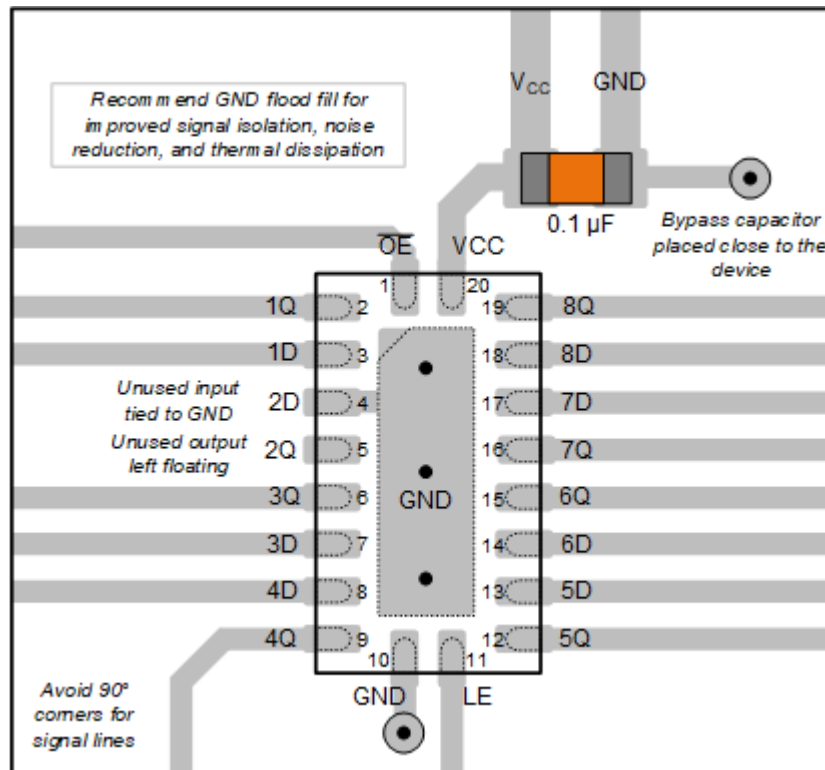


图 7-1. Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT373	Click here	Click here	Click here	Click here	Click here
SN74AHCT373	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision N (August 2023) to Revision O (August 2024) Page

- 向 [器件信息](#) 表添加了封装尺寸..... 1
- Updated R^θ JA values: PW = 83 to 116.8, all values in °C/W 5

Changes from Revision M (July 2023) to Revision N (August 2023) Page

- 添加了 [器件信息表](#)、[引脚功能表](#)、[ESD 等级表](#)、[热信息表](#)、[器件功能模式](#)、[器件和文档支持](#) 部分以及 [机械](#)、[封装和可订购信息](#) 部分..... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686701Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686701Q2A SNJ54AHCT 373FK	Samples
5962-9686701QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J	Samples
5962-9686701QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W	Samples
SN74AHCT373DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373	Samples
SN74AHCT373DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	AHCT373	
SN74AHCT373DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373	Samples
SN74AHCT373N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT373N	Samples
SN74AHCT373NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT373	Samples
SN74AHCT373PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	HB373	
SN74AHCT373PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB373	Samples
SNJ54AHCT373FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686701Q2A SNJ54AHCT 373FK	Samples
SNJ54AHCT373J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QR A SNJ54AHCT373J	Samples
SNJ54AHCT373W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686701QS A SNJ54AHCT373W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT373, SN74AHCT373 :

● Catalog : [SN74AHCT373](#)

● Military : [SN54AHCT373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT373DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT373NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT373DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT373DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT373NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHCT373PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686701Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686701QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT373N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT373W	W	CFP	20	25	506.98	26.16	6220	NA

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

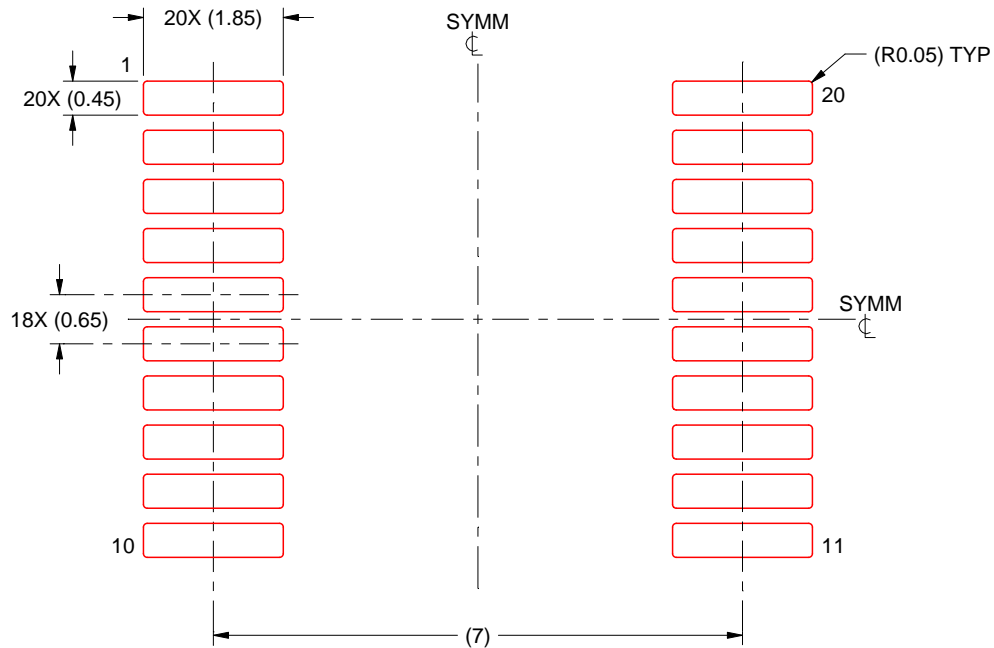
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

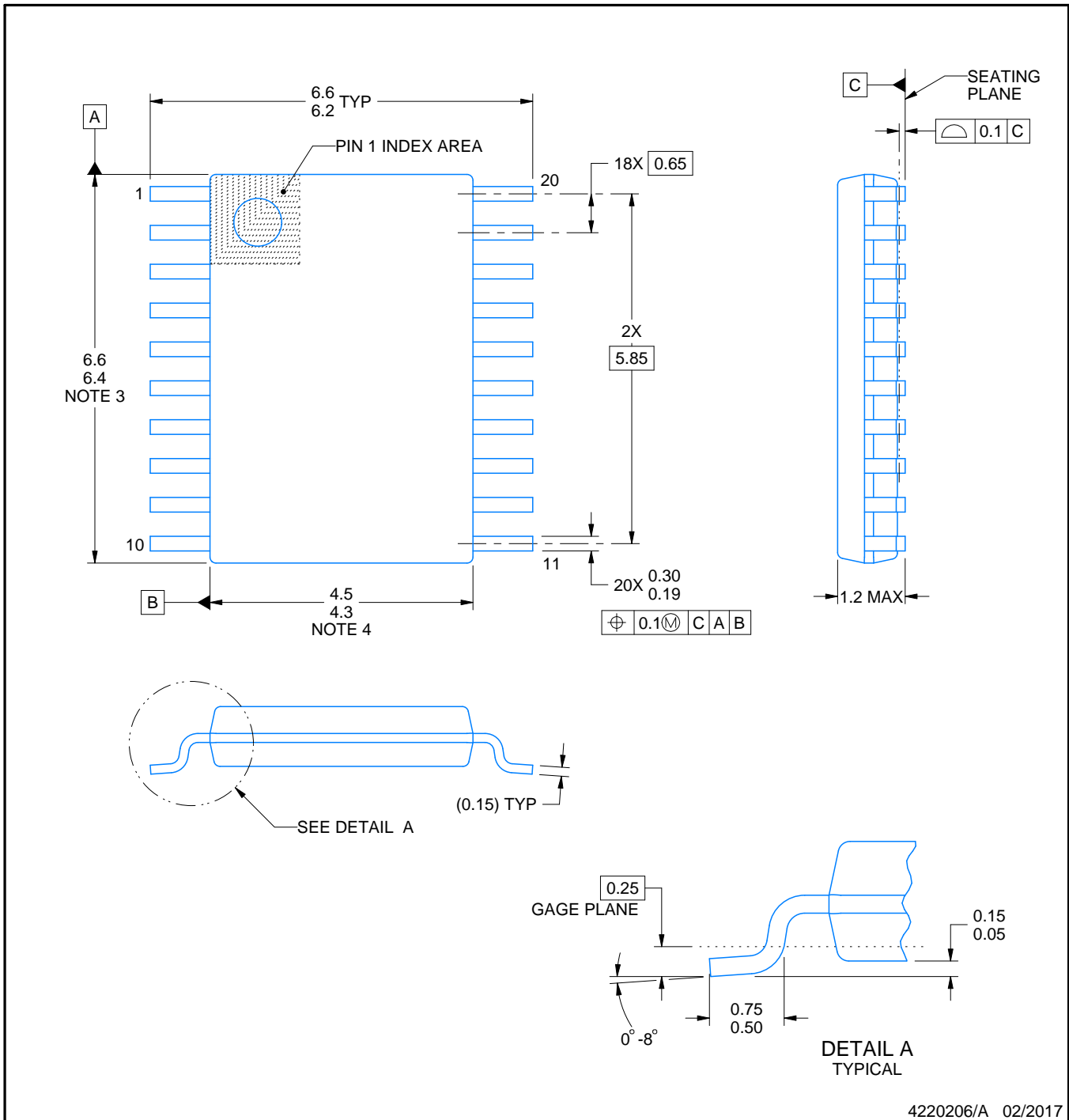
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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