# SN74CB3T3125 四通道 FET 总线开关 2.5V、3.3V 低压总线开关，带可耐受 5V 电压的电平转换器

## 1 特性

- 输出电压转换跟踪 $V_{CC}$
- 所有数据 I/O 端口均支持混合模式信号运行
  - 5V 输入降至 3.3V 输出电平位移，$V_{CC}$ 为 3.3V
  - 5V/3.3V 输入降至 2.5V 输出电平位移，$V_{CC}$ 为 2.5V
- 支持器件加电与断电的 5V 耐压 I/O
- 具有接近零传播延迟的双向数据流
- 低导通状态电阻 ($r_{on}$) 特性（$r_{on}$ = 5Ω 典型）
- 低输入/输出电容可减小负载（$C_{io(OFF)}$ = 4.5pF 典型）
- 数据与控制输入提供下冲钳位二极管
- 低功耗（$I_{CC}$ = 20μA 最大值）
- 2.3V 至 3.6V 的 $V_{CC}$ 工作电压范围
- 数据 I/O 支持 0V 至 5V 信号电平（0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V）
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- $I_{off}$ 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

## 2 应用

- 支持数字 应用：电平转换、USB 接口、总线隔离
- 低功耗便携式设备的理想选择

## 3 说明

SN74CB3T3125 是一种具备低导通状态电阻 ($r_{on}$) 的高速 TTL 兼容型 FET 总线开关，可实现最短传播延迟。该器件提供可跟踪 $V_{CC}$ 的电压转换，能够在所有数据 I/O 端口上全面支持混合模式信号运行。SN74CB3T3125 支持使用 5V TTL，3.3V LVTTL，2.5V CMOS 转换标准以及用户定义转换水平的系统（参阅*典型直流电压转换特性*）。

SN74CB3T3125 被划分为四个 1 位总线开关，各自具备输出使能（1$\overline{OE}$、2$\overline{OE}$、3$\overline{OE}$、4$\overline{OE}$）输入。可以作为四个 1 位总线开关或者一个 4 位总线开关。$\overline{OE}$ 为低时，相关 1 位总线开关打开，A 端口连接至 B 端口，可在两个端口之间实现双向数据流。$\overline{OE}$ 为高时，相关 1 位总线开关关闭，A、B 端口存在高阻抗状态。

该器件完全 适用于 使用 $I_{off}$ 的局部断电应用。$I_{off}$ 特性确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

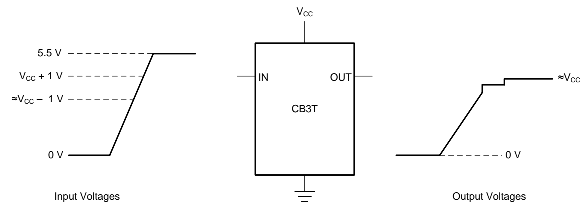
为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 应通过一个上拉电阻器被连接至 $V_{CC}$；该电阻器的最小值由驱动器的电流吸入能力来决定。

器件信息[(1)]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SN74CB3T3125 | VQFN – RGY (14) | 3.50mm x 3.50mm |
| | TSSOP – PW (14) | 5.00mm x 4.40mm |
| | TVSOP – DGV (14) | 3.60mm x 4.40mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型直流电压转换特性




If the input high voltage ($V_{IH}$) level is greater than or equal to $V_{CC}$ + 1 V, and less than or equal to 5.5 V, the output high voltage ($V_{OH}$) level will be equal to approximately the $V_{CC}$ voltage level.

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision B (August 2012) to Revision C** **Page**

- 添加了*应用* 列表、*器件信息* 表、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局*部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 删除了订购信息表。 ... 1
- Changed $t_{en}$ $V_{CC}$ = 3.3 V MAX value From: 4.4 ns To: 8 ns in the *Switching Characteristic* ... 5

**Changes from Revision A (April 2009) to Revision B** **Page**

- 更新了*典型直流电压转换特性* ... 1



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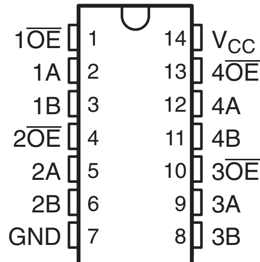
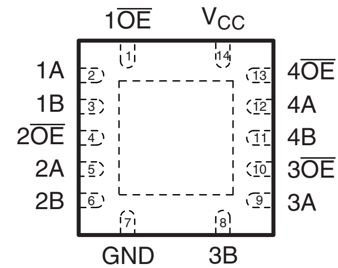
## 5 Pin Configuration and Functions




### Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1$\overline{OE}$ | 1 | I | Active-low enable for switch 1 |
| 1A | 2 | I/O | Switch 1 A terminal |
| 1B | 3 | I/O | Switch 1 B terminal |
| 2$\overline{OE}$ | 4 | I | Active-low enable for switch 2 |
| 2A | 5 | I/O | Switch 2 A terminal |
| 2B | 6 | I/O | Switch 2 B terminal |
| GND | 7 | - | Ground |
| 3A | 8 | I/O | Switch 3 A terminal |
| 3B | 9 | I/O | Switch 3 B terminal |
| 3$\overline{OE}$ | 10 | I | Active-low enable for switch 3 |
| 4A | 11 | I/O | Switch 4 A terminal |
| 4B | 12 | I/O | Switch 4 B terminal |
| 4$\overline{OE}$ | 13 | I | Active-low enable for switch 4 |
| $V_{CC}$ | 14 | - | Supply voltage pin |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range[2] | | –0.5 | 7 | V |
| $V_{IN}$ | Control input voltage range[2] [3] | | –0.5 | 7 | V |
| $V_{I/O}$ | Switch I/O voltage range[2] [3] [4] | | –0.5 | 7 | V |
| $I_{IK}$ | Control input clamp current | $V_{IN}$ < 0 | | –50 | mA |
| $I_{I/OK}$ | I/O port clamp current | $V_{I/O}$ < 0 | | –50 | mA |
| $I_{I/O}$ | ON-state switch current[5] | | | ±128 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | 5.5 | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74CB3T3125 | | | UNIT |
|---|---|---|---|---|---|
| | | VQFN (RGY) | TSSOP (PW) | TVSOP (DGV) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 55.5 | 123.3 | 154.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.9 | 53.0 | 64.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 30.9 | 66.3 | 88.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.6 | 9.1 | 10.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 30.9 | 65.7 | 87.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 14.6 | - | - | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 6.5 Electrical Characteristics[1]

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | | See Figure 3 through Figure 5 | | | | | |
| $I_{IN}$ | Control inputs | $V_{CC}$ = 3.6 V, $V_{IN}$ = 3.6 V to 5.5 V or GND | | | | ±10 | µA |
| $I_I$ | | $V_{CC}$ = 3.6 V, Switch ON, $V_{IN}$ = $V_{CC}$ or GND | $V_I$ = $V_{CC}$ – 0.7 V to 5.5 V | | | ±20 | µA |
| | | | $V_I$ = 0.7 V to $V_{CC}$ – 0.7 V | | | –40 | |
| | | | $V_I$ = 0 to 0.7 V | | | ±5 | |
| $I_{OZ}$[3] | | $V_{CC}$ = 3.6 V, $V_O$ = 0 to 5.5 V, $V_I$ = 0, Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | | ±10 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, $V_O$ = 0 to 5.5 V, $V_I$ = 0 | | | | 10 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, $V_{IN}$ = $V_{CC}$ or GND | $V_I$ = $V_{CC}$ or GND | | | 20 | µA |
| | | | $V_I$ = 5.5 V | | | 20 | |
| $\Delta I_{CC}$[4] | Control inputs | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 300 | µA |
| $C_{in}$ | Control inputs | $V_{CC}$ = 3.3 V, $V_{IN}$ = $V_{CC}$ or GND | | | 3 | | pF |
| $C_{io(OFF)}$ | | $V_{CC}$ = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, $V_{IN}$ = $V_{CC}$ or GND | | | 4.5 | | pF |
| $C_{io(ON)}$ | | $V_{CC}$ = 3.3 V, Switch ON, $V_{IN}$ = $V_{CC}$ or GND | $V_{I/O}$ = 5.5 V or 3.3 V | | 4 | | pF |
| | | | $V_{I/O}$ = GND | | 10 | | |
| $r_{on}$[5] | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V, $V_I$ = 0 | $I_O$ = 24 mA | | 5 | 8 | Ω |
| | | | $I_O$ = 16 mA | | 5 | 8 | |
| | | $V_{CC}$ = 3 V, $V_I$ = 0 | $I_O$ = 64 mA | | 5 | 7 | |
| | | | $I_O$ = 32 mA | | 5 | 7 | |

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
(2) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$[1] | A or B | B or A | | 0.15 | | 0.25 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1 | 8.5 | 1 | 8 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1 | 9 | 1 | 9 | ns |

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 6.7 Typical Characteristics

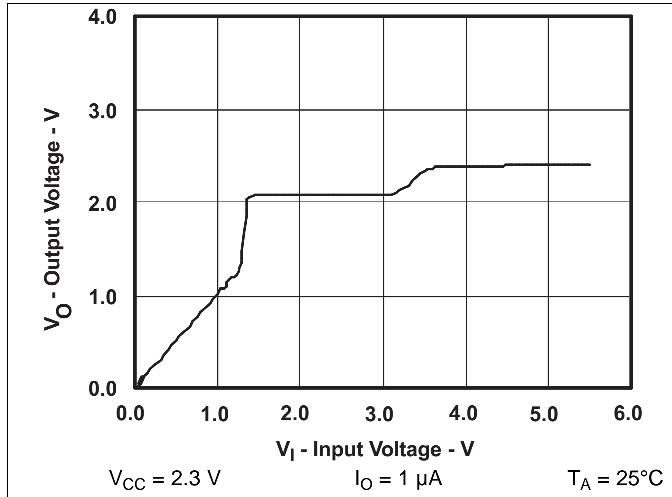


Figure 1. Data Output Voltage vs Data Input Voltage

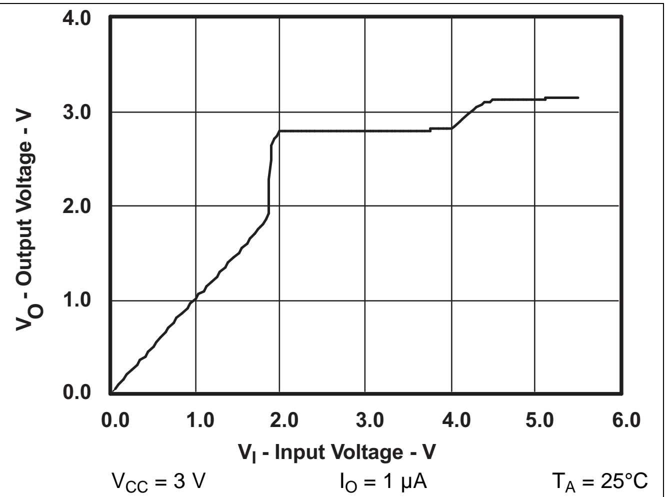


Figure 2. Data Output Voltage vs Data Input Voltage

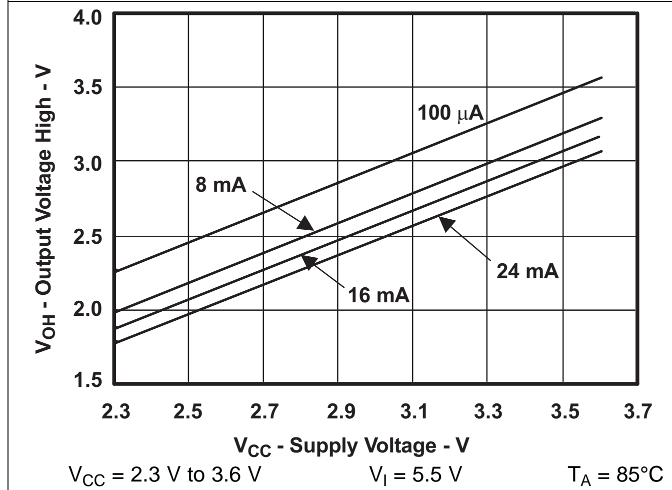


Figure 3. Output Voltage High vs Supply Voltage

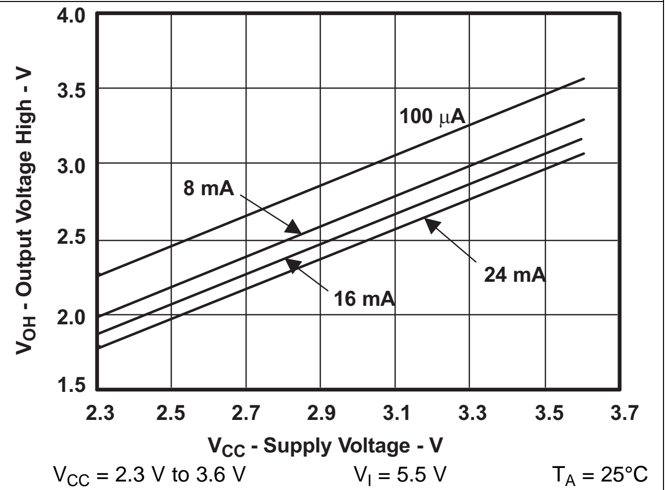


Figure 4. Output Voltage High vs Supply Voltage

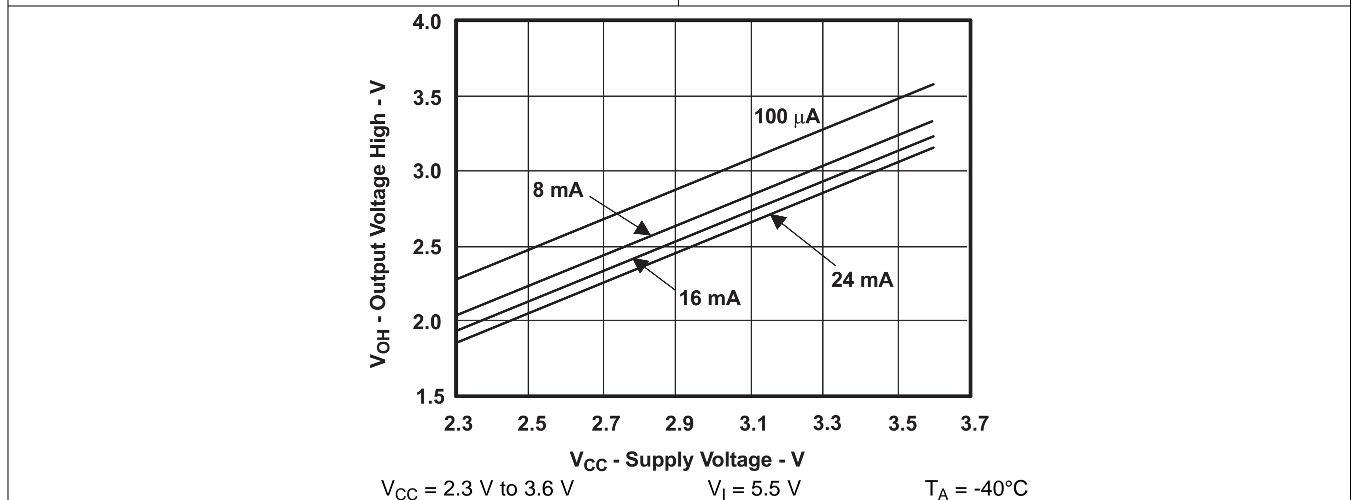


Figure 5. Output Voltage High vs Supply Voltage


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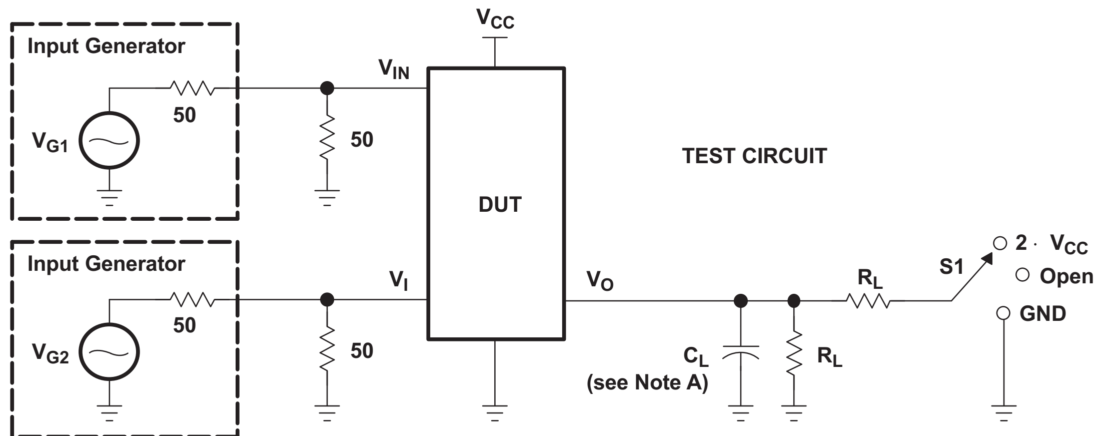
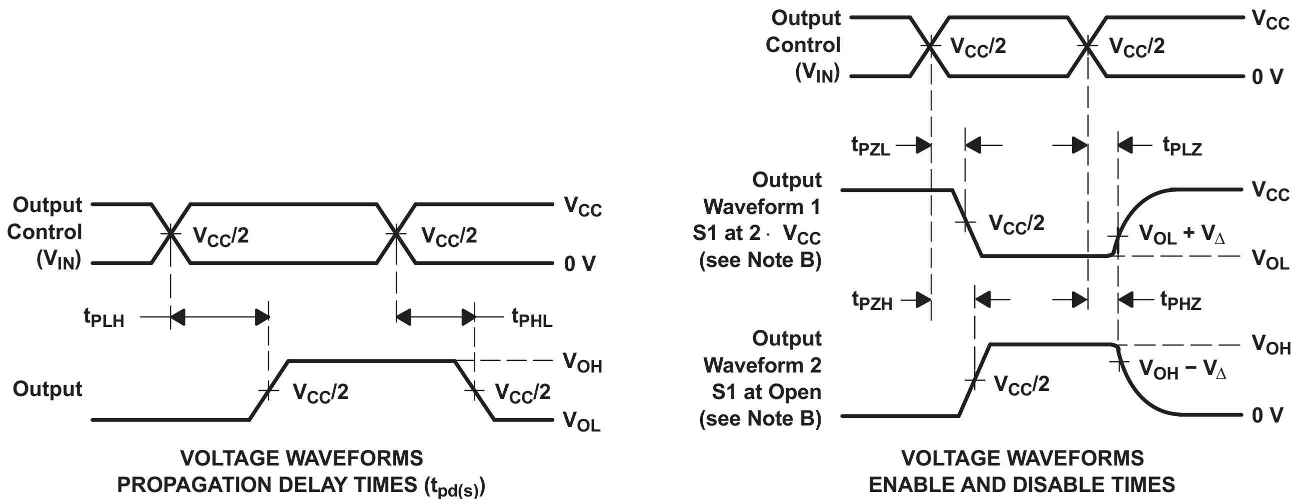
# 7 Parameter Measurement Information




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | V |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500<br>500 | 3.6 V or GND<br>5.5 V or GND | 30 pF<br>50 pF | |
| $t_{PLZ}/t_{PZL}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | 2 · $V_{CC}$<br>2 · $V_{CC}$ | 500<br>500 | GND<br>GND | 30 pF<br>50 pF | 0.15 V<br>0.3 V |
| $t_{PHZ}/t_{PZH}$ | 2.5 V ± 0.2 V<br>3.3 V ± 0.3 V | Open<br>Open | 500<br>500 | 3.6 V<br>5.5 V | 30 pF<br>50 pF | 0.15 V<br>0.3 V |




NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_O$ = 50 Ω, $t_r$ 2.5 ns, $t_f$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

**Figure 6. Test Circuit and Voltage Waveforms**

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# 8 Detailed Description

## 8.1 Overview

The SN74CB3T3215 device is organized as four 1-bit bus switches with separate ouput-enable (1OE, 2OE, 3OE, and 4 OE) inputs. When OE is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CB3T3125 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram

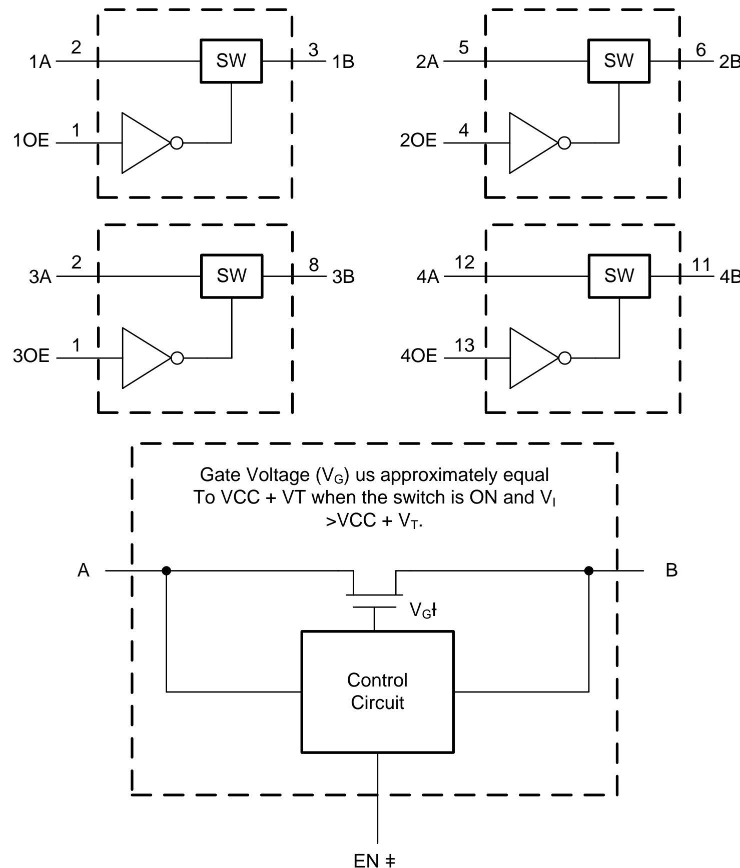


**Figure 7. Simplified Schematic, Each FET Switch (SW)**


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## 8.3 Feature Description

The SN74CB3T3125 is ideal for low-power portable equipment. Power consumption is low by design, $I_{CC}$ = 20 μA, On-state resistance is low ($r_{on}$ = 5 Ω) It has bidirectional data flow with near zero propagation delay. The devices minimizes loading due to the low input/output capacitance $C_{io(OFF)}$ = 4.5 pF Typical. Operating VCC range from 2.3 V to 3.6 V. The output tracks VCC. Data and control inputs provide undershoot clamp diodes. Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs. It supports mixed-mode signal operation on all data I/O ports. Data I/Os support 0- to 5-V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V). The device is protected from damaging current, Ioff supports partial shutdown which prevents the current from flowing back through the device when it is powered down. In addition, it has 5-V tolerant I/Os with device powered up or powered down. The device is latch-up resistant with 250 mA exceeding the JESD 17 standard, providing protection from destruction due to latch-up. This device is protected against electrostatic discharge. It is tested per JESD 22 using 2000-V Human-Body Model (A114-B, Class II), and 1000-V Charged-Device Model (C101).

## 8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74CB3T3125.

**Table 1. Function Table (Each Bus Switch)**

| INPUT $\overline{OE}$ | INPUT/OUTPUT A | FUNCTION |
|---|---|---|
| L | B | A port = B port |
| H | Z | Disconnect |

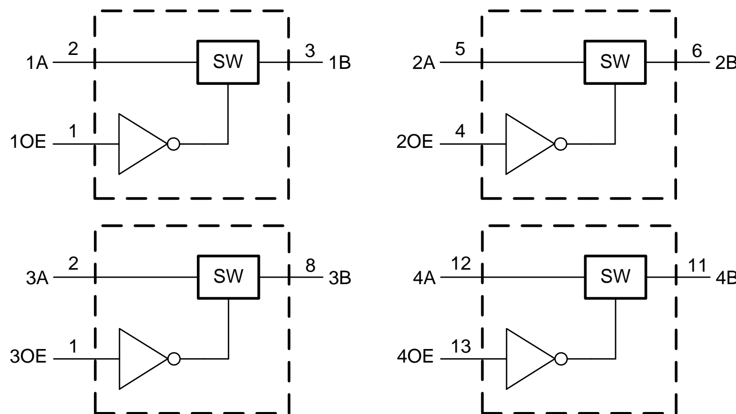


**Figure 8. Logic Diagram (Positive Logic)**

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3 V device. Ideally, set VCC to 3.3 V. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

## 9.2 Typical Application

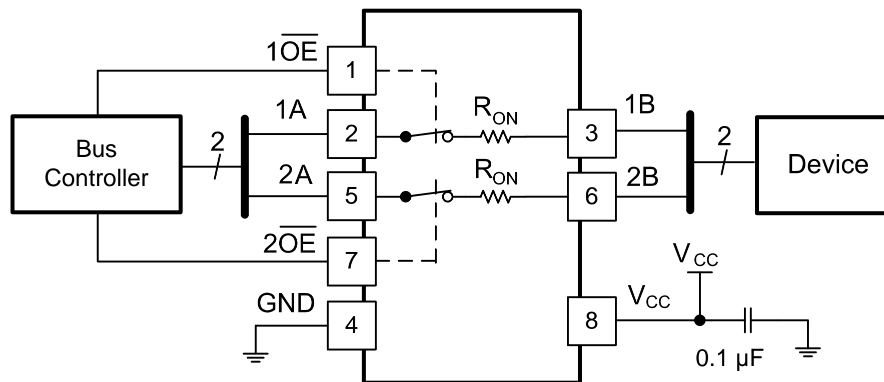


**Figure 9. Application Circuit**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Because this design is for down-translating voltage, no pull-up resistors are required.

### 9.2.2 Detailed Design Procedure

1. Recommended Input conditions – Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions* – Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid VCC.
2. Recommend output conditions – Load currents should not exceed 128 mA on each channel.


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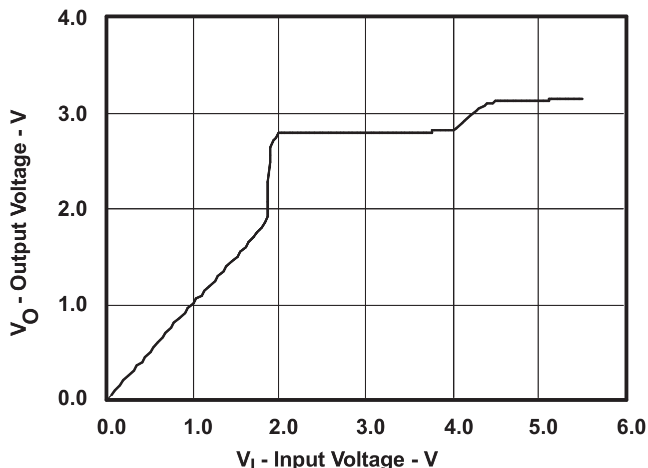
## Typical Application (continued)

### 9.2.3 Application Curves




$V_{CC}$ = 3 V    $I_O$ = 1 µA    $T_A$ = 25°C

**Figure 10. Data Output Voltage vs Data Input Voltage**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions.

Each VCC terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled VCC, then a 0.01-µF or 0.022-µF capacitor is recommended for each VCC because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example VCC and VDD, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

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# 11 Layout

## 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example

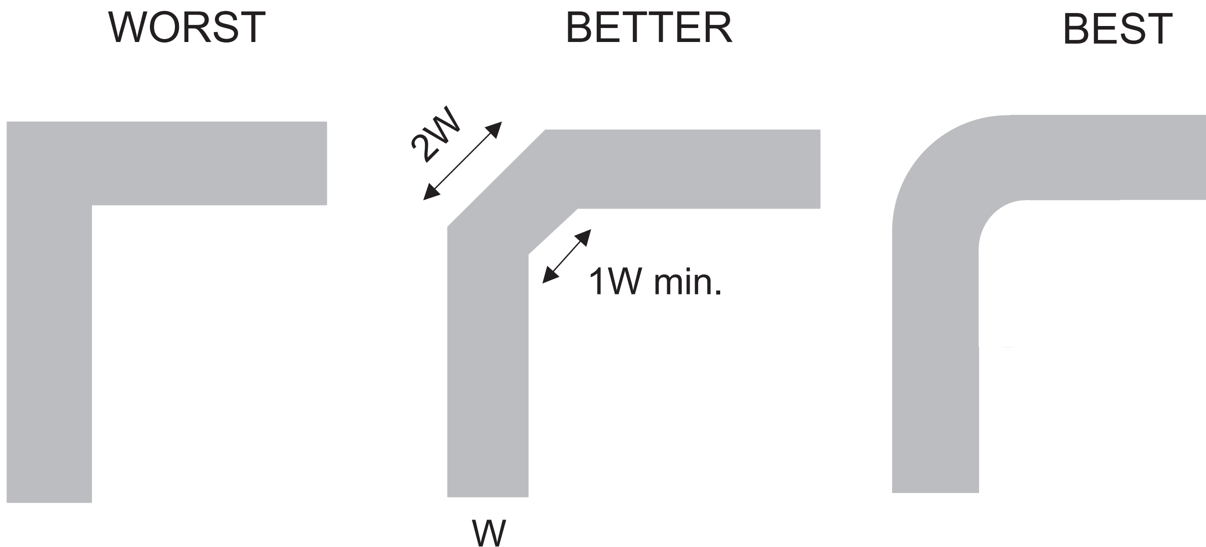


**Figure 11. Example Layout**


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# 12 器件和文档支持

## 12.1 器件支持

## 12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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## 12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CB3T3125DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS125 | Samples |
| SN74CB3T3125PW | LIFEBUY | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS125 | |
| SN74CB3T3125PWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS125 | Samples |
| SN74CB3T3125PWRE4 | LIFEBUY | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS125 | |
| SN74CB3T3125RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | KS125 | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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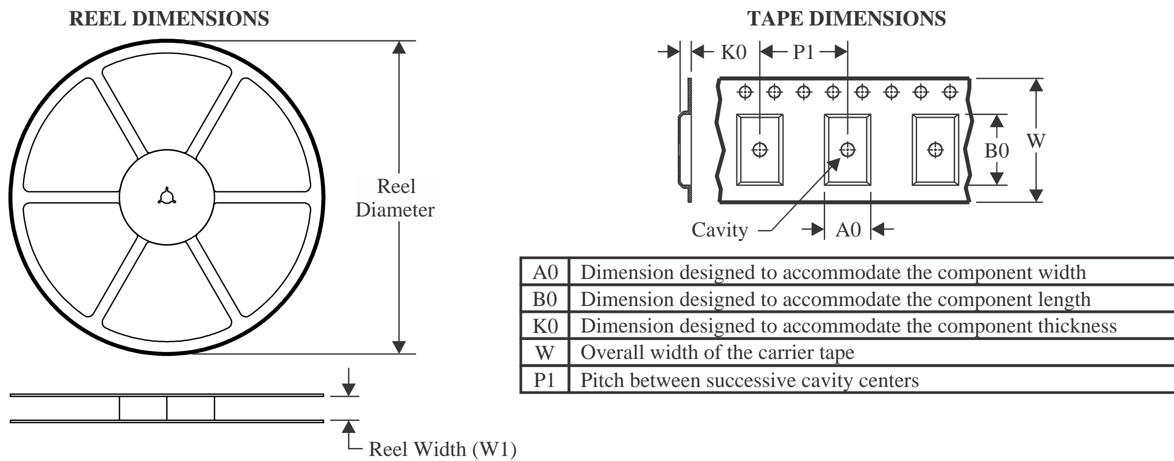
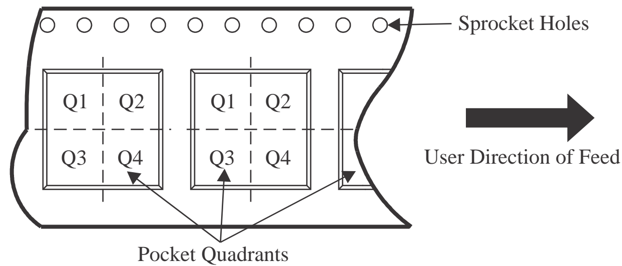
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

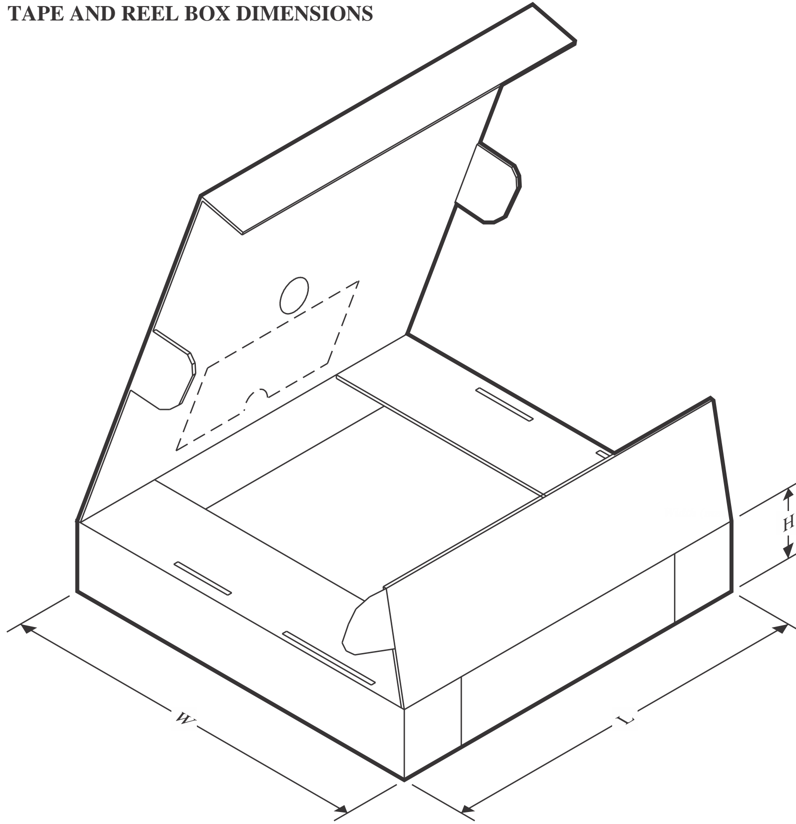
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CB3T3125DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CB3T3125PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CB3T3125RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

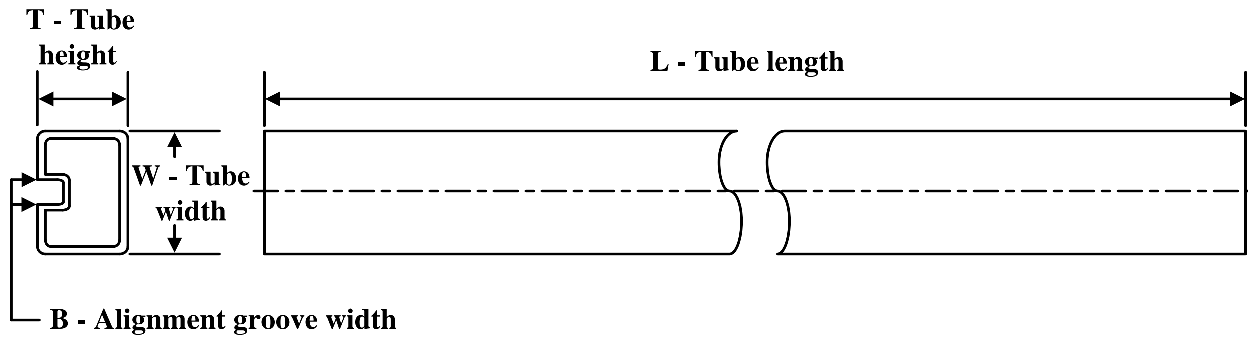
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CB3T3125DGVR | TVSOP | DGV | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CB3T3125PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CB3T3125RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74CB3T3125PW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

Pin 1 Index Area
Top and Bottom
F

0,20 Nominal
Lead Frame

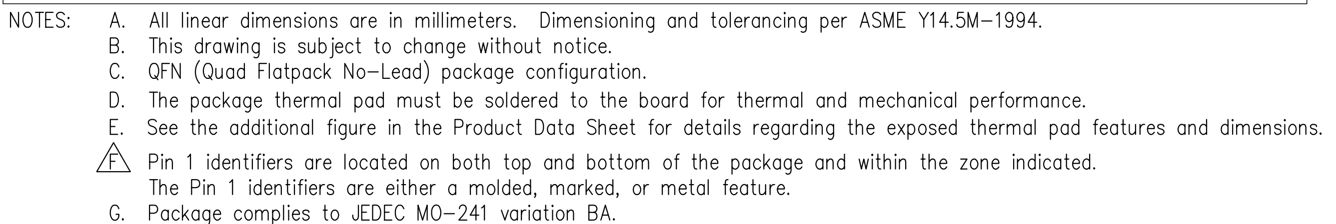
Seating Plane

0,05
0,00
Seating Height

THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

Bottom View

4203539-2/I 06/2011


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

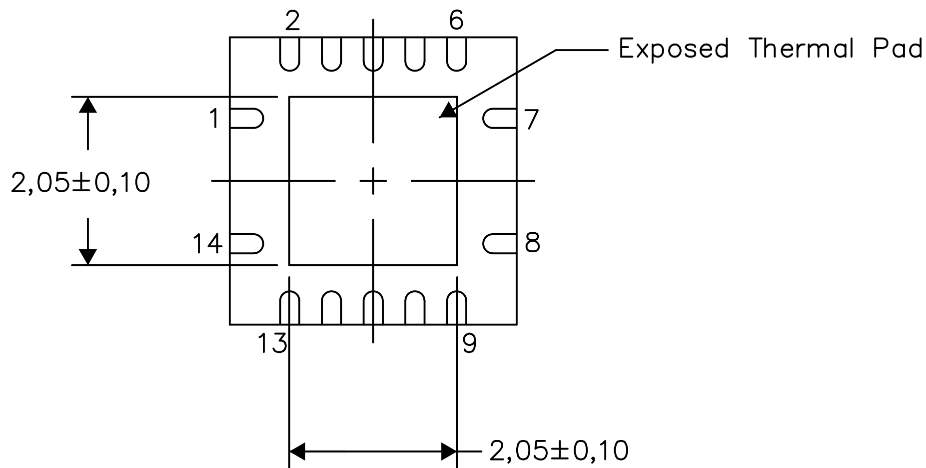
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

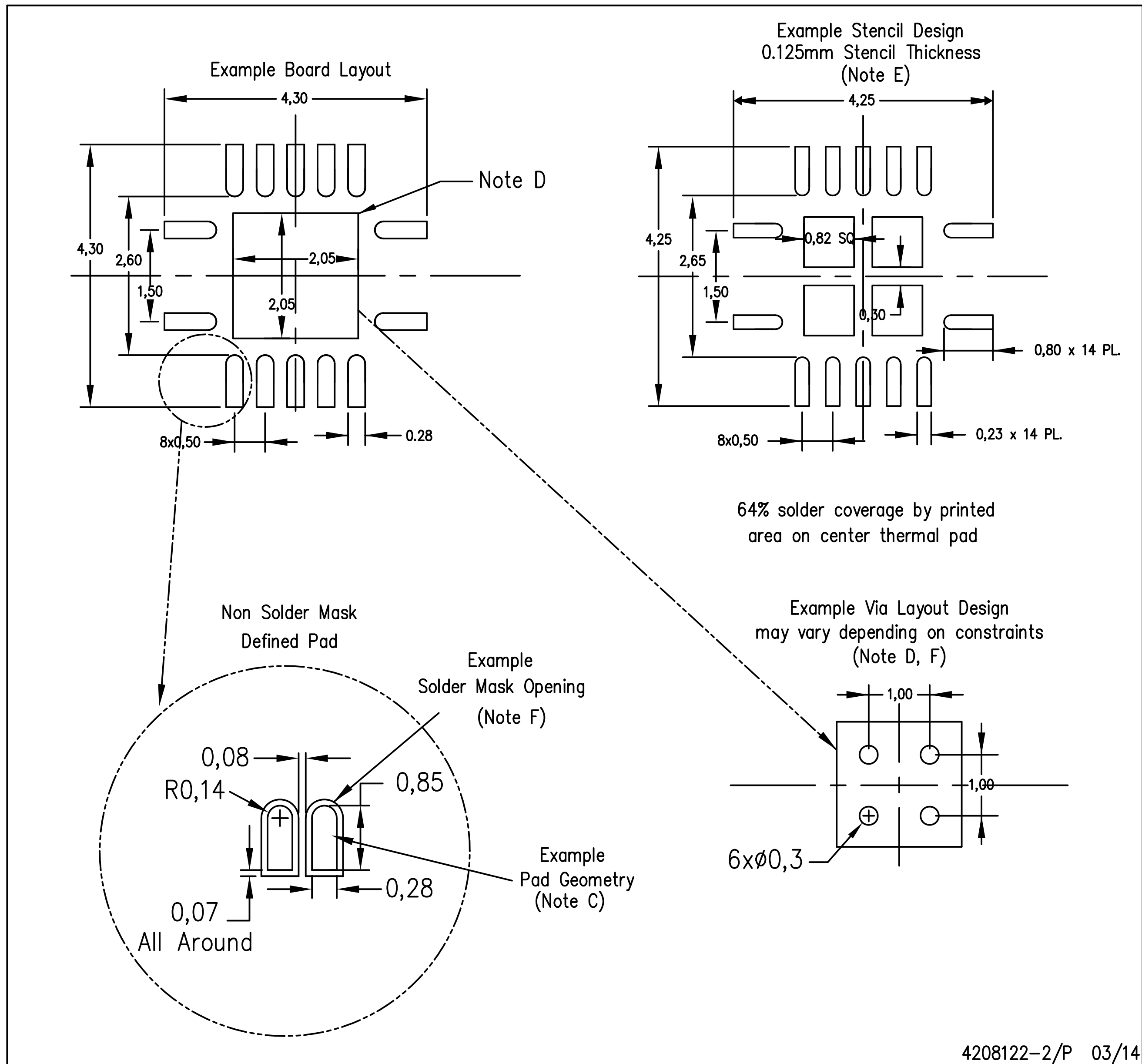



Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

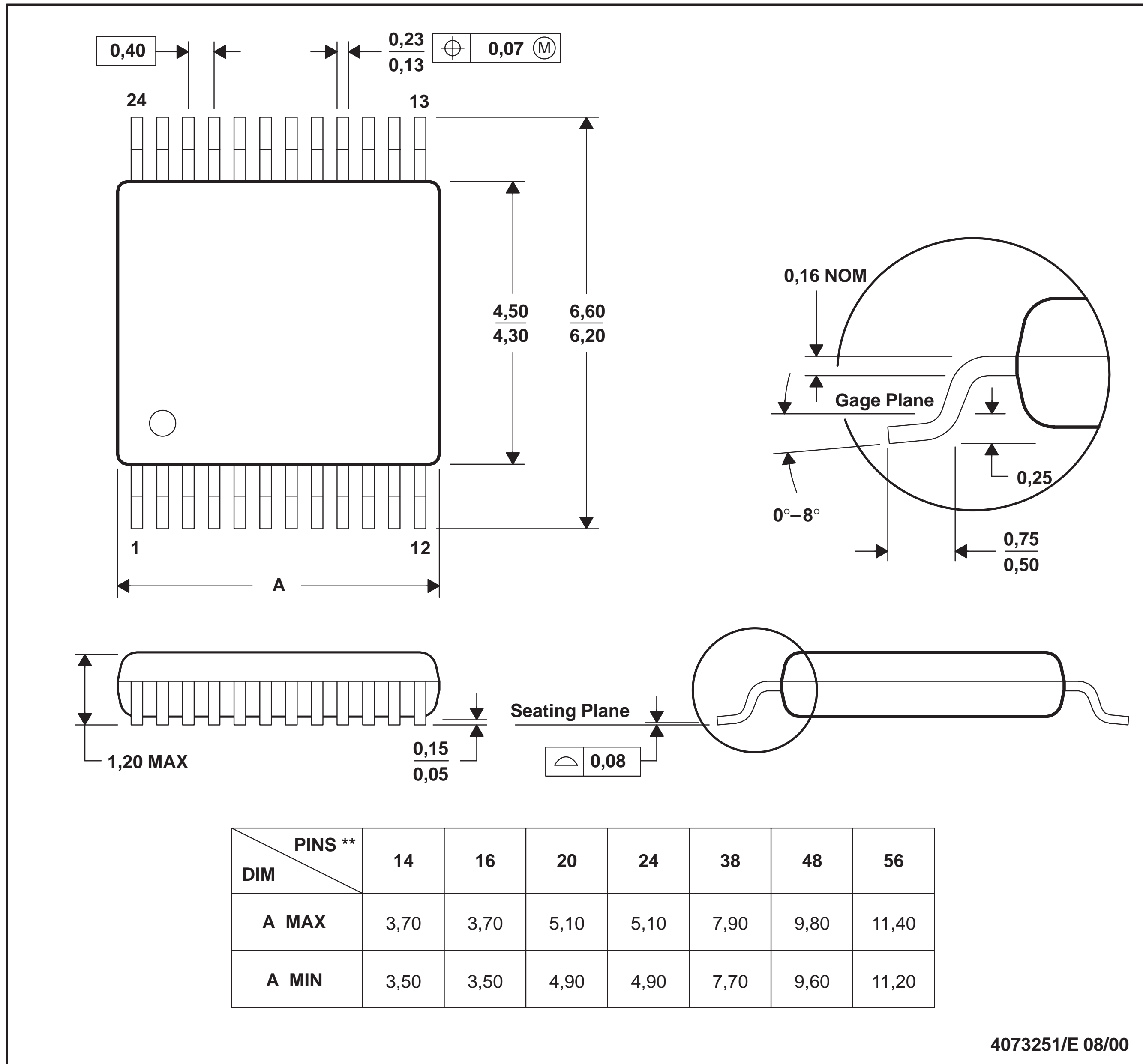
NOTE: All linear dimensions are in millimeters




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**



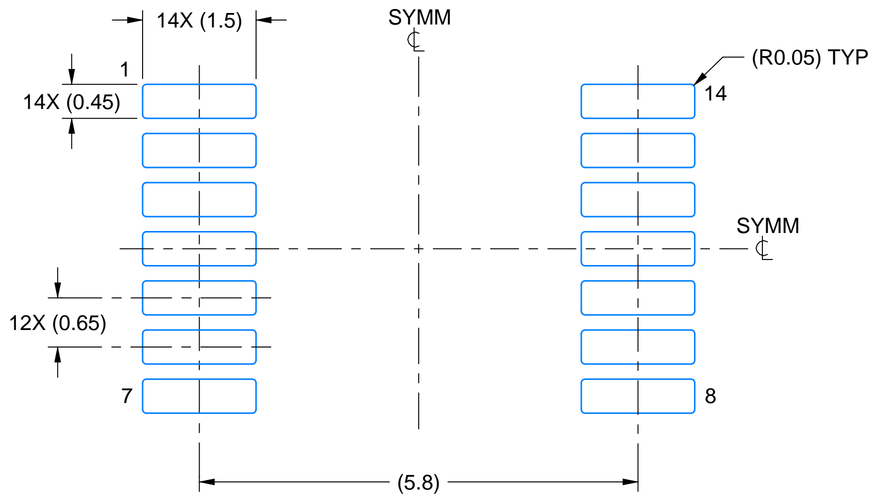

| PINS ** / DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

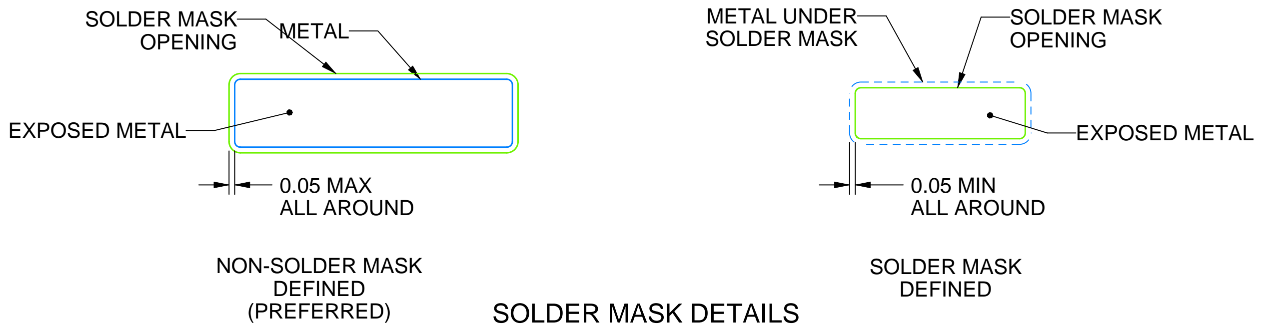
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

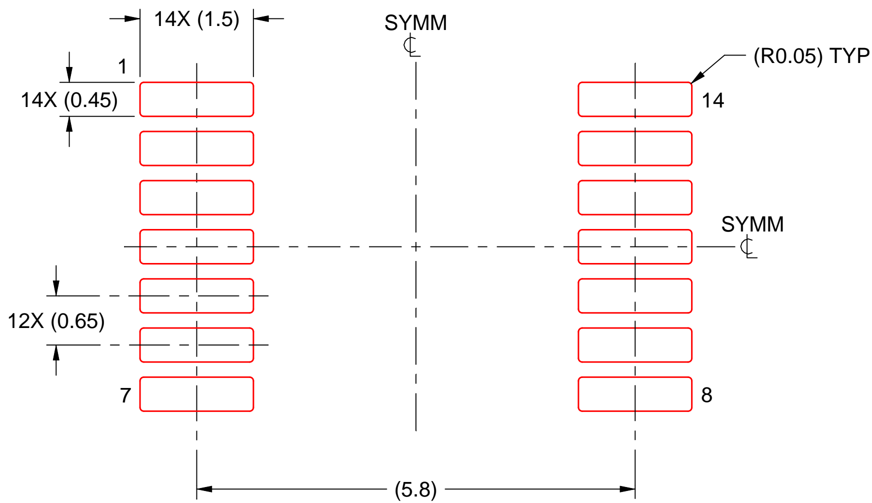
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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