SN74HC4852 具有注入电流效应控制功能的双通道 4 线至 1 线模拟多路复用器/多路解复用器

1 特性

- 注入电流交叉耦合 <1mV/mA（请参阅图 8-1）
- 低开关间串扰
- 与 SN74HC4052、SN74LV4052A 和 CD4052B 引脚兼容
- 2V 至 5.5V V_{CC} 运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 模拟信号开关或多路复用：
  - 信号门控、调制器、静噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用
  - 音频和视频信号路由
- 传输门逻辑实施
- 模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
- 电机转速控制
- 电池充电器
- 直流/直流转换器

3 说明

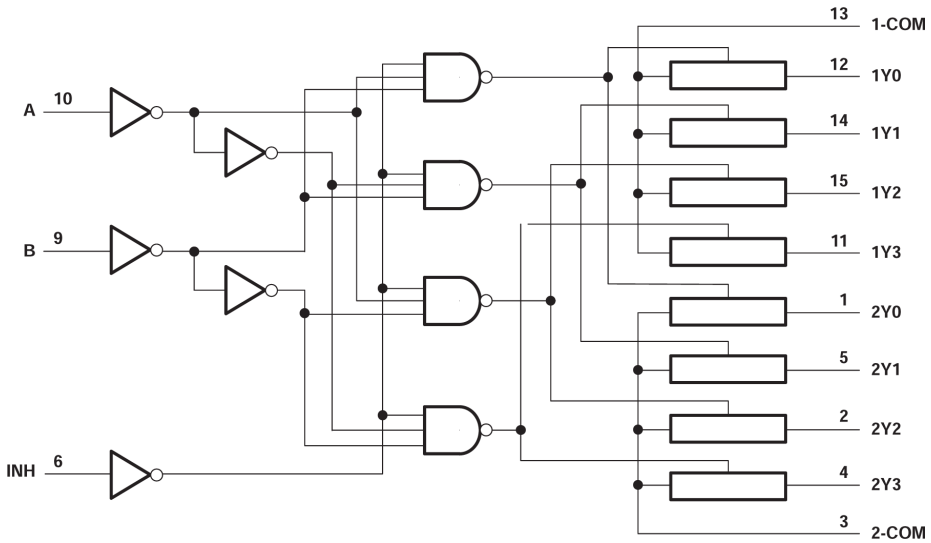
这款双路 4 线至 1 线 CMOS 模拟多路复用器/多路解复用器与 4052 功能引脚兼容，并且还具有注入电流效应控制功能。此控制功能在电压通常超过正常电源电压的汽车应用中具有出色的价值。

注入电流效应控制功能允许已禁用的模拟输入通道上的信号超过电源电压，而不会影响已启用的模拟通道的信号。这样就不再需要通常使用的外部二极管/电阻器网络将模拟通道信号保持在电源电压范围内。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN74HC4852	PW（TSSOP，16）	5mm × 6.4mm

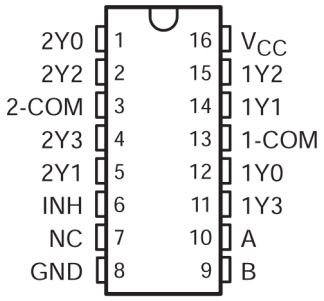
(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



功能图

Table of Contents

4 Pin Configuration and Functions



NC – No internal connection

图 4-1. PW Package, 16-Pin TSSOP (Top View)

表 4-1. Function Table

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1, A2)	–0.5	V_{CC}+0.5V	V
V_S or V_D	Source or drain voltage (Sx, D)	–0.5	V_{CC}+0.5V	V
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{CC})	–20	20	mA
I_{IOK}	I/O diode current (V_{IO} < 0 or V_{IO} > V_{CC})	–20	20	mA
I_T	Switch through current (V_{IO} = 0 to V_{CC})	–25	25	mA
I_{GND}	Continuous current through V_{CC} or GND	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74HC485x

THERMAL METRIC(1)		SN74HC485x PW (TSSOP) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2		5.5	V
V_{IH}	Input logic high	2V	1.5			V
		2.5V	2.1			
		3.3V	2.3			
		4.5V	3.15			
		5.5V	4.2			
V_{IL}	Input logic low	2V	0		0.5	V
		2.5V	0		0.7	
		3.3V	0		0.8	
		4.5V	0		0.95	
		5.5V	0		1.05	
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, A0, A1, A2)		0		V_{CC}	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	V_{CC} = 2V			1000	ns
		V_{CC} = 3V			800	
		V_{CC} = 3.3V			700	
		V_{CC} = 4.5V			500	
		V_{CC} = 5.5V			400	
T_A	Ambient temperature		–40		125	°C

5.5 Electrical Characteristics

At specified V_{CC} ±10%
Typical values measured at nominal V_{CC}.

PARAMETER		TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
				25°C			– 40°C to 85°C			– 40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
R_{ON}	On-state switch resistance	V_S = 0V to V_{CC} I_{SD} = 0.5mA	2V		500	650			670			700	Ω
			3V		215	280			320			360	
			3.3V		210	270			305			345	
			4.5V		160	210			240			270	
ΔR_{ON}	On-state switch resistance matching between inputs	V_S = V_{CC} / 2 I_{SD} = 0.5mA	2V		4	18			22			24	Ω
			3V		2	12			14			16	
			3.3V		2	12			14			16	
			4.5V		2	8			12			16	
I_I	Control input current	V_I = V_{CC} or GND	5V			±0.1			±0.1			±1	μA
$I_{S(OFF)}$	Off-state switch leakage current (any one channel)	Switch Off V_{INH}=V_{IH} V_D = V_{CC} / GND V_S = GND / V_{CC}	5V			±0.1			±0.5			±1	μA
	Off-state switch leakage current (common channel)					±0.2			±2			±4	μA
$I_{S(ON)}$	Channel on-state leakage current	Switch Off V_{INH}=V_{IL} V_D = V_{CC} / GND V_S = GND / V_{CC}	5V			±0.1			±0.5			±1	μA
I_{DD}	V_{CC} supply current	Logic inputs = 0V or V_{CC}	5V			2			5			10	μA
C_{IC}	Control input capacitance	A, B, C, INH			3.5	10			10			10	pF
C_{IS}	Common terminal capacitance	Switch off			22	40			40			40	pF
C_{OS}	Switch terminal capacitance	Switch off			6.7	15			15			15	pF
C_{PD}	Power Dissipation Capacitance	No Load t_r = t_f = 1ns f = 1MHz	3.3V		32								pF
			5V		37								

5.6 Timing Characteristics

At specified V_{CC} ±10%
Typical values measured at nominal V_{CC}.

PARAMETER		TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
				25°C			– 40°C to 85°C			– 40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS(1)													
t_{PD}	Propagation delay	C_L = 50pF Sx to D, D to Sx	2V	7	19.5	33	6		34	6		35	ns
			3V	3.6	12	16.5	2.5		18	2.5		19.5	
			3.3V	3.9	11	15	2.5		16.5	2.5		18.5	
			5V	2.3	8.6	11.6	2.1		12.5	2		13.5	
t_{TRAN}	Transition-time between inputs	R_L = 10kΩ, C_L = 50pF Ax to D, Ax to Sx	2V	19.6	44	94	15.4		103	13.8		103	ns
			3V	12.4	30	63	9.3		67	8.2		67	
			3.3V	11.4	23	51	8.5		54	7.5		54	
			5V	9.3	18	43	6.5		46	5.6		46	
$t_{ON(EN)}$	Turnon-time from enable	R_L = 10kΩ, C_L = 50pF EN to D, EN to Sx	2V	15	39	64	13.8		75	12.5		75	ns
			3V	7.9	30	45	6.2		50	5.5		55	
			3.3V	7	26.5	42.5	6.4		47.5	5.4		52.5	
			5V	4	24	40	4.3		45	3.4		50	
$t_{OFF(EN)}$	Turnoff time from enable	R_L = 10kΩ, C_L = 50pF EN to D, EN to Sx	2V	26	48.4	100	25		105	25		115	ns
			3V	15	21	90	14		100	14		110	
			3.3V	12	15	85	11		95	11		105	
			5V	24.5	41.4	80	24.2		90	24		100	

(1) t_{PLH}/t_{PHL}= t_{PD} propagation delay time, t_{PZH}/t_{PZL}= $t_{ON(EN)}$ enable delay time, t_{PHZ}/t_{PLZ} = $t_{OFF(EN)}$ disable delay time, t_{PLH}/t_{PHL} Channel select = t_{TRAN}

5.7 Injection Current Coupling

At specified V_{CC} ±10%
Typical values measured at nominal V_{CC} and T_A = 25°C.

PARAMETER		V_{CC}	TEST CONDITIONS		-40°C to 125°C			UNIT
					MIN	TYP	MAX	
INJECTION CURRENT COUPLING								
ΔV_{OUT}	Maximum shift of output voltage of enabled analog input(1)	3.3V	$R_S \leqslant$ 3.9kΩ	$I_{INJ} \leqslant$ 1mA		0.05	1	mV
		5V				0.1	1	
		3.3V		$I_{INJ} \leqslant$ 10mA		0.345	5	
		5V				0.067	5	
		3.3V	$R_S \leqslant$ 20kΩ	$I_{INJ} \leqslant$ 1mA		0.05	2	
		5V				0.11	2	
		3.3V		$I_{INJ} \leqslant$ 10mA		0.05	20	
		5V				0.024	20	

(1) I_{INJ} = total current injected into all disabled channels

6 Parameter Measurement Information

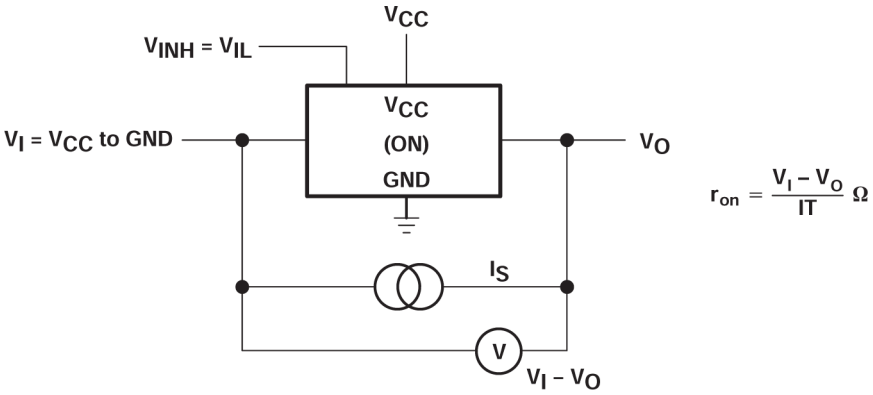


图 6-1. On-State Resistance Test Circuit

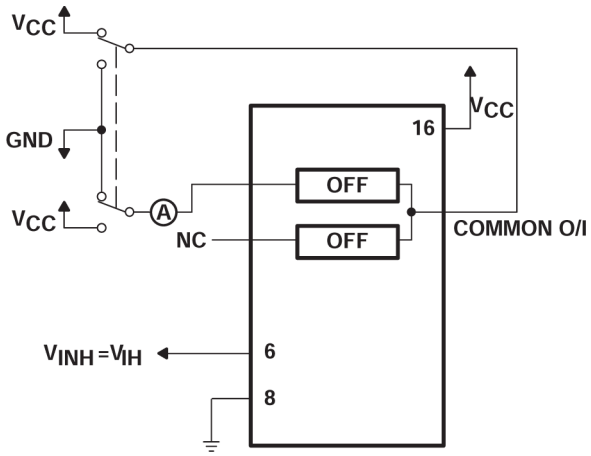


图 6-2. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

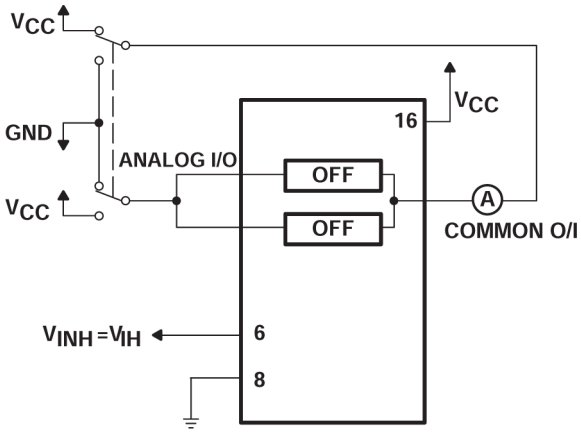


图 6-3. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

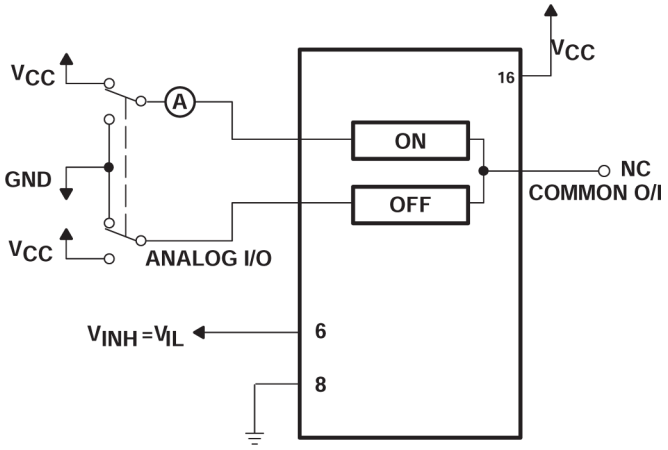


图 6-4. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup

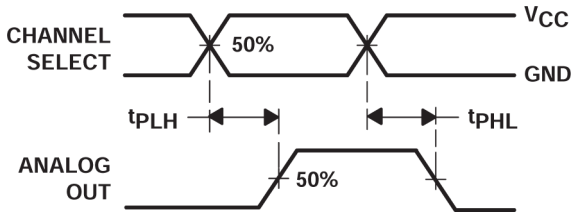


图 6-5. Propagation Delays, Channel Select to Analog Out

†

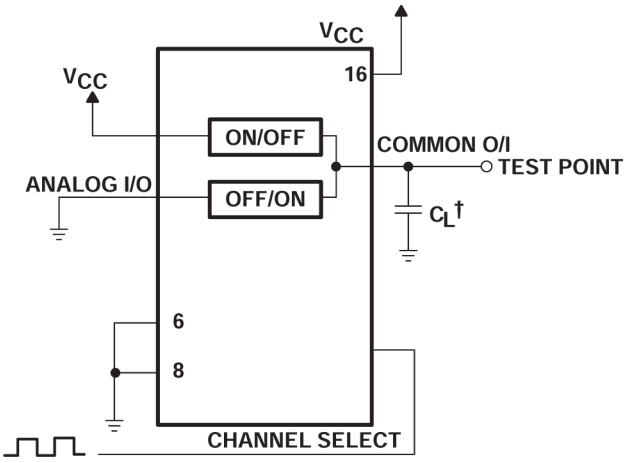


图 6-6. Propagation Delay, Channel Select to Analog Out, Test Setup

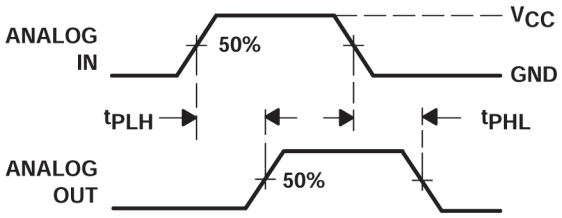


图 6-7. Propagation Delays, Analog in to Analog Out

† Includes all probe and jig capacitance

†

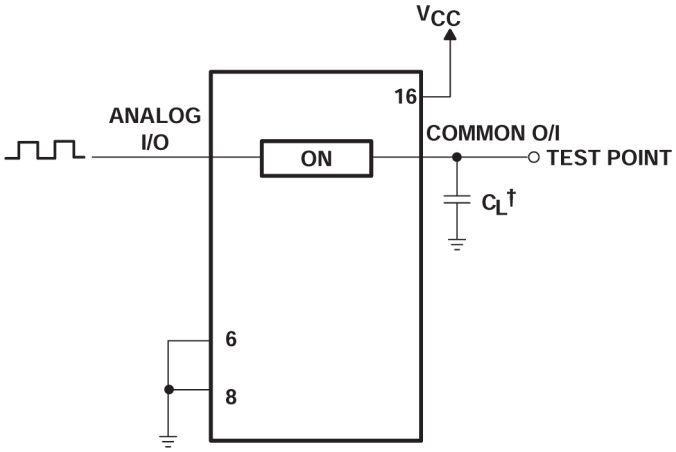


图 6-8. Propagation Delay, Analog in to Analog Out, Test Setup

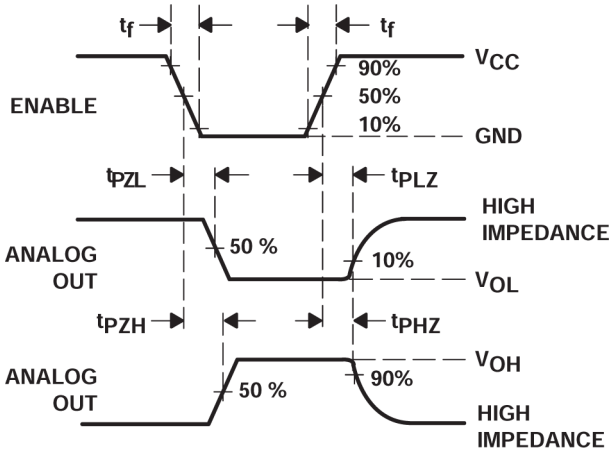


图 6-9. Propagation Delays, Enable to Analog Out

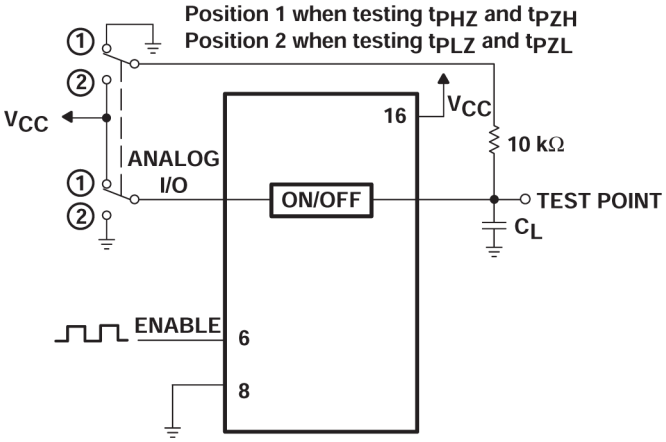


图 6-10. Propagation Delay, Enable to Analog Out, Test Setup

† Includes all probe and jig capacitance

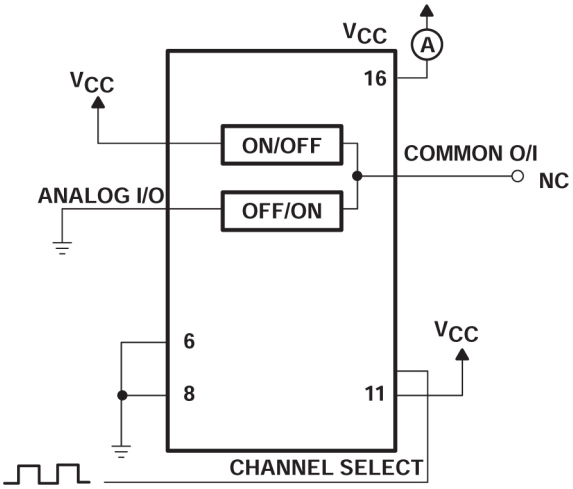
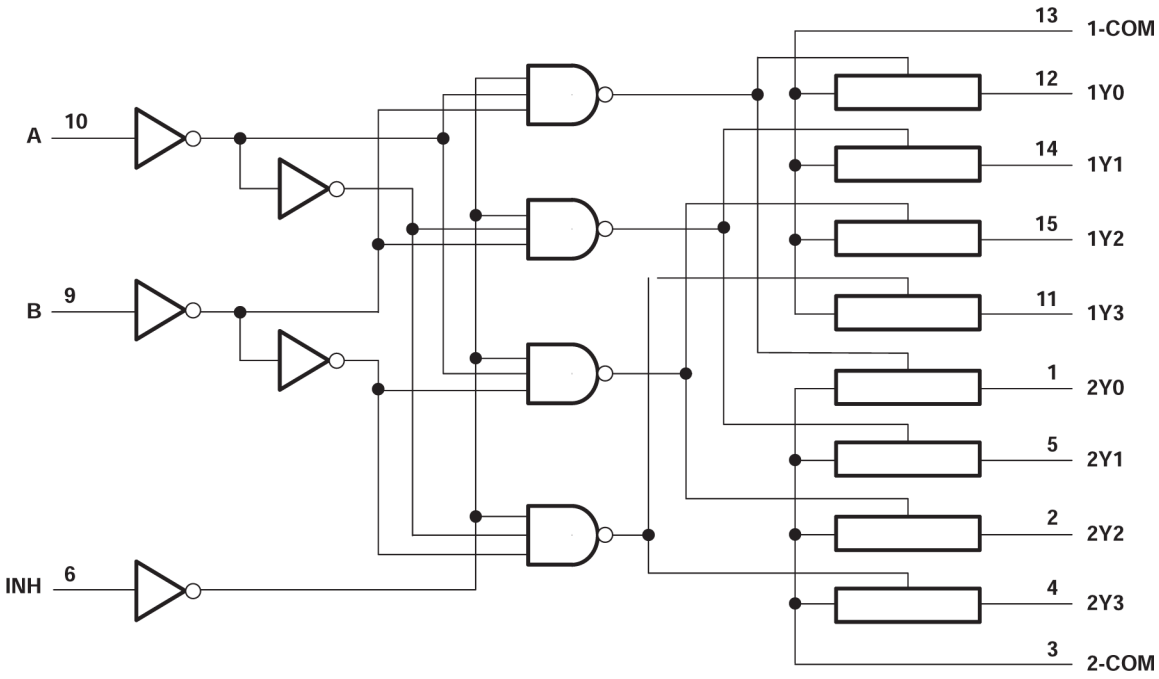


图 6-11. Power-Dissipation Capacitance, Test Setup

7 Detailed Description

7.1 Functional Block Diagram



8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

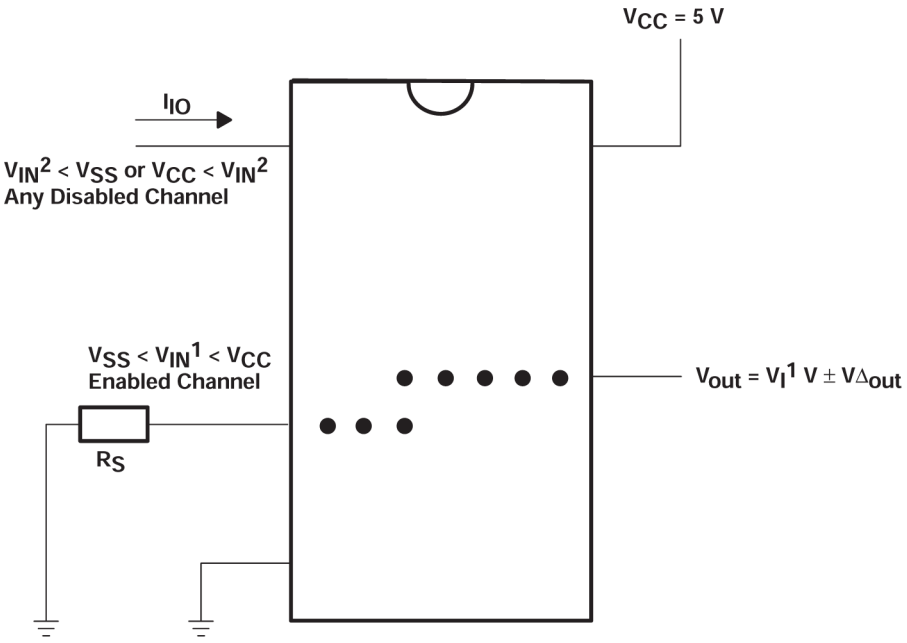


图 8-1. Injection-Current Coupling Specification

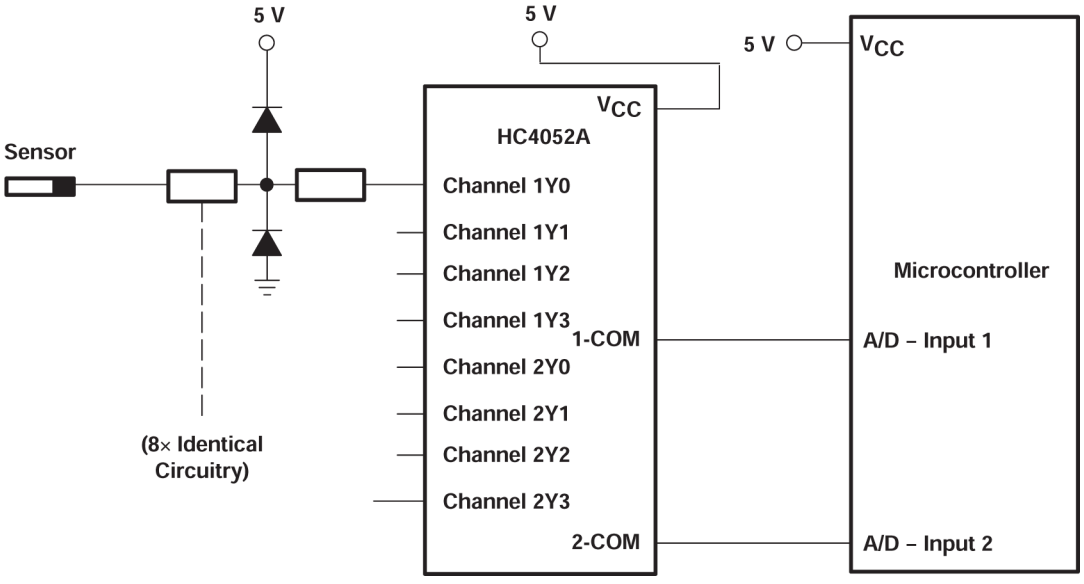


图 8-2. Actual Technology Requires 32 Passive Components and One Extra 6-v Regulator to Suppress Injection Current into a Standard HC4052 Multiplexer

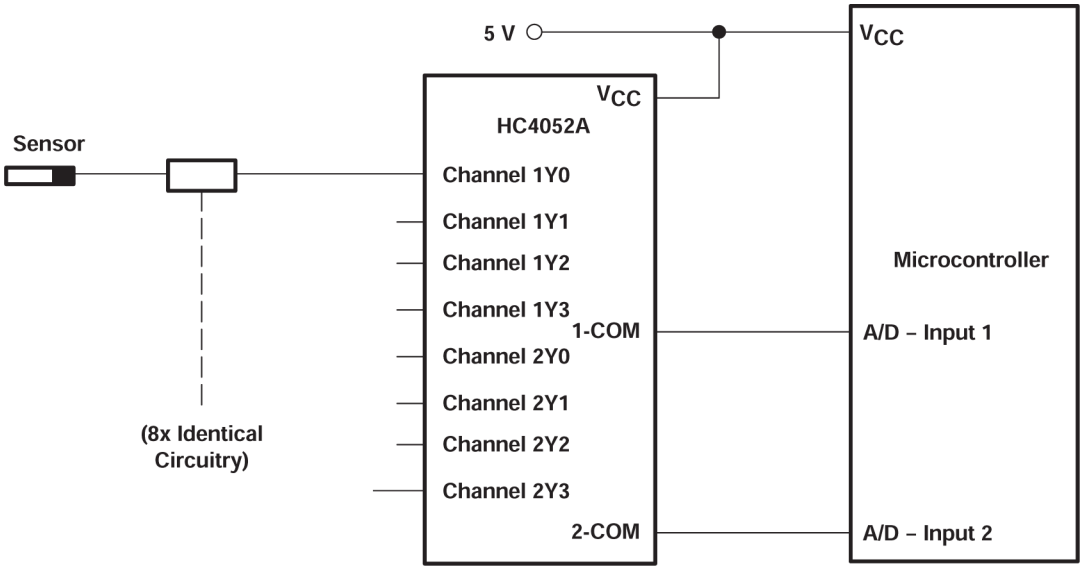


图 8-3. Solution by Applying the HC4852 Multiplexer

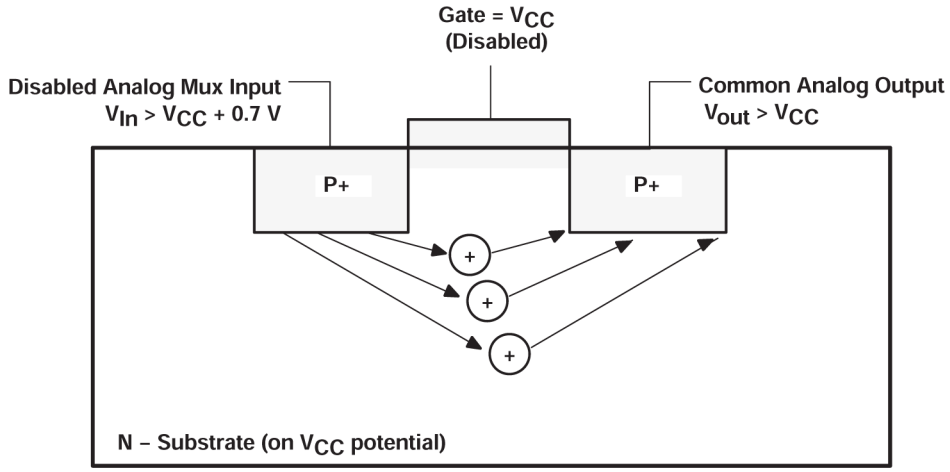


图 8-4. Diagram of Bipolar Coupling Mechanism (Appears If V_{In} Exceeds V_{CC}, Driving Injection Current into the Substrate)

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (March 2004) to Revision A (June 2024)	Page
• 通篇更新了表格、图和交叉参考的编号格式	1
• Changed VCC ABS Max from 7V to 6V	3
• Changed R θ JA	3
• Recommended supply changed from 6V to 5.5V and all test conditions using 6V were removed	4
• Changed tpd, ttran, tON, tOFF parameters	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4852D	NRND	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DGVR	NRND	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DR	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852DRG4	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	
SN74HC4852N	NRND	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC4852N	
SN74HC4852PW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	
SN74HC4852PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4852	Samples
SN74HC4852PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4852	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74HC4852 :

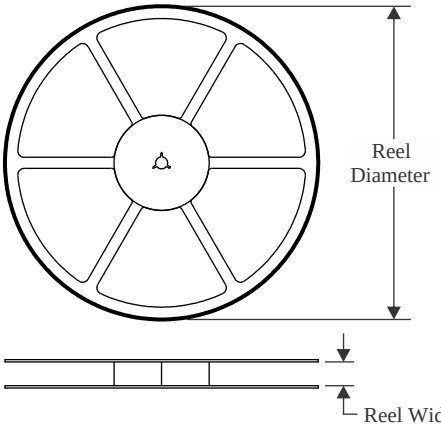
- Automotive : SN74HC4852-Q1

NOTE: Qualified Version Definitions:

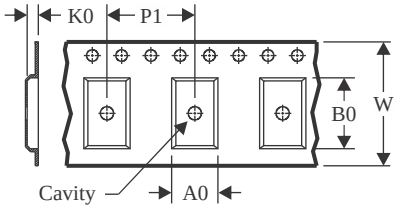
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

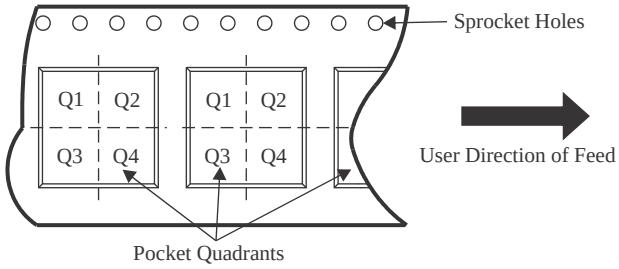


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

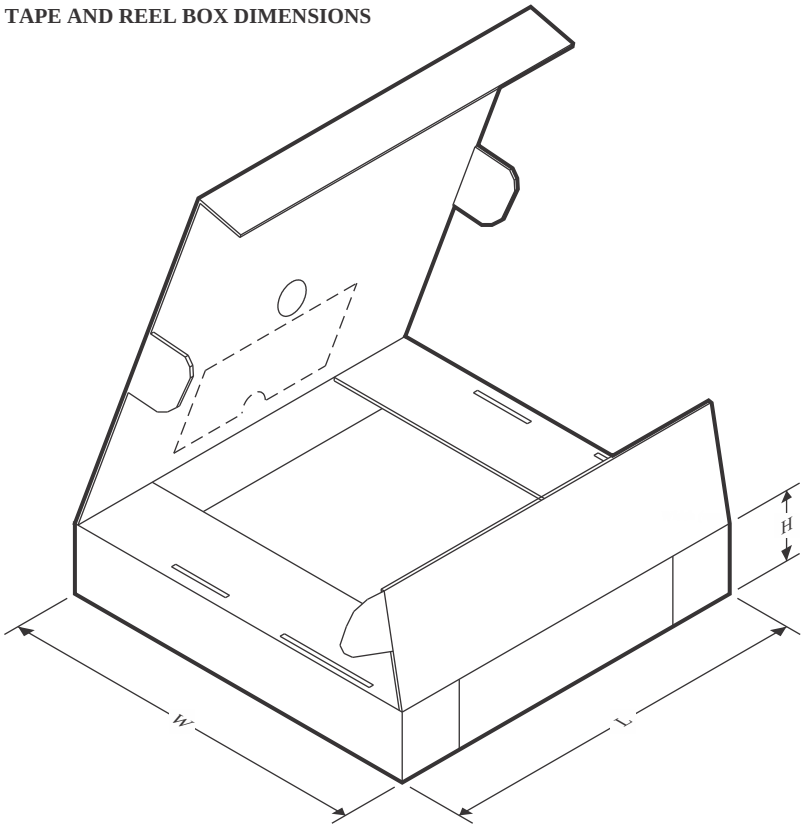
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4852DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74HC4852DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4852PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4852PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

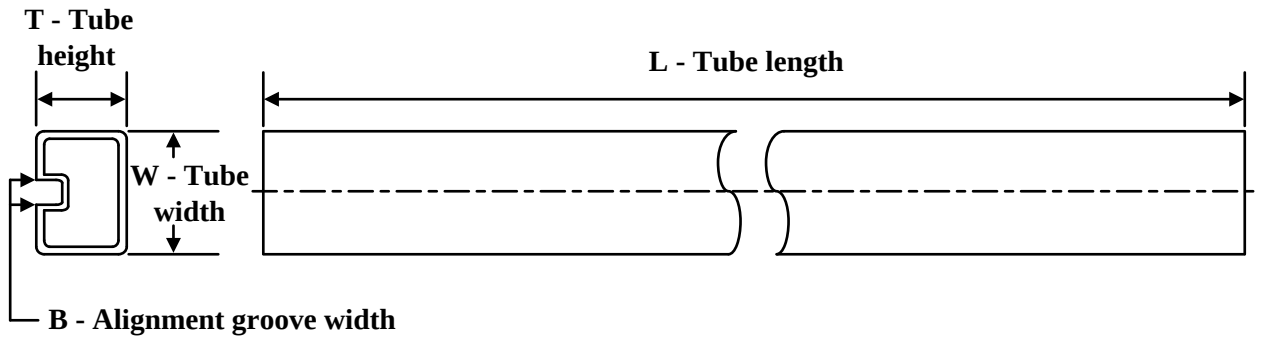
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4852DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74HC4852DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC4852PWR	TSSOP	PW	16	2000	210.0	185.0	35.0
SN74HC4852PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

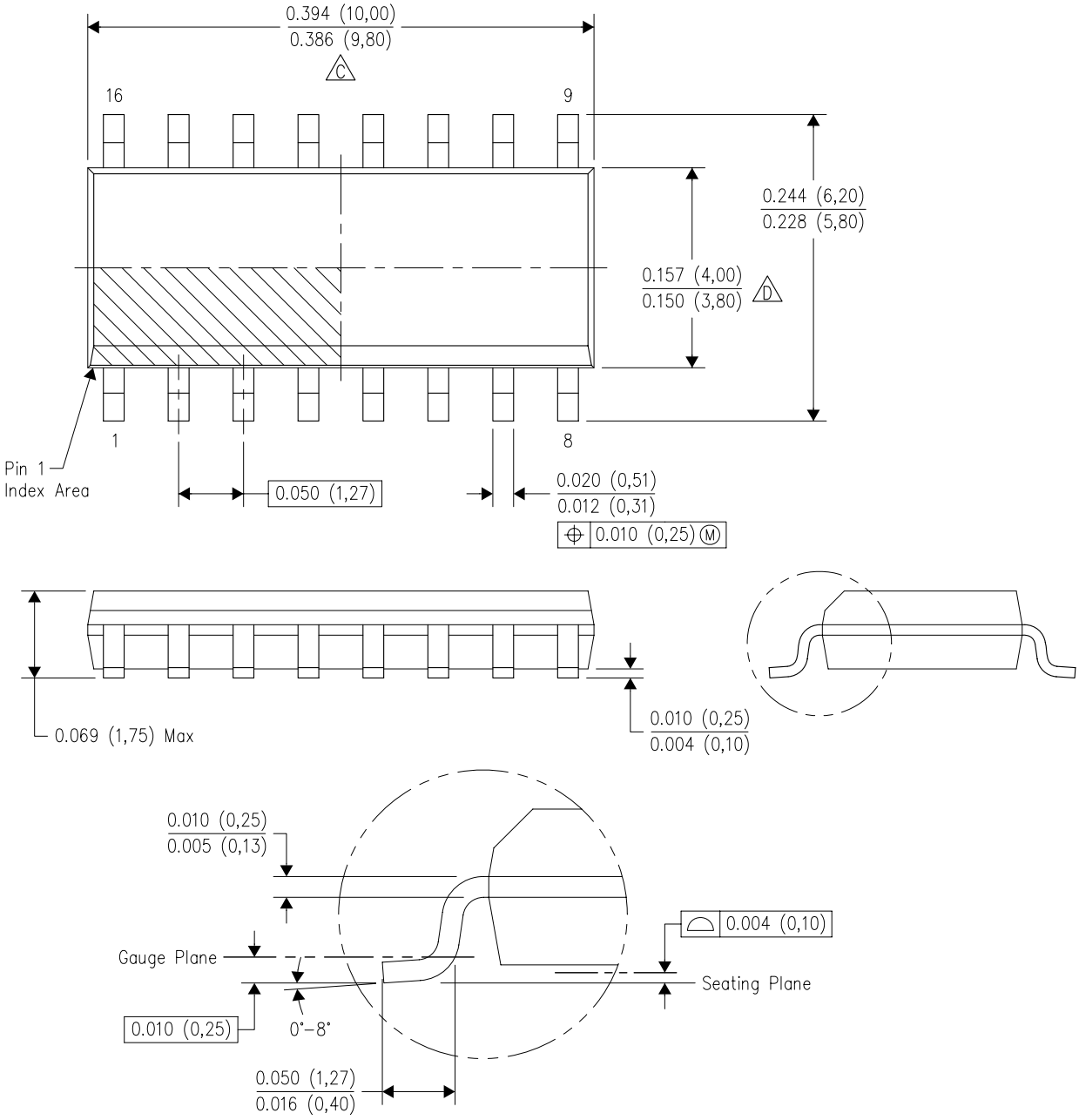
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC4852D	D	SOIC	16	40	507	8	3940	4.32
SN74HC4852N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4852PW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



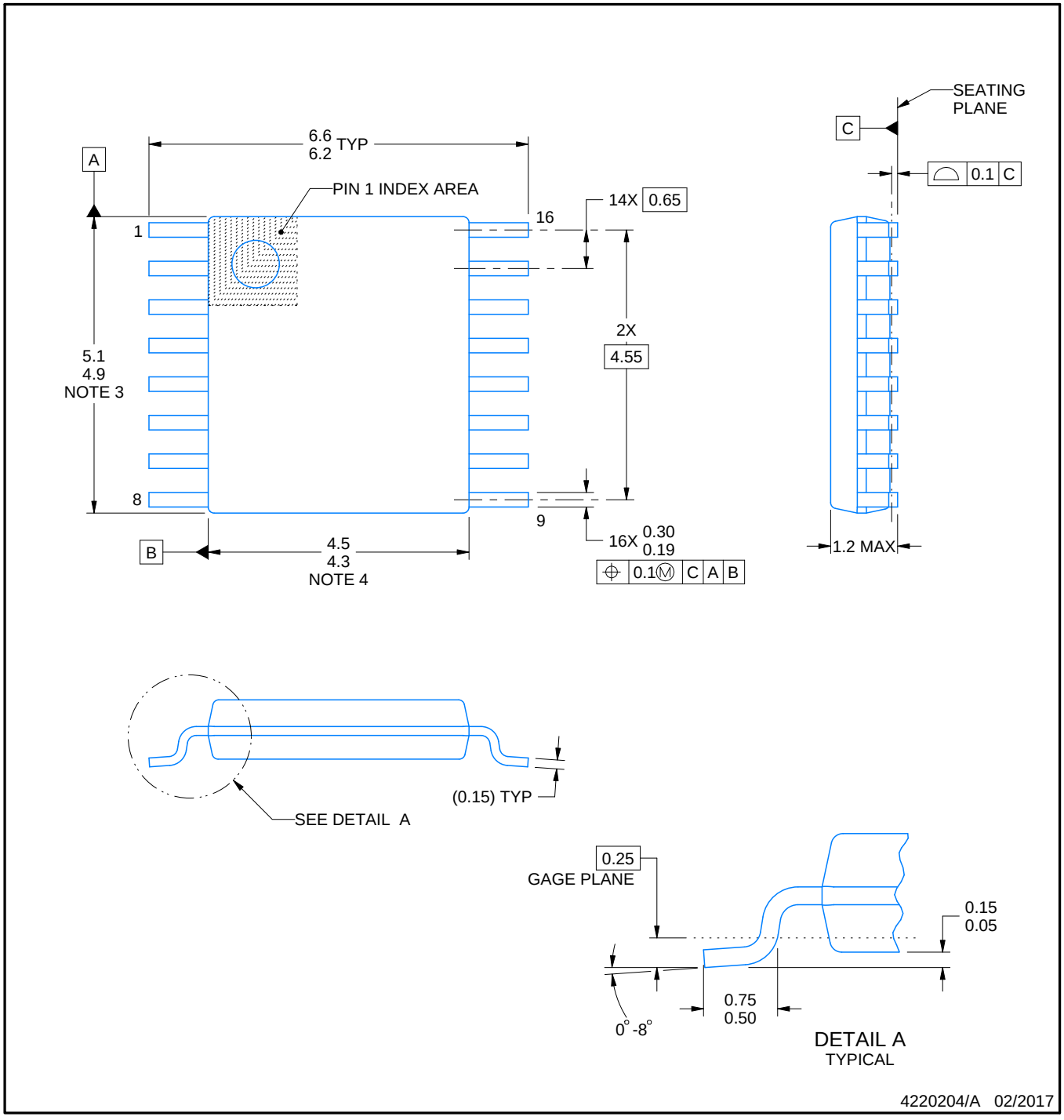
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

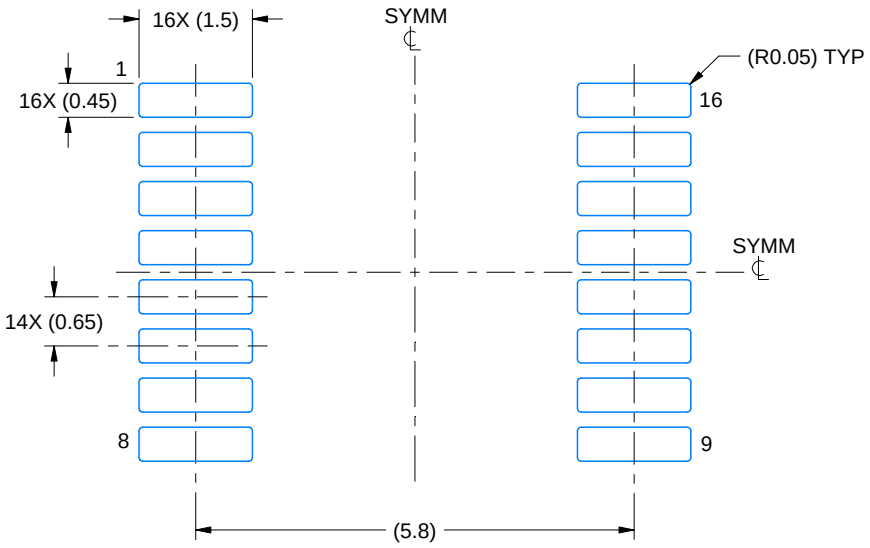
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

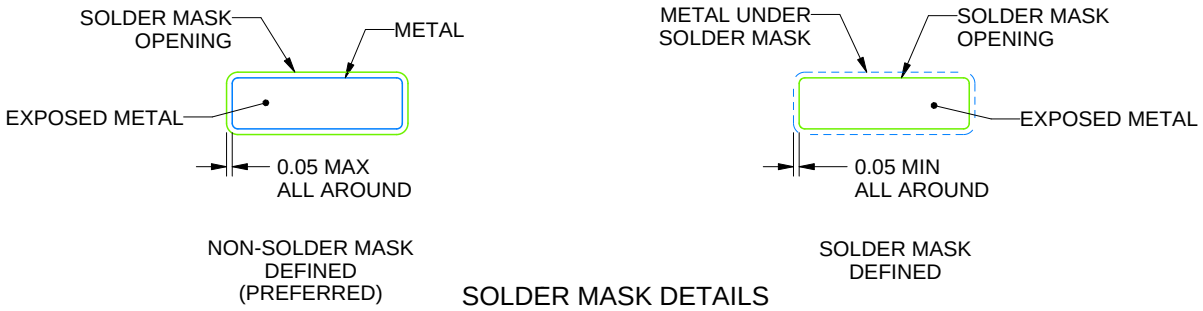


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

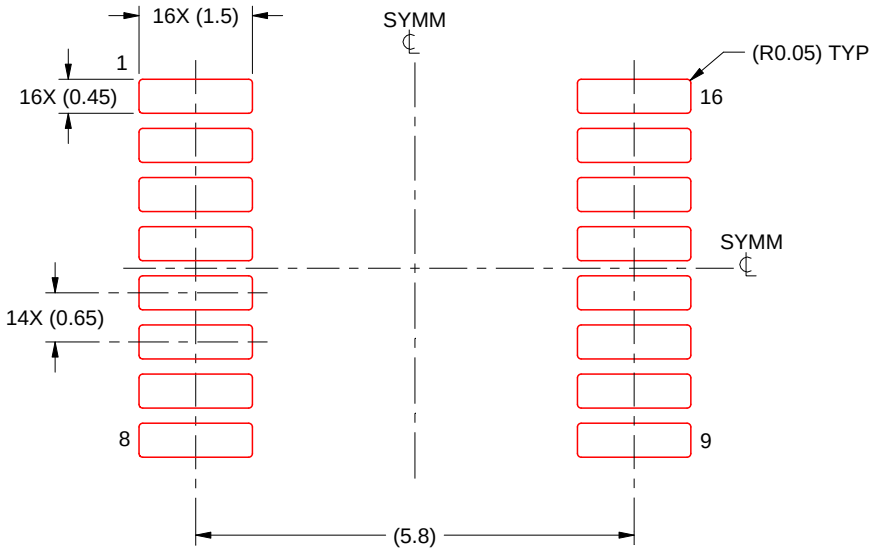


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

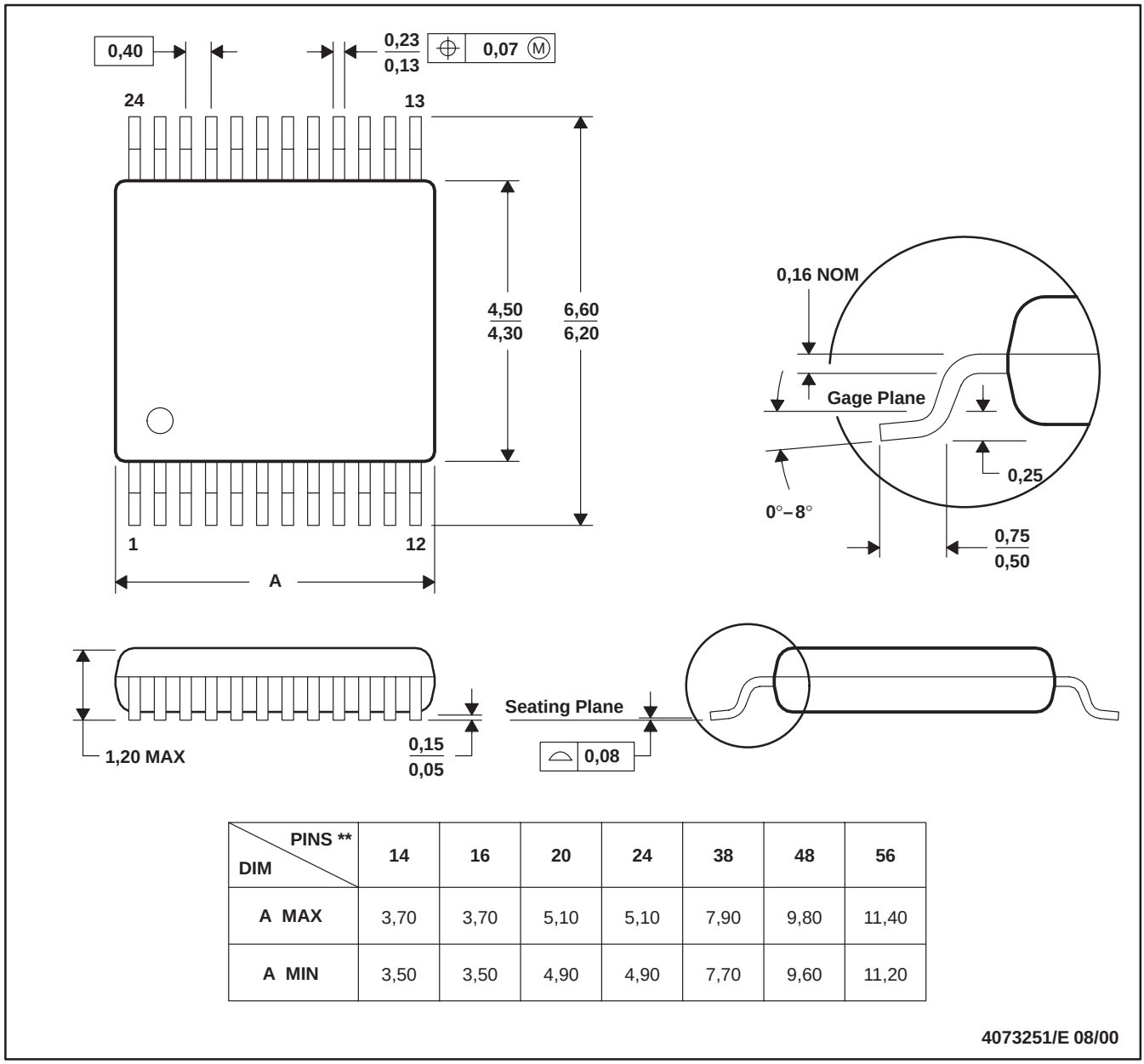
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

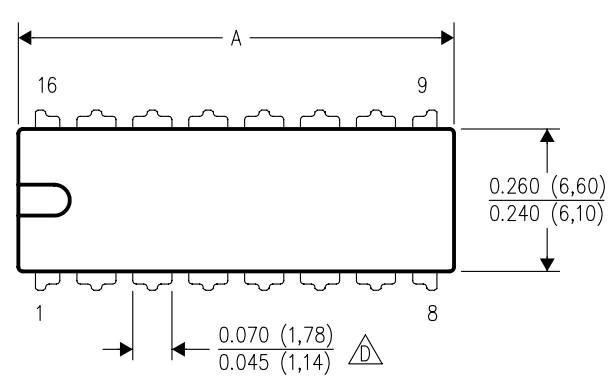
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

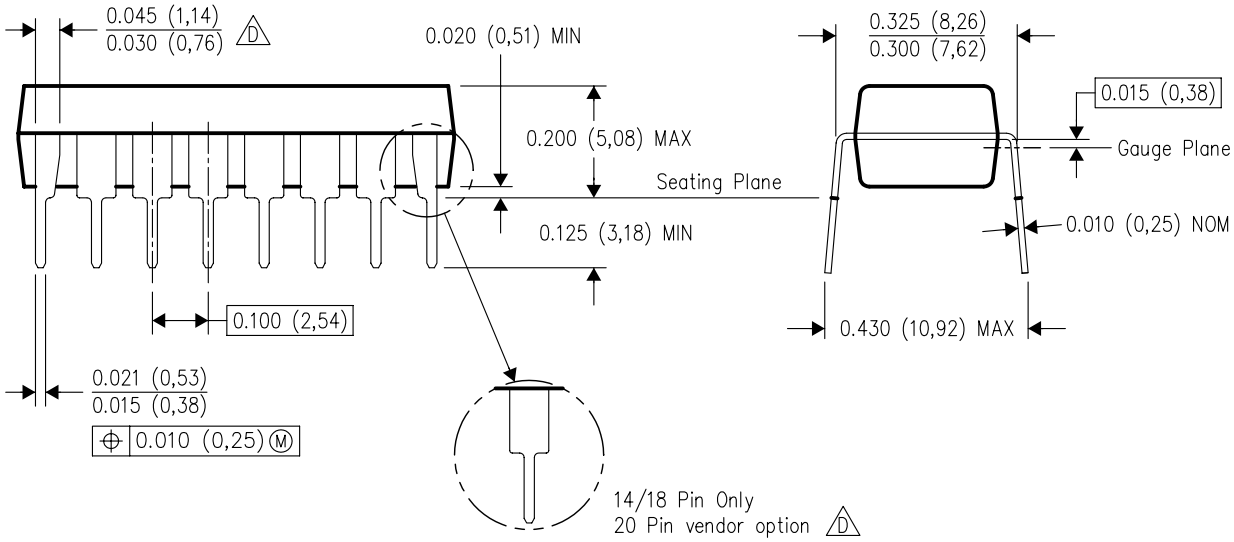
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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