具有清零和预设功能且通过汽车认证的 SN74HCS72-Q1 施密特触发输入双路 D 型负缘触发触发器

1 特性

- 符合面向汽车 应用的 AEC-Q100 标准：
  - 器件温度等级 1：–40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 宽工作电压范围：2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
  - I_{CC} 典型值为 100nA
  - 输入泄漏电流典型值为 ±100nA
- 电压为 5V 时，输出驱动为 ±7.8mA

2 应用

- 将瞬时开关转换为拨动开关
- 输入慢速边沿速率信号
- 可在高噪声环境中运行
- 启用具有唤醒模式的 CAN 控制器电源

3 说明

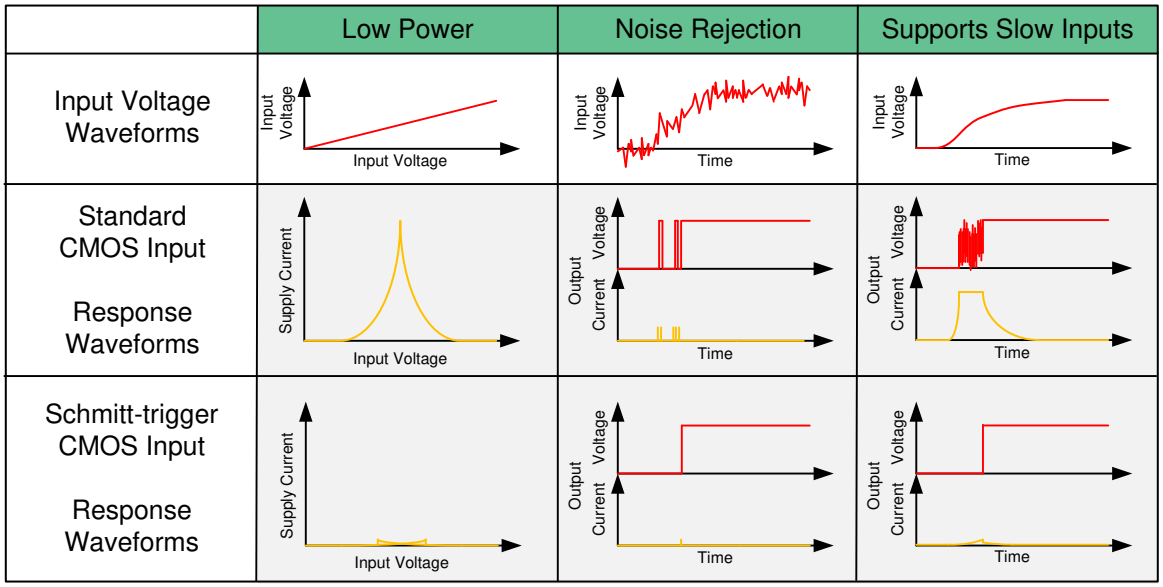
该器件包含两个独立的 D 型负缘触发触发器。所有输入均包括施密特触发，可实现慢速或高噪声输入信号。将预设 ($\overline{PRE}$) 输入设为低电平，会输出高电平。将清零 ($\overline{CLR}$) 输入设为低电平，会重新输出低电平。预设和清零功能是异步的，并且不依赖于其他输入的电平。当 $\overline{PRE}$ 和 $\overline{CLR}$ 处于非活动状态（高电平）时，数据 (D) 输入处满足设置时间要求的数据将传输到时钟 ($\overline{CLK}$) 脉冲负向缘上的输出（Q，$\overline{Q}$）处。经过保持时间间隔后，可以更改数据 (D) 输入处的数据而不影响输出（Q，$\overline{Q}$）处的电平。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74HCS72QDRQ1	SOIC (14)	8.70mm x 3.90mm
SN74HCS72QPWRQ1	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

施密特触发输入的优势



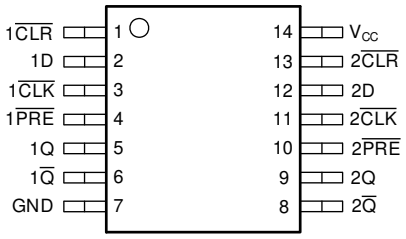
目录

4 修订历史记录

日期	修订版本	说明
2019 年 10 月	*	初始发行版。

5 Pin Configuration and Functions

D and PW Package
14-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1$\overline{CLR}$	1	Input	Clear for channel 1, active low
1D	2	Input	Data for channel 1
1$\overline{CLK}$	3	Input	Clock for channel 1, falling edge triggered
1$\overline{PRE}$	4	Input	Preset for channel 1, active low
1Q	5	Output	Output for channel 1
1$\overline{Q}$	6	Output	Inverted output for channel 1
GND	7	—	Ground
2$\overline{Q}$	8	Output	Inverted output for channel 2
2Q	9	Output	Output for channel 2
2$\overline{PRE}$	10	Input	Preset for channel 2, active low
2$\overline{CLK}$	11	Input	Clock for channel 2, falling edge triggered
2D	12	Input	Data for channel 2
2$\overline{CLR}$	13	Input	Clear for channel 2, active low
V_{CC}	14	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS72-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.1	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis (V_{T+} - V_{T-})(1)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.3		
			I_{OH} = -7.8 mA	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.30	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

(1) Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
f_{max}	Max switching frequency			2 V	20	31		MHz
				4.5 V	64	95		
				6 V	74	105		
t_{pd}	Propagation delay	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
		$\overline{CLK}$	Q or $\overline{Q}$	2 V		19	42	ns
				4.5 V		8	19	
				6 V		7	15	
t_t	Transition-time(1)		Q or $\overline{Q}$	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1) t_t = t_r or t_f, whichever is larger

6.7 Timing Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See Parameter Measurement Information.

PARAMETER			V_{CC}	MIN	TYP	MAX	UNIT
f_{clock}	Clock frequency		2 V			20	MHz
			4.5 V			64	
			6 V			74	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	8	7		ns
			4.5 V	7	5		
			6 V	7	5		
		$\overline{CLK}$ high or low	2 V	10	5		ns
			4.5 V	9	3		
			6 V	8	2		
t_{su}	Setup time before $\overline{CLK}$ low	Data	2 V	16	11		ns
			4.5 V	6	1		
			6 V	3	1		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	7			ns
			4.5 V	0			
			6 V	0			
t_h	Hold time	Data after CLK ↓	2 V	5			ns
			4.5 V	3			
			6 V	2			

6.8 Typical Characteristics

T_A = 25°C

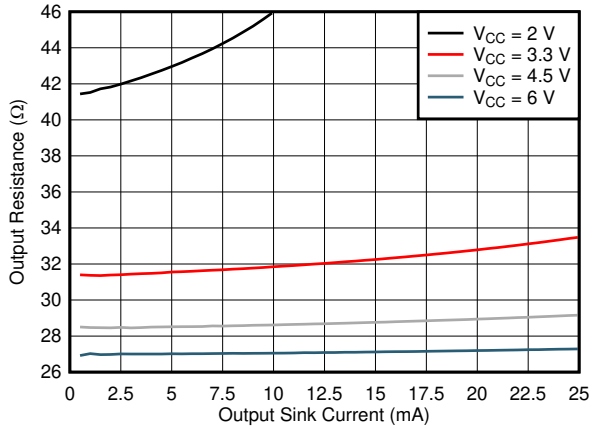


图 1. Output driver resistance in LOW state.

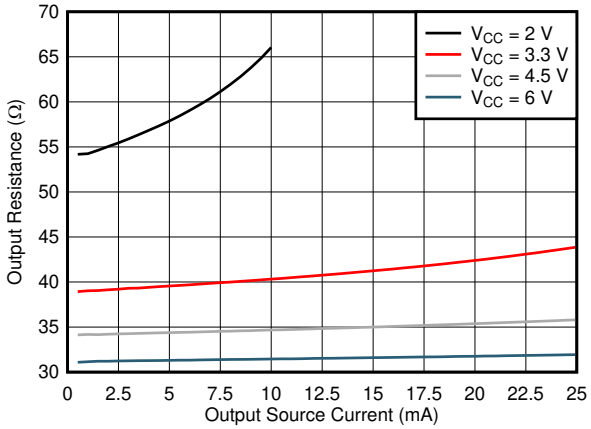


图 2. Output driver resistance in HIGH state.

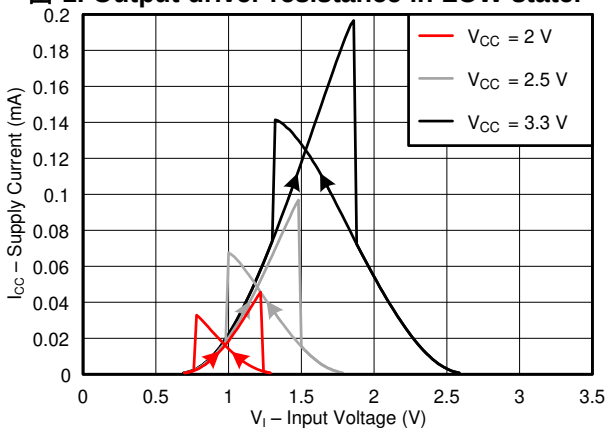


图 3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

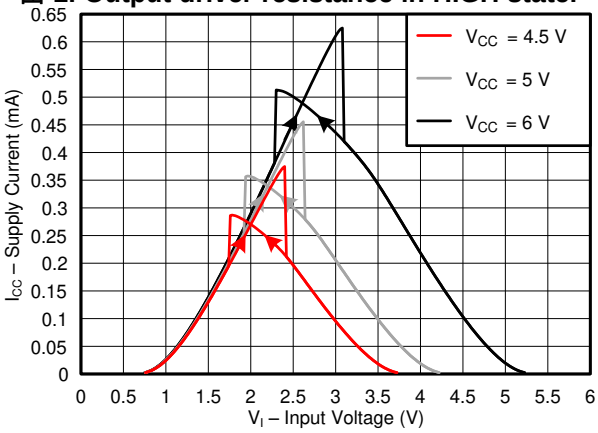


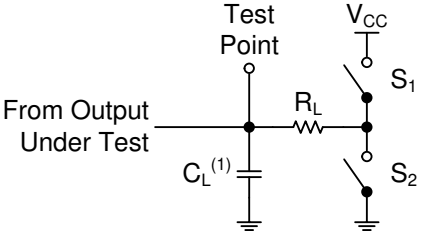
图 4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



C_L includes probe and test-fixture capacitance.

图 5. Load Circuit

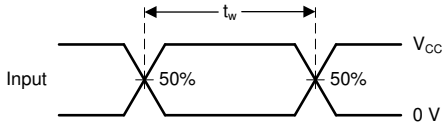


图 6. Voltage Waveforms, Pulse Duration

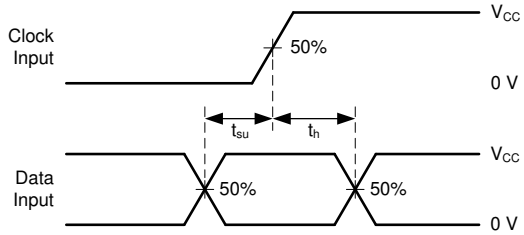
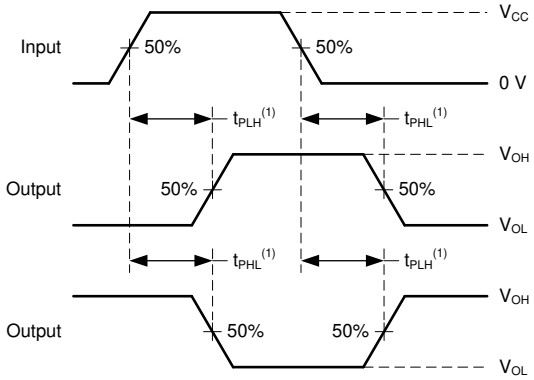


图 7. Voltage Waveforms, Setup and Hold Times



Voltage Waveforms, Propagation Delay specifications t_{PLH} and t_{PHL} are the same as t_{pd}.

图 8. Voltage Waveforms Propagation Delays

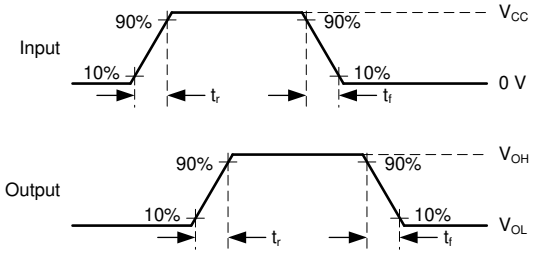


图 9. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

图 10 describes the SN74HCS72-Q1. As the SN74HCS72-Q1 is a dual D-Type negative-edge-triggered flip-flop with clear and preset, the diagram below describes one of the two device flip-flops.

8.2 Functional Block Diagram

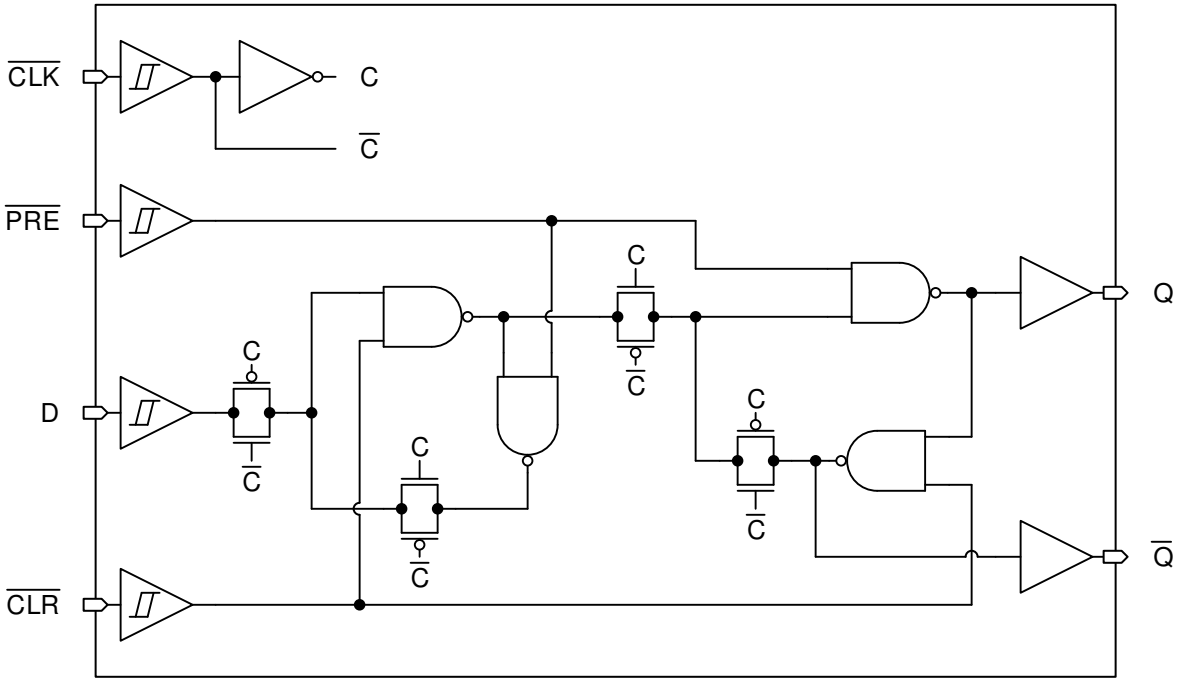


图 10. Logic Diagram (Positive Logic) for one channel of SN74HCS72-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Feature Description (接下页)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 图 11.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

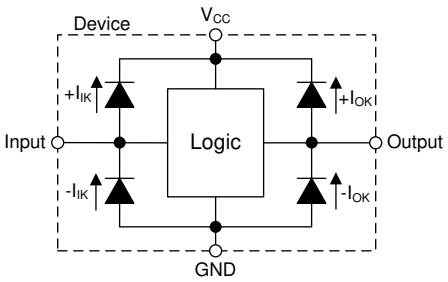


图 11. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 1 lists the functional modes of the SN74HCS72-Q1.

表 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	$\overline{CLK}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS72-Q1 is an ideal device for taking a CAN wake-up request and converting it to a power supply enable due to its low power consumption and noise rejecting inputs, which eliminate false triggers. CAN communication can occur when the vehicle ignition is off. Therefore, many circuits are designed to work in a standby or low power mode. Because a CAN wake-up request causes the RX pin to pulse LOW, the SN74HCS72-Q1 will trigger off the falling edge enabling the power for the CAN controller. Then the CAN controller powers on for the incoming communication. When communications are finished, the controller sends a reset pulse to the SN74HCS72-Q1 and CAN transceiver putting the circuit back into a standby mode.

9.2 Typical Application

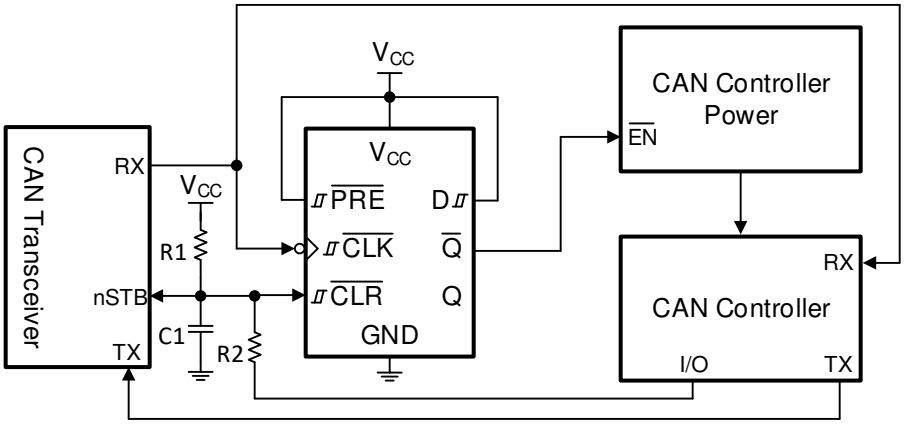


图 12. Power Enable Using CAN Wake-up Request

9.2.1 Design Requirements

The SN74HCS72-Q1 device allows flexibility by having complementary outputs for active-high or active-low enables. The supply should be selected such that the device is always powered along with the CAN transceiver. The same supply for both devices is recommended.

With the SN74HCS72-Q1, a power on reset circuit only requires a resistor (R) and capacitor (C) to create a delay. The R and C values create a delay that is approximately 2.2×RC. In this application, it is desired to have the output ($\overline{Q}$) in the HIGH state at startup, so R1 and C1 are connected directly to the $\overline{CLR}$ pin, as shown in 图 12. A second resistor is needed to limit the current into the CAN controller when it sets the circuit back into standby mode. It is required for the R1 resistor to be at least ten times larger than R2 to avoid a divider circuit ($R2 \leq 10R1$).

The D input can be tied either to V_{CC} or ground depending on the desired implementation. In this example, it is tied to V_{CC} to obtain a HIGH signal from $\overline{Q}$ when a wake-up request occurs.

Typical Application (接下页)

9.2.1.1 Output Considerations

In general, the load needs to be considered in the design to determine if the device will have the capability to drive it. For this application, we assume that the flip-flop output is transmitting over a relatively short trace (under 10 cm) to a CMOS input.

Primary load factors to consider:

- Load Capacitance: approximately 15 pF
  - See the *Switching Characteristics* section for the capacitive loads tested with this device.
  - Increasing capacitance will proportionally increase output transition times.
  - Decreasing capacitance will proportionally decrease output transition times, and can produce ringing due to very fast transition rates. A 25-Ω resistor can be added in series with the output if ringing needs to be dampened.
- Load Current: expected maximum of 10 µA
  - Leakage current into connected devices.
  - Parasitic current from other components.
  - Resistive load current.
- Output Voltage: see *Electrical Characteristics* for output voltage ratings at a given current.
  - Output HIGH (V_{OH}) and output LOW (V_{OL}) voltage levels affect the input voltage, V_{IH} and V_{IL}, respectively, to subsequent devices.

9.2.1.2 Input Considerations

The SN74HCS72-Q1 has Schmitt-trigger inputs. Schmitt-trigger inputs have no limitation on transition rate, however the input voltage must be larger than $V_{T+(max)}$ to be guaranteed to be read as a logic high, and below $V_{T-(min)}$ to be guaranteed to be read as a logic low, as defined in the *Electrical Characteristics*. Do not exceed the values specified in the *Absolute Maximum Ratings* or the device could be damaged.

9.2.1.3 Timing Considerations

The SN74HCS72-Q1 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *Timing Characteristics* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *Timing Characteristics*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *Timing Characteristics*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *Timing Characteristics*.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Input signals to Schmitt-trigger inputs, like those found on the HCS family of devices, can support unlimited edge rates.
   - Input thresholds are listed in the *Electrical Characteristics*.
   - Inputs include positive clamp diodes. Input voltages can exceed the device's supply so long as the clamp current ratings are observed from the *Absolute Maximum Ratings*. Do not exceed the absolute maximum voltage rating of the device or it could be damaged.
2. Recommended Output Conditions:
   - Load currents should not exceed the value listed in the *Absolute Maximum Ratings*.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the

Typical Application (接下页)

output current.

9.2.3 Application Curve

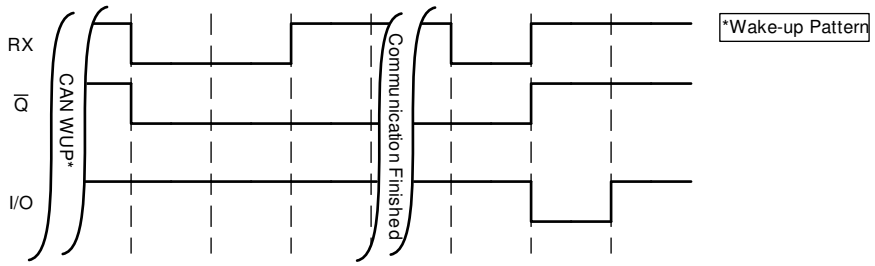


图 13. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-µF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

11 Layout

11.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in 图 14 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

11.2 Layout Example

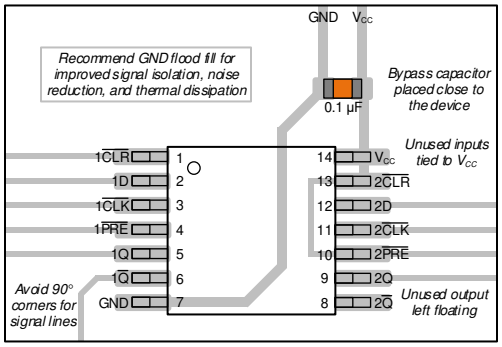


图 14. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《慢速或浮点 CMOS 输入的影响》*应用报告
- 德州仪器 (TI)，*《使用全新 HCS 逻辑系列降低噪声并节省电力》* 应用报告
- 德州仪器 (TI)，*《了解施密特触发》* 应用报告

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS72QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q1	Samples
SN74HCS72QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS72Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

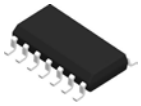
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

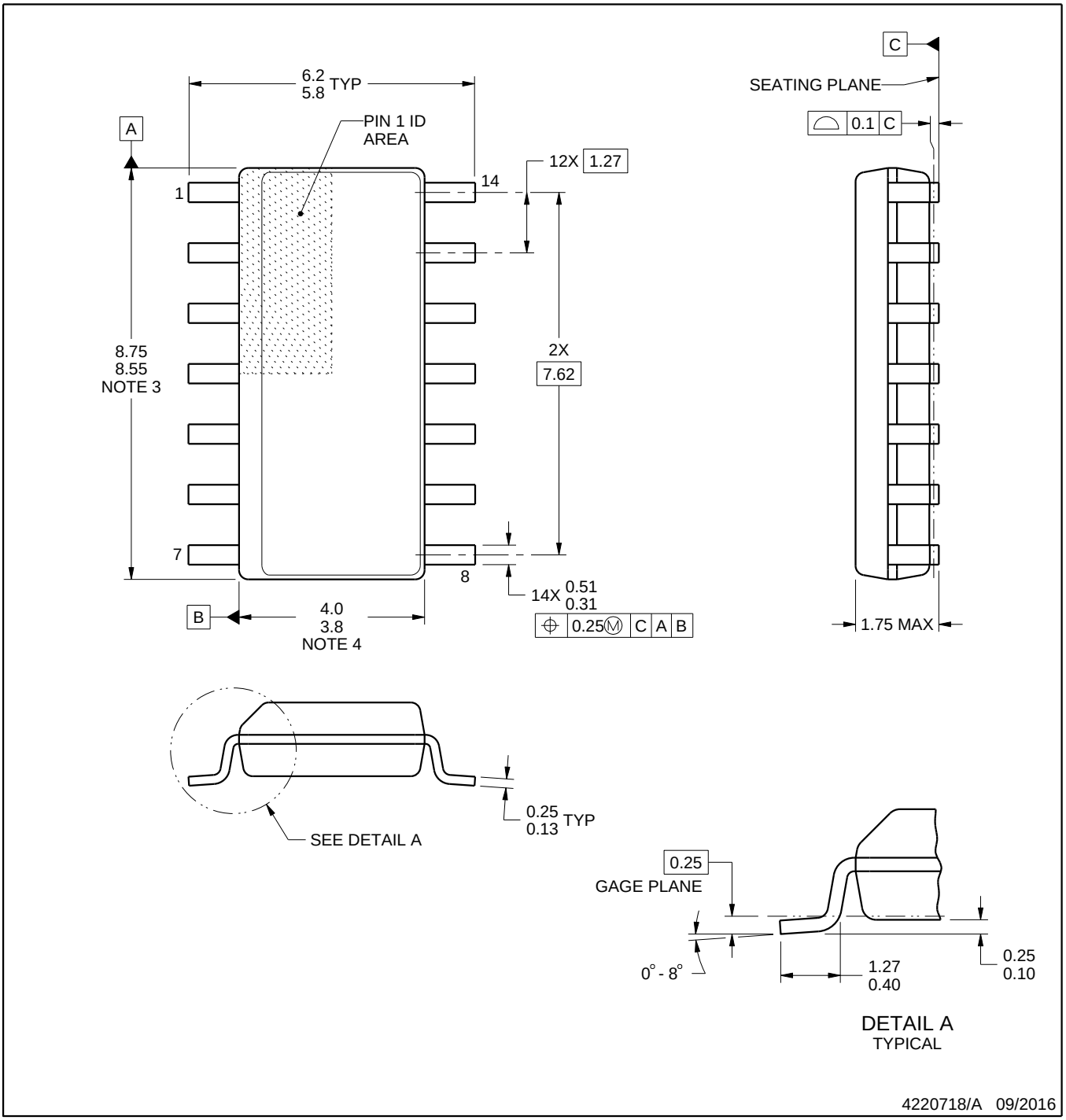


PACKAGE OUTLINE

D0014A

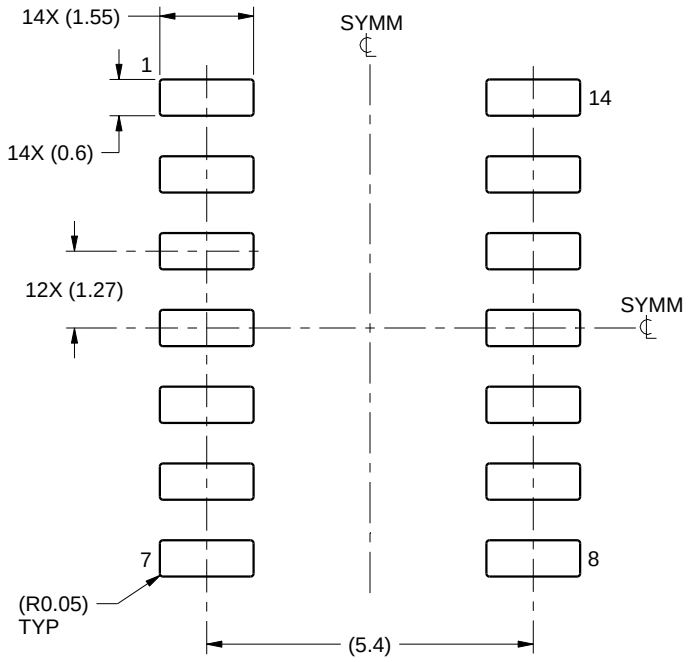
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

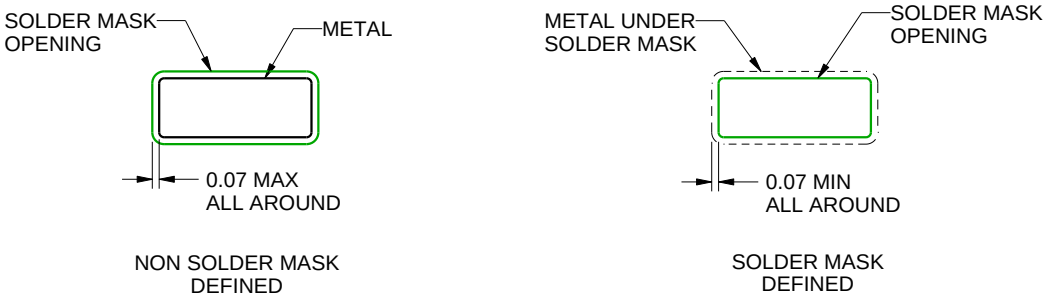


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

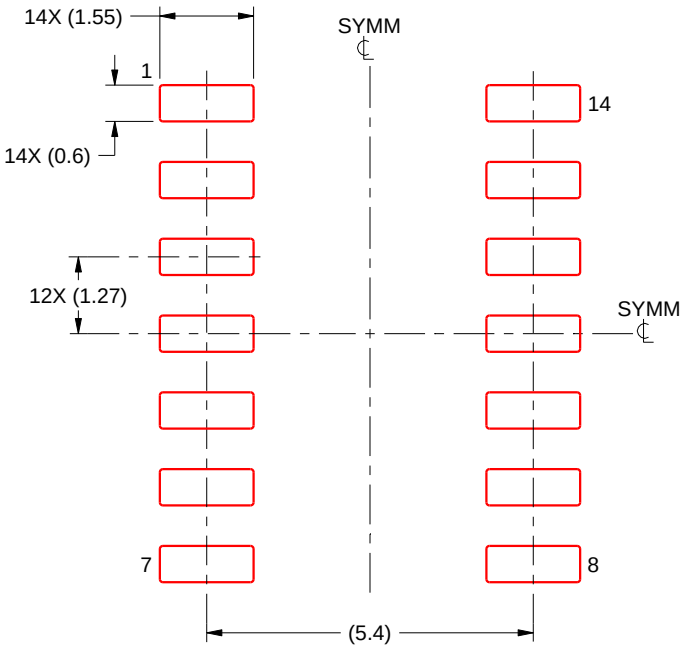
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

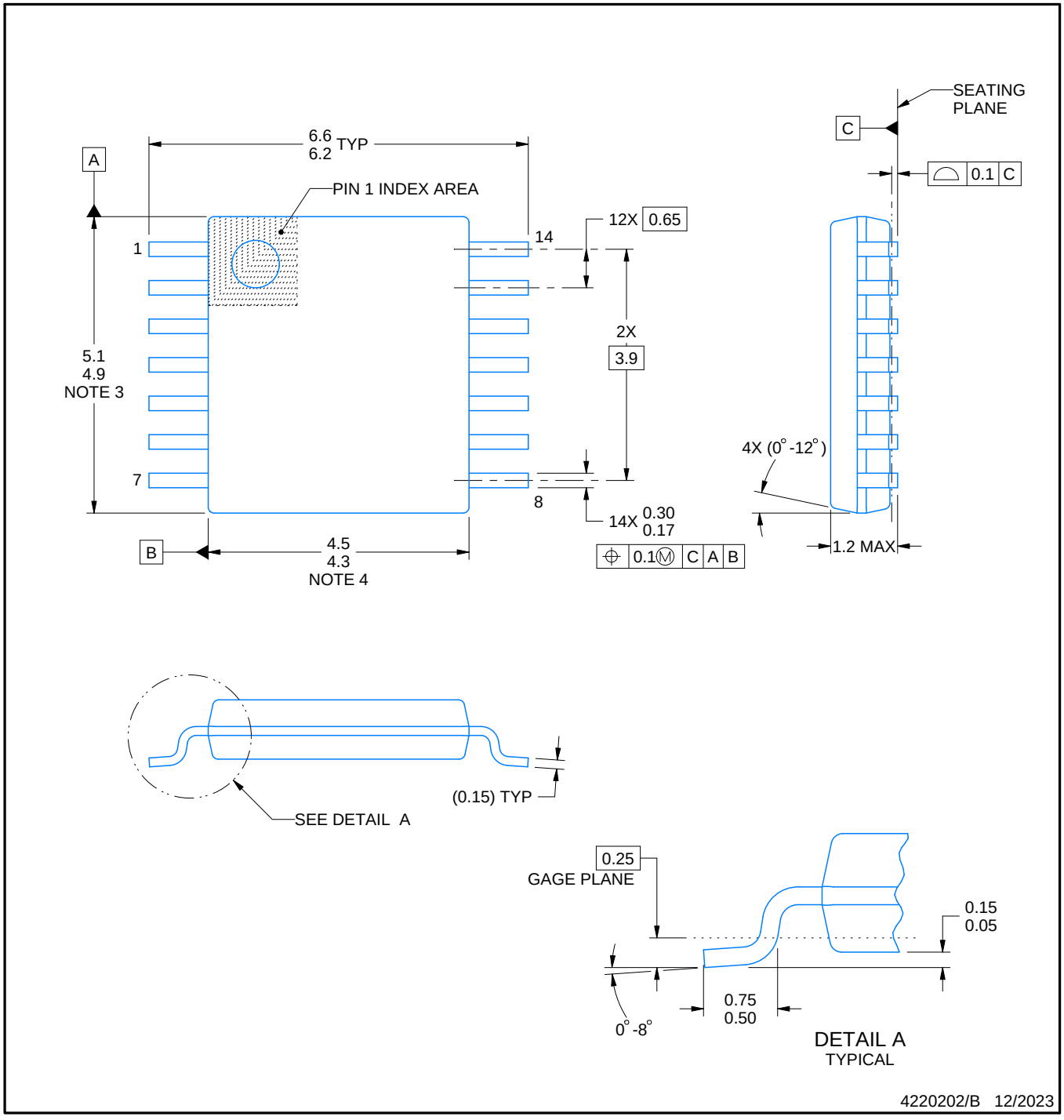
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

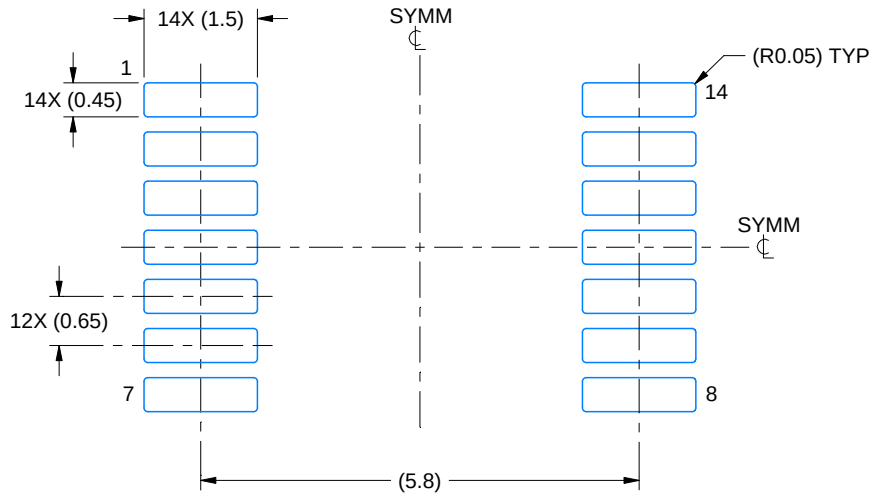
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

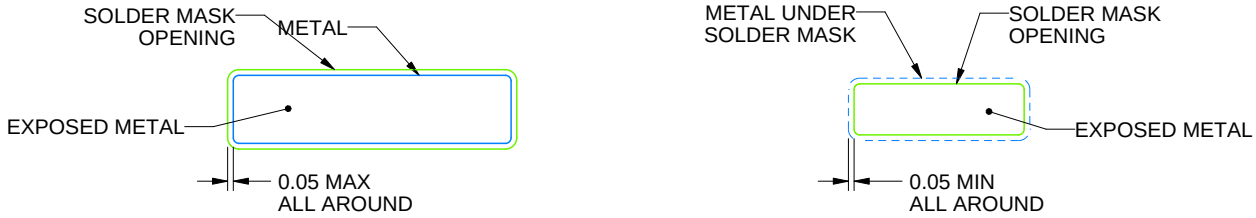


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

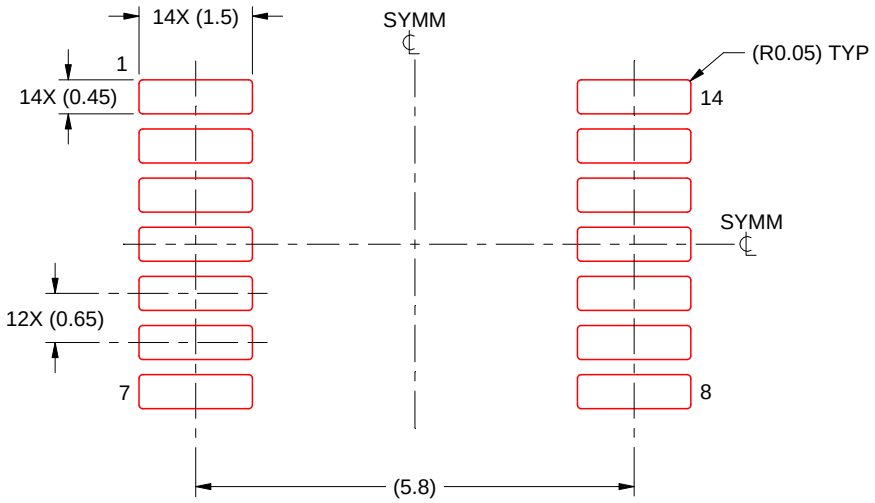


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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