SN74LVC1G80-Q1 单路正缘触发 D 型触发器

1 特性

- 符合汽车应用 认证
- 具有符合 AEC-Q100 标准的下列结果：
  - ±4000 V 人体放电模型 (HBM) ESD 分类等级 3A
  - ±1000 V 带电器件模型 (CDM) ESD 分类等级 C5
- 支持 5V V_{CC} 运行
- 输入接受的电压达到高达 5.5V
- 支持向下转换到 V_{CC}
- 3.3V 时 t_{pd} 最大值为 4.26ns
- 低功耗，10μA 最大 I_{CC}
- 电压为 3.3V 时，输出驱动为 ±24mA
- I_{off} 支持部分断电模式和后驱动保护

2 应用

- 汽车信息娱乐系统
- 汽车仪表盘
- 汽车 ADAS
- 汽车车身电子设备
- HEV/EV 动力传动系统

3 说明

SN74LVC1G80-Q1 器件是一款通过汽车 AEC-Q100 认证的单路正缘触发 D 型触发器，专为 1.65V 到 5.5V V_{CC} 操作而设计。

当数据 (D) 输入处的数据满足设置时间要求时，该数据将传输到时钟脉冲正向缘上的 $\overline{Q}$ 输出。时钟触发出现在一个特定电压电平上，并且不与时钟脉冲的上升时间直接相关。经过保持时间间隔后，可以更改 D 输入处的数据而不影响输出处的电平。

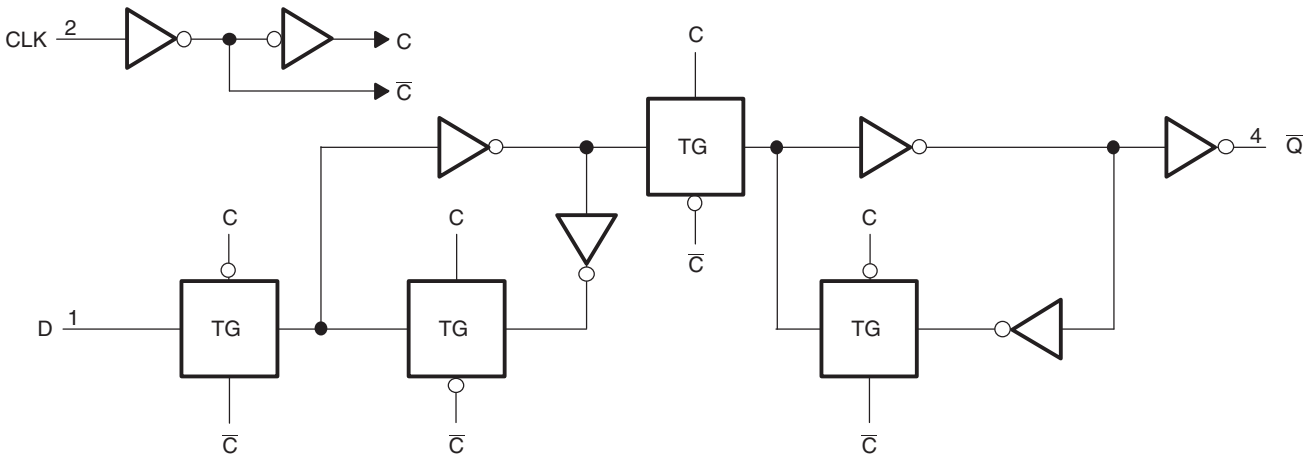
该器件完全 适用于 使用 I_{off} 的局部掉电应用。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流反流到器件中，从而防止损坏器件。

器件信息(1)

器件型号	封装	封装尺寸
SN74LVC1G80-Q1	SC70 (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

逻辑图（正逻辑）



(1) TG - 传输门

目录

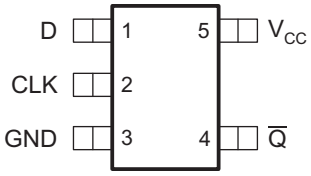
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 4 月	*	初始发行版

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



Pin Functions(1)

PIN		I/O	DESCRIPTION
NO.	NAME		
1	D	I	Data input
2	CLK	I	Positive-Edge-Triggered Clock input
3	GND	—	Ground pin
4	$\overline{Q}$	O	Inverted output
5	V_{CC}	—	Positive Supply

(1) See *机械、封装和可订购信息* for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in .

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G80-Q1 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –4 mA	1.65 V	1.2			
	I_{OH} = –8 mA	2.3 V	1.9			
	I_{OH} = –16 mA	3 V	2.4			
	I_{OH} = –24 mA		2.3			
	I_{OH} = –32 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45	
	I_{OL} = 8 mA	2.3 V			0.3	
	I_{OL} = 16 mA	3 V			0.4	
	I_{OL} = 24 mA				0.55	
	I_{OL} = 32 mA	4.5 V			0.55	
I_I CLK or D inputs	V_I = 5.5 V or GND	0 to 5.5 V			±10	µA
I_{off}	V_I or V_O = 5.5 V	0			±10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_i	V_I = V_{CC} or GND, T_A = –40°C to 85°C	3.3 V		3.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements: T_A = –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.7 Timing Requirements: T_A = –40°C to +125°C

over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8 V ± 0.15 V		160	MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8 V ± 0.15 V	2.5		ns
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5.5 V ± 0.5 V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8 V ± 0.15 V	2.3		ns
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
		Data low	V_{CC} = 1.8 V ± 0.15 V	2.5		
			V_{CC} = 2.5 V ± 0.2 V	1.5		
			V_{CC} = 3.3 V ± 0.3 V	1.3		
			V_{CC} = 5.5 V ± 0.5 V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8 V ± 0.15 V	0		ns
			V_{CC} = 2.5 V ± 0.2 V	0.2		
			V_{CC} = 3.3 V ± 0.3 V	0.9		
			V_{CC} = 5.5 V ± 0.5 V	0.4		

6.8 Switching Characteristics: T_A = –40°C to +85°C, C_L = 15 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	3	9.1	ns
			V_{CC} = 2.5 V ± 0.2 V	1.5	6	
			V_{CC} = 3.3 V ± 0.3 V	1.3	4.2	
			V_{CC} = 5 V ± 0.5 V	1.1	3.8	

6.9 Switching Characteristics: T_A = –40°C to +85°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	9.9	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	7	
			V_{CC} = 3.3 V ± 0.3 V	2	5.2	
			V_{CC} = 5 V ± 0.5 V	1.3	4.5	

6.10 Switching Characteristics: T_A = –40°C to +125°C, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, T_A = –40°C to +125°C, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8 V ± 0.15 V	160		MHz
			V_{CC} = 2.5 V ± 0.2 V			
			V_{CC} = 3.3 V ± 0.3 V			
			V_{CC} = 5 V ± 0.5 V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8 V ± 0.15 V	4.4	12.5	ns
			V_{CC} = 2.5 V ± 0.2 V	2.3	8.5	
			V_{CC} = 3.3 V ± 0.3 V	2	6	
			V_{CC} = 5 V ± 0.5 V	1.3	5.5	

6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V	24	pF
			V_{CC} = 2.5 V	24	
			V_{CC} = 3.3 V	25	
			V_{CC} = 5 V	27	

6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 6.5 V.

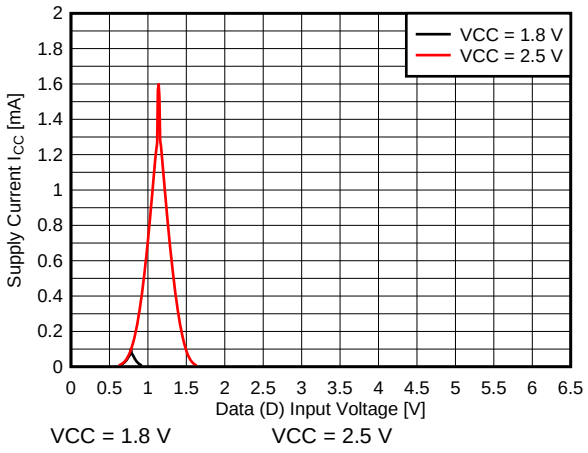


Figure 1. Supply Current (I_{CC}) vs Data (D) Input Voltage

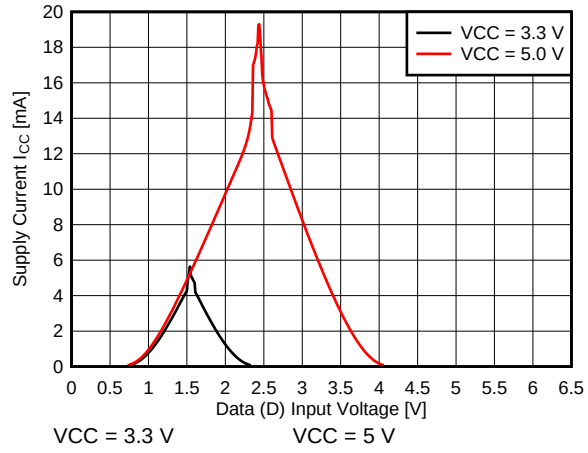
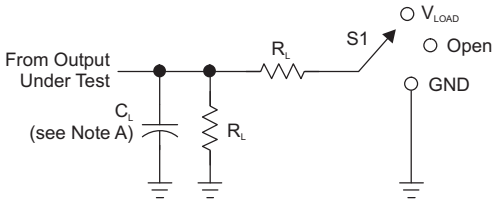


Figure 2. Supply Current (I_{CC}) vs Data (D) Input Voltage

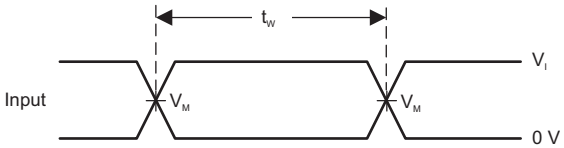
7 Parameter Measurement Information



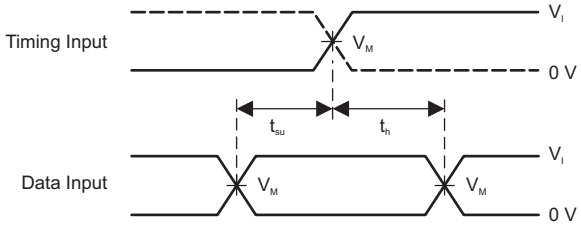
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

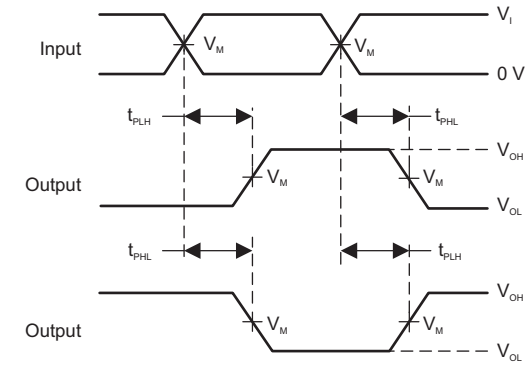
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	15 pF	1 MW	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.3 V



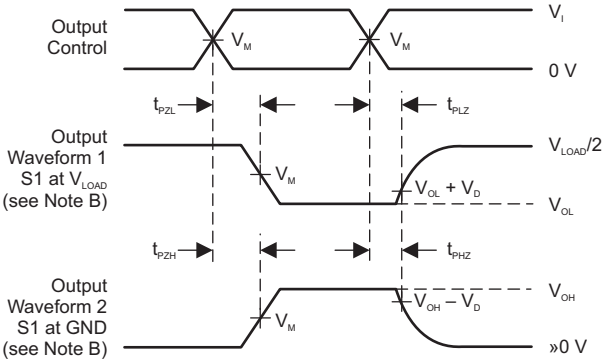
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

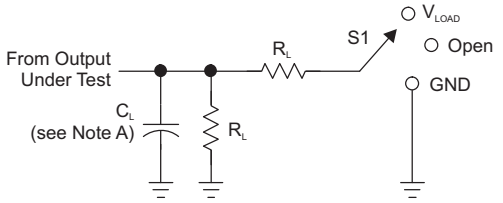


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

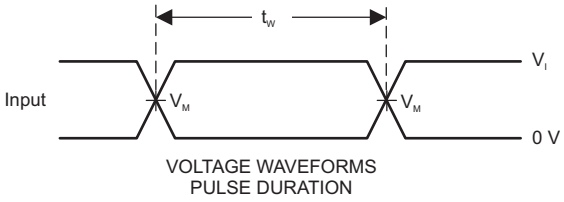
Parameter Measurement Information (continued)



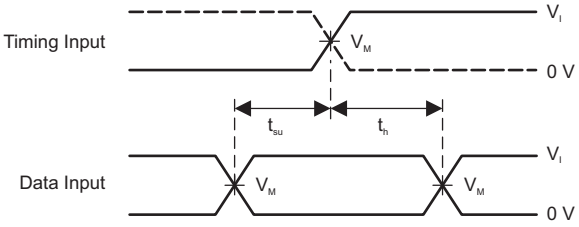
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

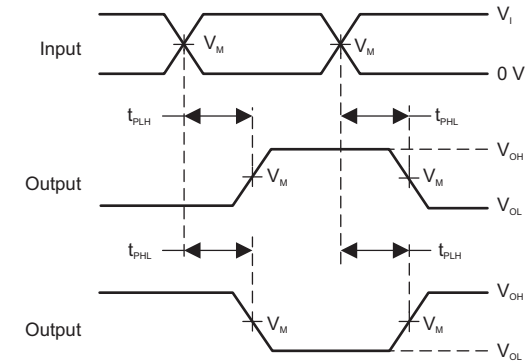
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 W	0.3 V



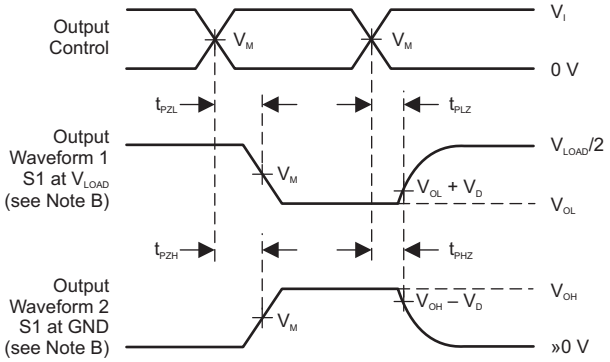
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



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F. t_{PZL} and t_{PZH} are the same as t_{en}.
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Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G80-Q1 is a single positive-edge-trigger D-type flip-flop and is AEC-Q100 qualified for automotive applications. Data at the input (D) is transferred to the output ($\overline{Q}$) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram

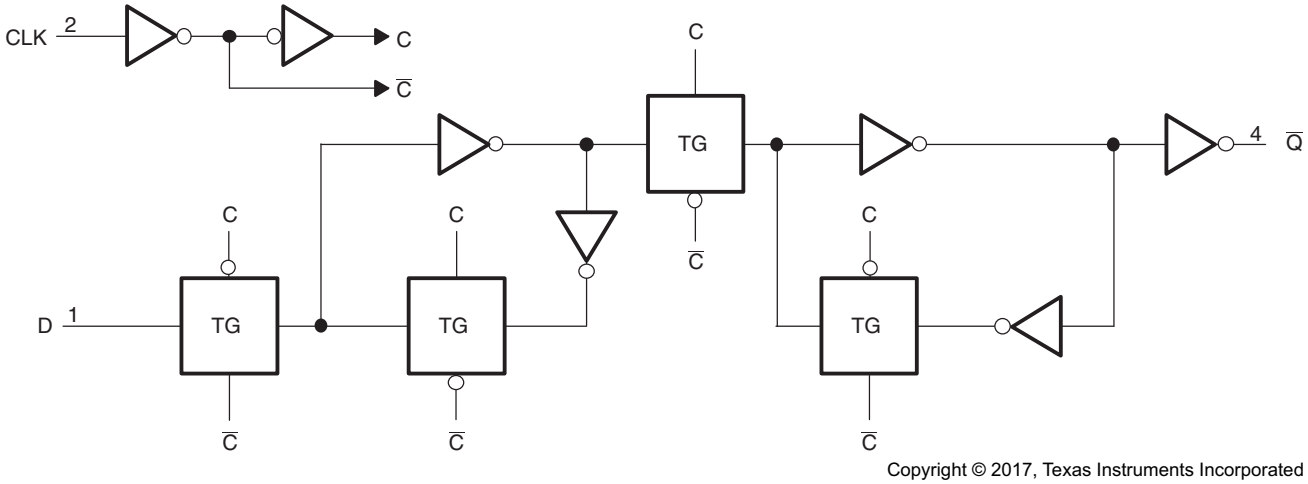

Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Recommended Operating Conditions*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

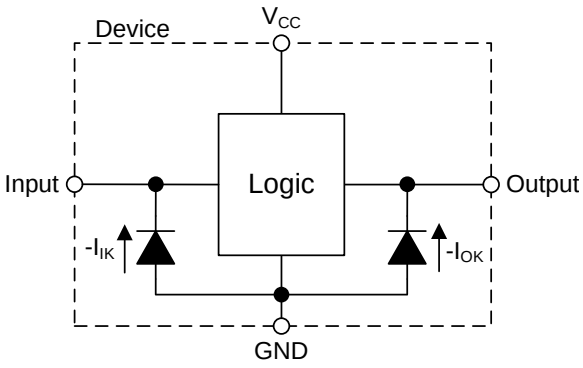

Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings* .

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G80-Q1.

Table 1. Function Table

INPUTS		OUTPUT $\overline{Q}$
CLK	D	
↑	H	L
↑	L	H
L	X	Q_0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A useful application for the SN74LVC1G80-Q1 is using it as a frequency divider. By feeding back the output ($\overline{Q}$) to the input (D), the output will toggle on every rising edge of the clock waveform. The output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80-Q1 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but should be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin could be set to an input and used to monitor the clock division.

9.2 Typical Application

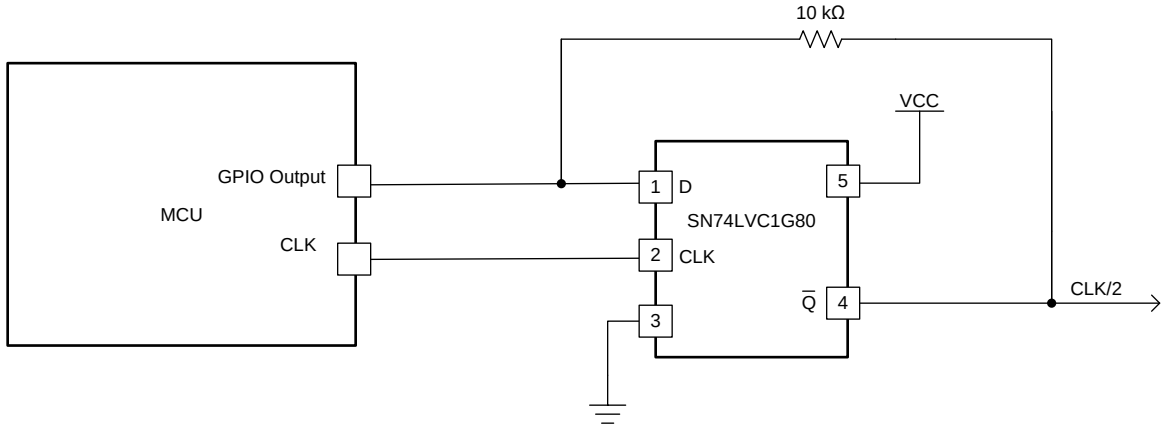

Figure 7. Clock Frequency Division

9.2.1 Design Requirements

For this application, a resistor needs to be placed on the feedback line in order for the initialization voltage from the microcontroller to overpower the signal coming from the output ($\overline{Q}$). Without it the state at the input would be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80-Q1.

The SN74LVC1G80-Q1 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Input voltages are recommended to not go below 0 V and not exceed 5.5 V for any V_{CC}. See *Recommended Operating Conditions*.
2. Recommended output conditions:
   - Load currents should not exceed ±50 mA. See *Absolute Maximum Ratings* .
   - Output voltages are recommended to not go below 0 V and not exceed the V_{CC} voltage. See *Recommended Operating Conditions*.
3. Feedback resistor:
   - A 10-kΩ resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1 MΩ, would cause too much of a voltage drop, causing the output to no longer be able to drive the input. On the other hand, a resistor too low, such as a 1 Ω, would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

9.2.3 Application Curve

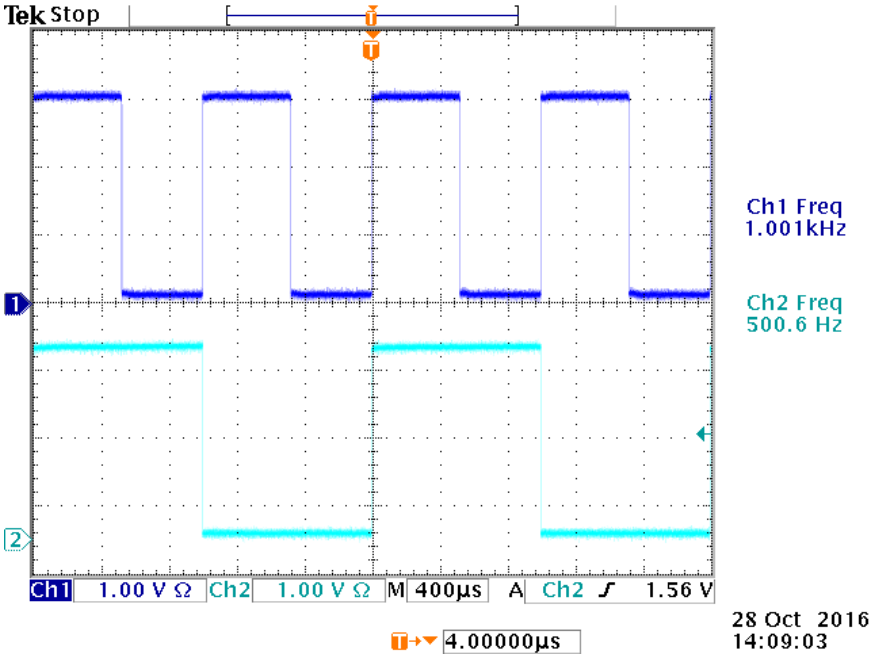

Figure 8. Frequency Division

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in *Recommended Operating Conditions*. A 0.1-µF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

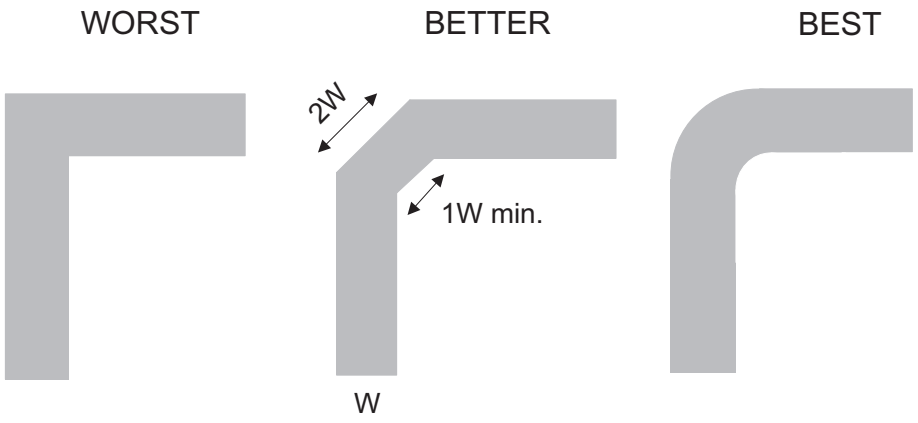

Figure 9. Trace Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《慢速或浮点 CMOS 输入的影响》，SCBA004。

12.2 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.4 商标

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G80QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	17U	Samples
SN74LVC1G80QDCKTQ1	ACTIVE	SC70	DCK	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	17U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

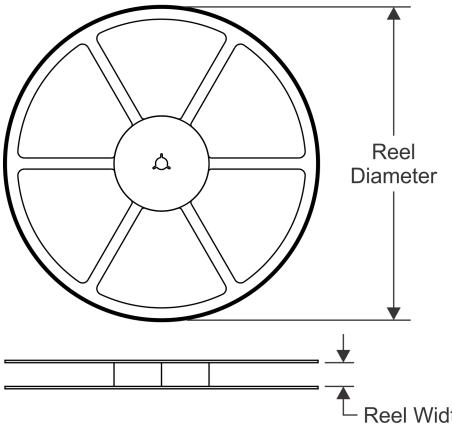
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

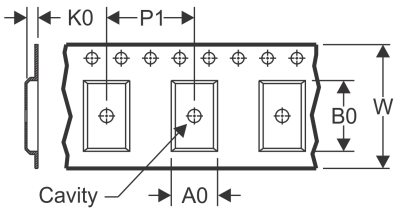
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

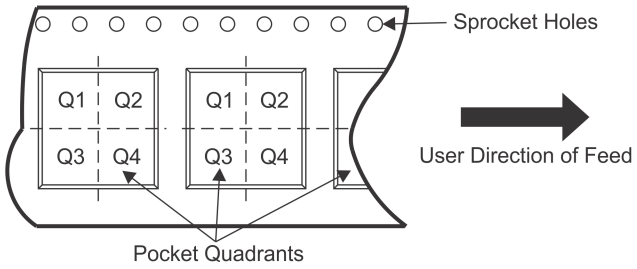


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

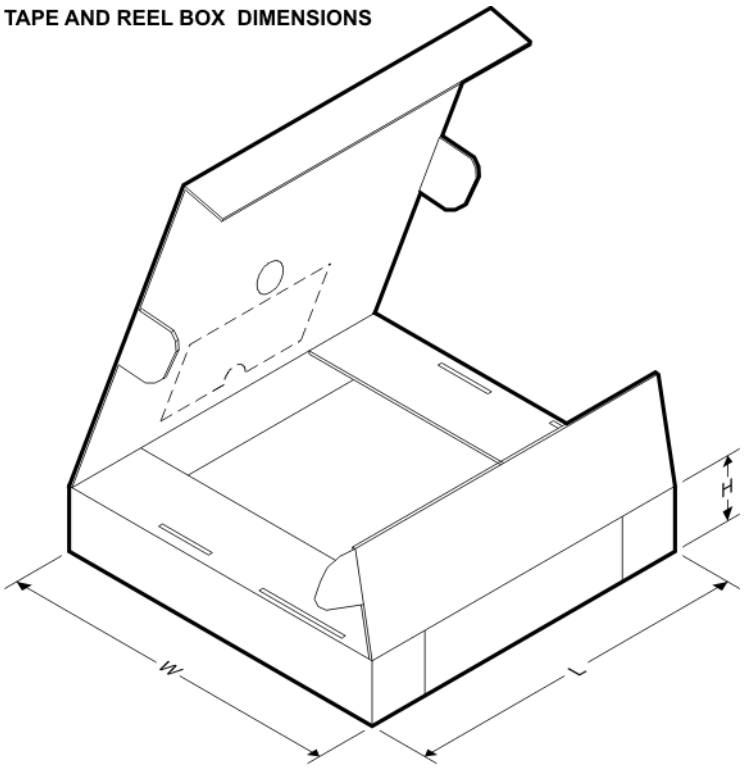
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

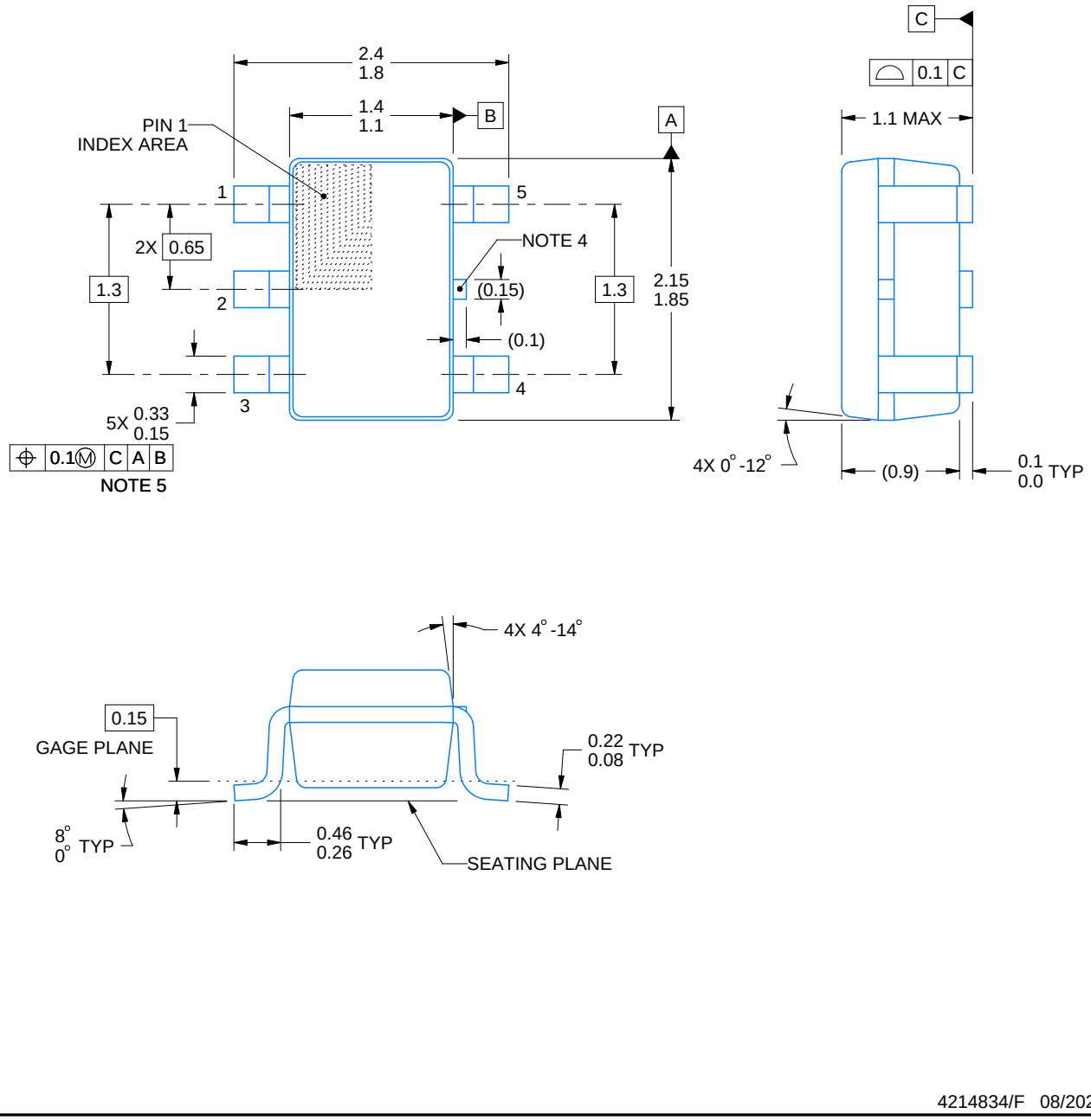
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	340.0	340.0	38.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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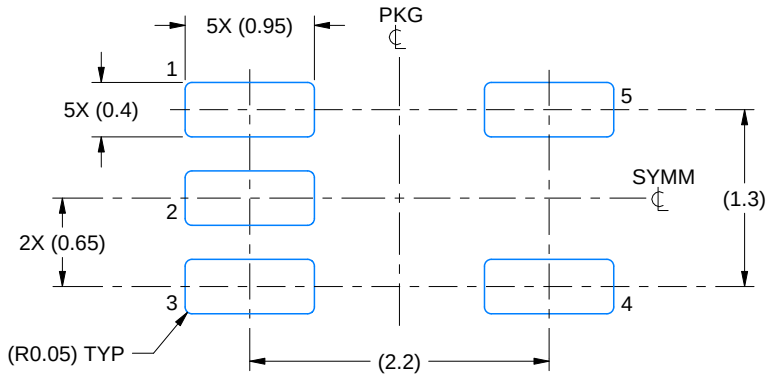
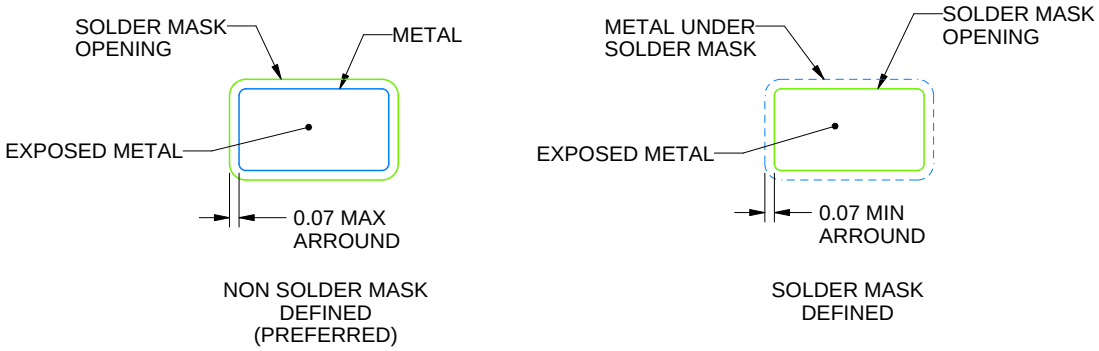
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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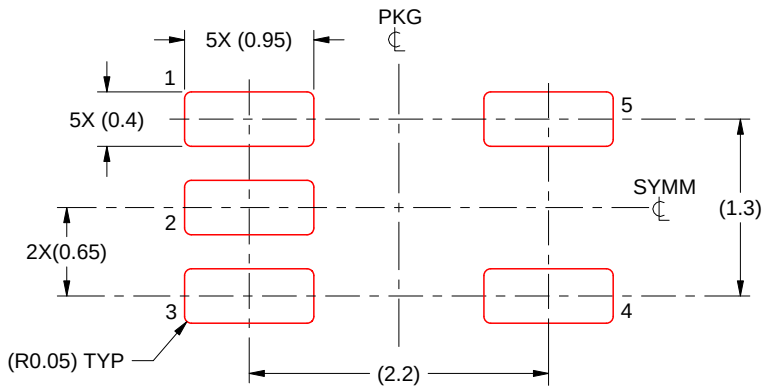
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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