SN65LBC173、SN75LBC173 四通道低功耗差分线路接收器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B、EIA/TIA-423-B、RS-485 和 ITU 建议 V.10 和 V.11 的要求。
- 可以低至 20ns 的脉冲持续时间运行
- 适用于嘈杂环境中长总线上的多点总线传输
- 输入灵敏度：±200mV
- 低功耗：20 mA（最大值）
- 开路失效防护设计
- 与 SN75173 和 AM26LS32 引脚兼容

2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动器

3 说明

SN65LBC173 和 SN75LBC173 是具有三态输出的单片四通道差分线路接收器。二者均旨在满足 ANSI 标准 EIA/TIA-422-B、EIA/TIA-423-B、RS-485 以及数项 ITU 建议 V.10 和 V.11 的要求。这个器件针对数据速率高达和超过每秒 10 兆位的平衡多点总线传输进行了优化。4 个接收器共用 2 个进行或操作的使能输入，一个在高电平时有效，一个在低电平时有效。

每个接收器在 12V 至 -7 V 的共模输入电压范围内特有高输入阻抗、输入滞后以增加抗扰度，以及 ±200mV 的输入灵敏度。故障安全设计确保了在输入为开路时，输出始终为高电平。这两款器件都使用德州仪器 (TI) 专有 LinBiCMOS™ 技术进行设计，该技术具有低功耗、高开关速度和稳健性。

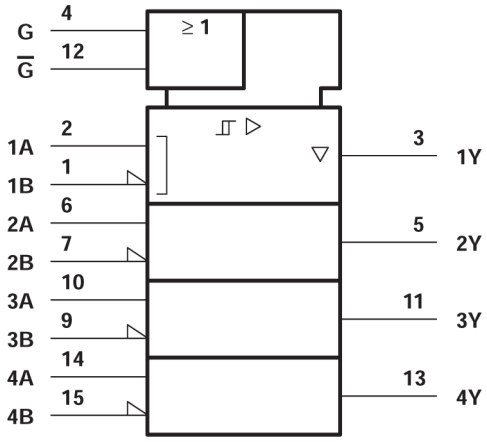
这些器件会在与 SN75LBC172 或 SN75LBC174 四通道线路驱动器配合使用时提供卓越性能。SN65LBC173 和 SN75LBC173 采用 16 引脚 DIP (N) 和 SOIC (D) 封装。

SN65LBC173 可在 -40°C 至 85°C 的工业温度范围内运行。SN75LBC173 可在 0°C 至 70°C 的商用温度范围内运行。

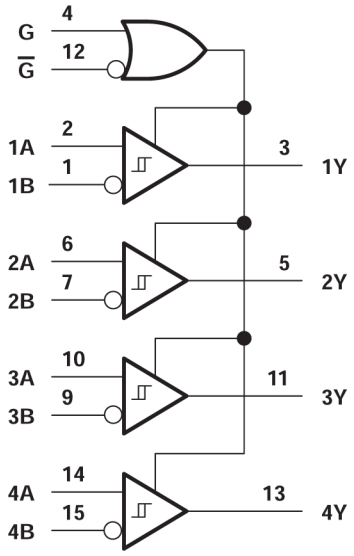
封装信息

器件型号	封装(1)	封装尺寸(2)
SN65LBC173 SN75LBC173	D（SOIC，16）	9.9mm × 6mm
	N（PDIP、16）	19.3mm × 9.4mm

(1) 有关详细信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

4 Pin Configuration and Functions

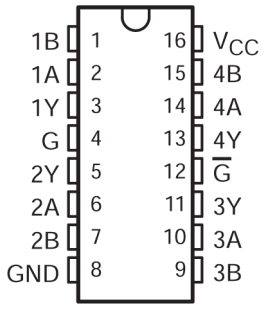


图 4-1. D or N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Inverting Differential Input
1A	2	I	Channel 1 Non-Inverting Differential Input
1Y	3	O	Channel 1 Output
G	4	I	Active High Receiver Enable
2Y	5	O	Channel 2 Output
2A	6	I	Channel 2 Non-Inverting Differential Input
2B	7	I	Channel 2 Inverting Differential Input
GND	8	GND	Device Ground
3B	9	I	Channel 3 Inverting Differential Input
3A	10	I	Channel 3 Non-Inverting Differential Input
3Y	11	O	Channel 3 Output
$\overline{G}$	12	I	Active Low Receiver Enable
4Y	13	O	Channel 4 Output
4A	14	I	Channel 4 Non-Inverting Differential Input
4B	15	I	Channel 4 Inverting Differential Input
V_{CC}	16	POW	Device Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage range		−0.3	7	V
V_I	Input voltage (A or B inputs)			±25	V
V_{ID} (3)	Differential input voltage			±25	V
	Voltage range at Y, G, $\overline{G}$		−0.3	V_{CC} + 0.5	V
	Continuous total dissipation		See Dissipation Rating Table		
T_A	Operating free-air temperature range:	SN65LBC173	−40	85	°C
		SN75LBC173	0	70	°C
T_{stg}	Storage temperature range		−65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Ratings

PACKAGE	$T_A \leqslant$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	1100 mW	8.7 mW/°C	708 mW	578 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (N)	UNIT
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}	G inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A	SN65LBC173	−40		85	°C
	SN75LBC173	0		70	

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
$V_{IT}+$	Positive-going input threshold voltage		I_O = −8 mA					0.2	V
$V_{IT}-$	Negative-going input threshold voltage		I_O = 8 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT}+ - V_{IT}-$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 8 mA			0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	μA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V		0.8	1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V		−0.5	−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V		−0.4	−0.8	
I_{IH}	High-level input current		V_{IH} = 5 V					±20	μA
I_{IL}	Low-level input current		V_{IL} = 0 V					−20	μA
I_{OS}	Short-circuit output current		V_O = 0				−80	−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Switching Characteristics

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See 图 6-1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	30	ns
t_{PZH}	Output enable time to high level	See 图 6-2		17	30	ns
t_{PZL}	Output enable time to low level	See 图 6-3		18	30	ns
t_{PHZ}	Output disable time from high level	See 图 6-2		35	45	ns
t_{PLZ}	Output disable time from low level	See 图 6-3		25	40	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See 图 6-2		0.5	6	ns
t_t	Transition time	See 图 6-1		5	10	ns

5.7 Typical Characteristics

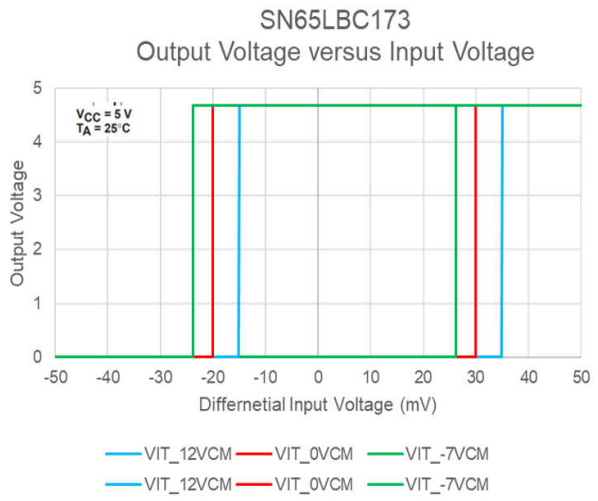


图 5-1. Output Voltage vs Differential Input Voltage

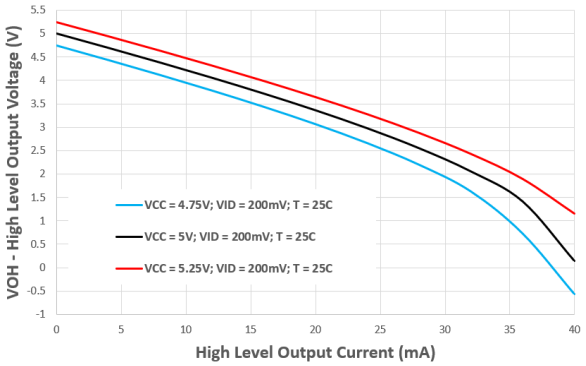


图 5-2. High-level Output Voltage vs High-level Output Current

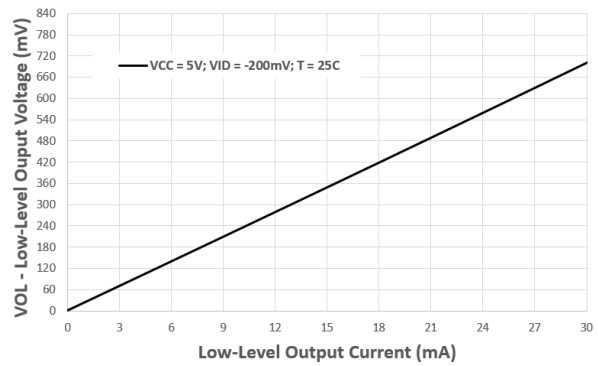


图 5-3. Low-level Output Voltage vs Low-level Output Current

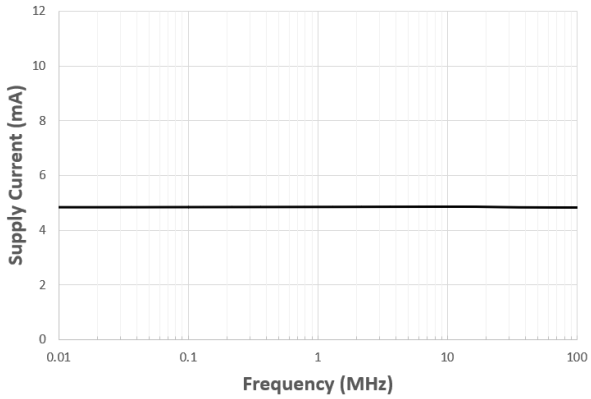


图 5-4. Average Supply Current vs Frequency

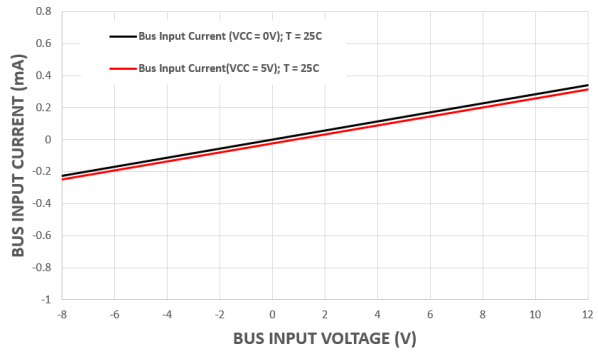


图 5-5. Bus Input Current vs Input Voltage (Complementary Input at 0 V)

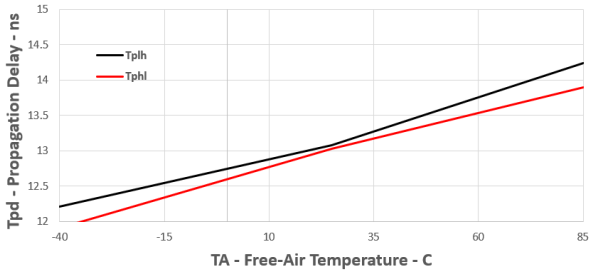


图 5-6. Propagation Delay Time vs Free-air Temperature

6 Parameter Measurement Information

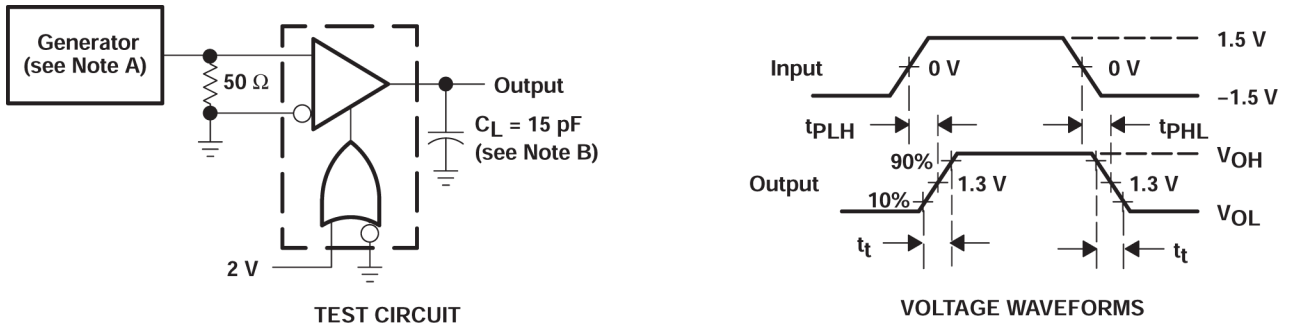
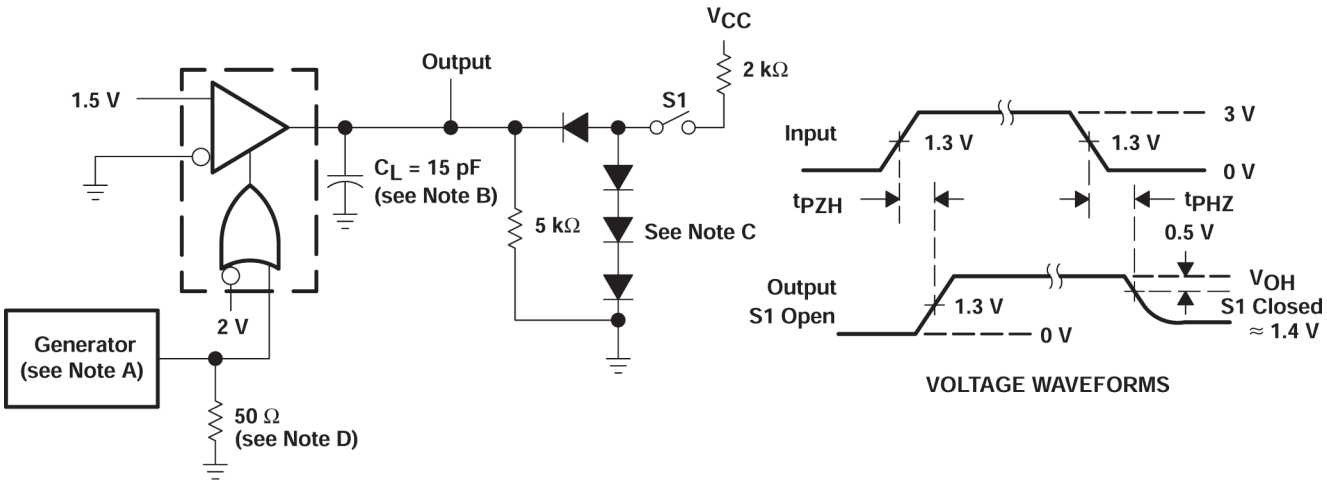
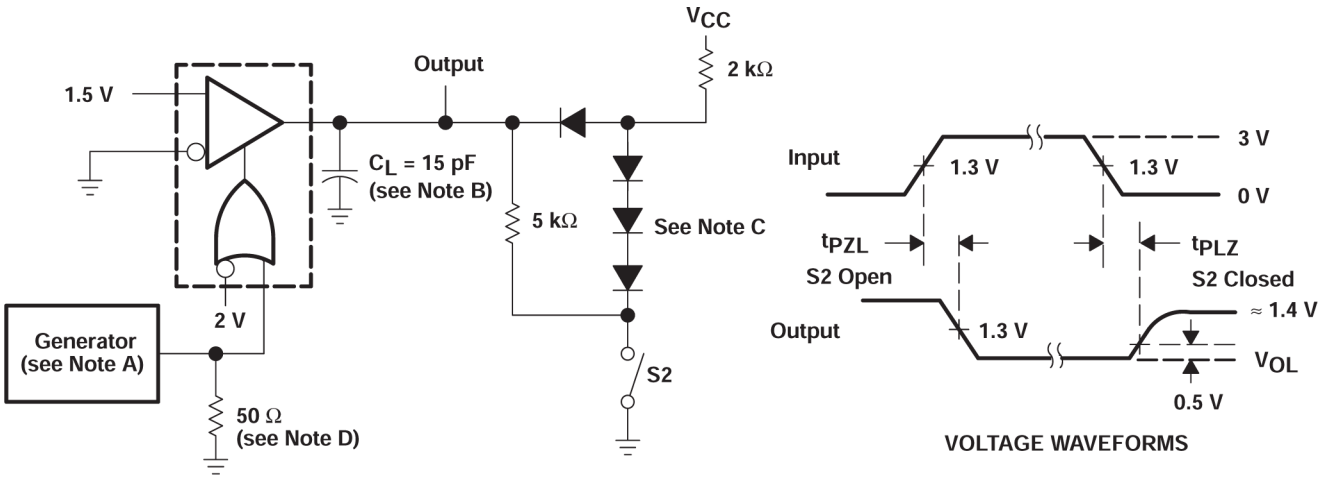


图 6-1. t_{pd} and t_t Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

图 6-2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leqslant 6$ ns, $t_f \leqslant 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

图 6-3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Function Table (Each Receiver)

DIFFERENTIAL INPUTS	ENABLES(1)		OUTPUT
A−B	G	$\overline{G}$	Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
−0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

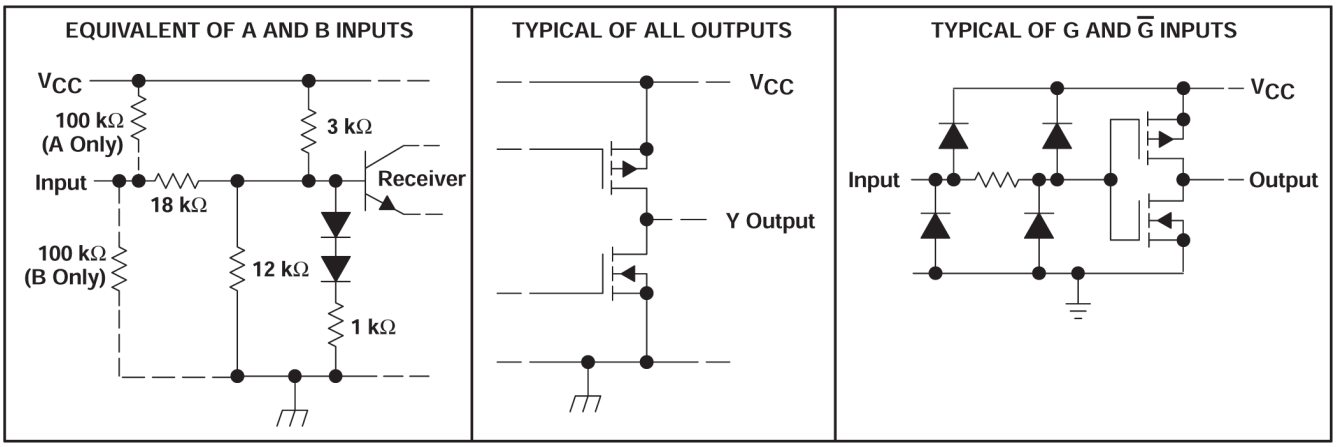


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (August 2000) to Revision F (August 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC173D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	65LBC173	
SN65LBC173DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC173	Samples
SN65LBC173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC173N	Samples
SN75LBC173D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	75LBC173	
SN75LBC173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC173N	Samples
SN75LBC173NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC173N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN75LBC173 :

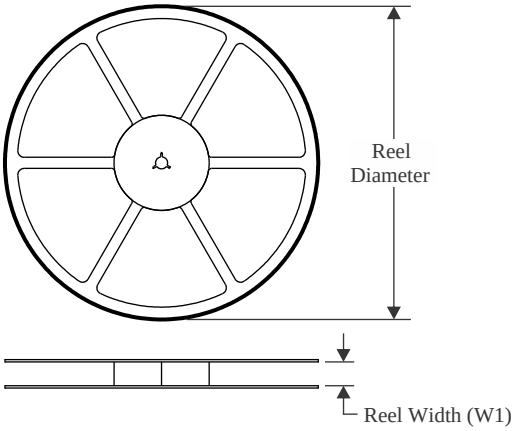
- Military : SN55LBC173

NOTE: Qualified Version Definitions:

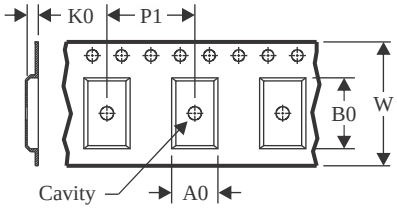
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

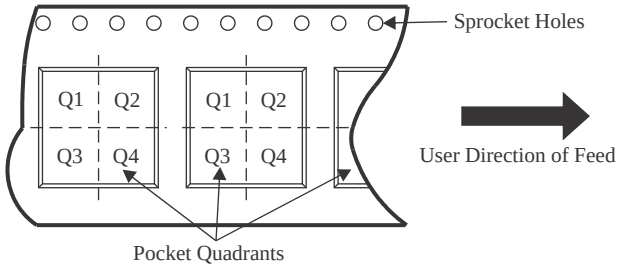


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

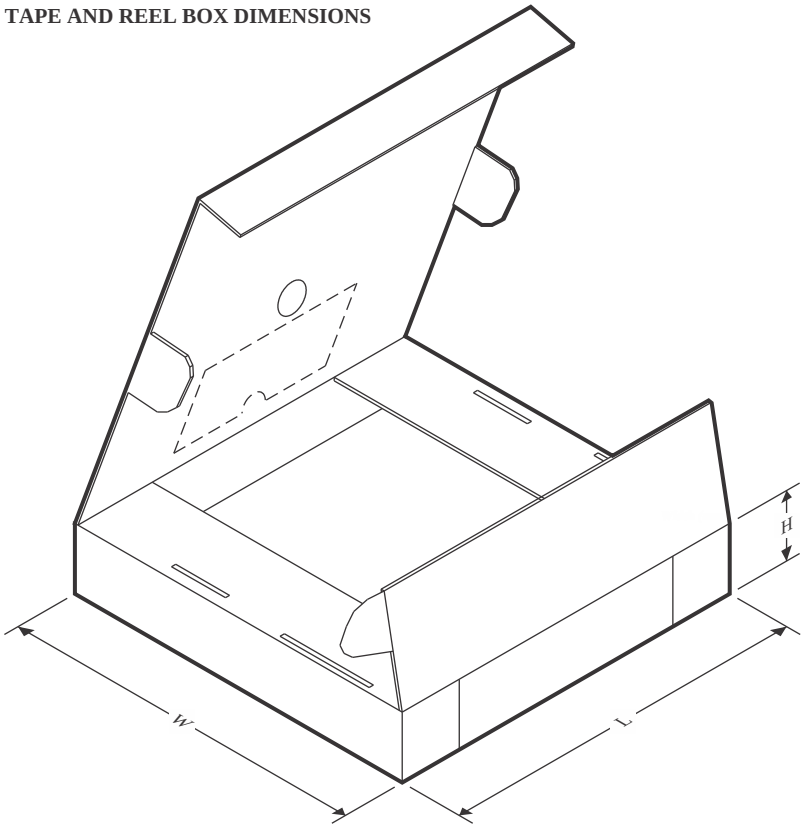
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

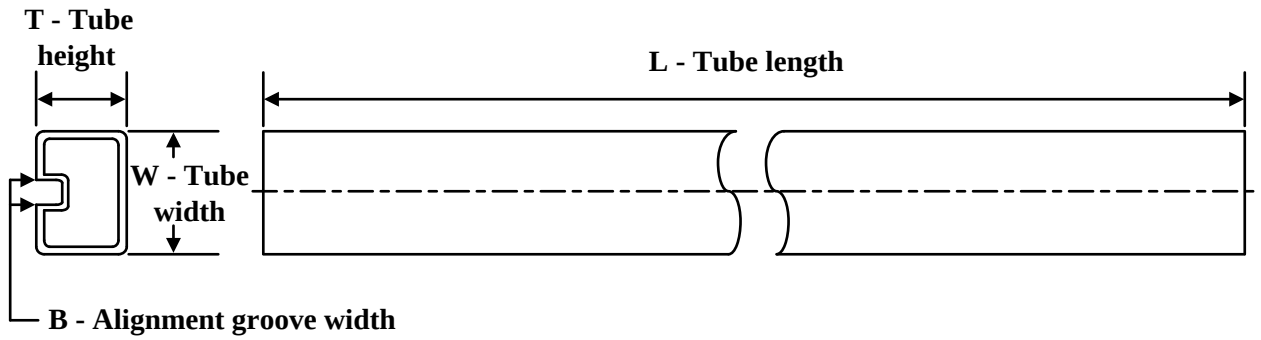
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC173DR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC173N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC173N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC173NE4	N	PDIP	16	25	506	13.97	11230	4.32

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