TAS5414C 四通道汽车售后加装 D 类放大器

1 特性

- 四通道单端模拟输入 D 类音频放大器
- 在 10% 总谐波失真 (THD) + N 上典型输出功率
  - 14.4V时，为 4Ω 负载每通道输出功率为 28W
  - 14.4V时，为 2Ω 负载每通道输出功率为 50W
  - 24V时，为 4Ω 负载每通道输出功率为 79W
  - 24V时，为 2Ω 负载每通道输出功率为 150W (PBTL)
- 通道可被并联 (PBTL)，适用于高电流 应用
- THD + N < 0.02%，1kHz，为 4Ω 负载提供 1W
- 已获专利的杂音抑制技术
  - 具有增益斜波控制的软静音
  - 共模斜波修整
- 已获专利的 AM 干扰避免
- 已获专利的逐周期电流限制
- 75dB 电源抑制比 (PSRR)
- 针对器件配置和控制的 4 地址 I^2C 串行接口
- 通道增益：12dB，20dB，26dB，32dB
- 负载诊断功能：
  - 输出打开和短接负载
  - 输出到电源和输出到接地短接
  - 已获专利的高频扬声器侦测
- 保护和监控功能：
  - 短路保护
  - 负载突降保护达 50V
  - 偶然开放式接地和电源容错
  - 已获专利的在音乐播放的同时进行输出直流电平侦测
  - 过热保护
  - 过压和欠压条件
  - 片段侦测器
- 64 引脚四方扁平无引线 (QFP) (PHD) 功率封装（散热片朝上）
- -20°C 至 105°C 环境温度范围

2 应用

- 售后加装音响主机
- 售后加装外部音频放大器

3 说明

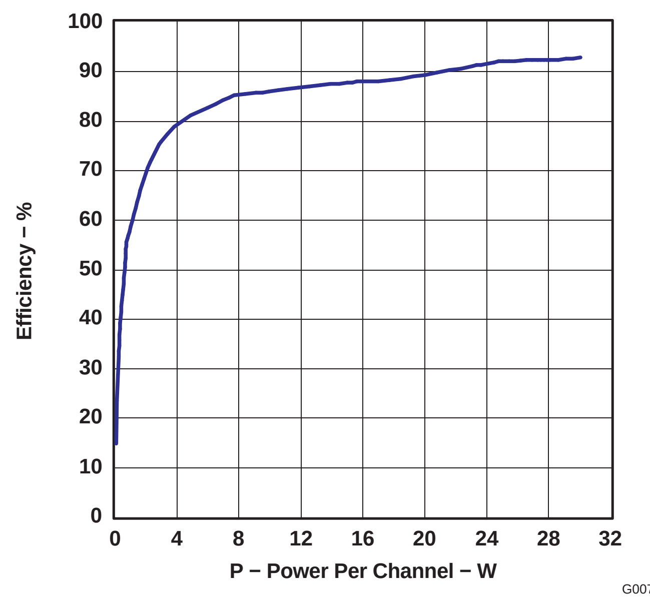
TAS5414C 器件是一款四通道 D 类音频放大器，专为汽车类音响主机和外部放大器模块而设计。在 14.4V 电源供电下，能够以低于 1% 的 THD+N 持续为 4Ω 负载提供四通道 23W 功率。每个通道还能够以 1% 的 THD+N 为 2Ω 负载提供 38W 的功率。TAS5414C 采用单端模拟量输入。此器件的 D 类数字脉宽调制 (PWM) 拓扑可大大提升传统线性放大器解决方案的效率。在正常音乐播放条件下，这有助于将放大器功耗减降低 10%。该器件具有内置负载诊断功能，用于检测和诊断误接的输出，从而帮助缩短制造过程中的测试时间。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TAS5414C	HTQFP (64)	14.00mm x 14.00mm

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

每通道效率与功耗对比



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4 修订历史记录

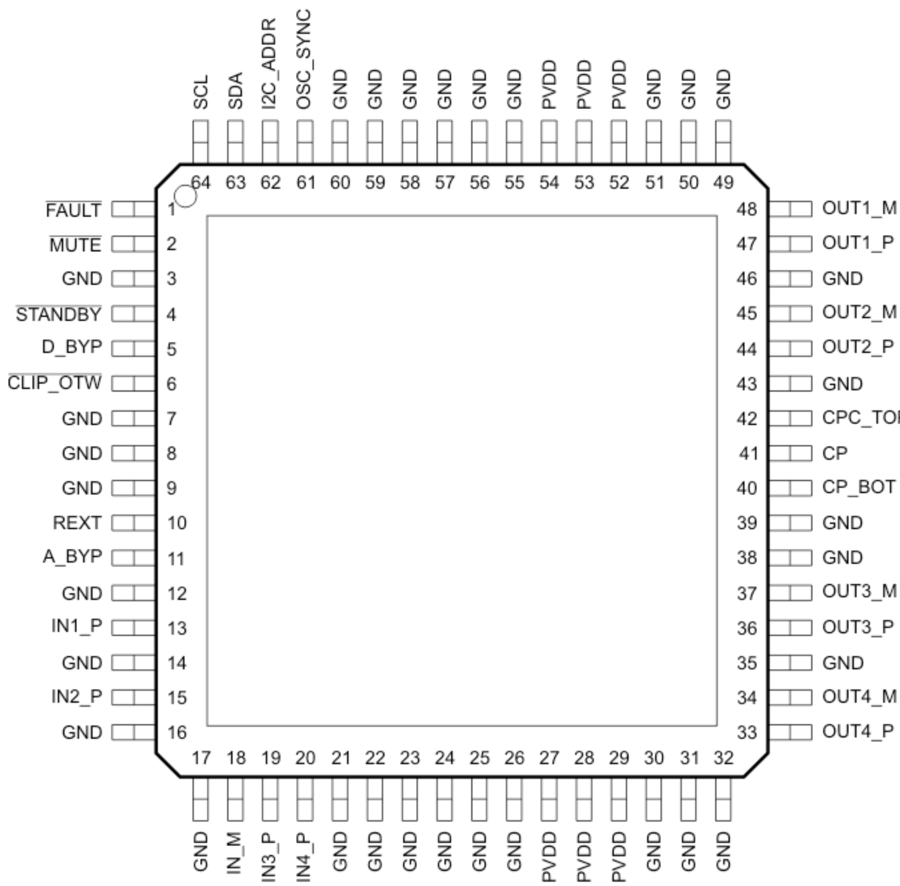
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	注释
2016 年 12 月	*	最初发布。

5 Pin Configuration and Functions

The pin assignments are shown as follows.

PHD Package
64-Pin HTQFP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	TAS5414C PHD Package NO.		
A_BYP	11	PBY	Bypass pin for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	6	DO	Reports CLIP, OTW, or both. It also reports tweeter detection during tweeter mode. Open-drain
CP	41	CP	Top of main storage capacitor for charge pump (bottom goes to PVDD)
CPC_BOT	40	CP	Bottom of flying capacitor for charge pump
CPC_TOP	42	CP	Top of flying capacitor for charge pump
D_BYP	5	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	1	DO	Global fault output (open drain): UV, OV, OTSD, OCSD, DC
GND	3, 7, 8, 9, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51, 55, 56, 57, 58, 59, 60	GND	Ground
I2C_ADDR	62	AI	I^2C address bit
IN1_P	13	AI	Non-inverting analog input for channel 1
IN2_P	15	AI	Non-inverting analog input for channel 2
IN3_P	19	AI	Non-inverting analog input for channel 3
IN4_P	20	AI	Non-inverting analog input for channel 4
IN_M	18	ARTN	Signal return for the four analog channel inputs (TAS5414C only)
$\overline{\text{MUTE}}$	2	AI	Gain ramp control: mute (low), play (high)
OSC_SYNC	61	DI/DO	Oscillator input from master or output to slave amplifiers
OUT1_M	48	PO	– polarity output for bridge 1
OUT1_P	47	PO	+ polarity output for bridge 1
OUT2_M	45	PO	– polarity output for bridge 2
OUT2_P	44	PO	+ polarity output for bridge 2
OUT3_M	37	PO	– polarity output for bridge 3
OUT3_P	36	PO	+ polarity output for bridge 3
OUT4_M	34	PO	– polarity output for bridge 4
OUT4_P	33	PO	+ polarity output for bridge 4
PVDD	27, 28, 29, 52, 53, 54	PWR	PVDD supply
REXT	10	AI	Precision resistor pin to set analog reference
SCL	64	DI	I^2C clock input from system I^2C master
SDA	63	DI/DO	I^2C data I/O for communication with system I^2C master
$\overline{\text{STANDBY}}$	4	DI	Active-low STANDBY pin. Standby (low), power up (high)

(1) DI = digital input, DO = digital output, AI = analog input, ARTN = analog signal return, PWR = power supply, PBY = power bypass, PO = power output, GND = ground, CP = charge pump.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
PVDD	DC supply voltage range	Relative to GND	–0.3	30	V
$PVDD_{MAX}$	Pulsed supply voltage range	t ≤ 100 ms exposure	–1	50	V
$PVDD_{RAMP}$	Supply voltage ramp rate			15	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or GND pin			±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		17	A
I_O	Maximum allowed dc current per output pin			±13.5	A
I_{O_MAX} (1)	Pulsed output current per output pin (single pulse)	t < 100 ms		±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins (2)	DC or pulsed		±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{\text{MUTE}}$ pin	DC or pulsed		±20	mA
I_{IN_ODMAX}	Maximum sink current for open-drain pins			7	mA
V_{LOGIC}	Input voltage range for pin relative to GND (SCL, SDA, I2C_ADDR pins)	Supply voltage range: 6V < PVDD < 24 V	–0.3	6	V
V_{MUTE}	Voltage range for $\overline{\text{MUTE}}$ pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3	7.5	V
$V_{STANDBY}$	Input voltage range for $\overline{\text{STANDBY}}$ pin	Supply voltage range: 6 V < PVDD < 24 V	–0.3	5.5	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3	3.6	V
V_{GND}	Maximum voltage between GND pins			±0.3	V
$V_{AIN\_AC\_MAX}$	Maximum ac-coupled input voltage for TAS5414C (2), analog input pins	Supply voltage range: 6 V < PVDD < 24 V		1.9	Vrms
T_J	Maximum operating junction temperature range		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Pulsed current ratings are maximum survivable currents externally applied to the device. The device may encounter high currents during reverse-battery, fortuitous open-ground, and fortuitous open-supply fault conditions.
(2) See the *Application Information* section for information on analog input voltage and ac coupling.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2500	V
		Charged device model (CDM), per AEC Q100-011 PHD Package	Corner pins excluding SCL	±750	V
			All pins (including SCL) except CP and CP_Top	±600	
			CP and CP_Top pins	±400	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions (1)

			MIN	TYP	MAX	UNIT
$PVDD_{OP}$	DC supply voltage range relative to GND		6	14.4	24	V
V_{AIN} (2)	Analog audio input signal level	AC-coupled input voltage	0		0.25–1 (3)	Vrms
T_A	Ambient temperature		–20		105	°C
T_J	Junction temperature	An adequate heat sink is required to keep T_J within specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω

(1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

Recommended Operating Conditions[1] (continued)

			MIN	TYP	MAX	UNIT
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_EXT}	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and V_{PU} supply	10		50	kΩ
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
R_{I2C_ADD}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and GND pins		10		50	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP} , C_{A_BYP}	External capacitance on D_BYP and A_BYP pins		10		120	nF
C_{OUT}	External capacitance to GND on OUT_X pins			150	680	nF
C_{IN}	External capacitance to analog input pin in series with input signal			0.47		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge pump capacitor	50V needed for Load Dump	0.47	1	1.5	µF
C_{MUTE}	$\overline{MUTE}$ pin capacitor		100	220	1000	nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			75		pF

6.4 Thermal Information

PARAMETER		VALUE (Typical)	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, PHD package	1.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. Refer to the *Thermal Information* section.	°C/W

6.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see Figure 36)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All four channels in MUTE mode		170	220	mA
I_{PVDD_Hi-Z}	PVDD idle current	All four channels in Hi-Z mode		93		mA
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, T_J ≤ 85°C		2	10	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T_c = 75°C		23		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	25	28		
		4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C	63	79		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c = 75°C		38		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	40	50		
		PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C		150		
		PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C		90		
EFF_P	Power efficiency	4 channels operating, 23-W output power/ch, L = 10 µH, T_J ≤ 85°C		90%		
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	Zero input, and A-weighting		60	100	µV
	Channel crosstalk	P = 1 W, f = 1 kHz, enhanced crosstalk enabled via I^2C (reg. 0x10)	70	85		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1 W, f = 1 kHz		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	

Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I^2C settings, master-mode operation (see Figure 36)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	63	85	106	kΩ
V_{IN_CM}	Common-mode input voltage	AC-coupled common-mode input voltage (zero differential input)		1.3		Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.3		V
G	Voltage gain (V_O/V_{IN})	Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	Not including bond wire resistance, T_J = 25°C		65	90	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal, G = 26 dB		±10	±50	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV_SET}	PVDD overvoltage shutdown set		24.6	26.4	28.2	V
V_{OV_CLEAR}	PVDD overvoltage shutdown clear		24.4	25.9	27.4	V
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown set		4.9	5.3	5.6	V
V_{UV_CLEAR}	PVDD undervoltage shutdown clear		6.2	6.6	7	V
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			4.8		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			5.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V
POWER-ON RESET (POR)						
V_{POR}	PVDD voltage for POR	I^2C active above this voltage			4	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V
REXT						
V_{REXT}	Rext pin voltage			1.27		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			4.9		V
OVERTEMPERATURE (OT) PROTECTION						
T_{OTW1_CLEAR}	Junction temperature for overtemperature warning		96	112	128	°C
T_{OTW1_SET} / T_{OTW2_CLEAR}			106	122	138	°C
T_{OTW2_SET} / T_{OTW3_CLEAR}			116	132	148	°C
T_{OTW3_SET} / T_{OTSD_CLEAR}			126	142	158	°C
T_{OTSD}	Junction temperature for overtemperature shutdown		136	152	168	°C
T_{FB}	Junction temperature for overtemperature foldback	Per channel	130	150	170	°C
CURRENT LIMITING PROTECTION						
I_{LIM}	Current limit (load current)	Level 1	5.5	7.3	9	A
		Level 2 (default)	10.6	12.7	15	
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX}	Maximum current (peak output current)	Level 1	7.8	9.8	12.2	A
		Level 2 (default), Any short to supply, ground, or other channels	11.9	14.8	17.7	

Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I²C settings, master-mode operation (see Figure 36)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TWEETER DETECT						
I_{TH_TW}	Load-current threshold for tweeter detect		330	445	560	mA
I_{LIM_TW}	Load-current limit for tweeter detect			2.1		A
STANDBY MODE						
V_{IH}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2			V
V_{IL}	$\overline{\text{STANDBY}}$ input voltage for logic-level low				0.7	V
I_{STBY}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	µA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.5 V for 200ms or I²C Mute Enabled		100		dB
DC DETECT						
$V_{TH\_DC\_TOL}$	DC detect threshold tolerance			25%		
t_{DCD}	DC detect step-response time for four channels				5.3	s
CLIP_OTW REPORT						
$V_{OH\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
$V_{OL\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level low (open-drain logic output)				0.5	V
$t_{DELAY\_CLIPDET}$	$\overline{\text{CLIP\_OTW}}$ signal delay when output clipping detected				20	µs
FAULT REPORT						
V_{OH_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
V_{OL_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level low (open-drain logic output)				0.5	

Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 filter, default I²C settings, master-mode operation (see Figure 36)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN, SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	740	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1	1.5	Ω
I²C ADDRESS DECODER						
$t_{LATCH\_I2CADDR}$	Time delay to latch I²C address after POR			300		µs
V_{I2C_ADDR}	Voltage on I2C_ADDR pin for address 0	Connect to GND	0%	0%	15%	V_{D_BYP}
	Voltage on I2C_ADDR pin for address 1	External resistors in series between D_BYP and GND as a voltage divider	25%	35%	45%	
	Voltage on I2C_ADDR pin for address 2		55%	65%	75%	
	Voltage on I2C_ADDR pin for address 3	Connect to D_BYP	85%	100%	100%	
I²C						
t_{HOLD_I2C}	Power-on hold time before I²C communication	$\overline{\text{STANDBY}}$ high		1		ms
f_{SCL}	SCL clock frequency				400	kHz
V_{IH}	SCL pin input voltage for logic-level high	R_{PU_I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SCL pin input voltage for logic-level low		–0.5		1.1	V
V_{OH}	SDA pin output voltage for logic-level high	I²C read, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
V_O	SDA pin output voltage for logic-level low	I²C read, 3-mA sink current			0.4	V
V_{IH}	SDA pin input voltage for logic-level high	I²C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1		5.5	V
V_{IL}	SDA pin input voltage for logic-level low	I²C write, R_{I2C} = 5-kΩ pullup, supply voltage = 3.3 V or 5 V	–0.5		1.1	V
C_I	Capacitance for SCL and SDA pins				10	pF
OSCILLATOR						
V_{OH}	OSC_SYNC pin output voltage for logic-level high	I2C_ADDR pin set to MASTER mode	2.4			V
V_{OL}	OSC_SYNC pin output voltage for logic-level low				0.5	V
V_{IH}	OSC_SYNC pin input voltage for logic-level high	I2C_ADDR pin set to SLAVE mode	2			V
V_{IL}	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	I2C_ADDR pin set to MASTER mode, f_S = 500 kHz	3.76	4	4.24	MHz
		I2C_ADDR pin set to MASTER mode, f_S = 417 kHz	3.13	3.33	3.63	
		I2C_ADDR pin set to MASTER mode, f_S = 357 kHz	2.68	2.85	3.0	

6.6 Timing Requirements for I²C Interface Signals

over recommended operating conditions (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	0.6			µs
$t_{w(L)}$	SCL pulse duration, low	1.3			µs.
t_{su2}	Setup time for START condition	0.6			µs
t_{h2}	START condition hold time until generation of first clock pulse	0.6			µs
t_{su1}	Data setup time	100			ns
t_{h1}	Data hold time	0 (1)			ns
t_{su3}	Setup time for STOP condition	0.6			µs
C_B	Load capacitance for each bus line			400	pF

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

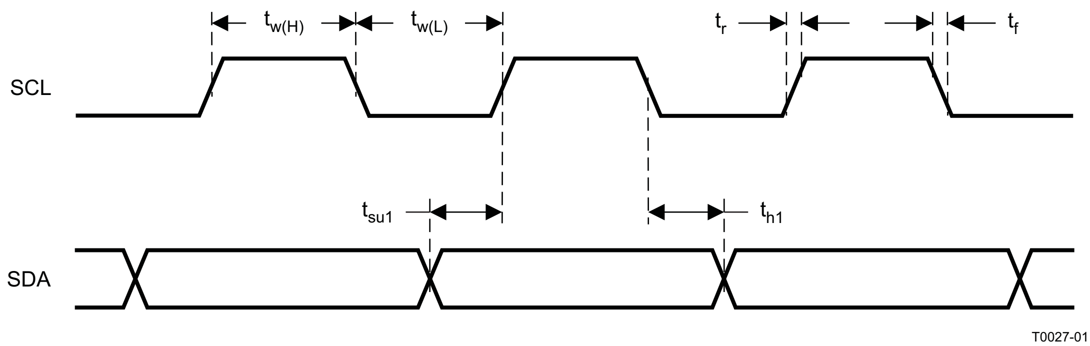


Figure 1. SCL and SDA Timing

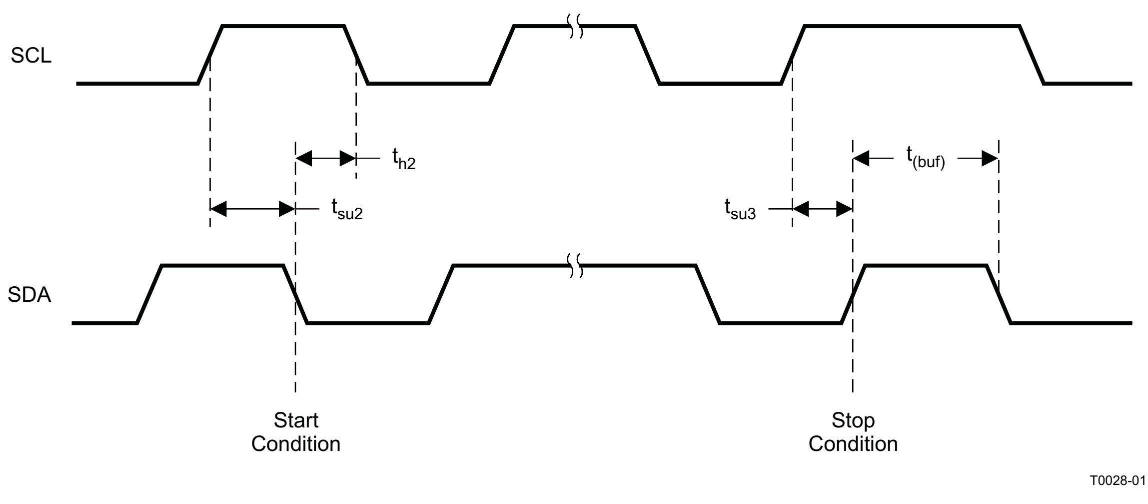


Figure 2. Timing for Start and Stop Conditions

6.7 Typical Characteristics

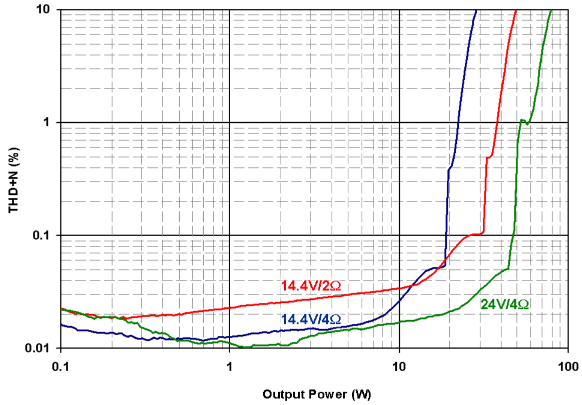


Figure 3. THD+N vs BTL Output Power at 1kHz

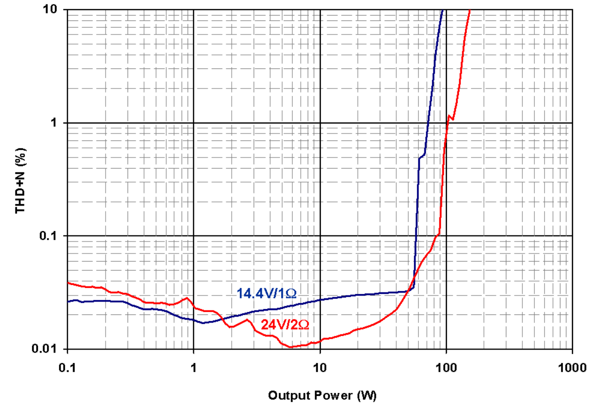


Figure 4. THD+N vs PBTL Output Power at 1kHz

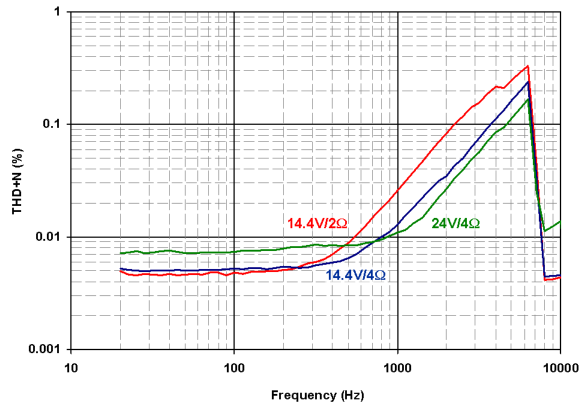


Figure 5. THD+N vs Frequency at 1 Watt

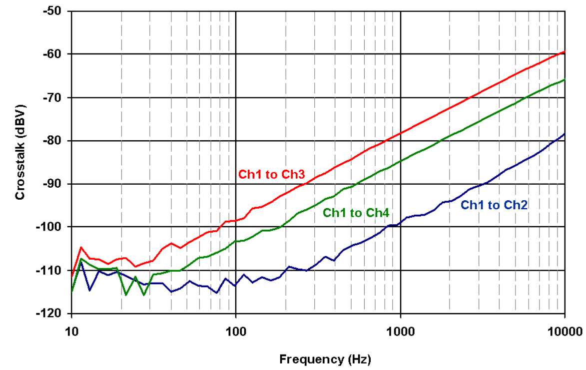


Figure 6. Crosstalk vs Frequency

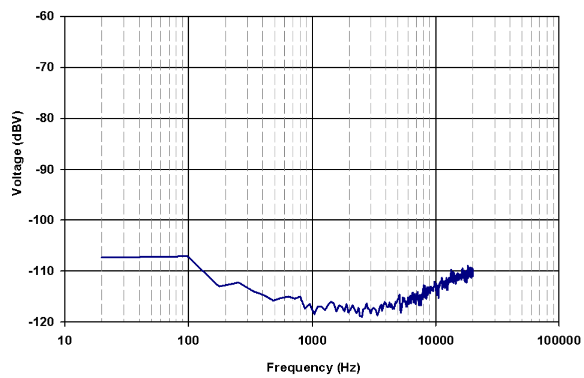


Figure 7. Noise FFT

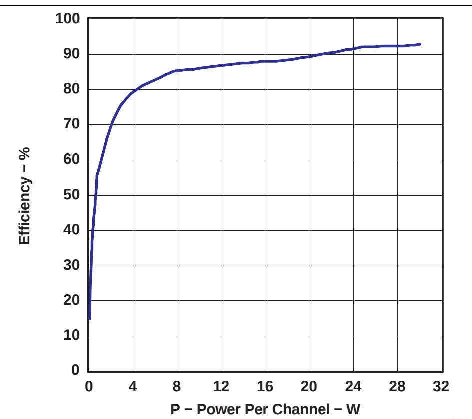


Figure 8. Efficiency
Four Channels AT 4 Ω Each

Typical Characteristics (continued)

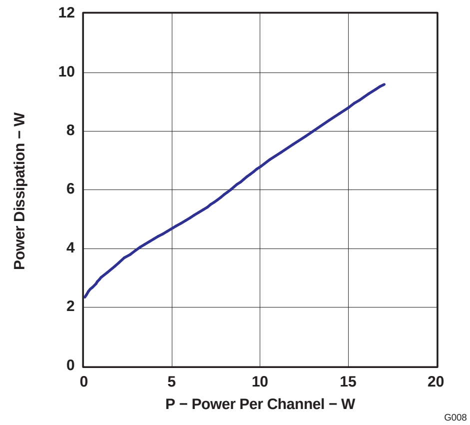


Figure 9. Device Power Dissipation Four Channels at 4 Ω Each

7 Detailed Description

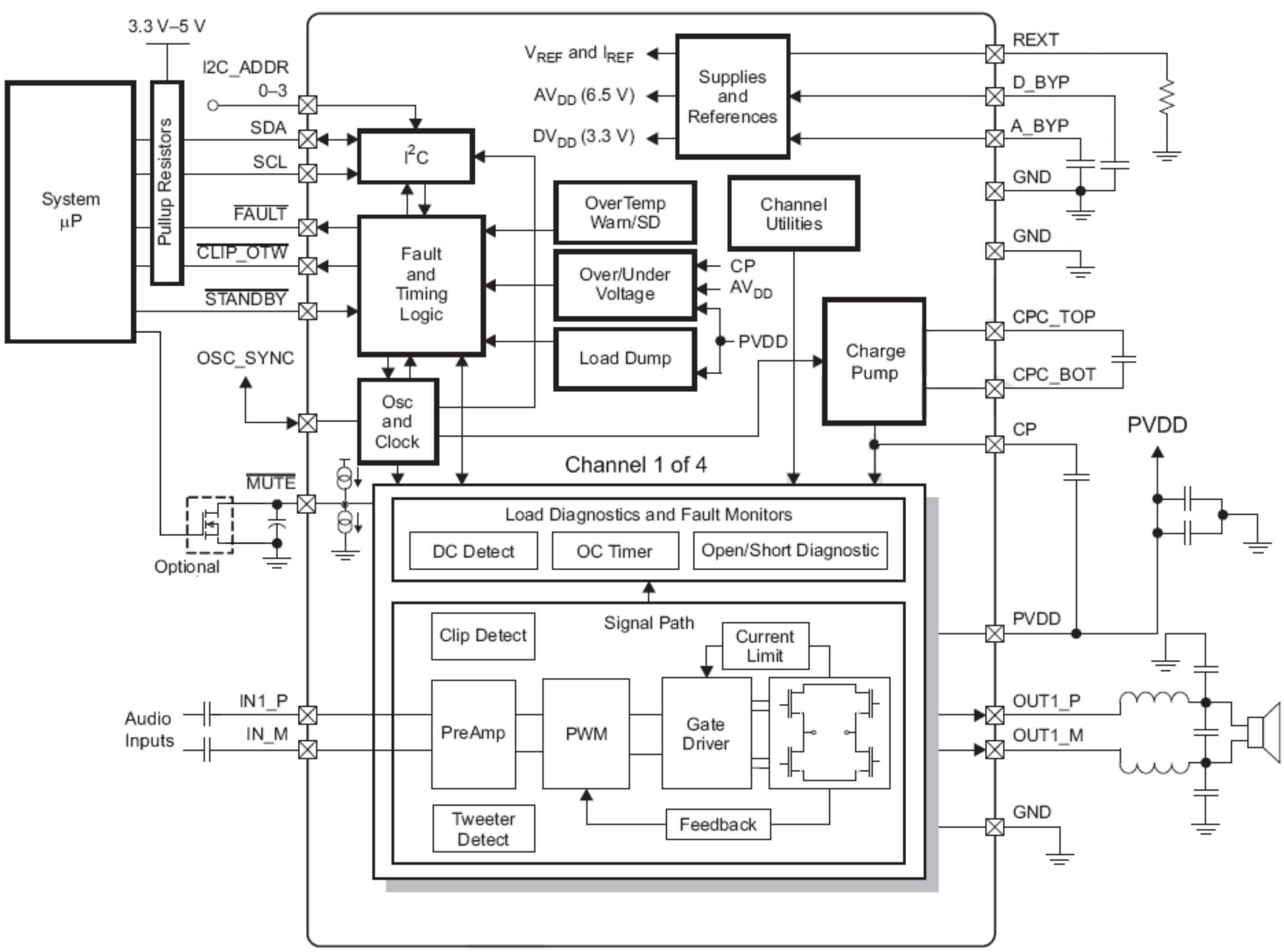
7.1 Overview

The TAS5414C is a single-chip, four-channel, analog-input audio amplifier. The design uses an ultra-efficient class-D technology developed by Texas Instruments. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

There are eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

7.2 Functional Block Diagram



7.3 Feature Descption

7.3.1 Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. A dedicated, internally regulated supply pwoers the preamplifier, giving it excellent noise immunity and channel separation. The preamplifier also includes:

1. **Mute Pop-and-Click Control** — The device ramps the gain gradually when receiving a mute or play command. The start or stopping of switching in a class-D amplifier can cause another form of click and pop. The TAS5414C incorporates a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require rapid protection response by the TAS5414C, which does not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when encountering an OV, UV, OC, OT, or dc fault. Also, activation of the STANDBY pin may not be pop-free.
2. **Gain Control** — Setting of gains for the four channels occurs in the preamplifier via I^{2}C control registers, outside of the global feedback resistors of the device, thus allowing for stability of the system at all gain settings with properly loaded conditions.

7.3.2 Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5414C, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

7.3.3 Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

7.3.4 Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs can handle large voltage transients during load dump.

7.3.5 Load Diagnostics

The device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The TAS5414C includes functions for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to PVDD
- Short across load
- Open load
- Tweeter detection

Reporting to the system of the presence of any of the short or open conditions occurs via I^{2}C register read. One can read the tweeter-detect status from the CLIP_OTW pin when properly configured.

1. **Output Short and Open Diagnostics** — The device contains circuitry designed to detect shorts and open conditions on the outputs. Invocation of the load diagnostic function can only occur when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. Testing covers all four phases on each channel, all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, the only tests available are short to PVDD and short to GND. Load diagnostics can occur at power up before moving the amplifier out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* before performing the load diagnostic. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. Performance of the diagnostics is as shown in Figure 10. Figure 11 shows the impedance ranges for the open-load and shorted-load diagnostics. Reading the results of the diagnostics is from the diagnostic register via I^{2}C for each channel. With the default settings and MUTE capacitor, the S2G and S2P phase take approximately 20 ms each, the OL phase

Feature Descption (continued)

takes approximately 100 ms, and the SL takes approximately 230 ms. In I^2C register 0x10, bit D4 can extend the test time for S2P and S2G to 80 ms each. To prevent false S2G and S2P faults, this time extension is necessary if the output pins have a capacitance higher than 680 nF to ground .

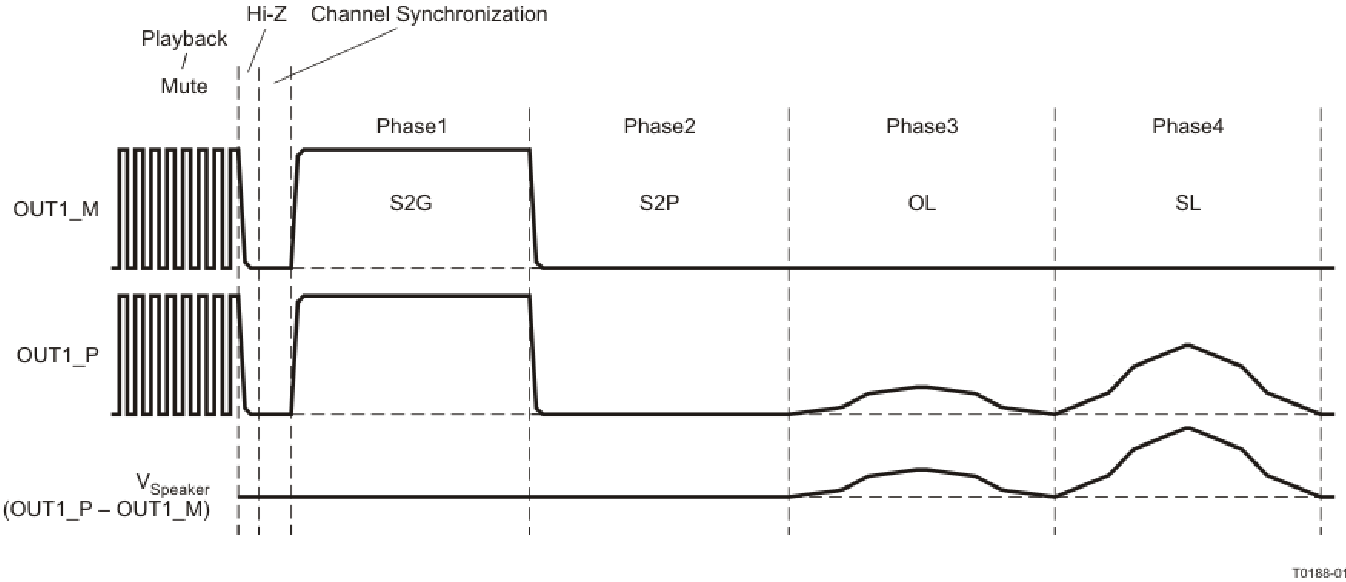


Figure 10. Load Diagnostics Sequence of Events

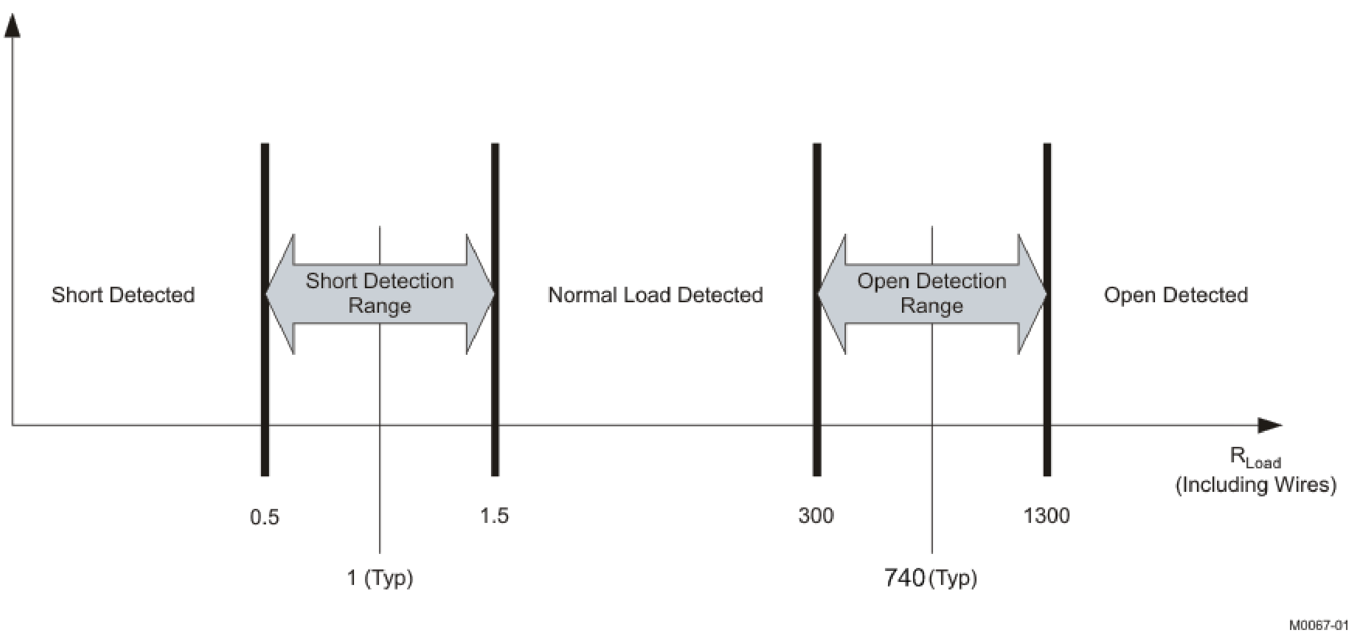


Figure 11. Open- and Shorted-Load Detection

2. **Tweeter Detection** — Tweeter detection is an alternate operating mode used to determine the proper connection of a frequency-dependent load (such as a speaker with a crossover). Invoking of weeter detection is via I^2C, with individual testing of all four channels recommended. Tweeter detection uses the average cycle-by-cycle current limit circuit (see *CBC* section) to measure the current delivered to the load. The proper implementation of this diagnostic function depends on the amplitude of a user-supplied test signal and on the impedance-versus-frequency curve of the acoustic load. The system (external to the TAS5414C) must generate a signal to which the load responds. The frequency and amplitude of this signal must be calibrated by the user to result in a current draw that is greater than the tweeter detection threshold when the load

Feature Descption (continued)

under test is present, and less than the detection threshold if the load is unconnected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter-detection mode, is in the Electrical Characteristics section of the data sheet. Reporting of the tweeter-detection results is on the CLIP_OTW pin during the application of the test signal. With tweeter detection activated (indicating that the tested load is present), pulses on the CLIP_OTW pin begin to toggle. The pulses on the CLIP_OTW pins report low whenever the current exceeds the detection threshold, and the pin remains low until the current no longer exceeds the threshold. The minimum low-pulse period that one can expect is equal to one period of the switching frequency. Having an input signal that increases the duration of detector activation (for example, increasing the amplitude of the input signal) increases the amount of time for which the pin reports low.
NOTE: Because tweeter detection is an alternate *operating mode*, place the channels to be tested in Play mode (via register 0x0C) after tweeter detection has been activated in order to commence the detection process. Additionally, set up the CLIP_OTW pin via register 0x0A to report the results of tweeter detection.

7.3.6 Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)** — The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow to the average current limit (I_{LIM}) threshold. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, temporarily limiting power at the peaks of the musical signal and normal operation continues without disruption on removal of the overload. The TAS5414C does not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCSD)** — Under severe short-circuit events, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels shut down in such a scenario. The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the I^2C fault register saves a record of the affected channels. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.
3. **DC Detect**—This circuit detects a dc offset at the output of the amplifier continuously during normal operation. If the dc offset reaches the level defined in the I^2C registers for the specified time period, the circuit triggers. By default, a dc detection event does not shut the output down. Disabling and enabling the shutdown function is via I^2C. If enabled, the triggered channel shuts down, but the others remain playing, but with the FAULT pin asserted. The I^2C registers define the dc level.
4. **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal passed to the CLIP_OTW pin asserts it until the 100% duty-cycle PWM signal is no longer present. All four channels connect to the same CLIP_OTW pin. Through I^2C, one can change the CLIP_OTW signal clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on this pin (see the *Tweeter Detection* section). The microcontroller in the system can monitor the signal at the CLIP_OTW pin, and may have a configuration that reduces the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD) and Thermal Foldback** — By default, the CLIP_OTW pin setting indicates an OTW. One can make changes via I^2C commands. If selected to indicate a temperature warning, CLIP_OTW pin assertion occurs when the die temperature reaches warning level 1 as shown in the electrical specifications. The OTW has three temperature thresholds with a 10°C hysteresis. I^2C register 0x04 indicates each threshold in bits 5, 6, and 7. The device still functions until the temperature reaches the OTSD threshold, at which time the outputs go into Hi-Z mode and the device asserts the FAULT pin. I^2C is still active in the event of an OTSD, and one can read the registers for faults, but all audio ceases abruptly. After the OTSD resets, one can turn the device back on through I^2C. The OTW indication remains until the temperature drops below warning level 1. The thermal foldback decreases the channel gain.
6. **Undervoltage (UV) and Power-on-Reset (POR)** — The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the device asserts the FAULT pin and updates the I^2C registerd, depending on which voltage caused the event. Power-on reset (POR) occurs when PVDD drops low enough. A POR event causes the I^2C to go into a high-impedance state. After the device recovers from the POR event, the device re-initialization occur via I^2C.

Feature Descption (continued)

7. **Overvoltage (OV) and Load Dump** — The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the device asserts the $\overline{\text{FAULT}}$ pin iand updates the I²C register. The device can withstand 50-V load-dump voltage spikes.

7.3.7 I²C Serial Communication Bus

The device communicates with the system processor via the I²C serial communication bus as an I²C slave-only device. The processor can poll the device via I²C to determine the operating status. All reports of fault conditions and detections are via I²C. There are also numerous features and operating conditions that one can set via I²C.

The I²C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.
- Select the AM non-interference switching frequency
- Select the functionality of the OTW_CLIP pin
- Enable or disable the dc-detect function with selectable threshold
- Place a channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set the detection threshold, and initiate the function
- Initiate the open- and shorted-load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I²C bus, the TAS5414C includes a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C_ADDR pin sets the device in master or slave mode and selects the I²C address for that device. Tie I2C_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D_BYP for slave 3. The OSC_SYNC pin is for synchronizing the internal clock oscillators, thereby avoid beat frequencies. One can apply an external oscillator to this pin for external control of the switching frequency.

Table 1. Table 7. I2C_ADDR Pin Connection

I2C_ADDR VALUE	I2C_ADDR PIN CONNECTION	I²C ADDRESSES
0 (OSC MASTER)	To SGND pin	0xD8/D9
1 (OSC SLAVE1)	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDA/DB
2 (OSC SLAVE2)	65% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)	0xDC/DD
3 (OSC SLAVE3)	To D_BYP pin	0xDE/DF

(1) TI recommends R_{I2C_ADDR} resistors with 5% or better tolerance.

7.3.8 I²C Bus Protocol

The TAS5414C has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface programs the registers of the device and reads device status.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The transfer of address and data is in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 12 shows these conditions. The master generates the 7-bit slave address and the read/write bit to open communication with another device and then wait for an acknowledge condition. The TAS5414C holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. There must be an external pullup resistor for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that one can transmit between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

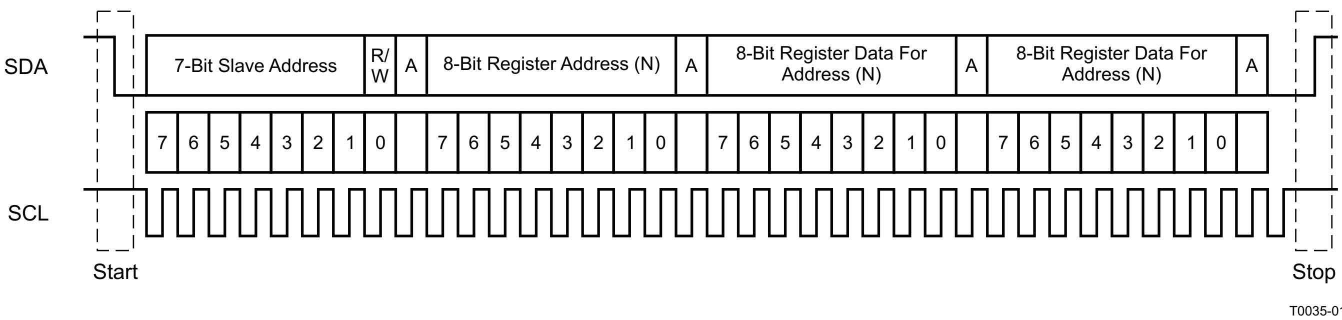


Figure 12. Typical I²C Sequence

Use the I2C_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I²C addresses and do not conflict with other licensed I²C audio devices. To communicate with the TAS5414C, the I²C master uses addresses shown in Figure 12. Transmission of read and write data can be via single-byte or multiple-byte data transfers.

7.3.9 Hardware Control Pins

There are four discrete hardware pins for real-time control and indication of device status.

1. $\overline{\text{FAULT}}$ pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the device to go into the Hi-Z mode or standby mode. On assertion of this pin, the device has protected itself and the system from potential damage. One can read the exact nature of the fault via I^2C with the exception of PVDD undervoltage faults below POR, in which case the I^2C bus is no longer operational. However, the fault is still indicated due to $\overline{\text{FAULT}}$ pin assertion.
2. $\overline{\text{CLIP\_OTW}}$ pin: Configured via I^2C, this active-low open-drain pin\ indicates one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. During tweeter detect diagnostics, assertion of this pin also occurs when a tweeter is present. If overtemperature warning is set, the device can also indicate thermal foldback on this pin.
3. $\overline{\text{MUTE}}$ pin: This active-low pin is used for hardware control of the mute-unmute function for all four channels. Capacitor C_{MUTE} controls the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, implementation of the mute function should be through I^2C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and TI does not recommended it except as an *emergency hard mute* function in case of a loss of I^2C control. Sharing the C_{MUTE} capacitor between multiple devices is disallowed.
4. $\overline{\text{STANDBY}}$ pin: On assertion of this active-low pin, the device goes into a complete shutdown, and the typical current-draw limit is 2 μA, typical. $\overline{\text{STANDBY}}$ can be used to shut down the device rapidly. If all channels are in Hi-Z, the device enters standby in approximately 1 ms. All I^2C register content is lost and the I^2C bus goes into the high-impedance state on assertion of the $\overline{\text{STANDBY}}$ pin.

7.3.10 AM Radio Avoidance

To reduce interference in the AM radio band, the device has the ability to change the switching frequency via I^2C commands. Table 2 lists the recommended frequencies. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to demodulation of the switching frequency by the AM radio.

Table 2. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
540–670	417	522–675	417
680–980	500	676–945	500
990–1180	417	946–1188	417
1190–1420	500	1189–1422	500
1430–1580	417	1423–1584	417
1590–1700	500	1585–1701	500

7.4 Device Functional Modes

Table 3 through Table 5 depict the operating modes and faults.

Table 3. Operating Modes

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	I^{2}C	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	Active	ON
Mute	Switching at 50%	Active	Active	Active	ON
Normal operation	Switching with audio	Active	Active	Active	ON

Table 4. Global Faults and Actions

FAULT OR EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
POR	Voltage fault	All	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Self-clearing
UV		Hi-Z, mute, normal	I^{2}C + $\overline{\text{FAULT}}$ pin		Hi-Z	Latched
CP UV						
OV						
Load dump		All	$\overline{\text{FAULT}}$ pin		Standby	Self-clearing
OTW	Thermal warning	Hi-Z, mute, normal	I^{2}C + $\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
OTSD	Thermal fault	Hi-Z, mute, normal	I^{2}C + $\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Latched

Table 5. Channel Faults and Actions

FAULT/ EVENT	FAULT OR EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED OR SELF-CLEARING
Open-short diagnostic	Diagnostic	Hi-Z (I^{2}C activated)	I^{2}C	None	None	Latched
Clipping	Warning	Mute / Play	$\overline{\text{CLIP\_OTW}}$ pin	None	None	Self-clearing
CBC load current limit	Online protection			Current Limit	Start OC timer	Self-clearing
OC fault	Output channel fault		I^{2}C + $\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	Latched
DC detect				Hard mute	Hi-Z	Latched
OT Foldback	Warning		I^{2}C + $\overline{\text{CLIP\_OTW}}$ pin	Reduce Gain	None	Self-clearing

7.4.1 Audio Shutdown and Restart Sequence

The gain ramp of the filtered output signal and the updating of the I^2C registers correspond to the MUTE pin voltage during the ramping process. The value of the external capacitor on the MUTE pin dictates the length of time that the MUTE pin takes to complete its ramp. With the default 220-nF capacitor, the turnon common-mode ramp takes approximately 26 ms and the gain ramp takes approximately 76 ms.

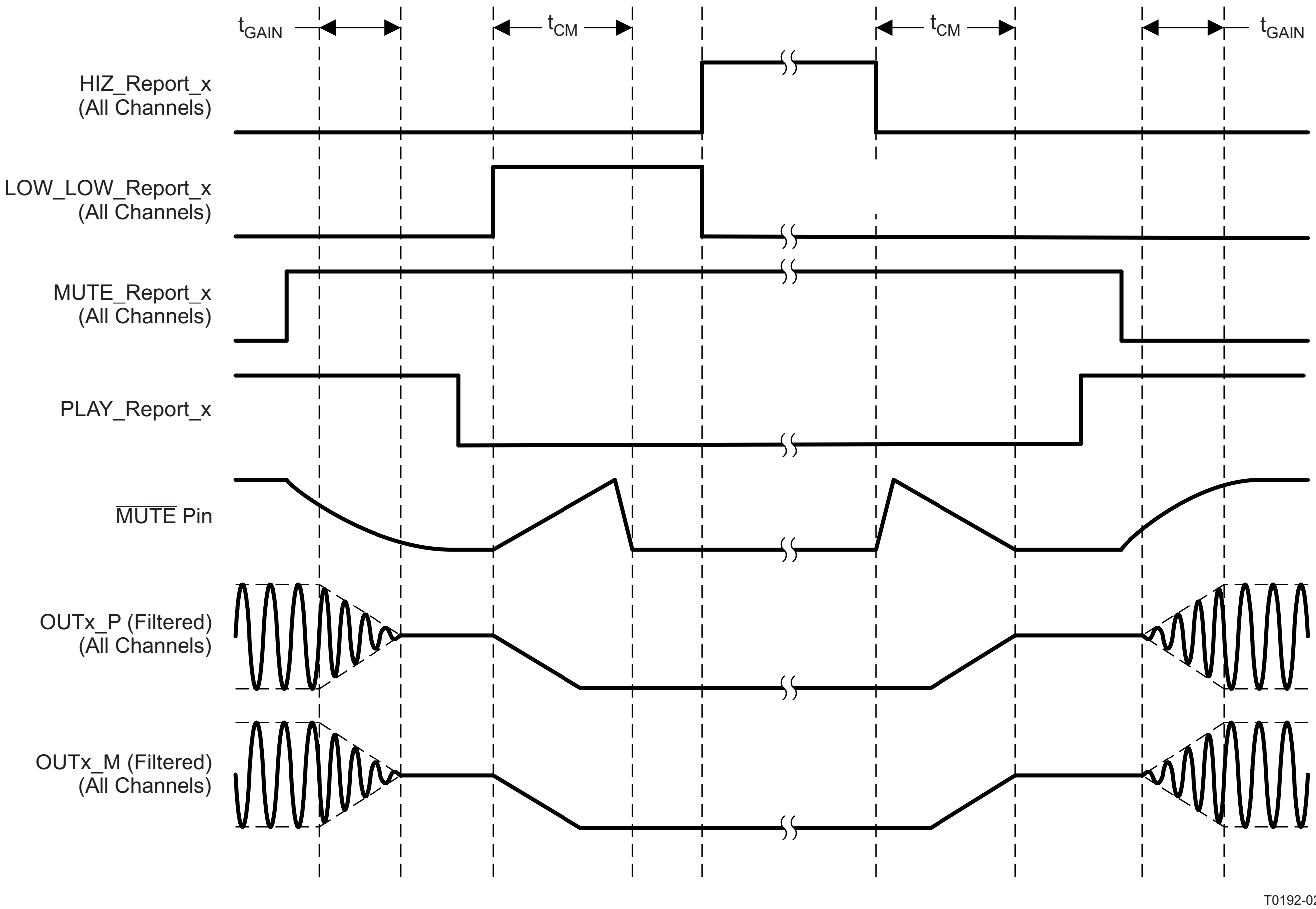


Figure 13. Timing Diagram for Click- and Pop-Free Shutdown and Restart Sequence

7.4.2 Latched-Fault Shutdown and Restart Sequence Control

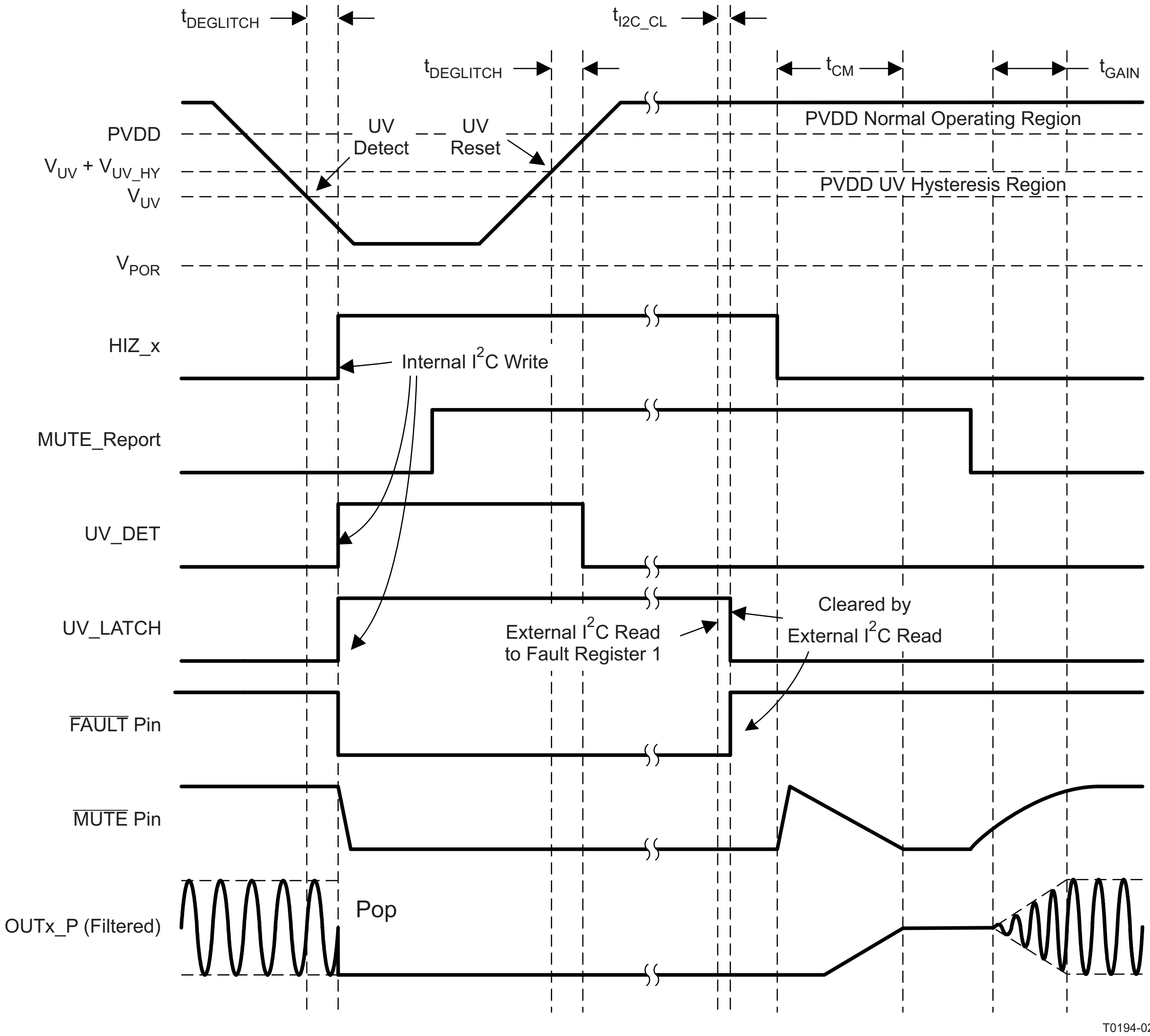


Figure 14. Timing Diagram for Latched-Global-Fault Shutdown and Restart (UV Shutdown and Recovery)

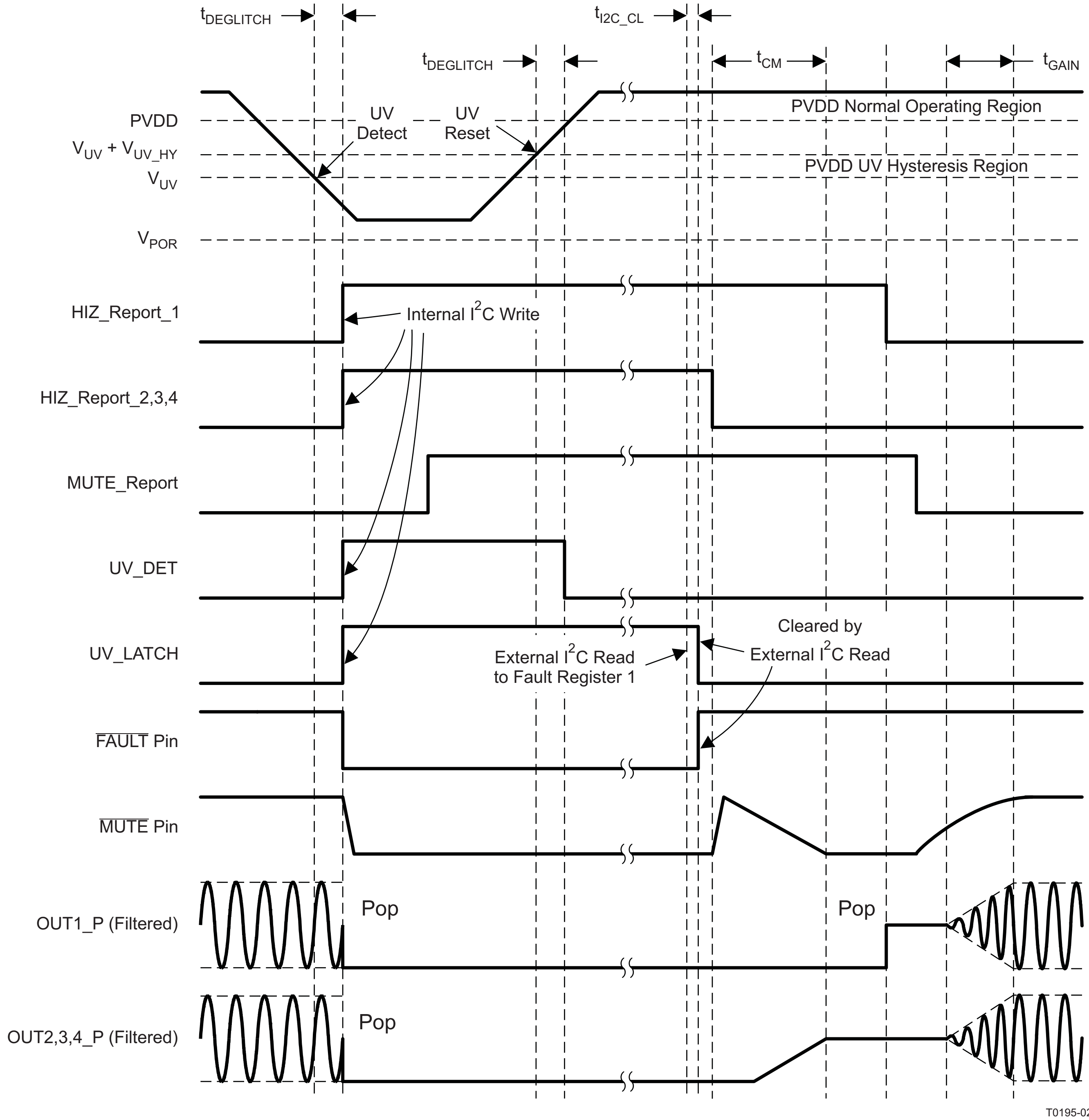


Figure 15. Timing Diagram for Latched-Global-Fault Shutdown and Individual-Channel Restart (UV Shutdown and Recovery)

7.5 Programming

7.5.1 Random Write

As shown in Figure 16, a random write or single-byte write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a single-byte write data transfer, the read/write bit is a 0. After receiving the correct I^{2}C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5414C again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte write transfer.

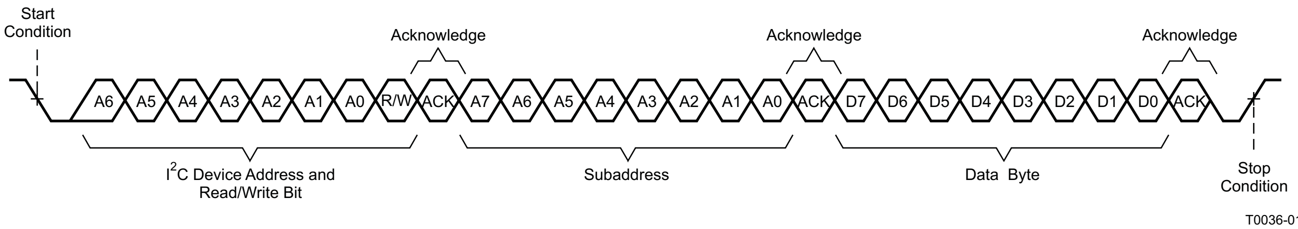


Figure 16. Random-Write Transfer

7.5.2 Sequential Write

A sequential write transfer is identical to a single-byte data-write transfer except for the transmisson of multiple data bytes by the master device to TAS5414C as shown in Figure 17. After receiving each data byte, the device responds with an acknowledge bit and automatically increments the I^{2}C subaddress by one.

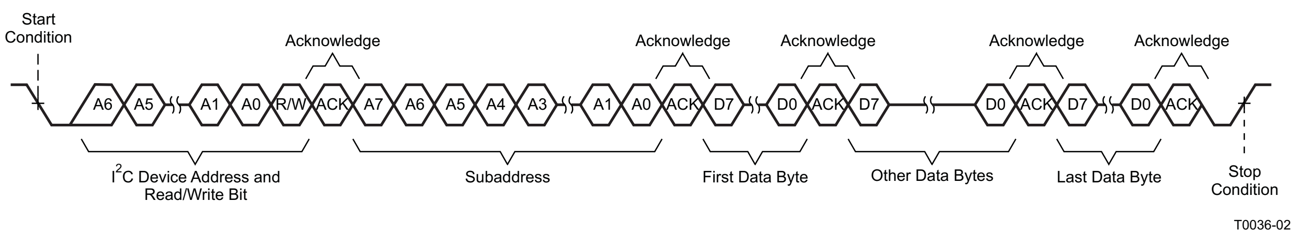


Figure 17. Sequential Write Transfer

Programming (continued)

7.5.3 Random Read

As shown in Figure 18, a random read or single-byte read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. For the single-byte read transfer, the master device transmits both a write followed by a read. Initially, a write transfers the address byte or bytes of the internal memory address to be read. Thus, the read/write bit is a 0. After receiving the address and the read/write bit, the TAS5414C responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the device address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the TAS5414C transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte read transfer.

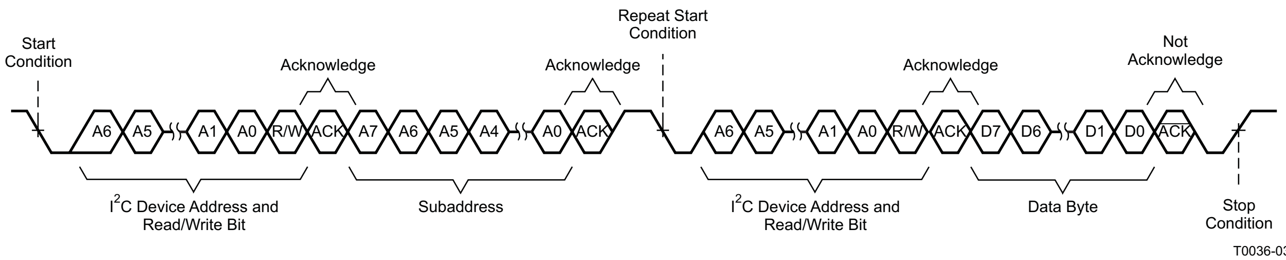


Figure 18. Random Read Transfer

7.5.4 Sequential Read

A sequential read transfer is identical to a single-byte read transfer except for the transmission of multiple data bytes by the TAS5414C to the master device as shown in Figure 19. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^{2}C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

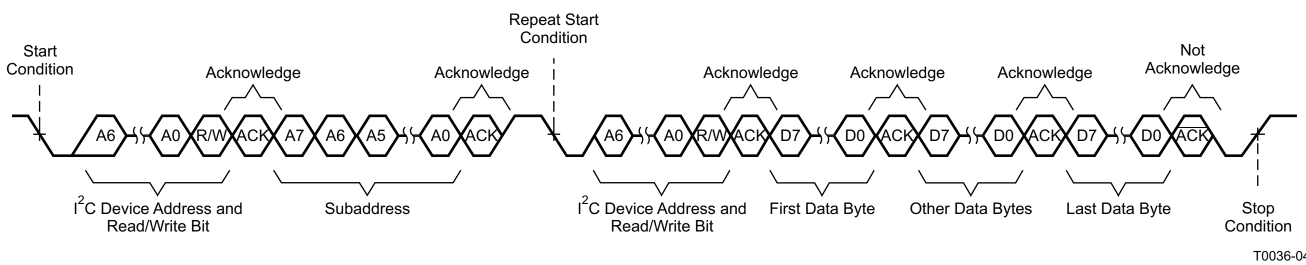


Figure 19. Sequential Read Transfer

7.6 Register Maps

7.6.1 Register Summary

Table 6. TAS5414C I^2C Addresses

I2C_ADDR VALUE		FIXED ADDRESS					SELECTABLE WITH ADDRESS PIN		READ/WRITE BIT	I^2C ADDRESS
		MSB	6	5	4	3	2	1	LSB	
0 (OSC MASTER)	I^2C WRITE	1	1	0	1	1	0	0	0	0xD8
	I^2C READ	1	1	0	1	1	0	0	1	0xD9
1 (OSC SLAVE1)	I^2C WRITE	1	1	0	1	1	0	1	0	0xDA
	I^2C READ	1	1	0	1	1	0	1	1	0xDB
2 (OSC SLAVE2)	I^2C WRITE	1	1	0	1	1	1	0	0	0xDC
	I^2C READ	1	1	0	1	1	1	0	1	0xDD
3 (OSC SLAVE3)	I^2C WRITE	1	1	0	1	1	1	1	0	0xDE
	I^2C READ	1	1	0	1	1	1	1	1	0xDF

Table 7. I^2C Address Register Definitions

ADDRESS	TYPE	REGISTER DESCRIPTION
0x00	Read	Latched fault register 1, global and channel fault
0x01	Read	Latched fault register 2, dc offset and overcurrent detect
0x02	Read	Latched diagnostic register 1, load diagnostics
0x03	Read	Latched diagnostic register 2, load diagnostics
0x04	Read	External status register 1, temperature and voltage detect
0x05	Read	External status register 2, Hi-Z and low-low state
0x06	Read	External status register 3, mute and play modes
0x07	Read	External status register 4, load diagnostics
0x08	Read, Write	External control register 1, channel gain select
0x09	Read, Write	External control register 2, overcurrent control
0x0A	Read, Write	External control register 3, switching frequency and clip pin select
0x0B	Read, Write	External control register 4, load diagnostic, master mode select
0x0C	Read, Write	External control register 5, output state control
0x0D	Read, Write	External control register 6, output state control
0x0E, 0x0F	–	Not used
0x10	Read, Write	External control register 7, dc detect threshold selection
0x13	Read	External status register 5, overtemperature shutdown and thermal foldback

7.6.2 Registers

7.6.2.1 Fault Register 1 (0x00) Protection

Figure 20. Fault Register 1 (0x00) Protection

7	6	5	4	3	2	1	0
PVDD_OV	PVVD_UV	AVVD_UV	CP_UV	OTSD	OCSD	DC_OFF	OTW
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Fault Register 1 (0x00) Protection Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_OV	R	0	PVDD overvoltage has occurred.
6	PVVD_UV	R	0	PVDD undervoltage has occurred.

Table 8. Fault Register 1 (0x00) Protection Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	AVDD_UV	R	0	AVDD, analog voltage, undervoltage has occurred.
4	CP_UV	R	0	Charge-pump undervoltage has occurred.
3	OTSD	R	0	Overtemperature shutdown has occurred.
2	OCSD	R	0	Overcurrent shutdown has occurred in any channel.
1	DC_OFF	R	0	DC offset has occurred in any channel.
0	OTW	R	0	Overtemperature warning has occurred.

7.6.3 Fault Register 2 (0x01) Protection

Figure 21. Fault Register 2 (0x01) Protection

7	6	5	4	3	2	1	0
DC_OFF_CH4	DC_OFF_CH3	DC_OFF_CH2	DC_OFF_CH1	OCSD_CH4	OCSD_CH3	OCSD_CH2	OCSD_CH1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Fault Register 2 (0x01) Protection Field Descriptions

Bit	Field	Type	Reset	Description
7	DC_OFF_CH4	R	0	DC offset channel 4 has occurred.
6	DC_OFF_CH3	R	0	DC offset channel 3 has occurred.
5	DC_OFF_CH2	R	0	DC offset channel 2 has occurred.
4	DC_OFF_CH1	R	0	DC offset channel 1 has occurred.
3	OCSD_CH4	R	0	Overcurrent shutdown channel 4 has occurred.
2	OCSD_CH3	R	0	Overcurrent shutdown channel 3 has occurred.
1	OCSD_CH2	R	0	Overcurrent shutdown channel 2 has occurred.
0	OCSD_CH1	R	0	Overcurrent shutdown channel 1 has occurred.

7.6.4 Diagnostic Register 1 (0x02) Load Diagnostics

Figure 22. Diagnostic Register 1 (0x02) Load Diagnostics

7	6	5	4	3	2	1	0
OL_CH2	SL_CH2	S2P_CH2	S2G_CH2	OL_CH1	SL_CH1	S2P_CH1	S2G_CH1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Diagnostic Register 1 (0x02) Load Diagnostics Field Descriptions

Bit	Field	Type	Reset	Description
7	OL_CH2	R	0	Open load channel 2 has occurred.
6	SL_CH2	R	0	Shorted load channel 2 has occurred.
5	S2P_CH2	R	0	Output short to PVDD channel 2 has occurred.
4	S2G_CH2	R	0	Output short to ground channel 2 has occurred.
3	OL_CH1	R	0	Open load channel 1 has occurred.
2	SL_CH1	R	0	Shorted load channel 1 has occurred.
1	S2P_CH1	R	0	Output short to PVDD channel 1 has occurred.
0	S2G_CH1	R	0	Output short to ground channel 1 has occurred.

7.6.5 Diagnostic Register 2 (0x03) Load Diagnostics

Figure 23. Diagnostic Register 2 (0x03) Load Diagnostics

7	6	5	4	3	2	1	0
OL_CH4	SL_CH4	S2P_CH4	S2G_CH4	OL_CH3	SL_CH3	S2P_CH3	S2G_CH3
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Diagnostic Register 2 (0x03) Load Diagnostics Field Descriptions

Bit	Field	Type	Reset	Description
7	OL_CH4	R	0	Open load channel 4 has occurred.
6	SL_CH4	R	0	Shorted load channel 4 has occurred.
5	S2P_CH4	R	0	Output short to PVDD channel 4 has occurred.
4	S2G_CH4	R	0	Output short to ground channel 4 has occurred.
3	OL_CH3	R	0	Open load channel 3 has occurred.
2	SL_CH3	R	0	Shorted load channel 3 has occurred.
1	S2P_CH3	R	0	Output short to PVDD channel 3 has occurred.
0	S2G_CH3	R	0	Output short to ground channel 3 has occurred.

7.6.6 External Status Register 1 (0x04) Fault Detection

Figure 24. External Status Register 1 (0x04) Fault Detection

7	6	5	4	3	2	1	0
OTW_LEVEL			OTSD_ST	CPUV_ST	AVDD_UV_ST	PVDD_UV_ST	PVDD_OV_ST
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. External Status Register 1 (0x04) Fault Detection Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OTW_LEVEL	R	000	Overtemperature warning: 000: Default value 001: Overtemperature warning 011: Overtemperature warning 1 101: Overtemperature warning 2 111: Overtemperature warning 3
4	OTSD_ST	R	0	Overtemperature shutdown is present.
3	CPUV_ST	R	0	Charge-pump voltage fault is present.
2	AVDD_UV_ST	R	0	AVDD, analog voltage fault is present.
1	PVDD_UV_ST	R	0	PVDD undervoltage fault is present.
0	PVDD_OV_ST	R	0	PVDD overvoltage fault is present.

7.6.7 External Status Register 2 (0x05) Output State of Individual Channels

Figure 25. External Status Register 2 (0x05) Output State of Individual Channels

7	6	5	4	3	2	1	0
CH4_LL_ST	CH3_LL_ST	CH2_LL_ST	CH1_LL_ST	CH4_HIZ_ST	CH3_HIZ_ST	CH2_HIZ_ST	CH1_HIZ_ST
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. External Status Register 2 (0x05) Output State of Individual Channels Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_LL_ST	R	0	Channel 4 low-low mode (0 = not low-low, 1 = low-low)(1)
6	CH3_LL_ST	R	0	Channel 3 low-low mode (0 = not low-low, 1 = low-low)(1)

Table 13. External Status Register 2 (0x05) Output State of Individual Channels Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH2_LL_ST	R	0	Channel 2 low-low mode (0 = not low-low, 1 = low-low)(1)
4	CH1_LL_ST	R	0	Channel 1 low-low mode (0 = not low-low, 1 = low-low)(1)
3	CH4_HIZ_ST	R	1	Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
2	CH3_HIZ_ST	R	1	Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
1	CH2_HIZ_ST	R	1	Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)
0	CH1_HIZ_ST	R	1	Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)

(1) *Low-low* is defined as both outputs actively pulled to ground.

7.6.8 External Status Register 3 (0x06) Play and Mute Modes

Figure 26. External Status Register 3 (0x06) Play and Mute Modes

7	6	5	4	3	2	1	0
CH4_MUTE_ST	CH3_MUTE_ST	CH2_MUTE_ST	CH1_MUTE_ST	CH4_PLAY_ST	CH3_PLAY_ST	CH2_PLAY_ST	CH1_PLAY_ST
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. External Status Register 3 (0x06) Play and Mute Modes Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_MUTE_ST	R	0	Channel 4 mute mode is enabled.
6	CH3_MUTE_ST	R	0	Channel 3 mute mode is enabled.
5	CH2_MUTE_ST	R	0	Channel 2 mute mode is enabled.
4	CH1_MUTE_ST	R	0	Channel 1 mute mode is enabled.
3	CH4_PLAY_ST	R	0	Channel 4 play mode is enabled.
2	CH3_PLAY_ST	R	0	Channel 3 play mode is enabled.
1	CH2_PLAY_ST	R	0	Channel 2 play mode is enabled.
0	CH1_PLAY_ST	R	0	Channel 1 play mode is enabled.

7.6.9 External Status Register 4 (0x07) Load Diagnostics

Figure 27. External Status Register 4 (0x07) Load Diagnostics

7	6	5	4	3	2	1	0
CH4_OTFB	CH3_OTFB	CH2_OTFB	CH1_OTFB	CH4_LD_MODE	CH3_LD_MODE	CH2_LD_MODE	CH1_LD_MODE
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. External Status Register 4 (0x07) Load Diagnostics Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_OTFB	R	0	Channel 4 is in overtemperature foldback.
6	CH3_OTFB	R	0	Channel 3 is in overtemperature foldback.
5	CH2_OTFB	R	0	Channel 2 is in overtemperature foldback.
4	CH1_OTFB	R	0	Channel 1 is in overtemperature foldback.
3	CH4_LD_MODE	R	0	Channel 4 is in load diagnostics mode.
2	CH3_LD_MODE	R	0	Channel 3is in load diagnostics mode.
1	CH2_LD_MODE	R	0	Channel 2 is in load diagnostics mode.
0	CH1_LD_MODE	R	0	Channel 1 is in load diagnostics mode.

7.6.10 External Control Register 1 (0x08) Gain Select

Figure 28. External Control Register 1 (0x08) Gain Select

7	6	5	4	3	2	1	0
GAIN_CH4		GAIN_CH3		GAIN_CH2		GAIN_CH1	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. External Control Register 1 (0x08) Gain Select Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GAIN_CH4	R/W	10	Set channel 4 gain. 10: Set channel 4 gain to 26 dB (Default) 00: Set channel 4 gain to 12 dB 01: Set channel 4 gain to 20 dB 11: Set channel 4 gain to 32 dB
5-4	GAIN_CH3	R/W	10	Set channel 3 gain. 10: Set channel 3 gain to 26 dB (Default) 00: Set channel 3 gain to 12 dB 01: Set channel 3 gain to 20 dB 11: Set channel 3 gain to 32 dB
3-2	GAIN_CH2	R/W	10	Set channel 2 gain. 10: Set channel 2 gain to 26 dB (Default) 00: Set channel 2 gain to 12 dB 01: Set channel 2 gain to 20 dB 11: Set channel 2 gain to 32 dB
1-0	GAIN_CH1	R/W	10	Set channel 1 gain. 10: Set channel 1 gain to 26 dB (Default) 00: Set channel 1 gain to 12 dB 01: Set channel 1 gain to 20 dB 11: Set channel 1 gain to 32 dB

7.6.11 External Control Register 2 (0x09) Overcurrent Control

Figure 29. External Control Register 2 (0x09) Overcurrent Control

7	6	5	4	3	2	1	0
CH4_OC	CH4_OC	CH4_OC	CH4_OC	RESERVED			THFB_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. External Control Register 2 (0x09) Overcurrent Control Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_OC	R/W	1	Set channel 4 overcurrent limit (0 - level 1, 1 - level 2)
6	CH3_OC	R/W	1	Set channel 3 overcurrent limit (0 - level 1, 1 - level 2)
5	CH2_OC	R/W	1	Set channel 2 overcurrent limit (0 - level 1, 1 - level 2)
4	CH1_OC	R/W	1	Set channel 1 overcurrent limit (0 - level 1, 1 - level 2)
3-1	Reserved	R/W	0	Reserved
0	THFB_DIS	R/W	0	Disable thermal foldback

7.6.12 External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration

Figure 30. External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration

7	6	5	4	3	2	1	0
CLIP_OTW_THFB	SYNC_PULSE	PHASE	HARD_STOP	CLIP_OTW_CONF		PWM_FREQ	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. External Control Register 3 (0x0A) Switching Frequency Select and Clip_OTW Configuration Field Descriptions

Bit	Field	Type	Reset	Description
7	CLIP-OTW_THFB	R/W	0	Configure $\overline{\text{CLIP\_OTW}}$ pin to report thermal foldback
6	SYNC_PULSE	R/W	0	Send sync pulse from OSC_SYNC pin (device must be in master mode).
5	PHASE	R/W	0	Set f_S to a 180° phase difference between adjacent channels.
4	HARD_STOP	R/W	0	Enable hard-stop mode.
3-2	CLIP_OTW_CONF	R/W	11	Configure $\overline{\text{CLIP\_OTW}}$ pin. 11: CLIP_OTW pin does not report thermal foldback (Default) 00: Configure $\overline{\text{CLIP\_OTW}}$ pin to report tweeter detect only. 01: Configure $\overline{\text{CLIP\_OTW}}$ pin to report clip detect only. 10: Configure $\overline{\text{CLIP\_OTW}}$ pin to report overtemperature warning only.
1-0	PWM_FREQ	R/W	01	Set f_S. 01: Set f_S = 417 kHz (Default) 00: Set f_S = 500 kHz 10: Set f_S = 357 kHz 11: Invalid frequency selection (do not set)

7.6.13 External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

Figure 31. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control

7	6	5	4	3	2	1	0
EN_CLK_OSC_SYNC	EN_SLAVE	EN_TW_DET	DIS_DC_DET	EN_CH4_LD	EN_CH3_LD	EN_CH2_LD	EN_CH1_LD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. (External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_CLK_OSC_SYNC	R/W	0	Enable clock output on OSC_SYNC pin (valid only in master mode)
6	EN_SLAVE	R/W	1	Enable slave mode (external oscillator is necessary)
5	EN_TW_DET	R/W	0	Enable tweeter-detect mode
4	DIS_DC_DET	R/W	1	Disable dc detection on all channels
3	EN_CH4_LD	R/W	0	Run channel 4 load diagnostics
2	EN_CH3_LD	R/W	0	Run channel 3 load diagnostics
1	EN_CH2_LD	R/W	0	Run channel 2 load diagnostics
0	EN_CH1_LD	R/W	0	Run channel 1 load diagnostics

7.6.14 External Control Register 5 (0x0C) Output Control

Figure 32. External Control Register 5 (0x0C) Output Control

7	6	5	4	3	2	1	0
RST	Reserved	DC_DET_SD_DIS	HIZ_TO_PLAY	CH4_MUTE	CH3_MUTE	CH2_MUTE	CH1_MUTE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. External Control Register 5 (0x0C) Output Control Field Descriptions

Bit	Field	Type	Reset	Description
7	RST	R/W	0	Reset device
6	Reserved	R/W	0	Reserved
5	DC_DET_SD_DIS	R/W	0	DC detect shutdown disabled, but still reports a fault
4	HIZ_TO_PLAY	R/W	1	Set non-Hi-Z channels to play mode, (unmute)
3	CH4_MUTE	R/W	1	Set channel 4 to mute mode, non-Hi-Z
2	CH3_MUTE	R/W	1	Set channel 3 to mute mode, non-Hi-Z
1	CH2_MUTE	R/W	1	Set channel 2 to mute mode, non-Hi-Z
0	CH1_MUTE	R/W	1	Set channel 1 to mute mode, non-Hi-Z

7.6.15 External Control Register 6 (0x0D) Output Control

Figure 33. External Control Register 6 (0x0D) Output Control

7	6	5	4	3	2	1	0
Reserved		PBTL_34	PBTL_12	CH4_LL	CH3_LL	CH2_LL	CH1_LL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. External Control Register 6 (0x0D) Output Control Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	0	Reserved
5	PBTL_34	R/W	0	Connect channel 3 and channel 4 for parallel BTL mode
4	PBTL_12	R/W	0	Connect channel 1 and channel 2 for parallel BTL mode
3	CH4_LL	R/W	0	Set channel 4 to low-low state
2	CH3_LL	R/W	0	Set channel 3 to low-low state
1	CH2_LL	R/W	0	Set channel 2 to low-low state
0	CH1_LL	R/W	0	Set channel 1 to low-low state

7.6.16 External Control Register 7 (0x10) Miscellaneous Selection

Figure 34. External Control Register 7 (0x10) Miscellaneous Selection

7	6	5	4	3	2	1	0
SLOWER_CM_RAMP	Reserved	SLOW_CM_RAMP	4X_LD	ADD_20MS	EN_XTALK_ENH	DC_DET_VAL	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. External Control Register 7 (0x10) Miscellaneous Selection

Bit	Field	Type	Reset	Description
7	SLOWER_CM_RAMP	R/W	0	Slower common-mode (CM) ramp-down from mute mode
6	Reserved	R/W	0	Reserved
5	SLOW_CM_RAMP	R/W	0	Slow common-mode ramp, increase the default time by 3x
4	4X_LD	R/W	0	Short-to-power (S2P) and short-to-ground (S2G) load-diagnostic phases take 4x longer

Table 22. External Control Register 7 (0x10) Miscellaneous Selection (continued)

Bit	Field	Type	Reset	Description
3	ADD_20MS	R/W	0	Adds a 20-ms delay between load diagnostic phases
2	EN_XTALK_ENH	R/W	0	Enable crosstalk enhancement
1-0	DC_DET_VAL	R/W	01	Set DC detect value 01: Default DC detect value (1.6 V, Default) 01: Minimum DC detect value (0.8 V) 10: Maximum DC detect value (2.4 V)

7.6.17 External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

Figure 35. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status

7	6	5	4	3	2	1	0
CH4_OTSD_ST	CH3_OTSD_ST	CH2_OTSD_ST	CH1_OTSD_ST	CH4_THFB_ST	CH3_THFB_ST	CH2_THFB_ST	CH1_THFB_ST
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. External Status Register 5 (0x13) Overtemperature and Thermal Foldback Status Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_OTSD_ST	R	0	Channel 4 in overtemperature shutdown
6	CH3_OTSD_ST	R	0	Channel 3 in overtemperature shutdown
5	CH2_OTSD_ST	R	0	Channel 2 in overtemperature shutdown
4	CH1_OTSD_ST	R	0	Channel 1 in overtemperature shutdown
3	CH4_THFB_ST	R	0	Channel 4 in thermal foldback
2	CH3_THFB_ST	R	0	Channel 3 in thermal foldback
1	CH2_THFB_ST	R	0	Channel 2 in thermal foldback
0	CH1_THFB_ST	R	0	Channel 1 in thermal foldback

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TAS5414C is a four-channel Class-D audio amplifier designed for use in head units and external amplifier modules. The device incorporates all the functionality needed to perform in the demanding OEM applications area.

8.2 Typical Application

Figure 36 shows a typical application circuit for the TAS5414C.

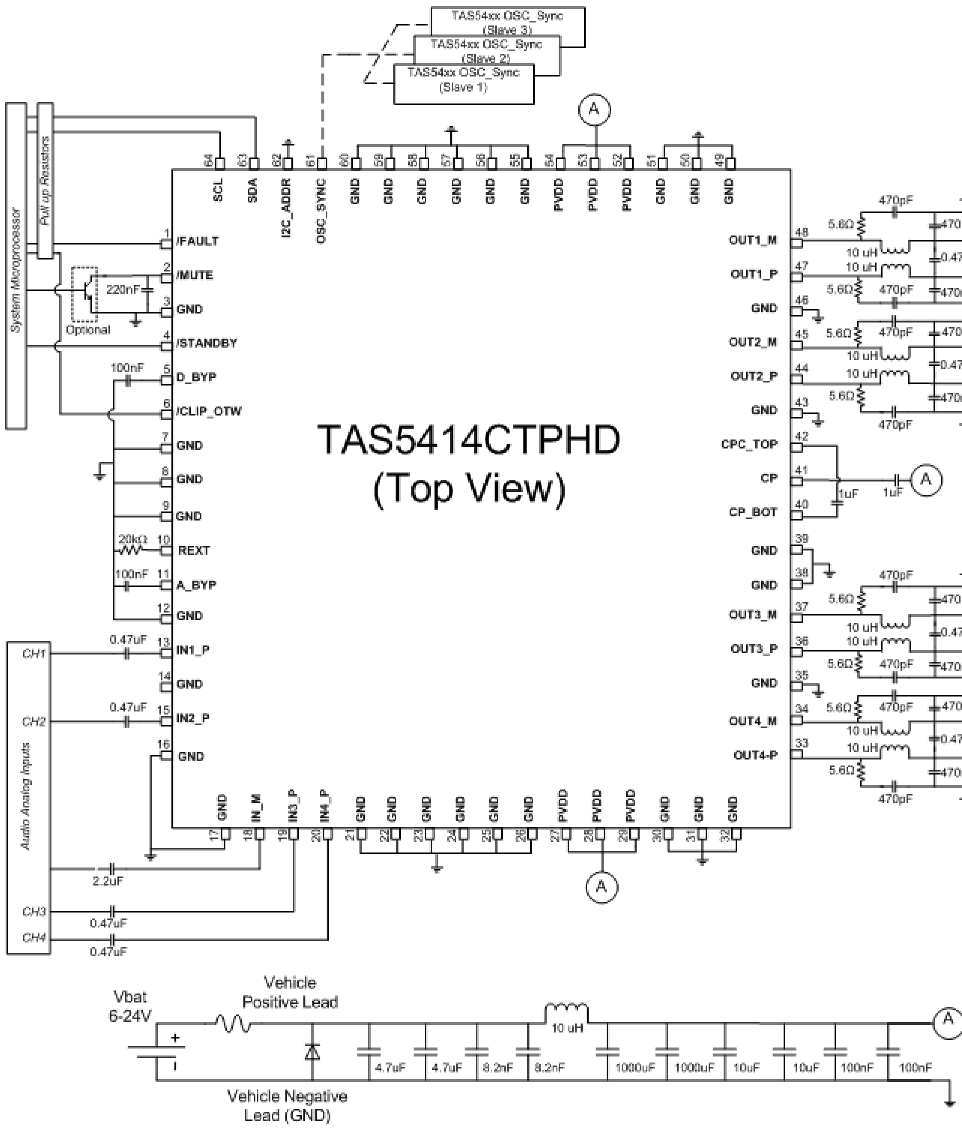


Figure 36. TAS5414C Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

- Power Supplies
  The device needs only a single power supply compliant with the recommended operation range. The device is designed to work with either a vehicle battery or regulated boost power supply.
- Communication
  The device communicates with the system controller with both discrete hardware control pins and with I^2C. The device is an I^2C slave and thus requires a master. If a master I^2C-compliant device is not present in the system, it is still possible to use the device, but only with the default settings. Diagnostic information is limited to the discrete reporting $\overline{\text{FAULT}}$ pin.
- External Components
  Table 24 lists the components required for the device.

Table 24. Supporting Components

EVM Designator	Quanity	Value	Size	Description	Use in Application
C37, C39, C48, C52	4	0.47µF ± 10%	1206	Film, 16-V	Analog audio input filter, bypass
C5, C6, C7, C8	4	330 µF ± 20%	10 mm	Low-ESR aluminum capacitor, 35-V	Power supply
C9, C10, C50, C51, C27, C28	6	1 µF ± 10%	0805	X7R ceramic capacitor, 50-V	Power supply
C53, C55	2	1uF ± 10%	0805	Film, 16-V	Analog audio input filter, bypass
C14, C23, C32, C43	4	470nF ± 10%	0805	X7R ceramic capacitor, 50-V	Amplifier output filtering
C11, C15, C20, C24, C29, C34, C40, C45	8	470 pF ± 10%	0603	X7R ceramic capacitor, 50-V	Amplifier output snubbers
C19, C33	2	0.1 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C4	1	2200 pF ± 10%	0603	X7R ceramic capacitor, 50-V	Power supply
C3	1	0.082 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C1, C2	2	4.7 µF ± 10%	1206	X7R ceramic capacitor, 25-V	Power supply
C12, C16, C21, C25, C30, C35, C41, C46	8	0.47 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Output EMI filtering
C18	1	220nF ± 10%	0603	X7R ceramic capacitor, 25-V	Mute timing
L1	1	10 µH ± 20%	13.5 mm ×13.5 mm	Shielded ferrite inductor	Power supply
L2, L3, L4, L5	4	10 µH ± 20%	12 mm × 14 mm	Dual inductor	Amplifier output filtering
R5, R6, R7	3	49.9 kΩ ± 1%	0805	Resistors, 0.125-W	Analog audio input filter
R8, R10, R12, R14, R17, R19, R26, R29	8	5.6 Ω ± 5%	0805	Resistors, 0.125-W	Output snubbers
R16	1	20.0 kΩ ± 1%	0805	Resistors, 0.125-W	Power supply

8.2.2 Detailed Design Procedure

8.2.2.1 Hardware and Software Design

- Step 1: Hardware Schematic Design: Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Step 2: Following the recommended layout guidelines, integrate the device and its supporting components into the system PCB file.
- Step 3: Thermal Design: The device has an exposed thermal pad which requires proper soldering. For more information, see the *Semiconductor and IC Package Thermal Metrics* , SPRA953, and the *PowerPAD Thermally Enhanced Package*, SLMA002G, application reports.
- Step 4: Develop software: The EVM User's Guide has detailed instructions for how to set up the device, interpret diagnostic information, and so forth. For information about control registers, see the *Table 7* section.
- For questions and support go to the E2E forums.

8.2.2.2 Parallel Operation (PBTL)

The device can drive more current by paralleling BTL channels on the load side of the LC output filter. Parallel operation requires identical I^2C settings for any two paralleled channels in order to have reliable system performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, and so on) should be sent to the paralleled channels at the same time. The device also supports load diagnostics for parallel connection. There is no support for paralleling on the device side of the LC output filter, which can result in device failure. When paralleling channels, use the parallel BTL I^2C control bits in register 0x0D. Parallel channels 1 and 2, and/or channels 3 and 4. Setting these bits allows the thermal foldback to react on both channels equally. Provide the audio input to channel 2 if paralleing channels 1 and 2, and channel 3 if paralleling channels 3 and 4.

8.2.2.3 Input Filter Design

For the TAS5414C device, the IN_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the four IN_P channels have a 1-µF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, then the IN_M channel should have a 4-µF capacitor in series with a 500-Ω resistor to GND (4 × 1 µF in parallel = 4 µF; 4 × 2 kΩ in parallel = 500 Ω).

8.2.2.4 Amplifier Output Filtering

The output FETs drive the amplifier outputs in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a low-pass filter to filter out the PWM modulation carrier frequency. People frequently call this filter the L-C filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole low-pass filter. The L-C filter attenuates the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which the load draws from the power supply. See the *Class-D LC Filter Design* application report, SLOA119 , for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

8.2.2.5 Line Driver Applications

In many audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The design is capable of supporting both applications; however, the one must design the output filter and system to handle the expected output load conditions.

8.2.3 Application Curves

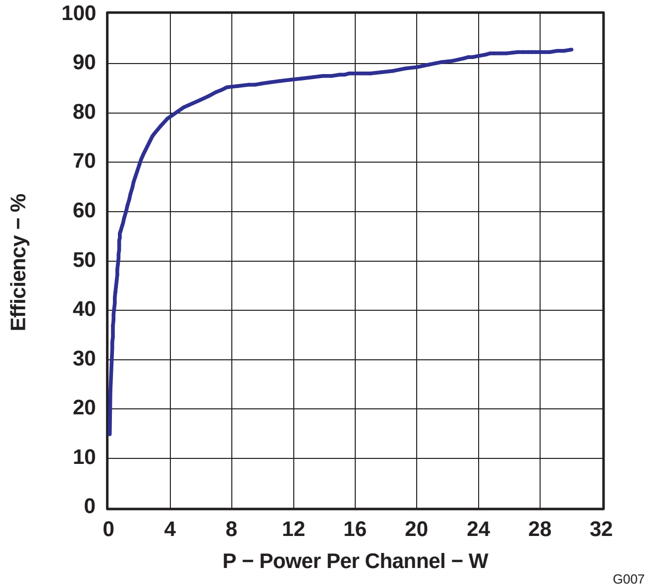


Figure 37. Efficiency
Four Channels AT 4 Ω Each

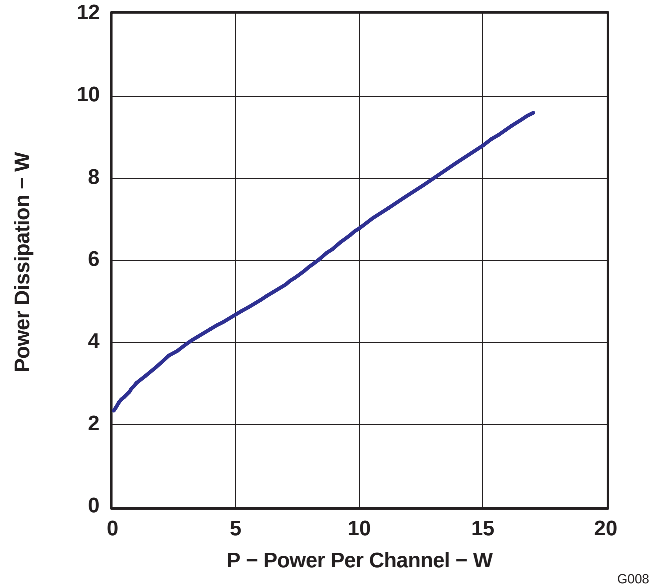


Figure 38. Device Power Dissipation
Four Channels at 4 Ω Each

9 Power Supply Recommendations

A car battery that can have a large voltage range most commonly provides the power for the device. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The supply for the high-side FET gate driver comes from a charge pump (CP). The charge pump supplies the gate-drive voltage for all four channels. AVDD, provided by an internal linear regulator powers the analog circuitry. This supply requires 0.1-µF, 10-V external bypass capacitor at the A_BYP pin. TI recommends not connecting any external components except the bypass capacitor to this pin. DVDD, which comes from an internal linear regulator, powers the digital circuitry. The D_BYP pin requires a 0.1-µF, 10-V external bypass capacitor. TI recommends not connecting any external components except the bypass capacitor to this pin.

The TAS5414C can withstand fortuitous open-ground and -power conditions. Fortuitous open ground usually occurs when a speaker wire shorts to ground, allowing for a second ground path through the body diode in the output FETs. The diagnostic capability allows debugging of the speakers and speaker wires, eliminating the need to remove the amplifier to diagnose the problem.

10 Layout

10.1 Layout Guidelines

- The EVM layout optimizes for low noise and EMC performance.
- The TAS5414C device has a thermal pad up, therefore a the layout must take into account an external heatsink.
- Layout also affects EMC performance.
- The EVM PCB illustrations form the basis for the layout discussions.

10.2 Layout Example

The areas indicated by the label "A", are critical to proper operation and EMC layout. The PVDD and ground decoupling capacitors should be close to the device. These decoupling capacitors must be on both groups of PVDD pins to ground. The ground connections of the snubber circuits must also be close to the grounds of the device. The grounds of the decoupling caps and the snubber circuits do not pass through vias before connecting to the device ground. This reduces the ground impedance for EMC mititgation.

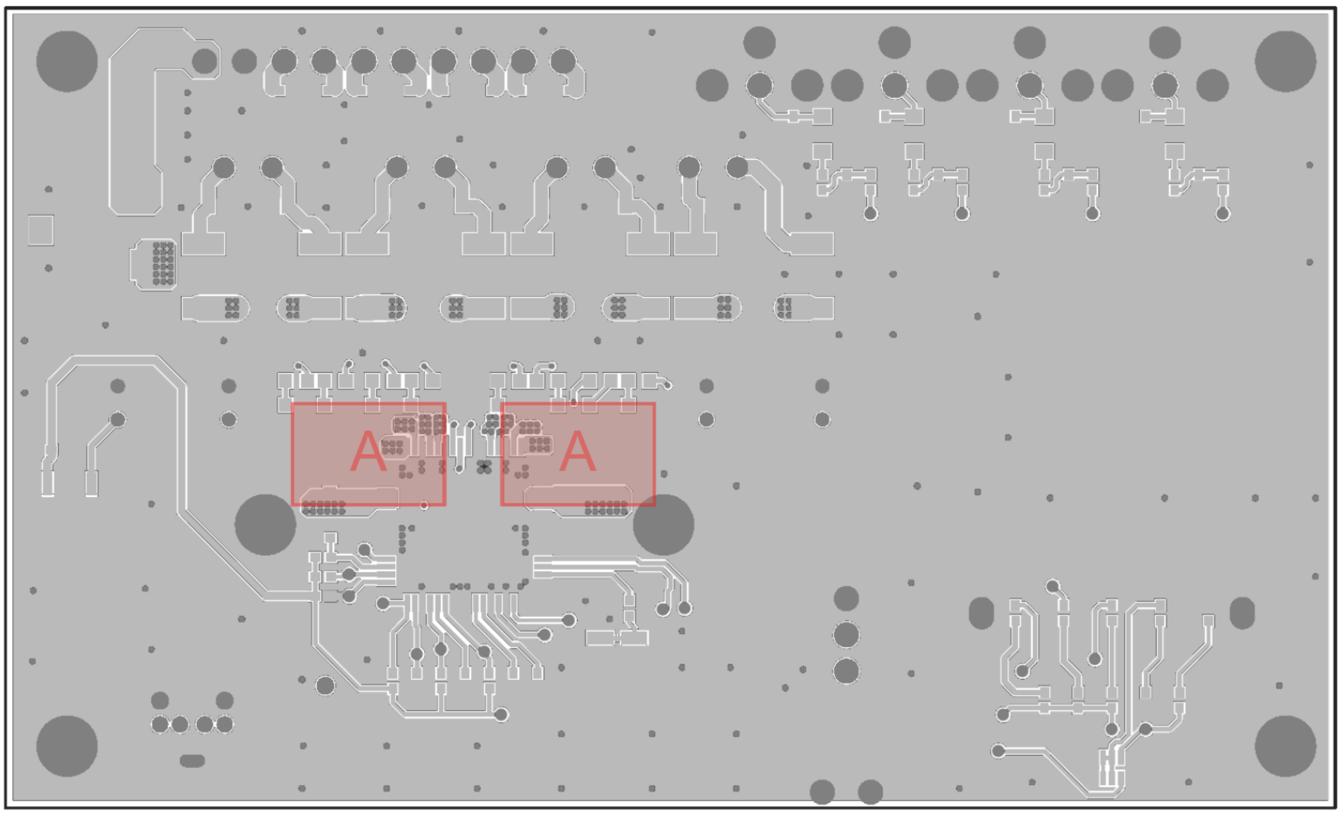


Figure 39. Top Layer

Layout Example (continued)

The area referenced as "B" are nets in the PCB layout that have large high frequency switching signals. These should be buried on an inner layer with ground planes on layers above and below to mitigate EMC.

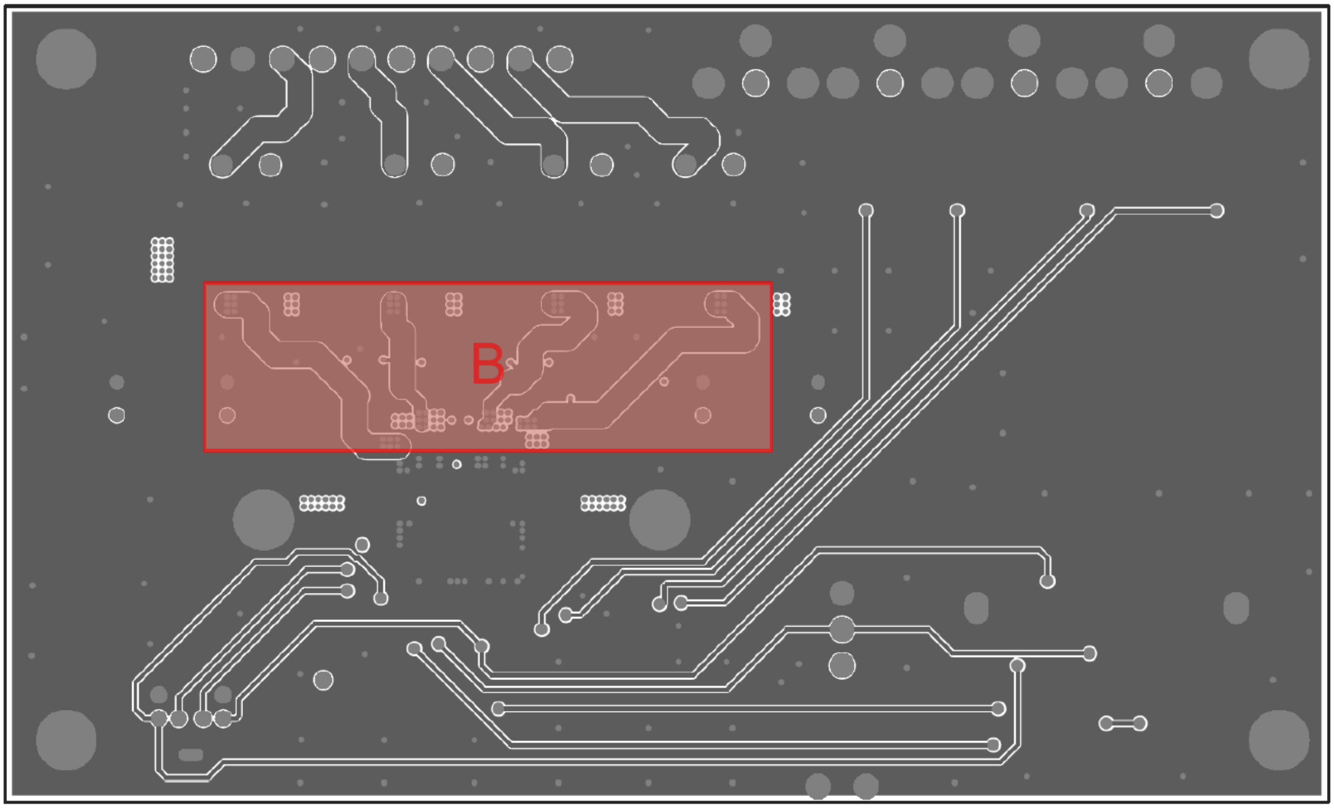


Figure 40. A Mid Layer

Layout Example (continued)

The bottom layer in the EVM is almost all ground plane. It can be seen that the other layers have ground planes that fill unused areas. All these ground planes need to be connected together through many vias to reduce the impedance between the ground layers. This allows for reduced EMI.

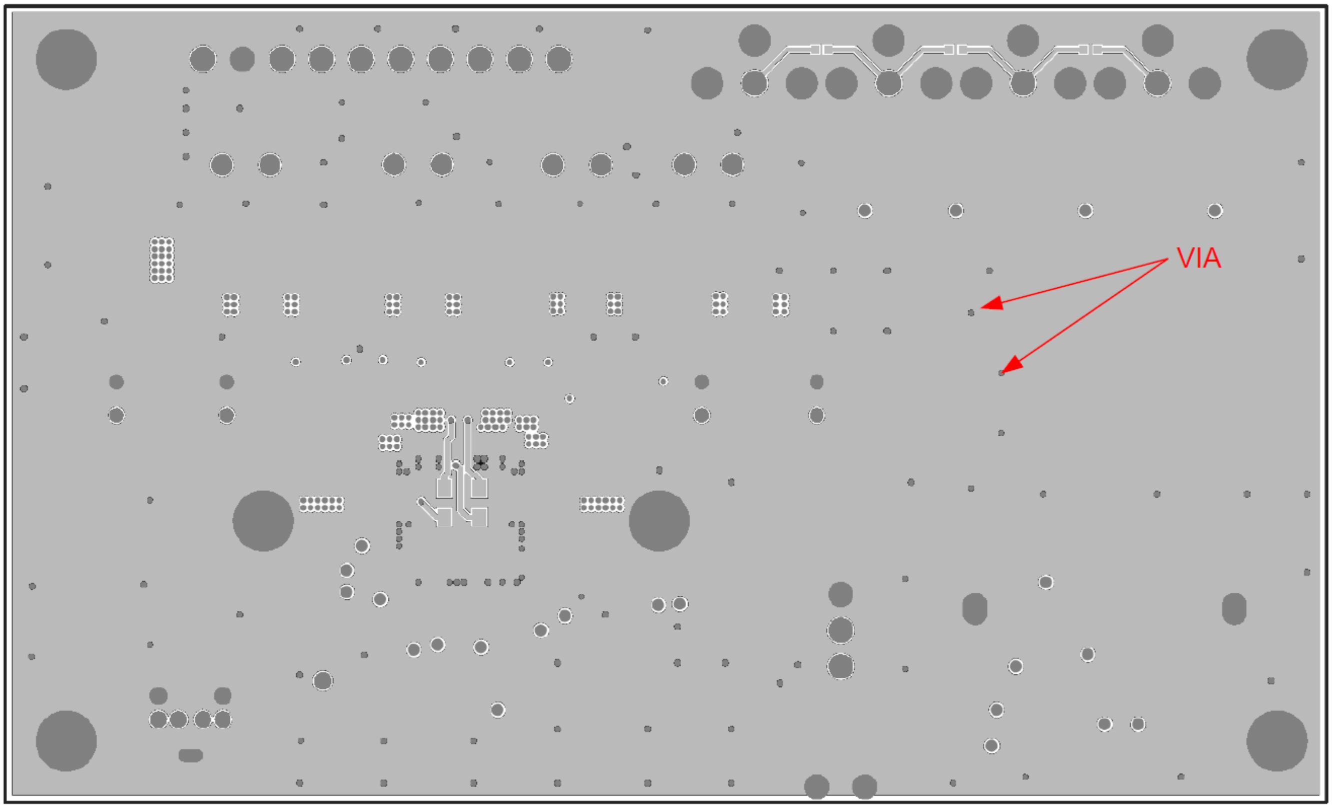


Figure 41. Bottom Layer

10.3 Thermal Consideration

The design of the thermally augmented package is for interface directly to heat sinks using a thermal interface compound (for example, Arctic Silver, Ceramique thermal compound). The heat sink then absorbs heat from the ICs and couples it to the local air. With proper thermal management this process can reach equilibrium at a lower temperature and heat can be continually removed from the ICs. Because of the device efficiency, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal resistance of the thermal grease
- Thermal resistance of the heat sink

One can calculate the thermal resistance of the thermal grease from the exposed heat slug area and the manufacturer's value for the area thermal resistance of the thermal grease (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size is as follows:

64-pin QFP 0.099 in^2 (64 mm^2)

Dividing the example area thermal resistance of the thermal grease by the area of the heat slug gives the actual resistance through the thermal grease:

64-pin QFP 0.07°C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal-grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. The heat-sink vendor generally predicts heat sink thermal resistance, either modeled using a continuous-flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal-grease resistance + heat-sink resistance.

Table 25 indicates modeled parameters for one device on a heat sink. The junction temperature setting is at 115°C while delivering 20 watts per channel into 4-Ω loads with no clipping. The assumed thickness of the thermal grease is about 0.001 inches (0.0254 mm).

Table 25. QFP Package Modeled Parameters

DEVICE	64-PIN QFP
Ambient temperature	25°C
Power to load	20 W × 4
Power dissipation	1.9 W × 4
ΔT inside package	7.6°C
ΔT through thermal grease	0.46°C
Required heatsink thermal resistance	10.78°C/W
Junction temperature	115°C
System $R_{\theta JA}$	11.85°C/W
$R_{\theta JA}$ × power dissipation	90°C

10.4 Electrical Connection of Heat Slug and Heat Sink

Electrically connect the heat sink attached to the heat slug of the device to GND, or leave it floating. Do not connect the heat slug to any other electrical node.

10.5 EMI Considerations

EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

EMI Considerations (接下页)

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The phase between channels is I^2C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5414CTPHD	ACTIVE	HTQFP	PHD	64	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS5414C	Samples
TAS5414CTPHDR	ACTIVE	HTQFP	PHD	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TAS5414C	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

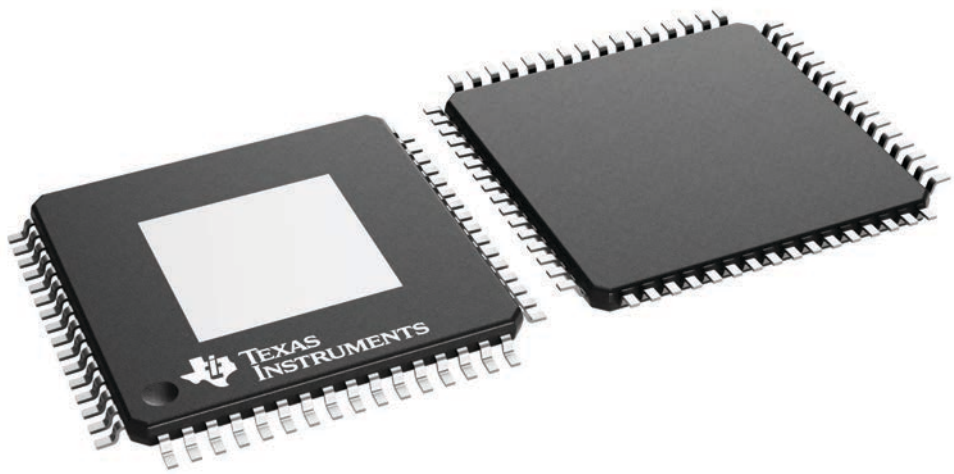
PHD 64

HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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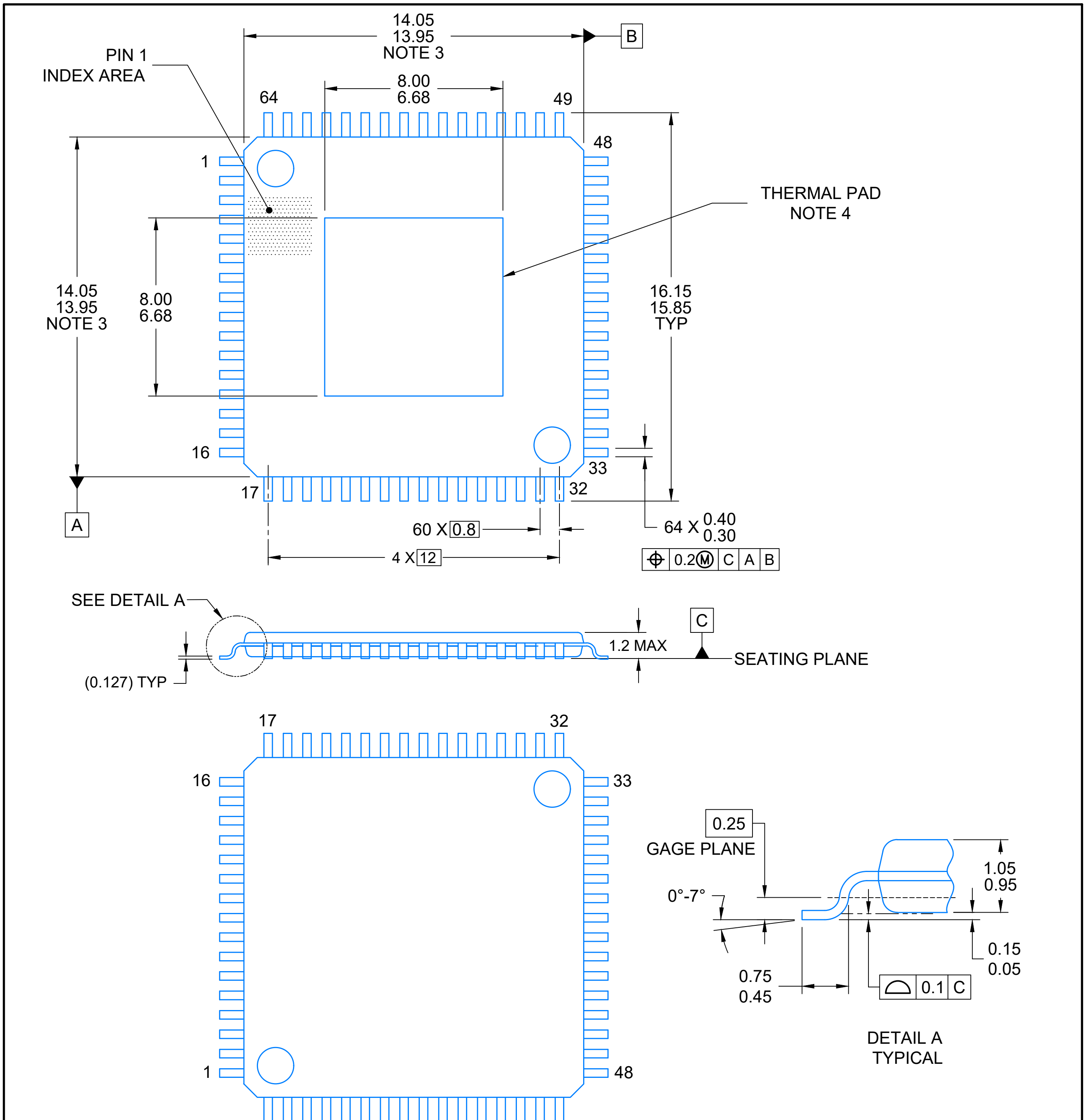
PLASTIC QUAD FLATPACK



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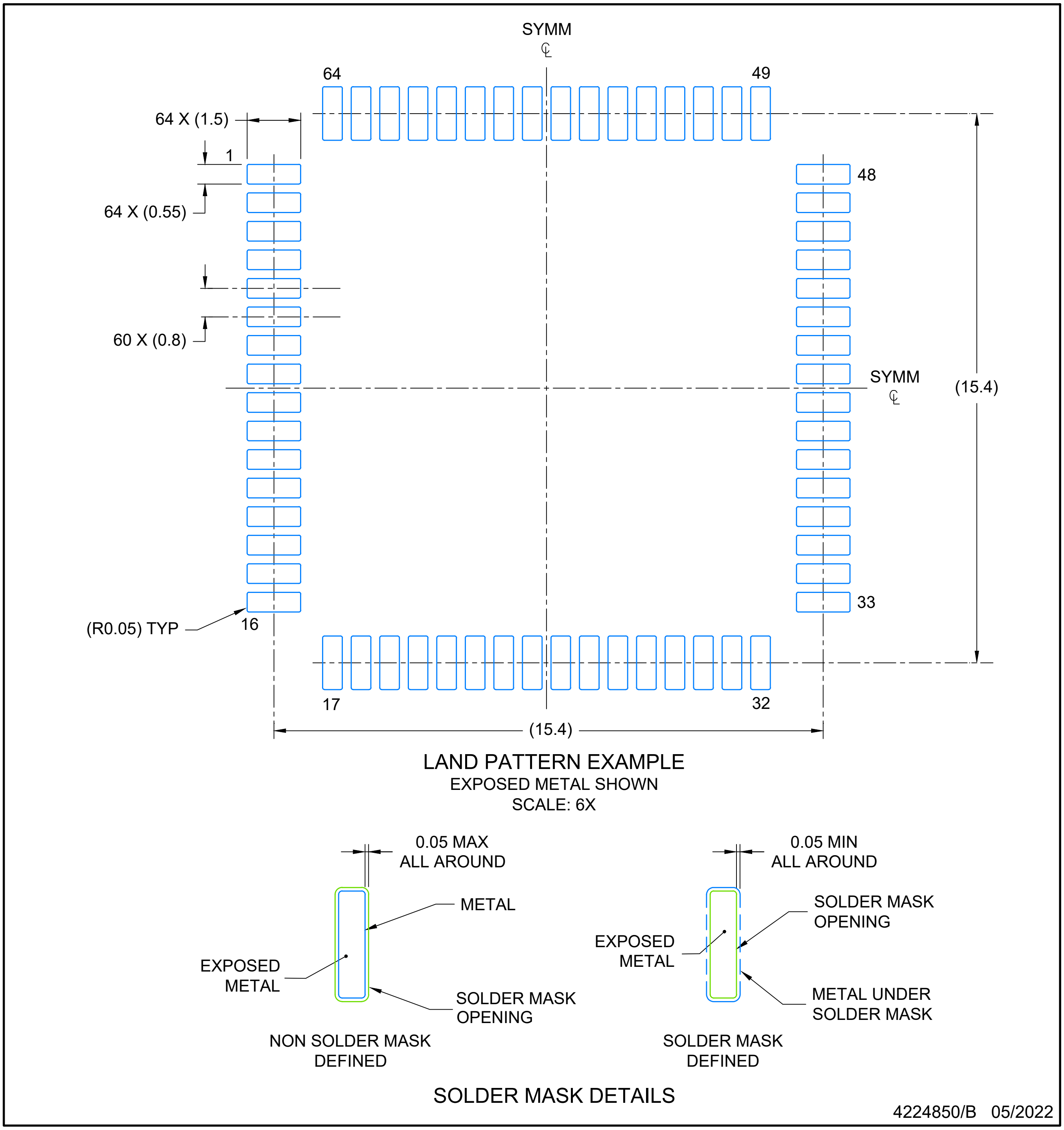
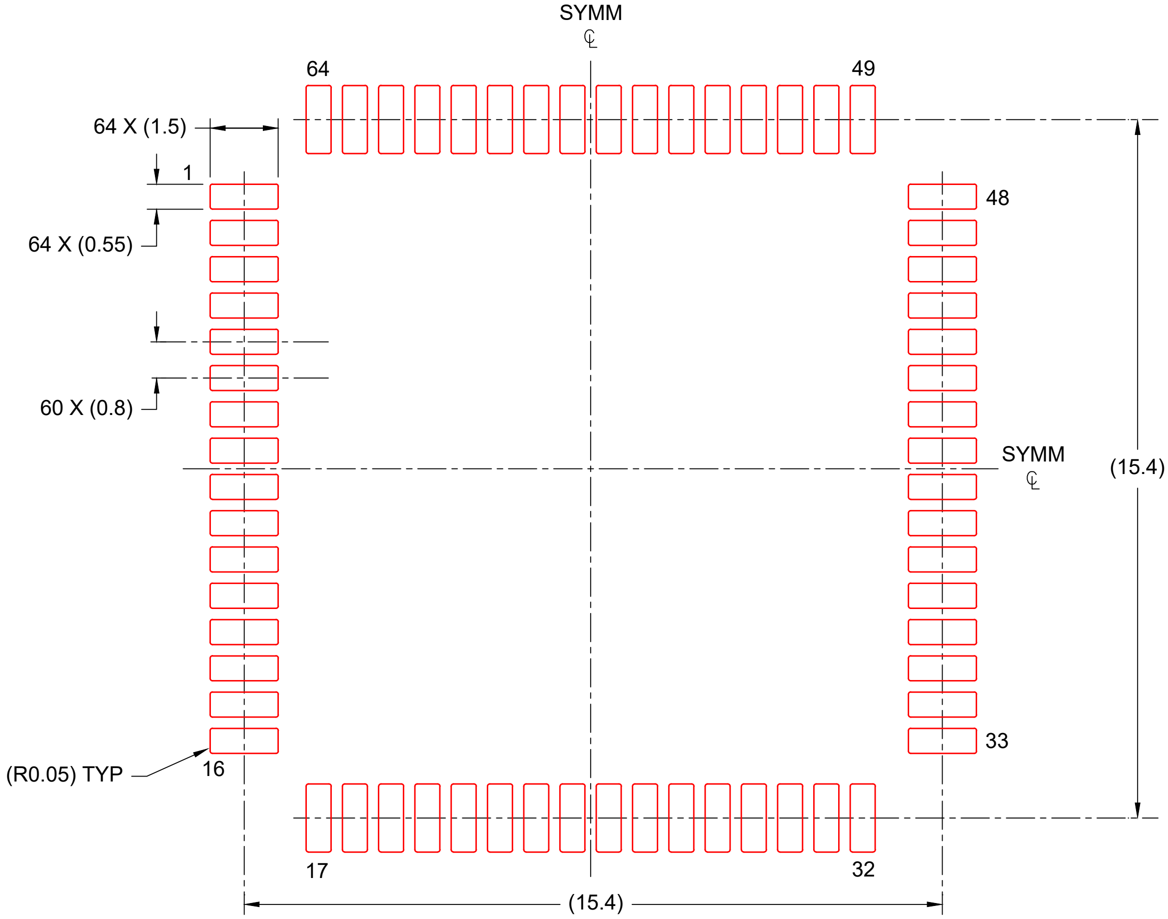
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
SCALE: 6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.