TCA9554 具有中断输出和配置寄存器的低压 8 位 I²C 和系统管理总线 (SMbus) 低功耗输入输出 (I/O) 扩展器

1 特性

- I²C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 1.65V 至 5.5V 的工作电源电压范围
- 可耐受 5V 电压的 I/O 端口
- 400kHz 快速 I²C 总线
- 3 个硬件地址引脚可在 I²C/SMBus 上支持最多 8 个器件
- 输入和输出配置寄存器
- 极性反转寄存器
- 内部加电复位
- 低待机电流消耗
- 所用通道在加电时被配置为输入
- 加电时无毛刺脉冲
- SCL/SDA 输入端上的噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求）
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品（例如：游戏机）
- 工业自动化
- 采用 GPIO 受限处理器的产品

3 说明

TCA9554 是一款 16 引脚器件，可为两线双向 I²C 总线（或 SMBus）协议提供 8 位通用并行输入和输出 (I/O) 扩展。该器件的工作电源电压范围为 1.65V 至 5.5V。器件支持 100kHz（标准模式）和 400kHz（快速模式）两种时钟频率。当开关、传感器、按钮、LED、风扇以及其他相似器件需要额外的 I/O 时，I/O 扩展器（如 TCA9554）可提供简单解决方案。

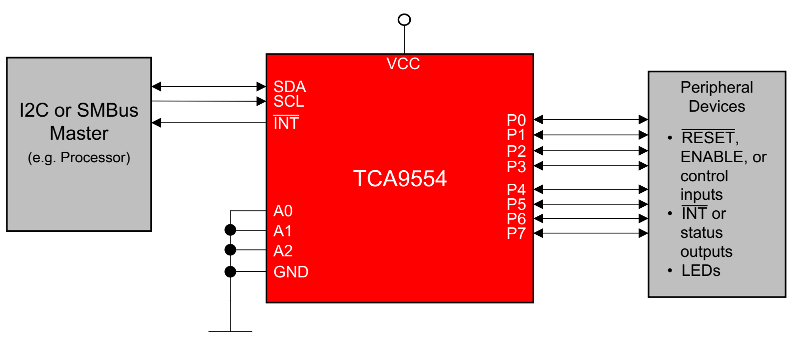
TCA9554 的 功能 包括当输入端口状态发生变化时，在 $\overline{\text{INT}}$ 引脚上生成中断。硬件可选地址引脚 A0、A1 和 A2 最多允许 8 个 TCA9554 器件位于同一 I²C 总线上。该器件还可通过电源循环供电以生成加电复位，从而复位到默认状态 。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TCA9554	TSSOP (16)	5.00mm x 4.40mm
	SSOP (16)	4.90mm × 3.90mm
	SSOP (16)	6.20mm x 5.30mm
	SOIC (16)	7.50mm x 10.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (August 2015) to Revision E	Page
• 已添加 DW 封装。	1
• Added Maximum junction temperature to the *Absolute Maximum Ratings* table	5
• Added I_{OL} for different T_j to the *Recommended Operating Conditions* table	5
• Changed I_{CC} standby into different input states, with increased maximums	7
• Changed C_{io}, C_i maximum	7
• Removed ΔI_{CC} spec from the *Electrical Characteristics* table, added ΔI_{CC} typical characteristics graph	7
• Clarified interrupt reset time (t_{ir}) with respect to falling edge of ACK related SCL pulse.	12
• Made changes to the *Interrupt Output ($\overline{INT}$)* section	16
• Made changes to the *Reads* section	22
• Added the *Calculating Junction Temperature and Power Dissipation* section	25
• Changed recommended supply sequencing values	27
• Power on reset requirements relaxed	27

Changes from Revision C (May 2015) to Revision D	Page
• 已添加 DB 封装。	1

Changes from Revision B (October 2014) to Revision C	Page
• Added standby mode current for $V_I = V_{CC}$ test condition	7
• Changed ΔI_{CC} for one P-port input at $V_I = V_{CC}$ - 0.6, and other P-port I/O at $V_I = V_{CC}$ or GND.	7
• Added clarification in datasheet that raising voltage above V_{CC} on P-port I/O will result in current flow from P-port to V_{CC}.	16

Changes from Revision A (March 2012) to Revision B **Page**

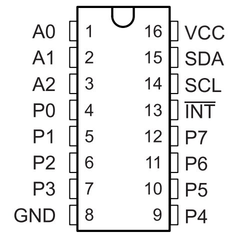
- 已添加 处理额定值表，特性 说明 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。 1
- Updated I_{OL} PARAMETER in the Electrical Characteristics table. 6

Changes from Original (November 2011) to Revision A **Page**

- 最初发布的完整版本。 1

5 Pin Configuration and Functions

PW, DB, DBQ, or DW Package
16-Pin TSSOP, SSOP, SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	1	I	Address input. Connect directly to V_{CC} or ground
A1	2	I	Address input. Connect directly to V_{CC} or ground
A2	3	I	Address input. Connect directly to V_{CC} or ground
GND	8	—	Ground
$\overline{INT}$	13	O	Interrupt output. Connect to V_{CC} through a pull-up resistor
P0	4	I/O	P-port input-output. Push-pull design structure. At power on, P0 is configured as an input
P1	5	I/O	P-port input-output. Push-pull design structure. At power on, P1 is configured as an input
P2	6	I/O	P-port input-output. Push-pull design structure. At power on, P2 is configured as an input
P3	7	I/O	P-port input-output. Push-pull design structure. At power on, P3 is configured as an input
P4	9	I/O	P-port input-output. Push-pull design structure. At power on, P4 is configured as an input
P5	10	I/O	P-port input-output. Push-pull design structure. At power on, P5 is configured as an input
P6	11	I/O	P-port input-output. Push-pull design structure. At power on, P6 is configured as an input
P7	12	I/O	P-port input-output. Push-pull design structure. At power on, P7 is configured as an input
SCL	14	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	15	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
VCC	16	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage (2)		–0.5	6	V
V_O	Output voltage (2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current through a single P-port	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current through a single P-port	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND by all P-ports			250	mA
	Continuous current through V_{CC}			–160	
$T_{j(MAX)}$	Maximum junction temperature			100	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	0.7 × V_{CC}	V_{CC} (1)	V
		A0, A1, A2, P7–P0	V_{CC} = 1.65 V to 2.7 V	0.7 × V_{CC}	5.5	
			V_{CC} = 3 V to 5.5 V	0.8 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	–0.5	0.3 × V_{CC}	V
		A0, A1, A2, P7–P0	V_{CC} = 1.65 V to 2.7 V	–0.5	0.3 × V_{CC}	
			V_{CC} = 3 V to 5.5 V	–0.5	0.2 × V_{CC}	
I_{OL}	Low-level output current (2)	P00–P07, P10–P17	T_j ≤ 65°C		25	mA
			T_j ≤ 85°C		18	
			T_j ≤ 100°C		9	
		$\overline{INT}$, SDA	T_j ≤ 85°C		6	
			T_j ≤ 100°C		3	
I_{OH}	High-level output current	Any P-port, P7–P0			–10	mA
I_{CC}	Continuous current through GND	All P-ports P7-P0, $\overline{INT}$, and SDA			200	mA
	Continuous current through V_{CC}	All P-ports P7-P0			–80	

(1) For voltages applied above V_{CC}, an increase in I_{CC} will result.
(2) The values shown apply to specific junction temperatures, which depend on the $R_{\theta JA}$ of the package used. See the *Calculating Junction Temperature and Power Dissipation* section on how to calculate the junction temperature.

Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TCA9554				UNIT
		PW (TSSOP)	DBQ (SSOP)	DB (SSOP)	DW (SOIC)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	121.7	113.2	84.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	72.9	63.6	48	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	64.2	64	49.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	24.4	21.2	22.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.5	63.8	63.4	48.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage(2)	I_{OH} = –8 mA	1.65 V	1.2			
			2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
		I_{OH} = –10 mA	1.65 V	1.1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
I_{OL}	SDA(3)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	11		mA
	P port(4)	V_{OL} = 0.5 V	1.65 V	8	10		
			2.3 V	8	13		
			3 V	8	15		
			4.5 V	8	17		
		V_{OL} = 0.7 V	1.65 V	10	14		
			2.3 V	10	17		
			3 V	10	20		
			4.5 V	10	24		
	$\overline{INT}$ (5)	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	7		
I_I	SCL, SDA	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	μA
	A0, A1, A2					±1	
I_{IH}	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	μA
I_{IL}	P port	V_I = GND	1.65 V to 5.5 V			–100	μA

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V_{CC} must be limited to a maximum current of 80 mA.
(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(5) The $\overline{INT}$ pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[(1)]	MAX	UNIT
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{SCL} = 400 kHz, no load, $t_{r,max}$ = 300 ns		5.5 V		34		µA
				3.6 V		15		µA
				2.7 V		9		µA
				1.65 V		5		µA
	Standby mode	I/O = inputs, f_{SCL} = 0 kHz	$V_I = V_{CC}$	5.5 V		1.9	3.5	µA
				3.6 V		1.1	1.8	µA
				2.7 V		1	1.6	µA
				1.95 V		0.4	1	µA
			V_I = GND	5.5 V		0.45	0.7	mA
				3.6 V		0.3	0.6	mA
				2.7 V		0.23	0.5	mA
				1.95 V		0.23	0.5	mA
C_i	SCL	$V_I = V_{CC}$ or GND		1.65 V to 5.5 V		3	8	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND		1.65 V to 5.5 V		5.5	9.5	pF
	P port					8	9.5	pF

6.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 11)

			MIN	MAX	UNIT
STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		µs
t_{sth}	I²C Start or repeated Start condition hold		4		µs
t_{sps}	I²C Stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{DD} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{DD} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		0.6		µs
t_{sps}	I²C Stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time			0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition			0.9	µs
C_b	I²C bus capacitive load			400	pF

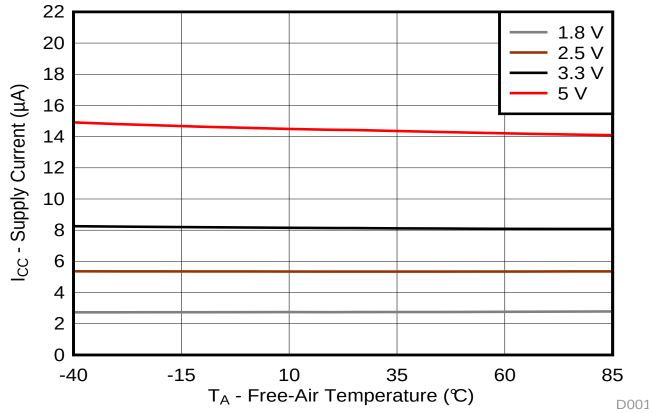
6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 12 and Figure 13)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
STANDARD MODE and FAST MODE						
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P7–P0		350	ns
t_{ps}	Input data setup time	P port	SCL	100		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

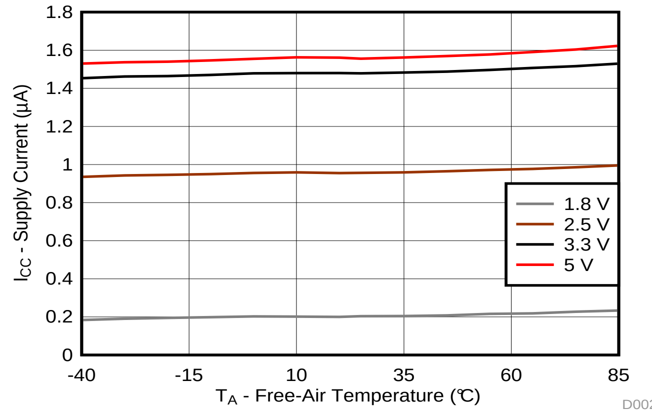
6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)



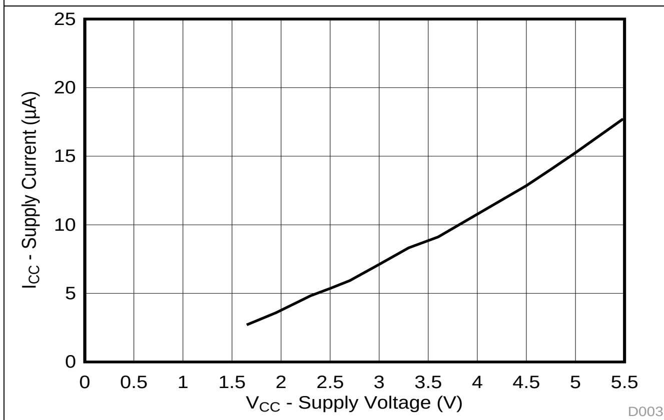
f_{SCL} = 400 kHz   I/Os = High or Low Inputs

Figure 1. Supply Current (I_{CC}, Operating Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 0 kHz   I/Os = High Inputs

Figure 2. Supply Current (ICC, Standby Mode) vs Temperature (T_A) at Four Supply Voltages



f_{SCL} = 400 kHz   I/Os = High or Low Inputs T_A = 25°C

Figure 3. Supply Current (I_{CC}, Operating Mode) vs Supply Voltage (V_{CC})

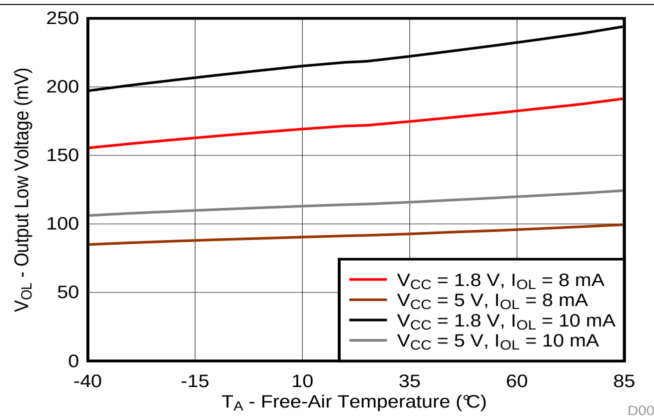
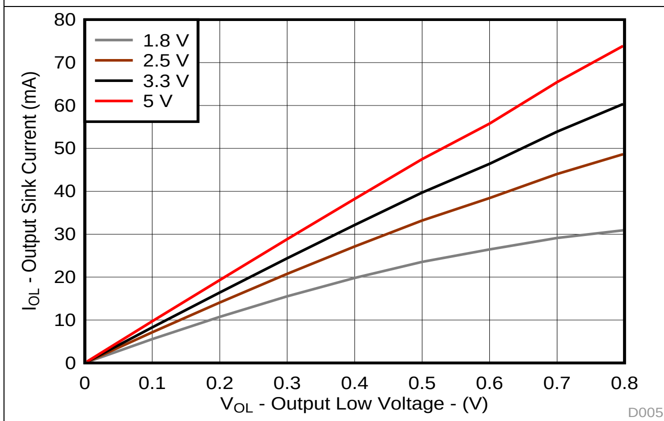


Figure 4. Output Low Voltage (V_{OL}) vs Temperature (T_A) for P-Port I/Os



T_A = 25°C

Figure 5. Sink Current (I_{OL}) vs Output Low Voltage (V_{OL}) for P-Ports at Four Supply Voltages

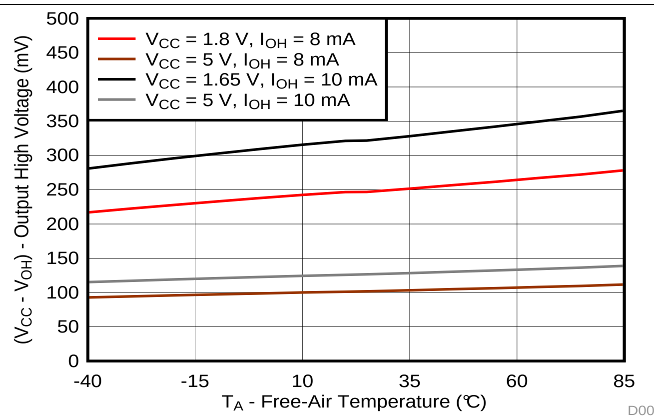


Figure 6. Output High Voltage (V_{CC} – V_{OH}) vs Temperature (T_A) for P-Ports

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

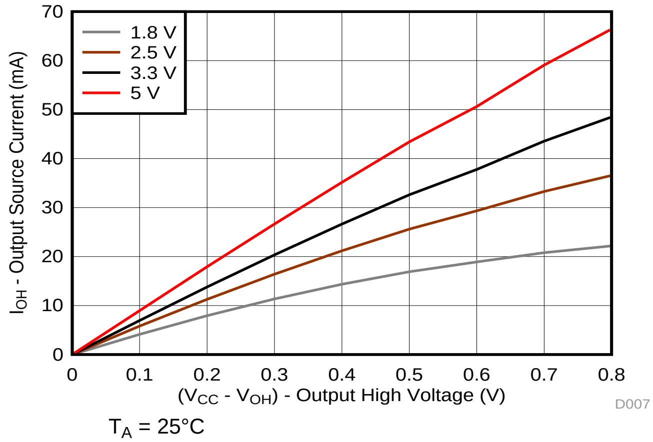


Figure 7. Source Current (I_{OH}) vs Output High Voltage (V_{OH}) for P-Ports at Four Supply Voltages

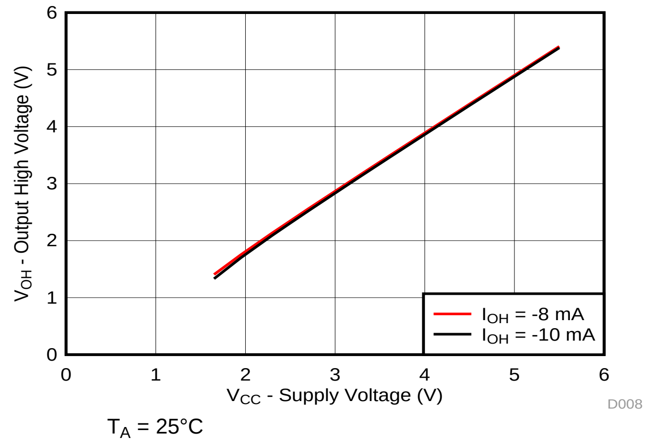


Figure 8. Output High Voltage (V_{OH}) vs Supply Voltage (V_{CC}) for P-Ports

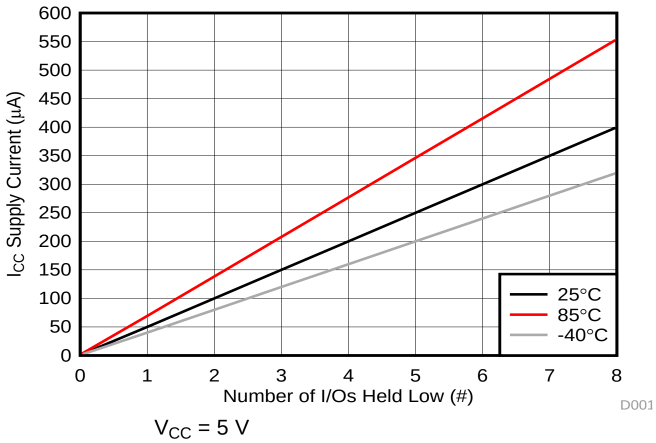


Figure 9. Supply Current (I_{CC}) vs Number of I/Os Held Low (#)

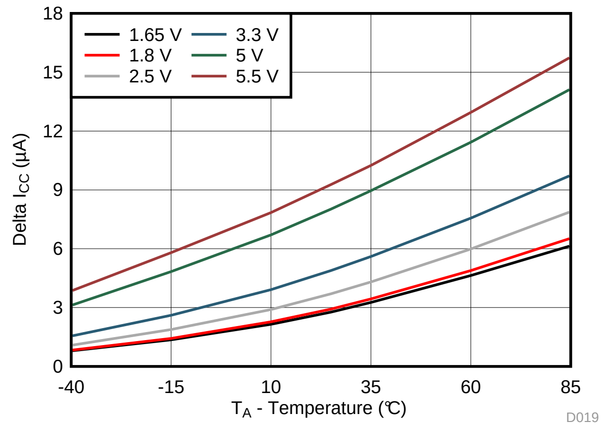
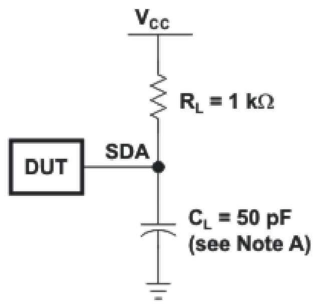
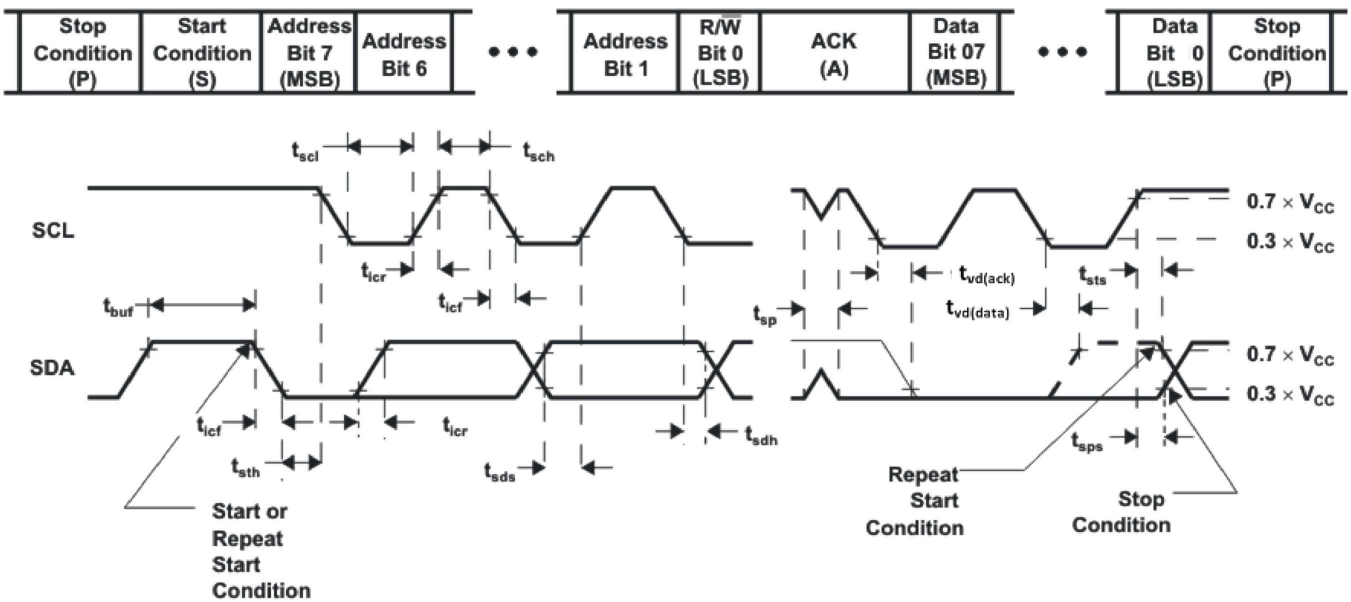


Figure 10. Δ I_{CC} vs Temperature for Different V_{CC} ($V_I = V_{CC} – 0.6$ V)

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

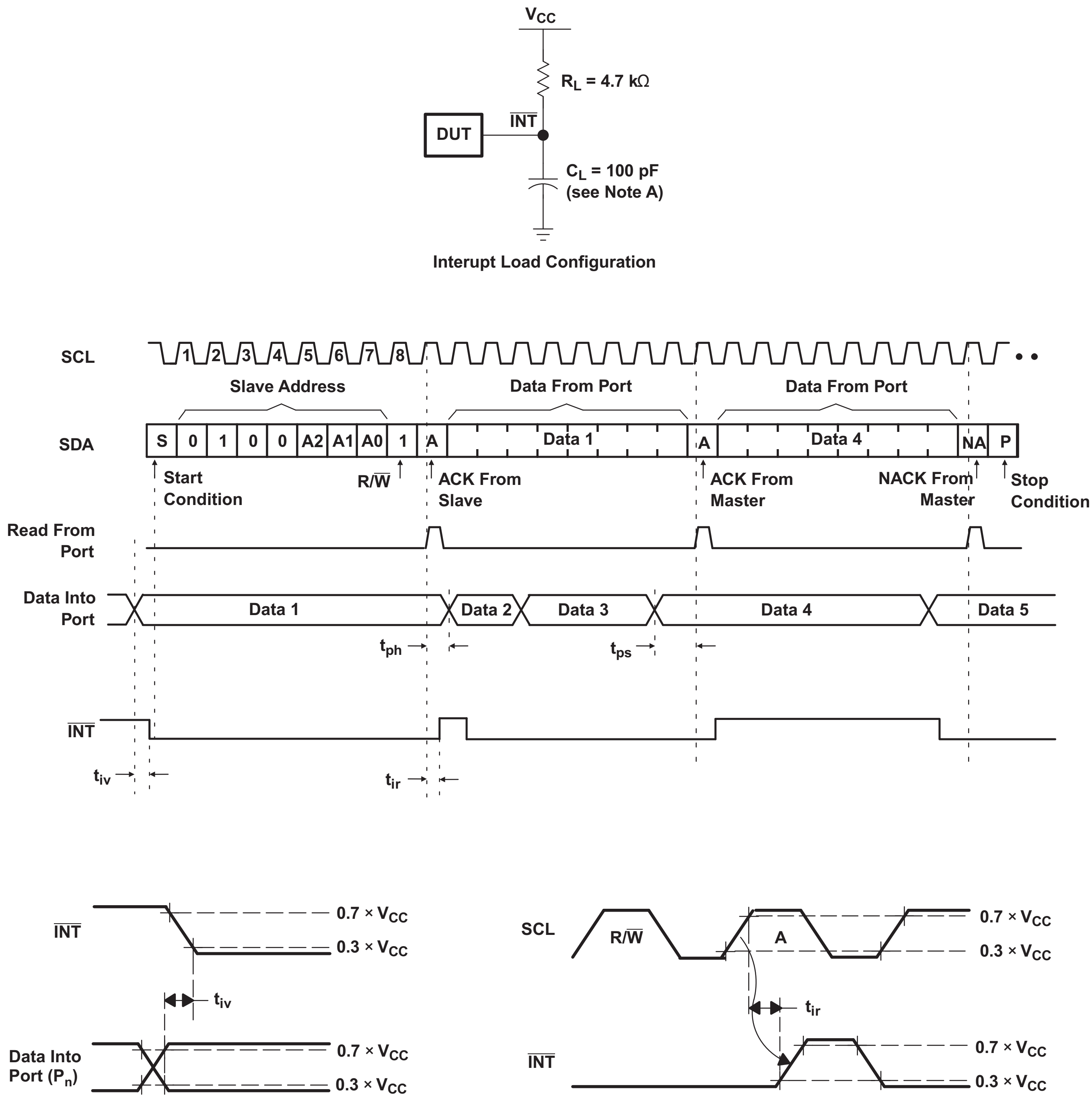
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

Figure 11. I^2C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



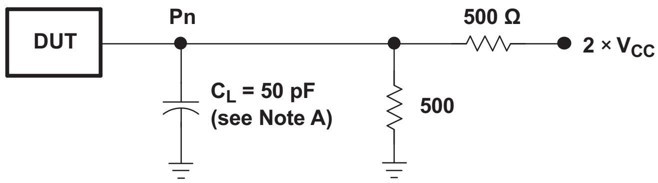
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

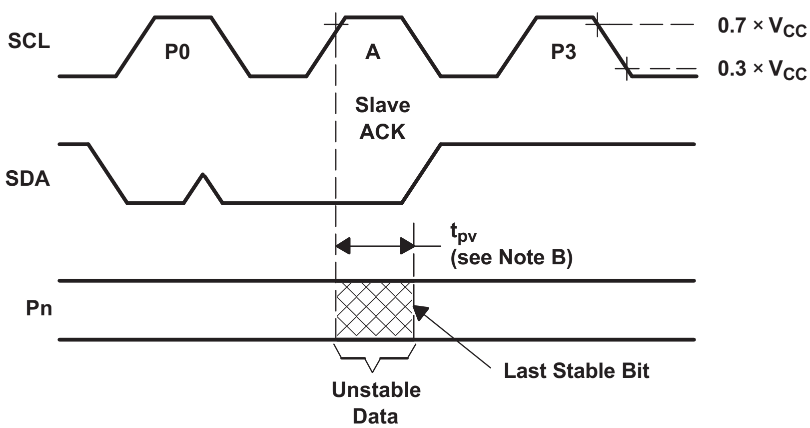
C. All parameters and waveforms are not applicable to all devices.

Figure 12. Interrupt Load Circuit and Voltage Waveforms

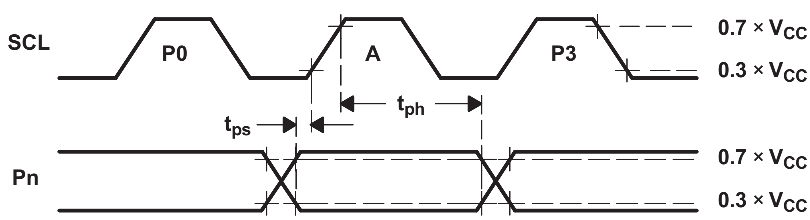
Parameter Measurement Information (continued)



P-Port Load Configuration



Write Mode (R/$\overline{W}$ = 0)



Read Mode (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 13. P-Port Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9554 is an 8-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I^2C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9554 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9554 can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C slave address and allow up to eight devices to share the same I^2C bus or SMBus.

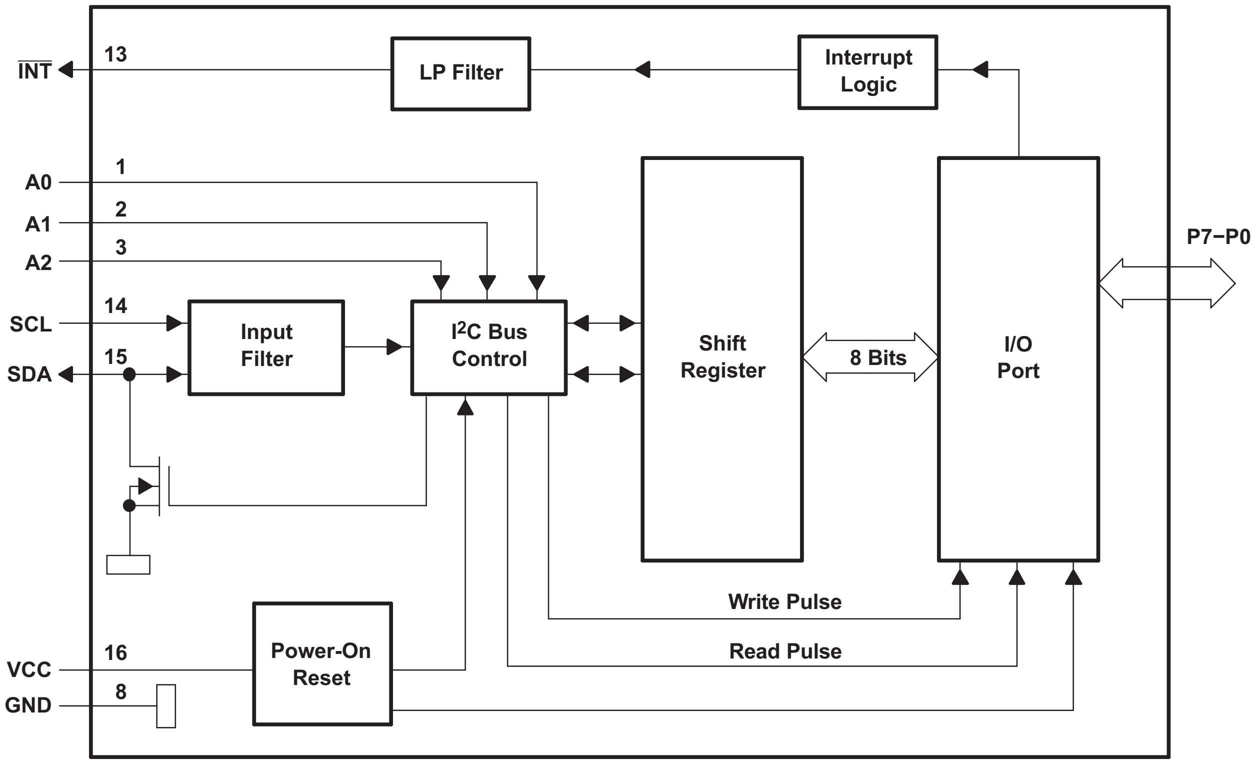
The system master can reset the TCA9554 in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I^2C /SMBus state machine.

The TCA9554 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9554 and TCA9554A are identical except for their fixed I^2C address. This allows for up to 16 of these devices (8 of each) on the same I^2C/SMBus.

The TCA9554 is identical to the TCA9534 except for the addition of the internal I/O pull-up resistors, which keeps P-ports from floating when configured as inputs.

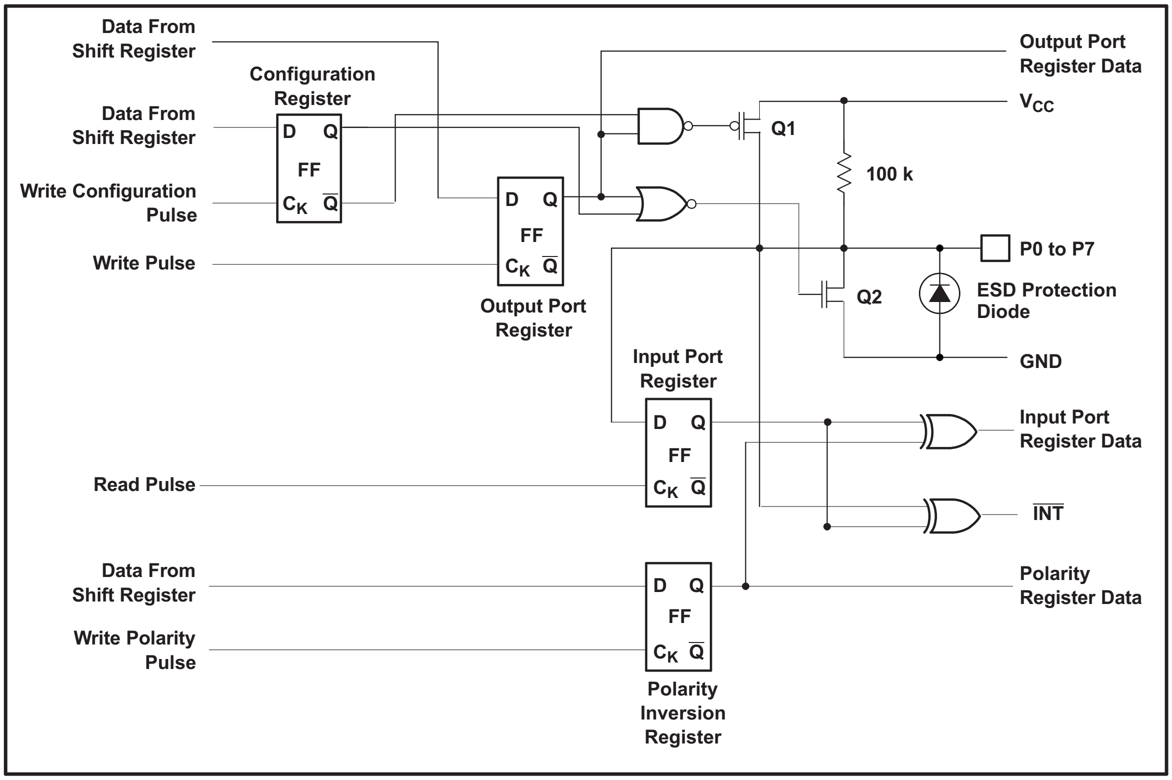
8.2 Functional Block Diagram



Pin numbers shown are for the PW package.

Figure 14. Functional Block Diagram

Functional Block Diagram (continued)



At power-on reset, all registers return to default values.

Figure 15. Simplified Schematic Of P0 To P7

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typical) to V_{CC}. The input voltage may be raised above V_{CC} to a maximum of 5.5 V, however it must be noted that because of the integrated 100 kΩ pull-up resistor it may result in current flow from I/O to VCC pin (Figure 15).

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

8.3.2 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of any P-port I/O configured as an input. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the ports is changed back to the original state or when data is read from the Input Port register. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as an interrupt on the $\overline{INT}$ pin.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to VCC, an internal power-on reset holds the TCA9554 in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9554 registers and SMBus/I²C state machine initializes to their default states. After that, V_{CC} must be lowered to below V_{PORF} and then back up to the operating voltage for a power-on reset cycle.

8.5 Programming

8.5.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input-output while the SCL input is high (see Figure 16). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 17).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 16).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 18). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

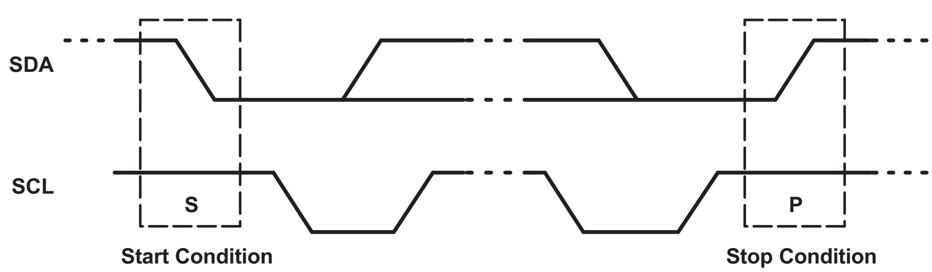


Figure 16. Definition of Start and Stop Conditions

Programming (continued)

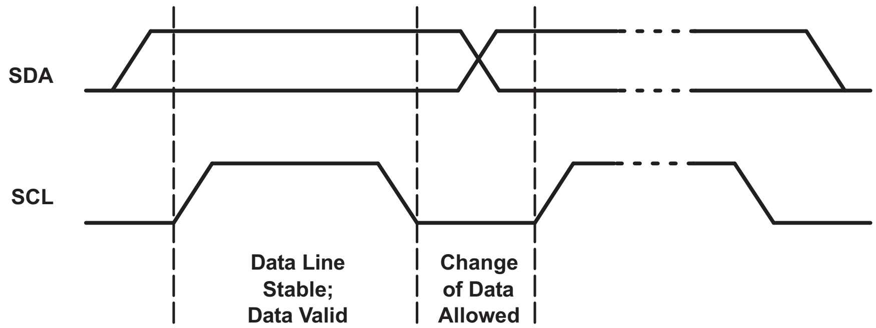


Figure 17. Bit Transfer

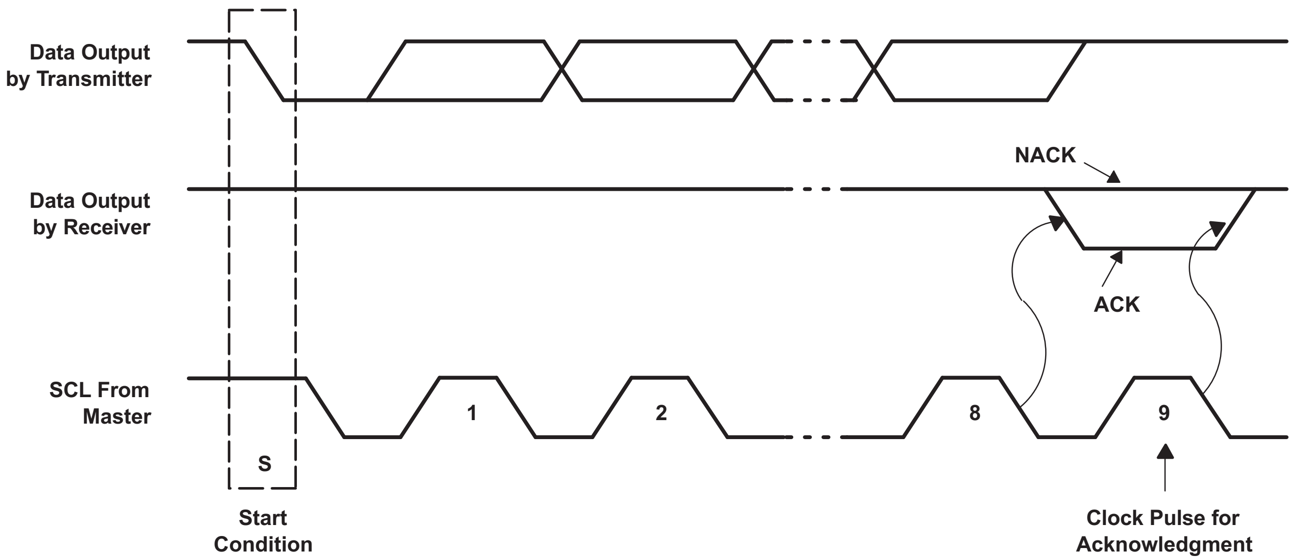


Figure 18. Acknowledgment on I²C Bus

Table 1 shows the TCA9554 interface definition.

Table 1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.6 Register Maps

8.6.1 Device Address

Figure 19 shows the address byte of the TCA9554.

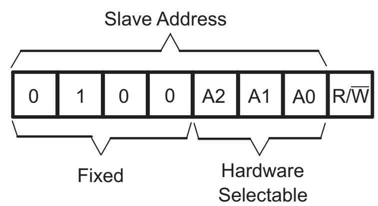


Figure 19. TCA9554 Address

Table 2 shows the TCA9554 address reference.

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9554 (see Figure 20). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	B2	B1	B0

Figure 20. Control Register Bits

Table 3 shows the TCA9554 command byte.

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	XXXX XXXX
0	1	0×01	Output Port	Read-write byte	1111 1111
1	0	0×02	Polarity Inversion	Read-write byte	0000 0000
1	1	0×03	Configuration	Read-write byte	1111 1111

8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next. See Table 4.

Table 4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See Table 5.

Table 5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See Table 6.

Table 6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See Table 7.

Table 7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9554 through write and read commands.

8.6.3.1.1 Writes

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W̄ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition. Note that the command byte/register address does NOT automatically increment. Writing multiple bytes during a write results in the last byte sent being stored in the register.

See the *Register Descriptions* section to see list of the TCA9554's internal registers and a description of each one.

Figure 21 shows an example of writing a single byte to a slave register.

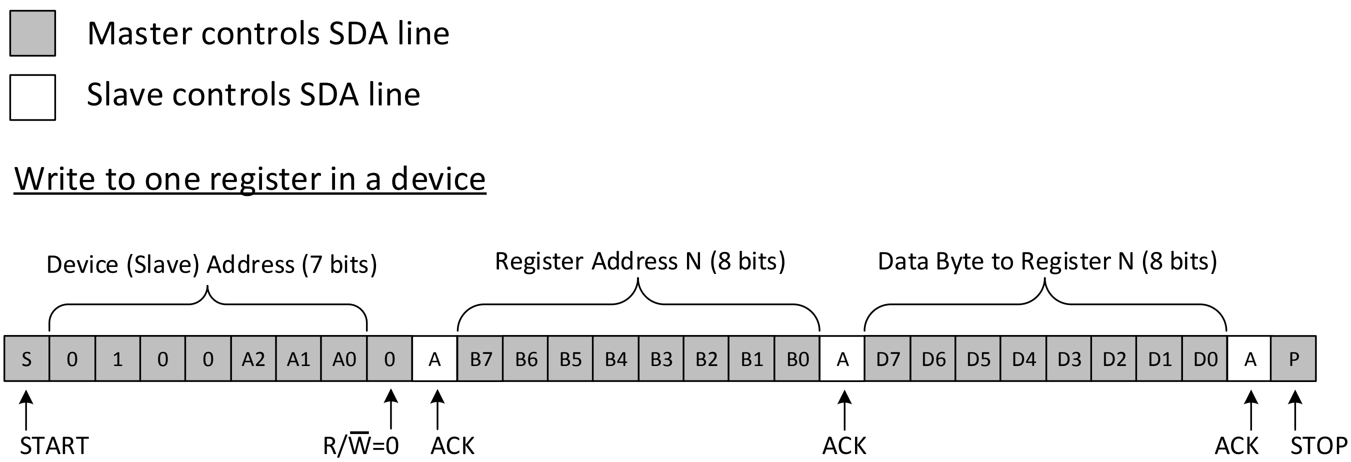


Figure 21. Write to Register

Figure 22 shows an example of how to write to the polarity inversion register.

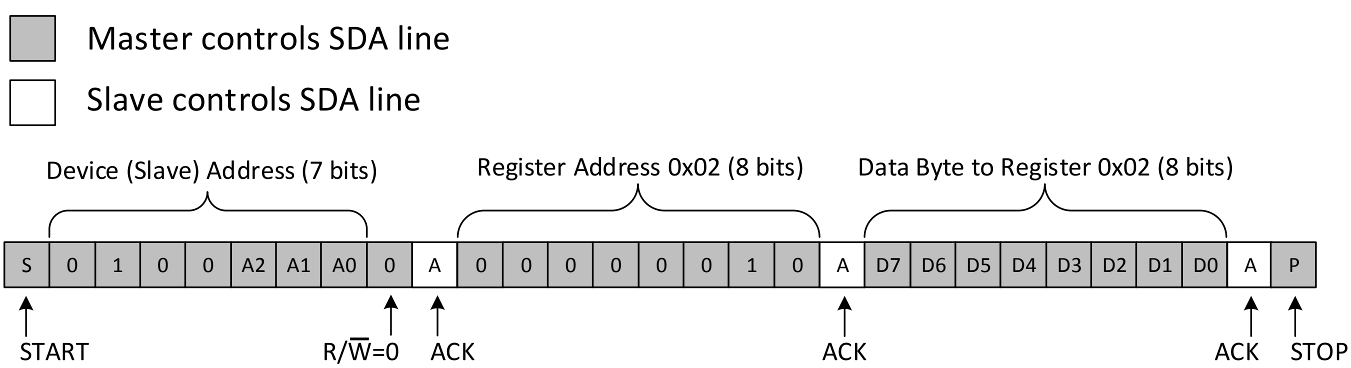


Figure 22. Write to the Polarity Inversion Register

Figure 23 shows an example of how to write to output port register.

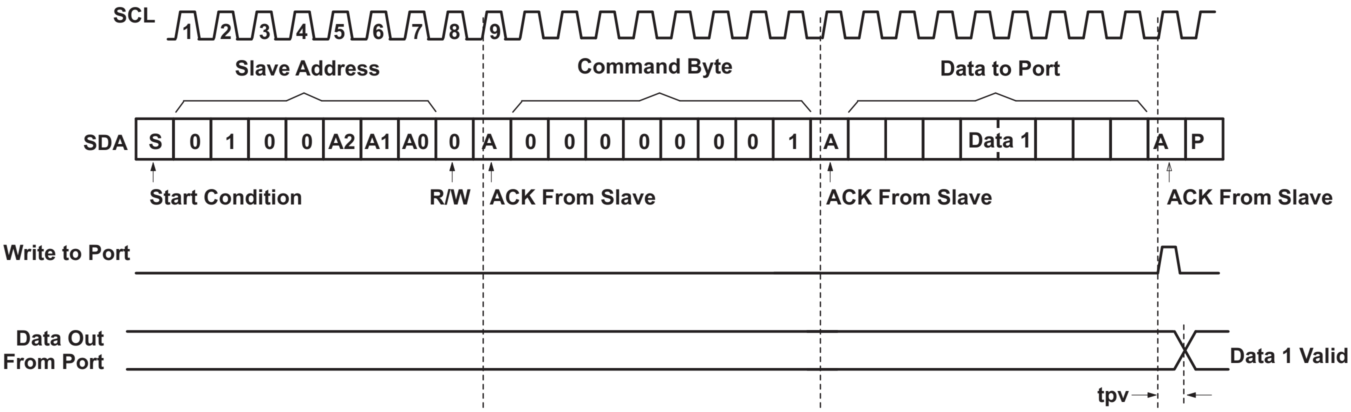


Figure 23. Write to Output Port Register

8.6.3.1.2 Reads

The bus master first must send the TCA9554 address with the LSB set to a logic 0 (see Figure 19 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9554 (see Figure 25). The command byte does not increment automatically. If multiple bytes are read, data from the specified command byte/register is going to be continuously read.

See the *Register Descriptions* section for the list of the TCA9554's internal registers and a description of each one.

Figure 24 shows an example of reading a single byte from a slave register.

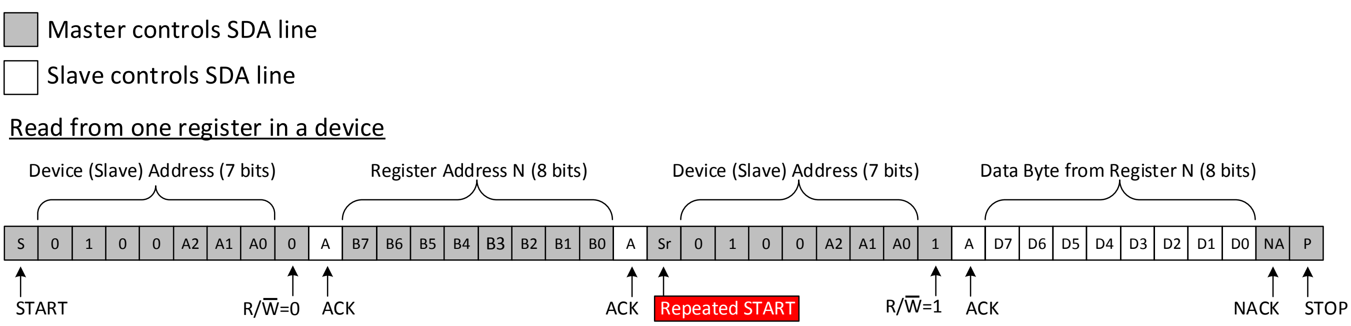
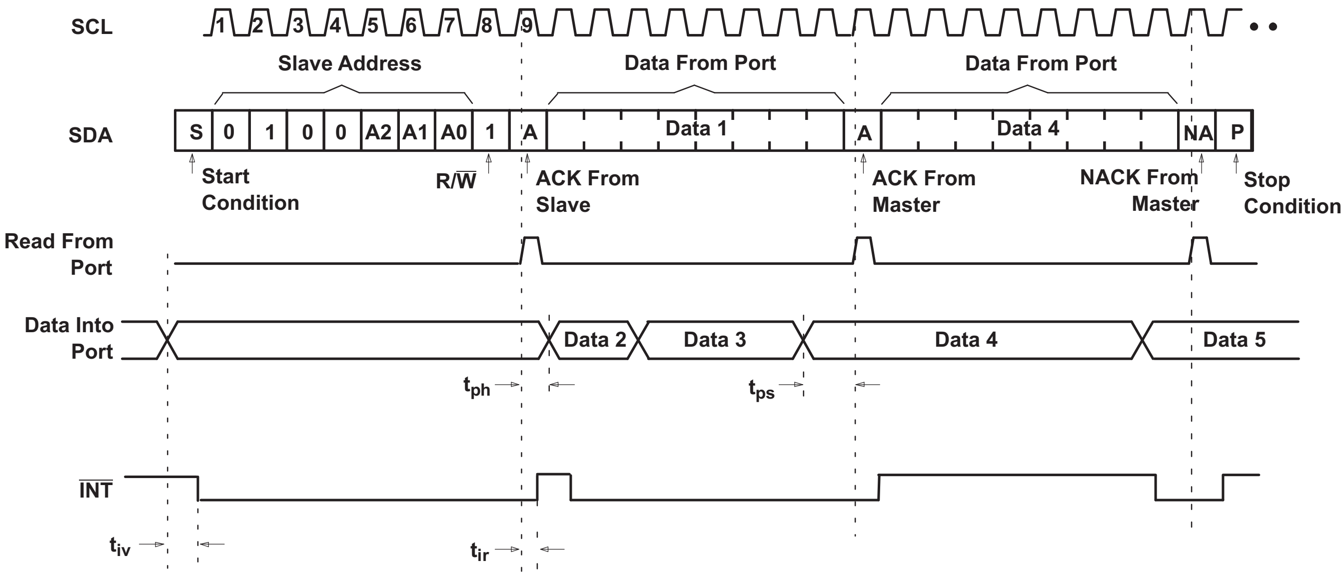


Figure 24. Read from Register

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte, additional bytes may be read, but the same register specified by the command byte is read.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 24 for these details).

Figure 25. Read Input Port Register

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

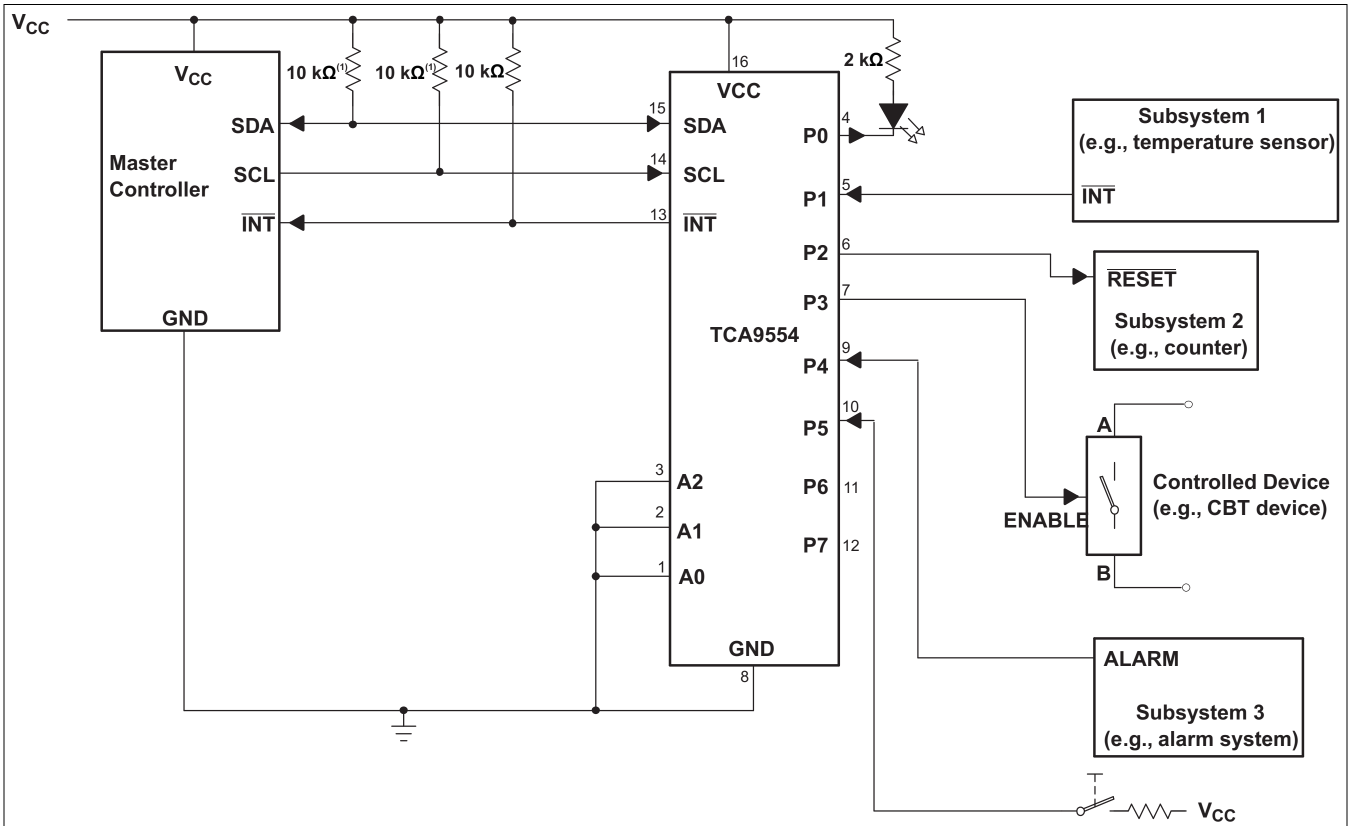
9.1 Application Information

Applications of the TCA9554 has this device connected as a slave to an I^{2}C master (processor), and the I^{2}C bus may contain any number of other slave devices. The TCA9554 is typically in a remote location from the master, placed close to the GPIOs to which the master must monitor or control.

IO Expanders such as the TCA9554 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

9.2 Typical Application

Figure 26 shows an application in which the TCA9554 can be used.



P6 and P7 are not used and have internal 100-kΩ pullup resistors to protect them from floating.

Figure 26. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with this device, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

9.2.1.2 Minimizing I_{CC} when I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 26. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED is off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 27 shows a high-value resistor in parallel with the LED. Figure 28 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

The TCA9554 has an integrated 100-kΩ pull-up resistor, so there is no need for an external pull-up.

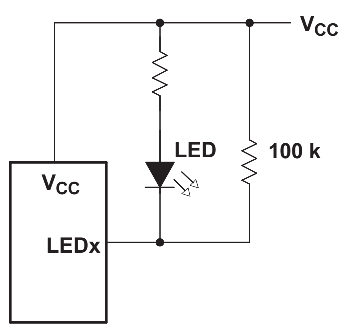


Figure 27. High-Value Resistor in Parallel With LED

Typical Application (continued)

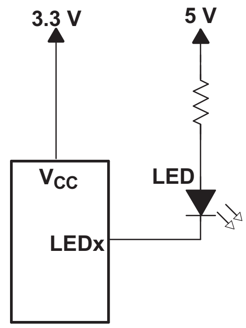


Figure 28. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 5.

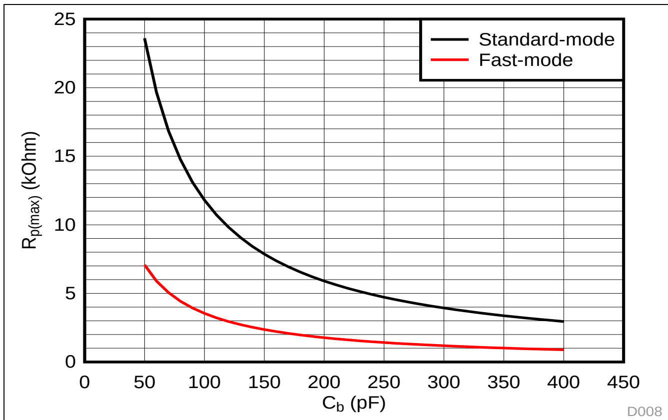
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9554, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

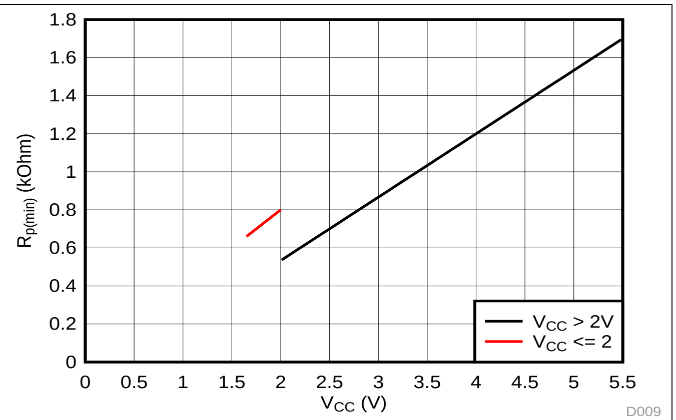
9.2.3 Application Curves



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 29. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 30. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the TCA9554 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The power-on reset is shown in Figure 31.

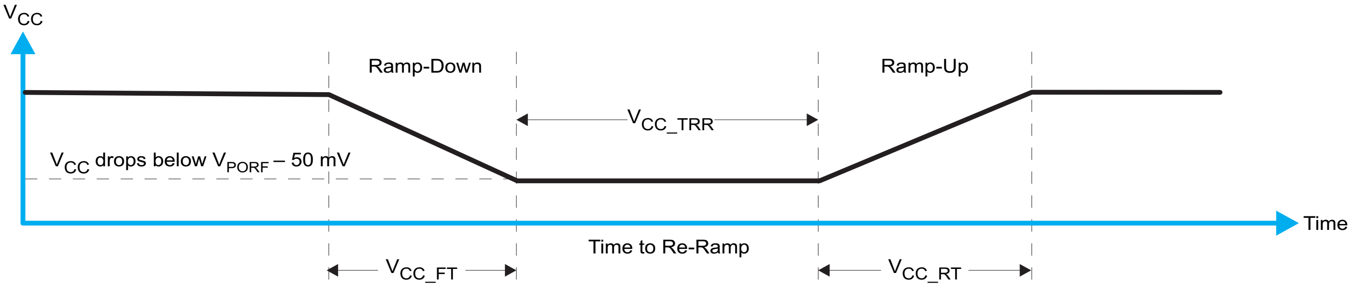


Figure 31. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 8 specifies the performance of the power-on reset feature for the TCA9554.

Table 8. Recommended Supply Sequencing and Ramp Rates(1)

PARAMETER			MIN	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 31	1	2000	ms
V_{CC_RT}	Rise rate	See Figure 31	0.1	2000	ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 31	2		µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs	See Figure 32		1.2	V
V_{CC_MV}	The minimum voltage that V_{CC} can glitch down to without causing a reset (V_{CC_GH} must not be violated)	See Figure 32	1.5		V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC}	See Figure 32		10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 32 and Table 8 provide more information on how to measure these specifications.

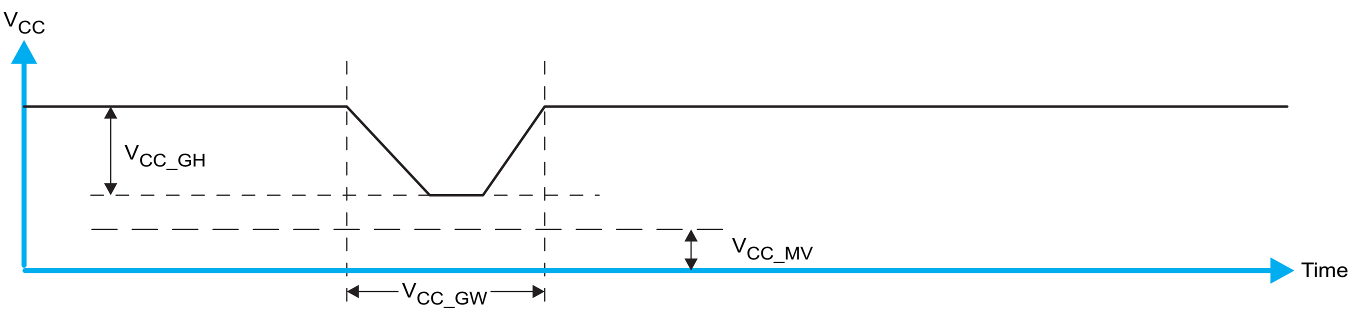


Figure 32. Glitch Width and Glitch Height

V_{PORR} is critical to the power-on reset. V_{PORR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of power-on-reset voltage differs based on the V_{CC} being lowered to or from 0 (V_{PORR} or V_{PORF}). Figure 33 and Table 8 provide more details on this specification.

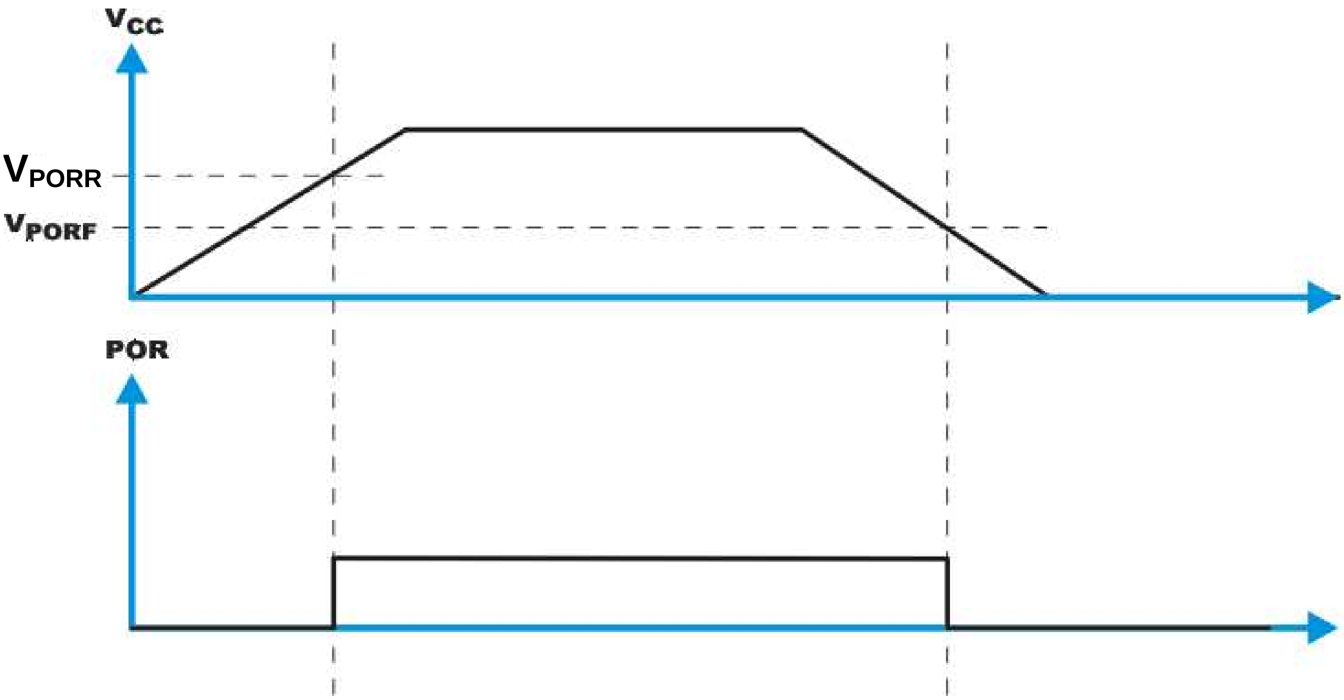


Figure 33. Waveform Describing V_{CC} Voltage Level at Which Power-On-Reset (POR) Occurs

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9554, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9554 as possible. These best practices are shown in Figure 34.

For the layout example provided in Figure 34, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 34.

11.2 Layout Example

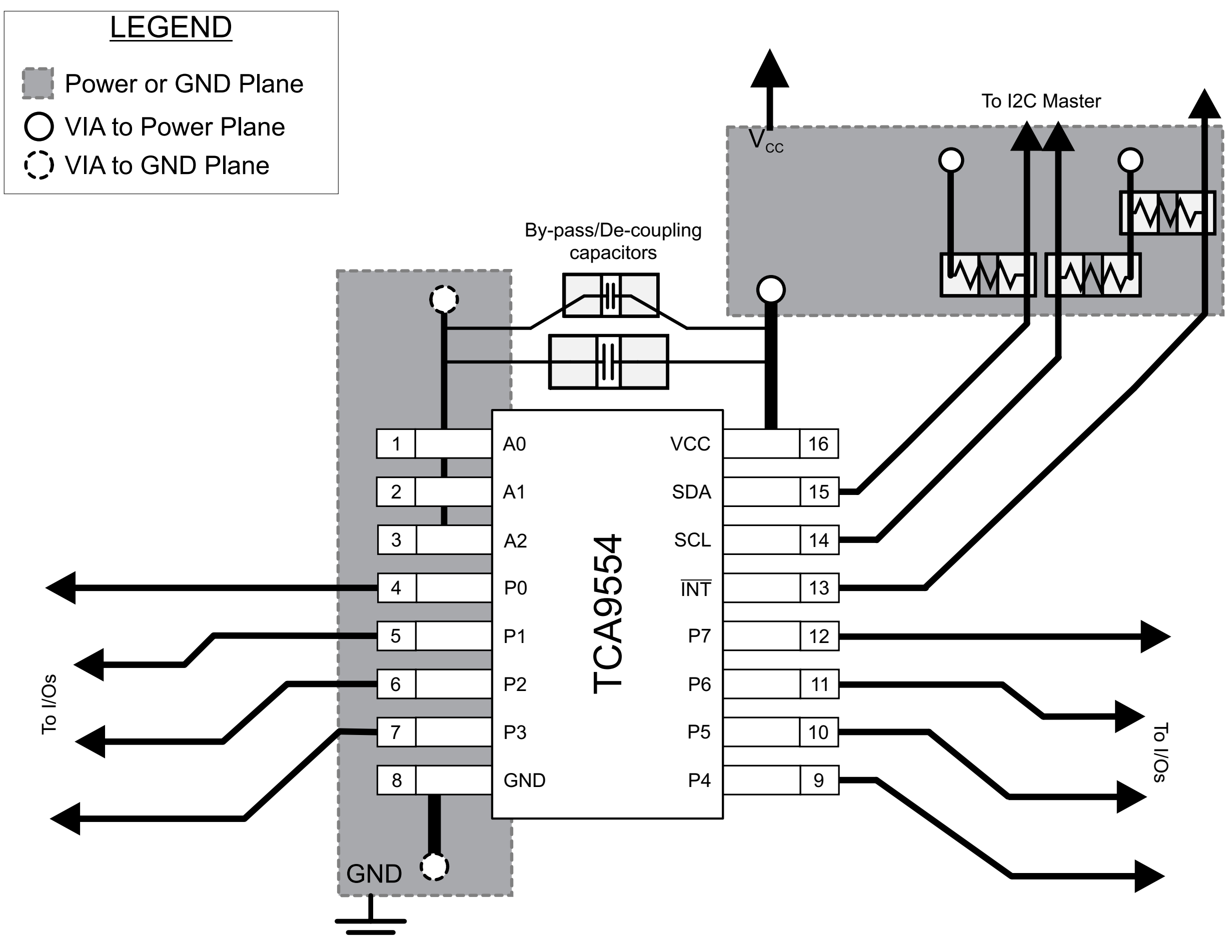


Figure 34. TCA9554 Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《I2C 上拉电阻计算》*
- *《I2C 总线在采用中继器时的最高时钟频率》*
- *《逻辑器件简介》*
- *《理解 I2C 总线》*
- *《为新设计挑选合适的 I2C 器件》*
- *《I/O 扩展器 EVM 用户指南》*

12.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9554DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9554	Samples
TCA9554DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD554	Samples
TCA9554DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9554	Samples
TCA9554DWT	ACTIVE	SOIC	DW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9554	Samples
TCA9554PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW554	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

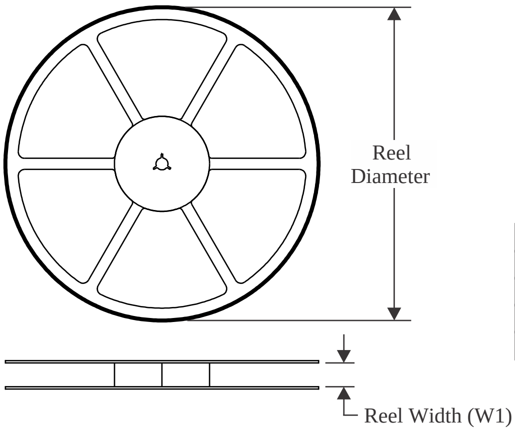
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

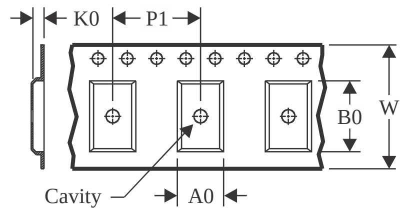
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

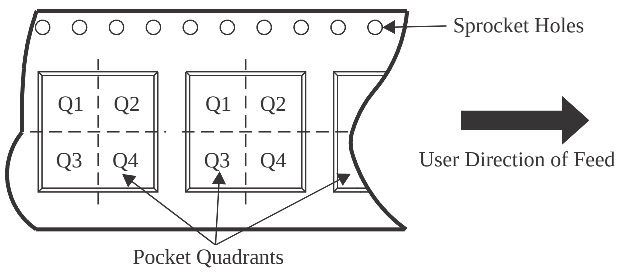


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

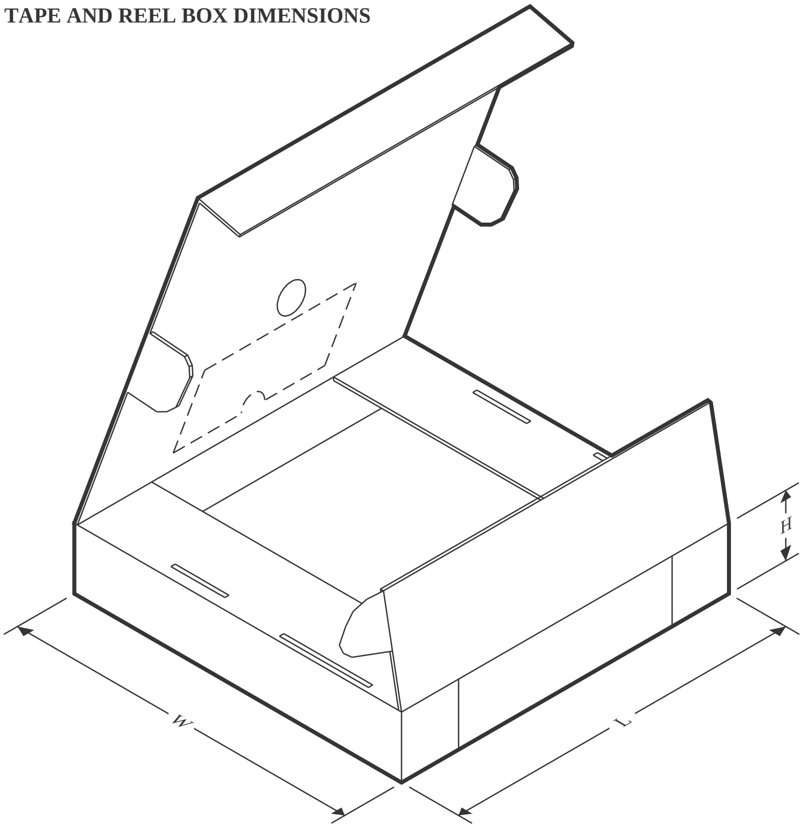
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

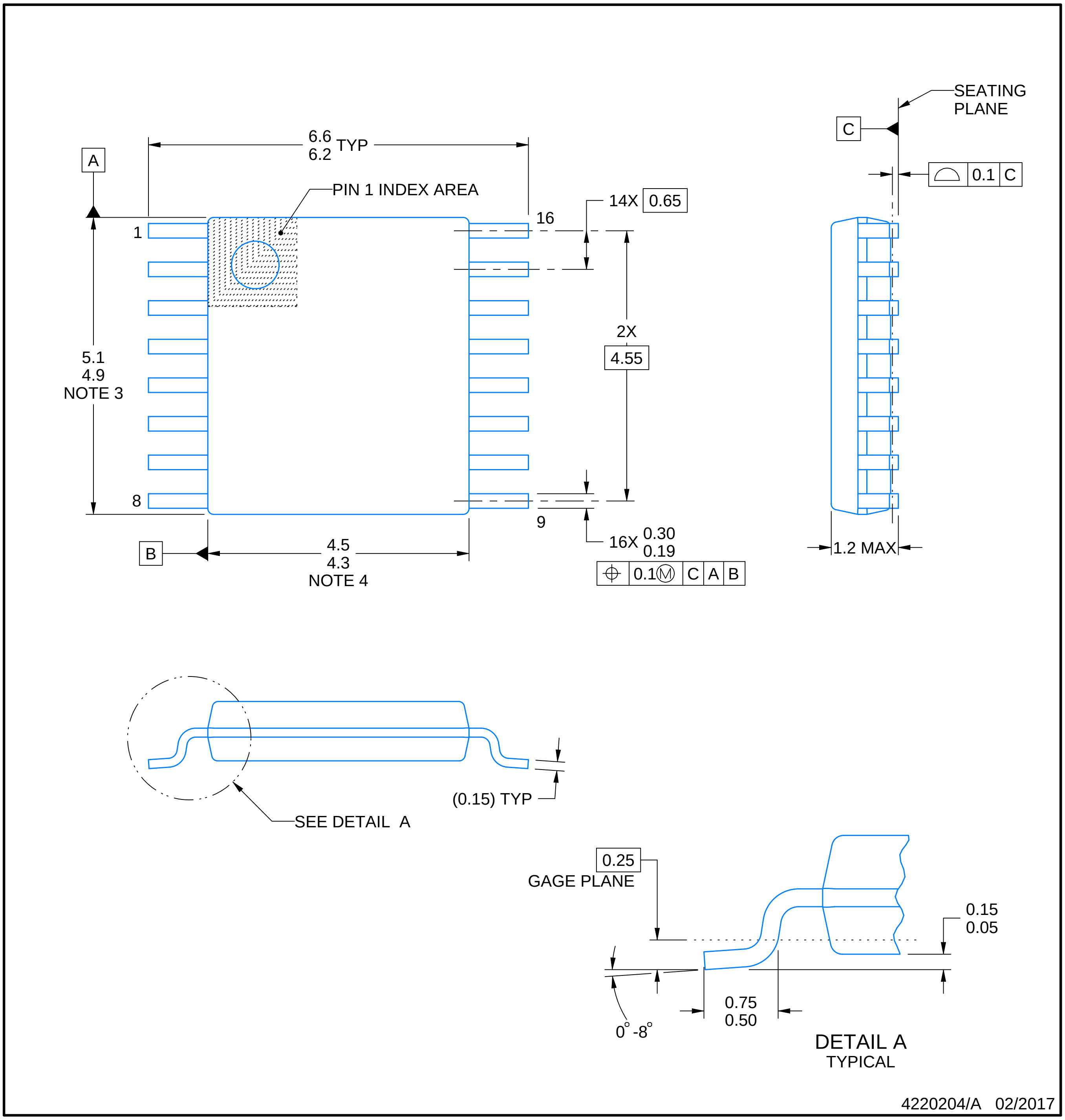
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9554DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCA9554DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TCA9554DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TCA9554PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



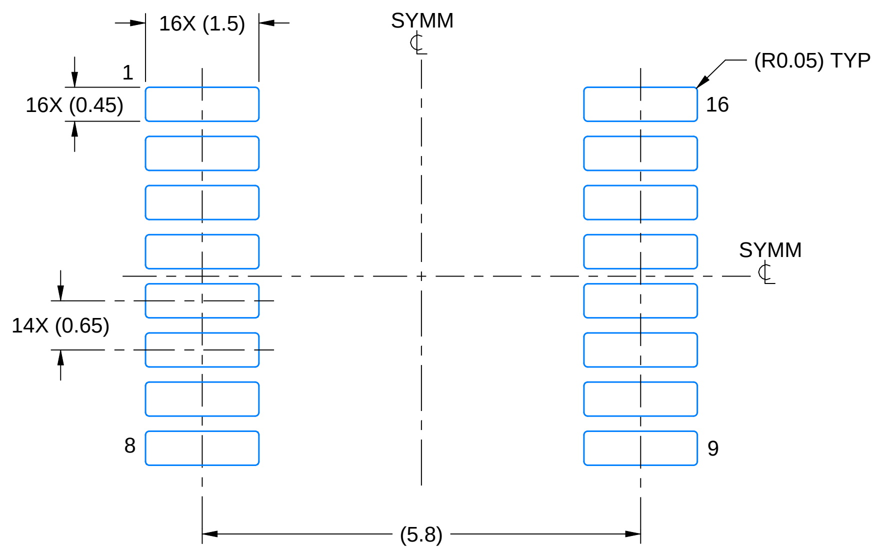
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9554DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TCA9554DBR	SSOP	DB	16	2000	356.0	356.0	35.0
TCA9554DWR	SOIC	DW	16	2000	350.0	350.0	43.0
TCA9554PWR	TSSOP	PW	16	2000	356.0	356.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



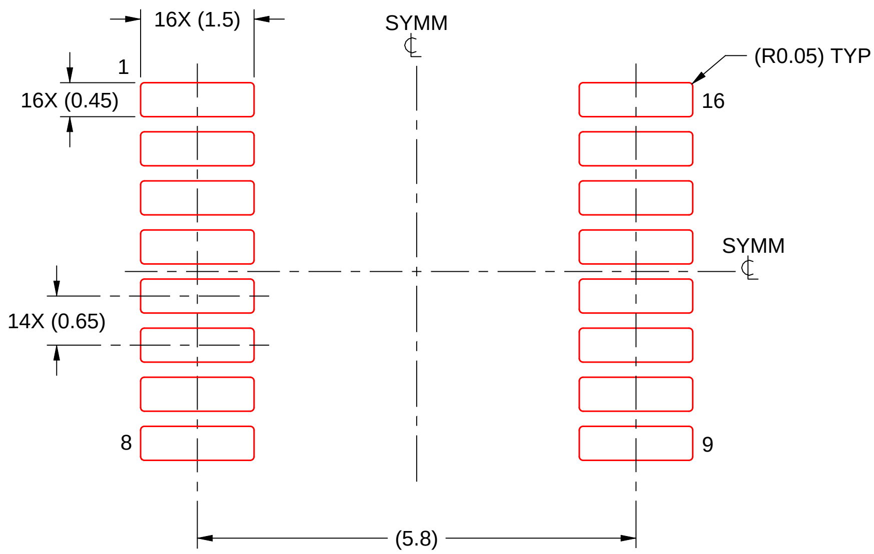
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

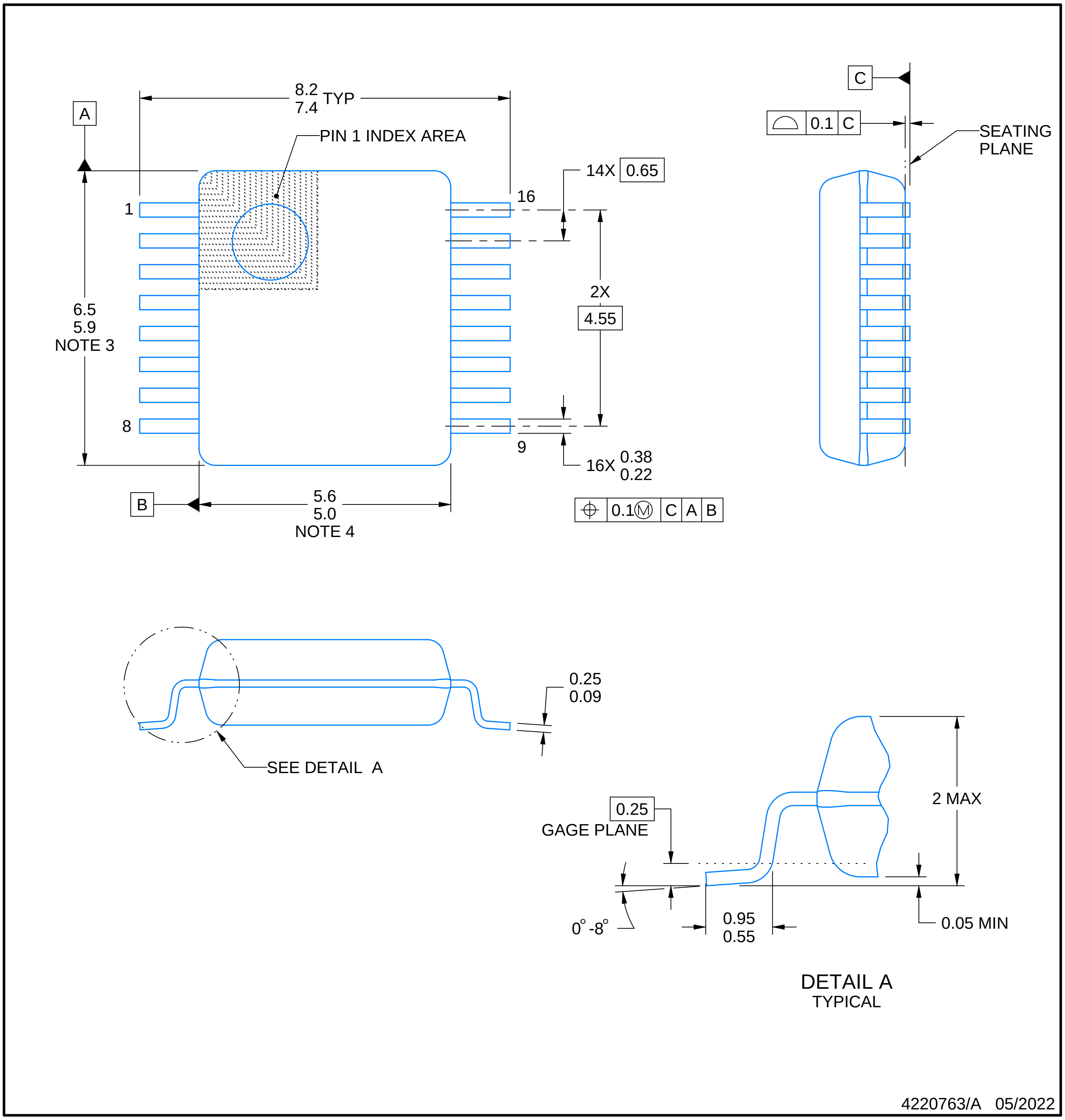


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

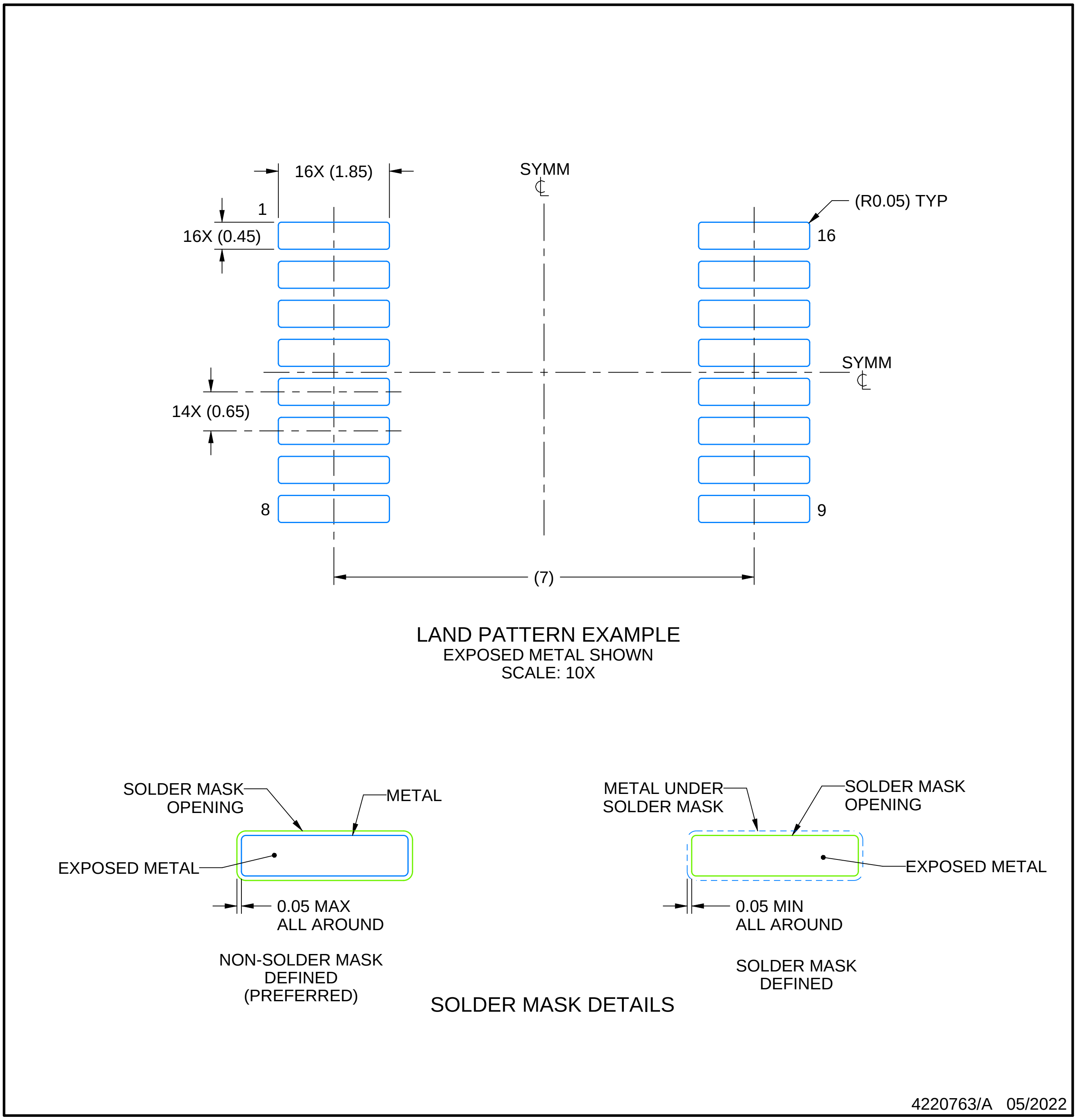
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



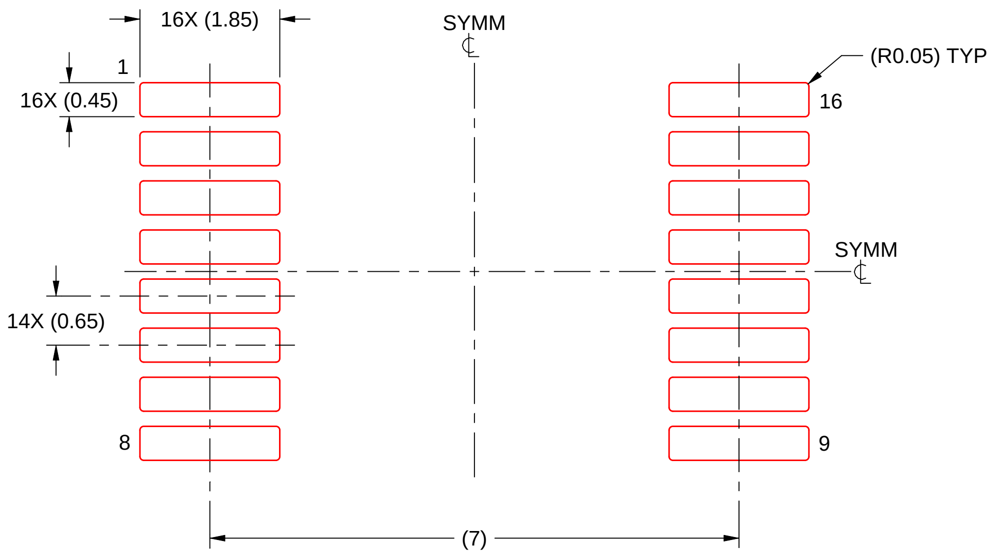
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

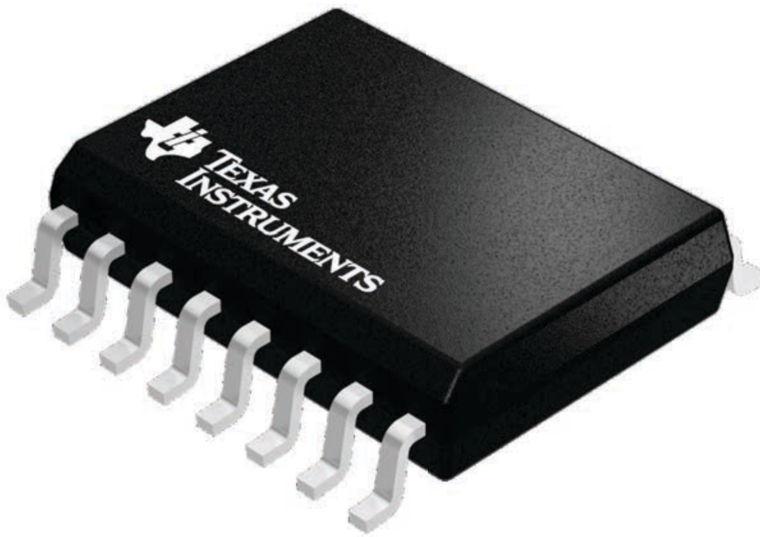
DW 16

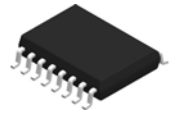
SOIC - 2.65 mm max height

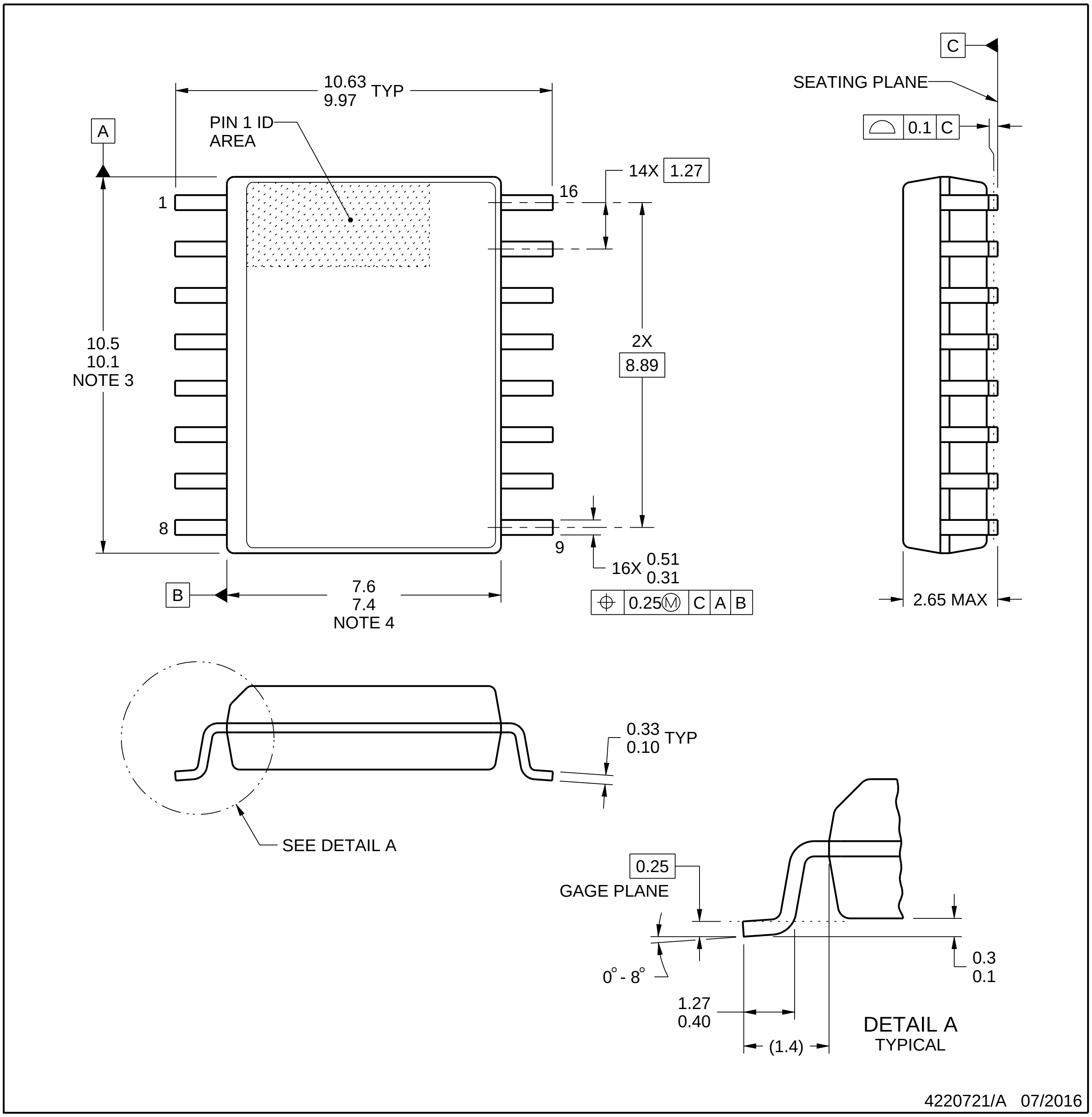
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

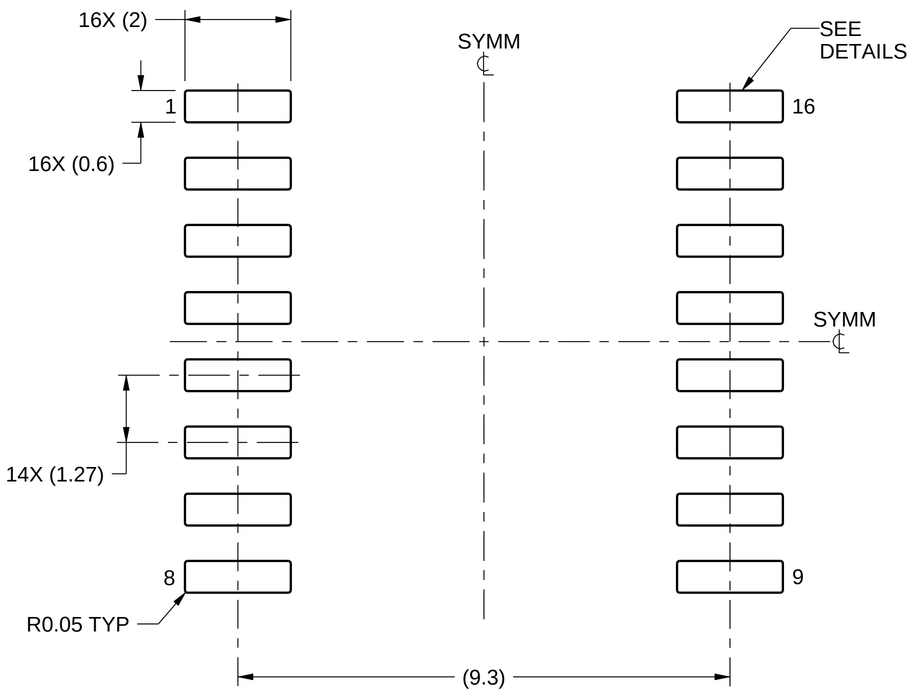




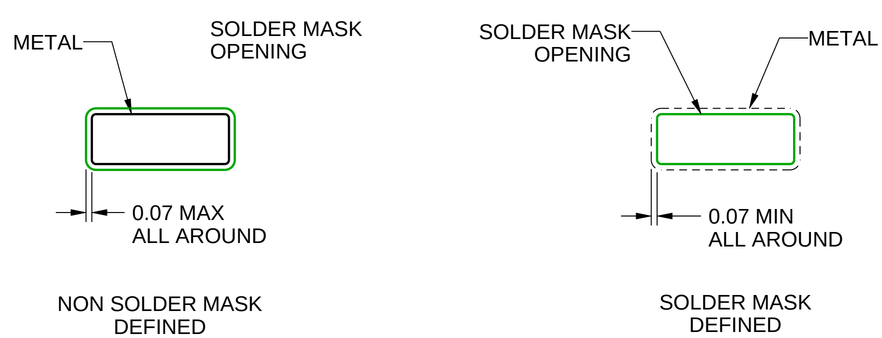


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

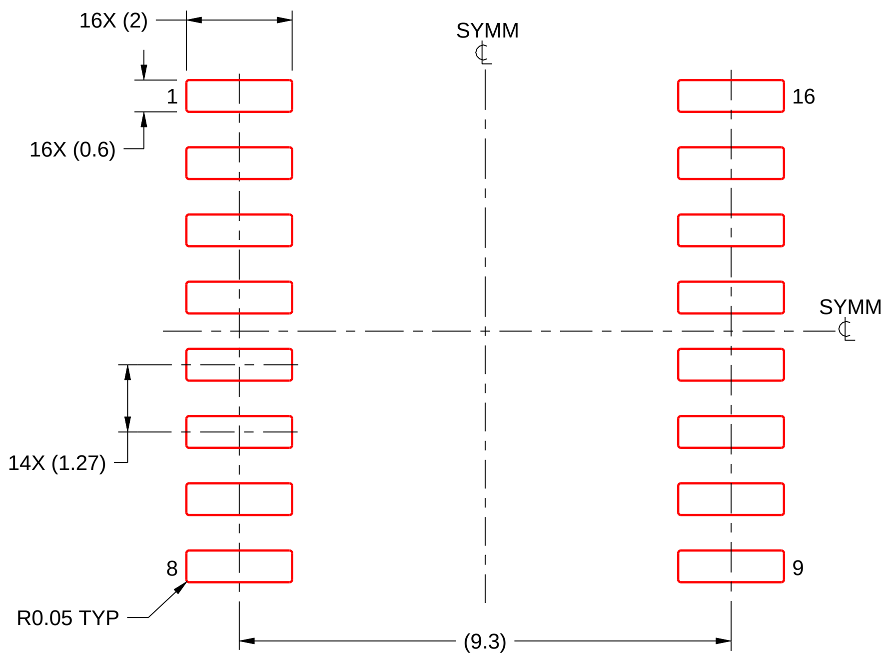


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

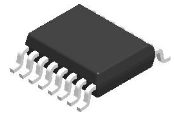


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

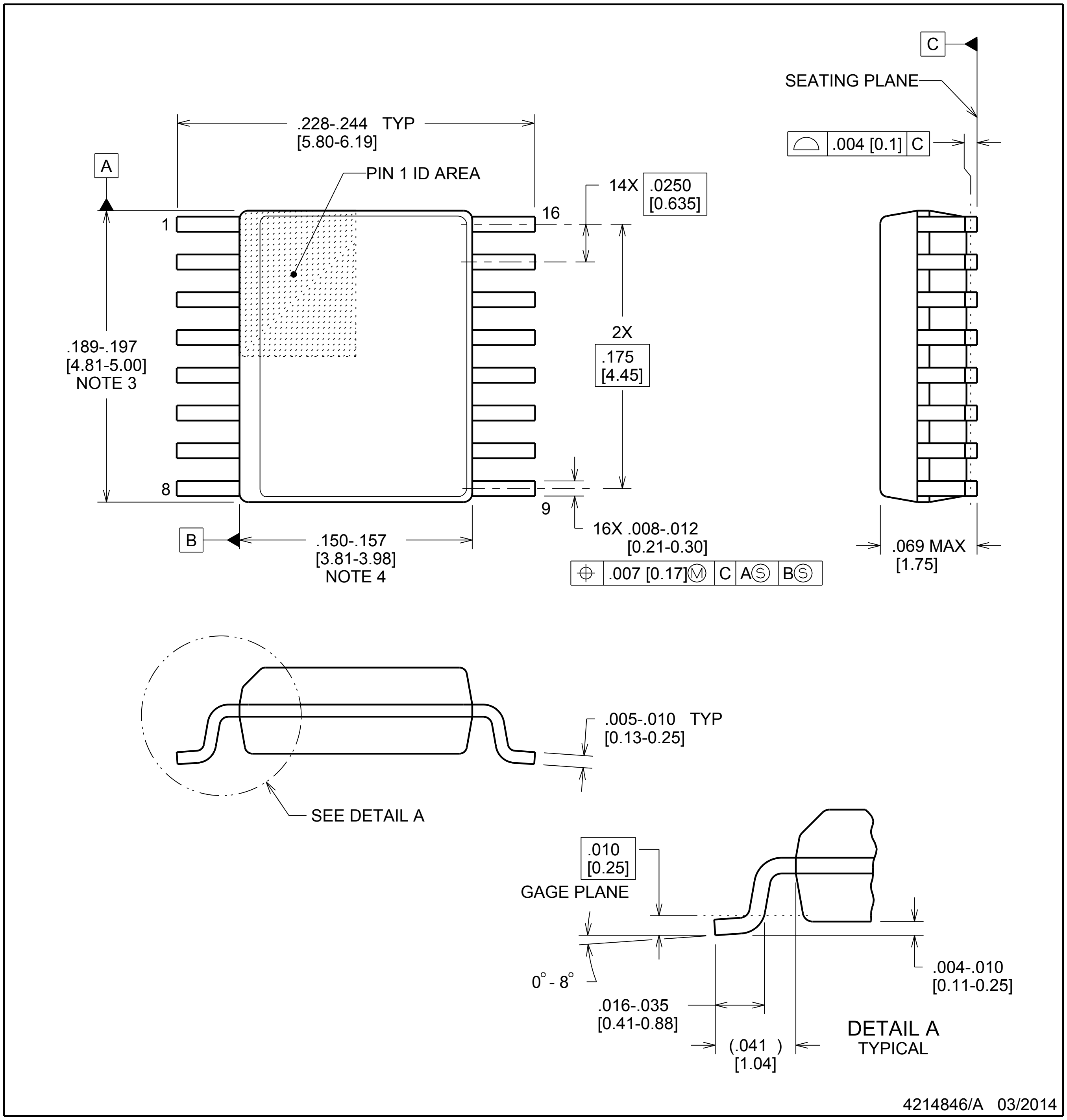


PACKAGE OUTLINE

DBQ0016A

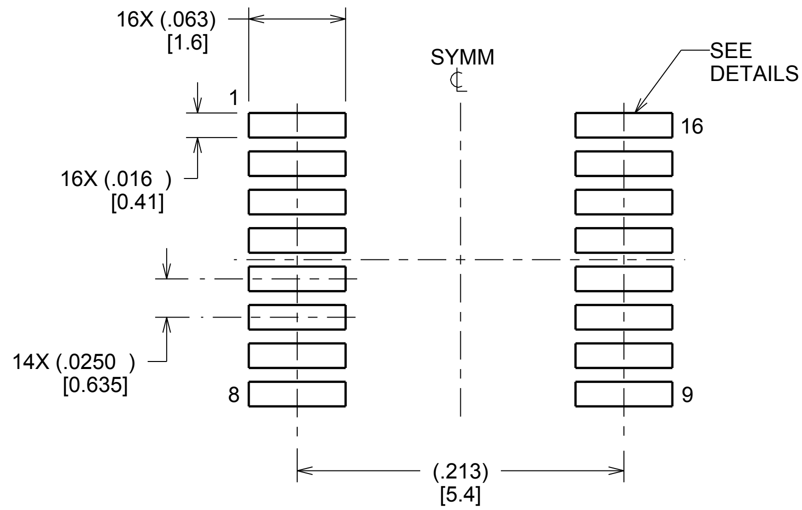
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

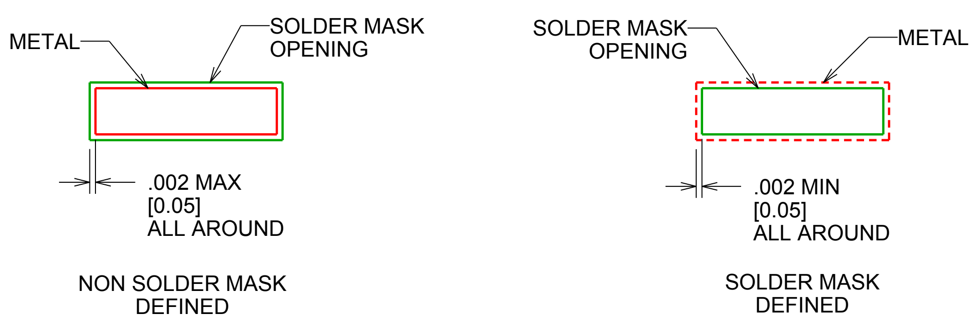


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

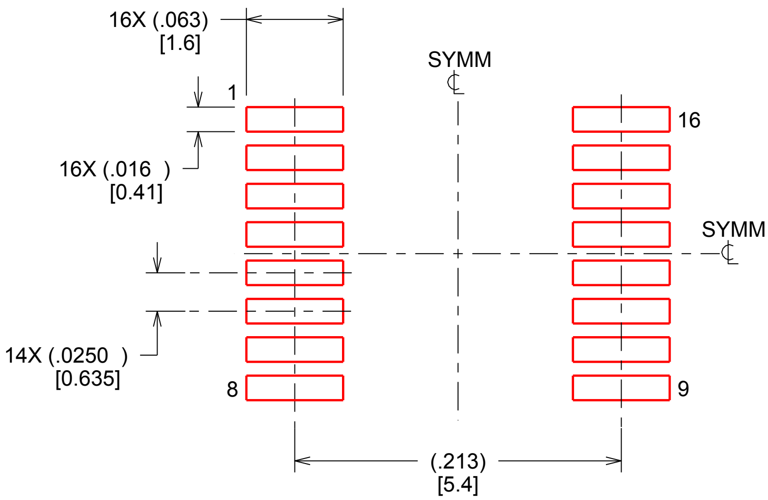


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265