

TLE202x-EP, TLE202xA-EP EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

SGLS235D – FEBRUARY 2004 – REVISED SEPTEMBER 2010

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Also Available in –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Supply Current . . . 300 μ A Max**
- **High Unity-Gain Bandwidth . . . 2 MHz Typ**
- **High Slew Rate . . . 0.45 V/ μ s Min**
- **Supply-Current Change Over Full Temp Range . . . 10 μ A Typ at $V_{CC\pm} = \pm 15$ V**
- **Specified for Both 5-V Single-Supply and ± 15 -V Operation**
- **Phase-Reversal Protection**
- **High Open-Loop Gain . . . 6.5 V/ μ V (136 dB) Typ**
- **Low Offset Voltage . . . 100 μ V Max**
- **Offset Voltage Drift With Time 0.005 μ V/mo Typ**
- **Low Input Bias Current . . . 50 nA Max**
- **Low Noise Voltage . . . 19 nV/ $\sqrt{\text{Hz}}$ Typ**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description

The TLE202x and TLE202xA devices are precision, high-speed, low-power operational amplifiers using a new Texas Instruments Excalibur process. These devices combine the best features of the OP21 with highly improved slew rate and unity-gain bandwidth.

The complementary bipolar Excalibur process utilizes isolated vertical pnp transistors that yield dramatic improvement in unity-gain bandwidth and slew rate over similar devices.

The addition of a bias circuit in conjunction with this process results in extremely stable parameters with both time and temperature. This means that a precision device remains a precision device even with changes in temperature and over years of use.

This combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices the ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. In addition, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

A variety of options are available in small-outline packaging for high-density systems applications.

The Q-suffix devices are characterized for operation over the full automotive temperature range of –40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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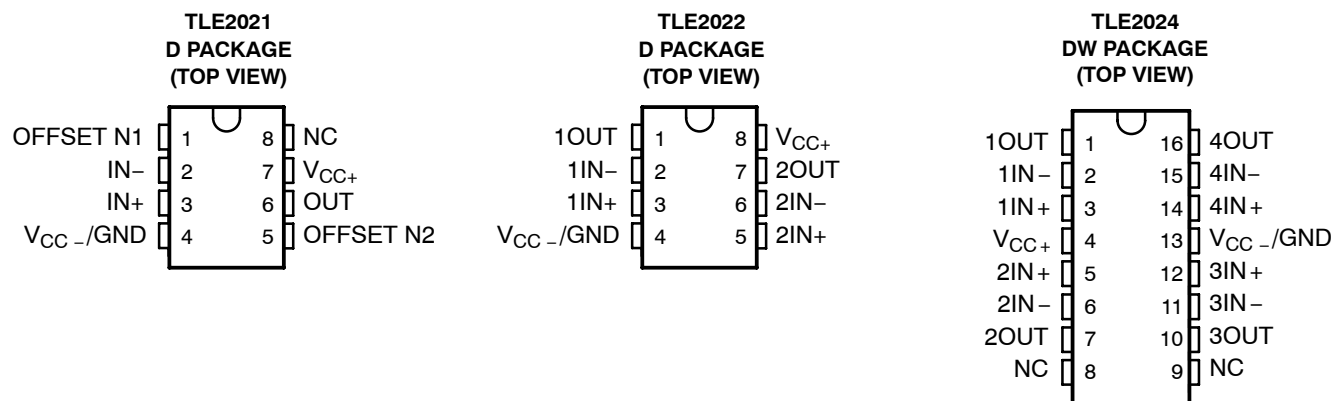
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ORDERING INFORMATION

T_A	$V_{IO,max}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	300 μ V	SOIC (D)	Tape and reel	TLE2021AQDREP	2021AE
	500 μ V	SOIC (D)	Tape and reel	TLE2021QDREP	2021QE
	300 μ V	SOIC (D)	Tape and reel	TLE2022AQDREP	2022AE
	500 μ V	SOIC (D)	Tape and reel	TLE2022QDREP	2022QE
	750 μ V	SOP (DW)	Tape and reel	TLE2024AQDWREP	2024AE
	1000 μ V	SOP (DW)	Tape and reel	TLE2024QDWREP	2024QE
-55°C to 125°C	500 μ V	SOIC (D)	Tape and reel	TLE2021MDREP	2021ME

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

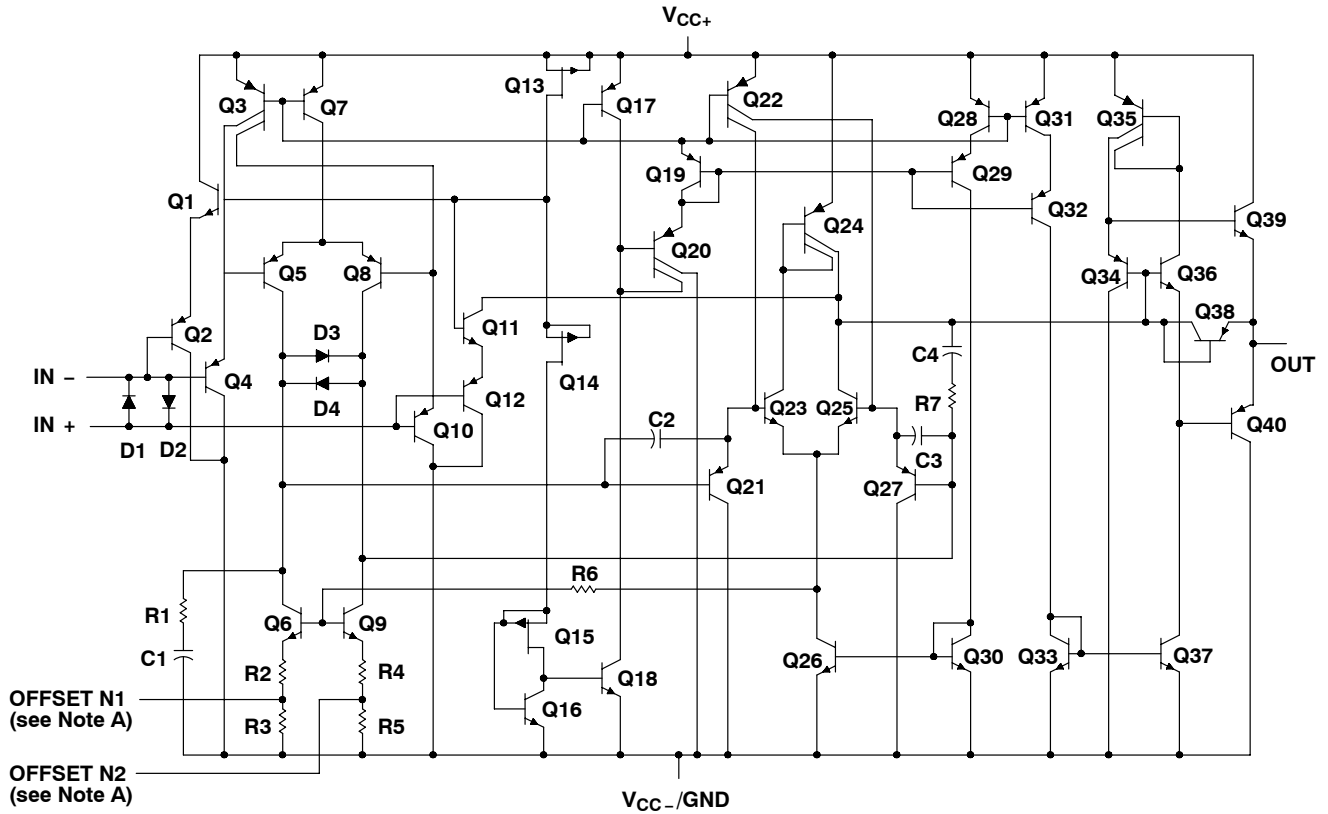


NC - No internal connection

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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT			
COMPONENT	TLE2021	TLE2022	TLE2024
Transistors	40	80	160
Resistors	7	14	28
Diodes	4	8	16
Capacitors	4	8	16

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	20 V
Supply voltage, V_{CC-} (see Note 1)	-20 V
Differential input voltage, V_{ID} (see Note 2)	± 0.6 V
Input voltage range, V_I (any input, see Note 1)	$\pm V_{CC}$
Input current, I_I (each input)	± 1 mA
Output current, I_O (each output):		
TLE2021	± 20 mA
TLE2022	± 30 mA
TLE2024	± 40 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Operating free-air temperature range, T_A : Q suffix	-40°C to 125°C
M suffix	-55°C to 125°C
Package thermal impedance, $R_{\theta JA}$ (see Notes 4 and 5):		
D (8-pin)	97°C/W
DW (16-pin)	57°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 3 seconds: D package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if a differential input voltage in excess of approximately ± 600 mV is applied between the inputs unless some limiting resistance is used.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		± 2	± 20	V
Common-mode input voltage, V_{IC}	$V_{CC} = \pm 5$ V	0	3.2	V
	$V_{CC\pm} = \pm 15$ V	-15	13.2	
Operating free-air temperature, T_A	Q suffix	-40	125	°C
	M suffix	-55	125	



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TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2021-EP			TLE2021A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad R_S = 50\ \Omega$	25°C	120	600		100	400	μV	
		Full range			800		550		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		Full range		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.005			0.005	$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C		0.2	6		0.2	6	nA
		Full range			10			10	
I_{IB} Input bias current		25°C		25	70		25	70	nA
		Full range			90			90	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		0 to 3.5	-0.3 to 4	V	
		Full range	0 to 3.2			0 to 3.2			
V_{OH} High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		4	4.3	V	
Full range			3.8			3.8			
V_{OL} Low-level output voltage		25°C		0.7	0.8		0.7	0.8	V
		Full range			0.95			0.95	
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V}, \quad R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		0.3	1.5	$\text{V}/\mu\text{V}$	
		Full range		0.1			0.1		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, \quad R_S = 50\ \Omega$	25°C	85	110		85	110	dB	
		Full range		80			80		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = 5\ \text{V to } 30\ \text{V}$	25°C	105	120		105	120	dB	
		Full range		100			100		
I_{CC} Supply current	$V_O = 2.5\ \text{V}, \quad \text{No load}$	25°C		170	300		170	300	μA
		Full range			300			300	
ΔI_{CC} Supply current change over operating temperature range		Full range			9			9	μA

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2021MDREP			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	120	600		μV
		Full range	850			
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.2	6		nA
		Full range	10			
I_{IB} Input bias current		25°C	25	70		nA
		Full range	90			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4		V
		Full range	0 to 3.2			
V_{OH} High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3		V
		Full range	3.8			
V_{OL} Low-level output voltage		25°C	0.7	0.8		V
		Full range	0.95			
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5		$\text{V}/\mu\text{V}$
		Full range	0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	85	110		dB
		Full range	80			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to }30\text{ V}$	25°C	105	120		dB
		Full range	100			
I_{CC} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	170	300		μA
		Full range	300			
ΔI_{CC} Supply current change over operating temperature range		Full range	9			μA

† Full range is -55°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2021-EP			TLE2021A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$	25°C	120	500		80	300	μV	
		Full range			700		450		
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage		Full range		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.006			0.006	$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C		0.2	6		0.2	6	nA
		Full range			10			10	
I_{IB} Input bias current	25°C		25	70		25	70	nA	
	Full range			90			90		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range		-15 to 13.2			-15 to 13.2		
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3	V	
Full range			13.8			13.8			
V_{OM-} Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1	V	
		Full range		-13.6			-13.6		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 0\ \text{V},$ $R_L = 10\ \text{k}\Omega$	25°C	1	6.5		1	6.5	$\text{V}/\mu\text{V}$	
		Full range		0.5			0.5		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin},$ $R_S = 50\ \Omega$	25°C	100	115		100	115	dB	
		Full range		96			96		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	105	120		105	120	dB	
		Full range		100			100		
I_{CC} Supply current	$V_O = 0,$ No load	25°C		200	350		200	350	μA
		Full range			350			350	
ΔI_{CC} Supply current change over operating temperature range		Full range			10			10	μA

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLE2021 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2021MDREP			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C	120	500		μV
		Full range		800		
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C	0.006			$\mu V/mo$
I_{IO} Input offset current		25°C	0.2	6		nA
		Full range		10		
I_{IB} Input bias current		25°C	25	70		nA
		Full range		90		
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13.5	-15.3 to 14		V
		Full range	-15 to 13.5			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 k\Omega$	25°C	14	14.3		V
		Full range	13.8			
V_{OM-} Maximum negative peak output voltage swing		25°C	-13.7	-14.1		V
		Full range	-13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 0$ V, $R_L = 10 k\Omega$	25°C	1	6.5		$V/\mu V$
		Full range	0.5			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50 \Omega$	25°C	100	115		dB
		Full range	96			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = 2.5$ V to $\pm 3^\circ$ V	25°C	105	120		dB
		Full range	100			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C	200	350		μA
		Full range		350		
ΔI_{CC} Supply current change over operating temperature range		Full range	10			μA

† Full range is $-55^\circ C$ to $125^\circ C$.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2022-EP			TLE2022A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	600			400			μV
		Full range	800			550			
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	6	0.4	6	nA		
		Full range	10			10			
I_{IB} Input bias current		25°C	35	70	33	70	nA		
		Full range	90			90			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	V		
		Full range	0 to 3.2		0 to 3.2				
V_{OH} High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	4	4.3	4	4.3	V		
		Full range	3.8			3.8			
V_{OL} Low-level output voltage		25°C	0.7	0.8	0.7	0.8	V		
		Full range	0.95			0.95			
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\text{ V to }4\text{ V}, R_L = 10\ \text{k}\Omega$	25°C	0.3	1.5	0.4	1.5	$\text{V}/\mu\text{V}$		
		Full range	0.1			0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	85	100	87	102	dB		
		Full range	80			82			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = 5\text{ V to }30\text{ V}$	25°C	100	115	103	118	dB		
		Full range	95			98			
I_{CC} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	450	600	450	600	μA		
		Full range	600			600			
ΔI_{CC} Supply current change over operating temperature range		Full range	37			37			μA

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLE2022 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2022-EP			TLE2022A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	150	500		120	300	μV	
		Full range		700		450			
αV_{IO} Temperature coefficient of input offset voltage		Full range	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	6		0.4	6	nA	
		Full range		10		10			
I_{IB} Input bias current	25°C	35	70		33	70	nA		
	Full range		90		90				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	14	14.3		14	14.3	V	
		Full range	13.8			13.8			
V_{OM-} Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.8	4		1	7	$\text{V}/\mu\text{V}$	
		Full range	0.8			1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}, R_S = 50\ \Omega$	25°C	95	106		97	109	dB	
		Full range	91			93			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	100	115		103	118	dB	
		Full range	95			98			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C	550	700		550	700	μA	
		Full range		700		700			
ΔI_{CC} Supply current change over operating temperature range		Full range	60			60		μA	

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2024-EP			TLE2024A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	1100			850			μV
		Full range	1300			1050			
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.005			0.005			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.6	6	0.5	6	nA		
		Full range	10			10			
I_{IB} Input bias current	25°C	45	70	40	70	nA			
	Full range	90			90				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3.5	-0.3 to 4	0 to 3.5	-0.3 to 4	V		
		Full range	0 to 3.2		0 to 3.2				
V_{OH} High-level output voltage	$R_L = 10\ \text{k}\Omega$	25°C	3.9	4.2	3.9	4.2	V		
		Full range	3.7			3.7			
V_{OL} Low-level output voltage		25°C	0.7	0.8	0.7	0.8	V		
		Full range	0.95			0.95			
A_{VD} Large-signal differential voltage amplification	$V_O = 1.4\ \text{V to } 4\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.2	1.5	0.3	1.5	$\text{V}/\mu\text{V}$		
		Full range	0.1			0.1			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	80	90	82	92	dB		
		Full range	80			82			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	98	112	100	115	dB		
		Full range	93			95			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C	800	1200	800	1200	μA		
		Full range	1200			1200			
ΔI_{CC} Supply current change over operating temperature range		Full range	50			50			μA

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLE2024 electrical characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLE2024-EP			TLE2024A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 50\ \Omega$	25°C	1000			750			μV
		Full range	1200			950			
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.006			0.006			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.6	6		0.2	6	nA	
		Full range	10			10			
I_{IB} Input bias current		25°C	50	70		45	70	nA	
	Full range	90			90				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	-15 to 13.5	-15.3 to 14		-15 to 13.5	-15.3 to 14	V	
		Full range	-15 to 13.2			-15 to 13.2			
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	13.8	14.1		13.8	14.2	V	
V_{OM-} Maximum negative peak output voltage swing		25°C	-13.7	-14.1		-13.7	-14.1	V	
		Full range	-13.6			-13.6			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L = 10\ \text{k}\Omega$	25°C	0.4	2		0.8	4	V/ μV	
		Full range	0.4			0.8			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, R_S = 50\ \Omega$	25°C	92	102		94	105	dB	
		Full range	88			90			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 2.5\ \text{V to } \pm 15\ \text{V}$	25°C	98	112		100	115	dB	
		Full range	93			95			
I_{CC} Supply current	$V_O = 0, \text{ No load}$	25°C	1050	1400		1050	1400	μA	
		Full range	1400			1400			
ΔI_{CC} Supply current change over operating temperature range			Full range	85			85		

† Full range is -40°C to 125°C .

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLE2021 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1	25°C		0.5		$\text{V}/\mu\text{s}$
V_n	Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$	25°C		21		nV/Hz
		$f = 1\text{ kHz}$	25°C		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C		0.16		μV
		$f = 0.1\text{ to }10\text{ Hz}$	25°C		0.47		
I_n	Equivalent input noise current		25°C		0.9		pA/Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		1.2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		42°		

TLE2021 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 10\text{ V}$, See Figure 1	25°C	0.45	0.65		$\text{V}/\mu\text{s}$
			Full range	0.4			
V_n	Equivalent input noise voltage (see Figure 2)		$f = 10\text{ Hz}$	25°C	19		nV/Hz
			$f = 1\text{ kHz}$	25°C	15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		$f = 0.1\text{ to }1\text{ Hz}$	25°C	0.16		μV
			$f = 0.1\text{ to }10\text{ Hz}$	25°C	0.47		
I_n	Equivalent input noise current		25°C		0.09		pA/Hz
B_1	Unity-gain bandwidth	See Figure 3	25°C		2		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		46°		

† Full range is -40°C to 125°C for the Q-suffix devices.

TLE2022 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1		0.5		$\text{V}/\mu\text{s}$
V_n	Equivalent input noise voltage (see Figure 2)	$f = 10\text{ Hz}$		21		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$		0.16		μV
		$f = 0.1\text{ to }10\text{ Hz}$		0.47		
I_n	Equivalent input noise current			0.1		$\text{pA}/\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°		



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TLE2022 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 10\text{ V}$, See Figure 1	25°C	0.45	0.65		V/ μs
			Full range	0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19		nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz	25°C		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47		
I_n	Equivalent input noise current		25°C		0.1		pA/ $\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°		

† Full range is -40°C to 125°C.

TLE2024 operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = 1\text{ V to }3\text{ V}$, See Figure 1		0.5		V/ μs
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz		21		nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		0.16		μV
		f = 0.1 to 10 Hz		0.47		
I_n	Equivalent input noise current			0.1		pA/ $\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3		1.7		MHz
ϕ_m	Phase margin at unity gain	See Figure 3		47°		

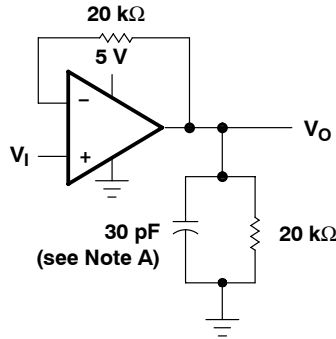
TLE2024 operating characteristics at specified free-air temperature, $V_{CC} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_O = \pm 10\text{ V}$, See Figure 1	25°C	0.45	0.7		V/ μs
			Full range	0.4			
V_n	Equivalent input noise voltage (see Figure 2)	f = 10 Hz	25°C		19		nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz	25°C		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.16		μV
		f = 0.1 to 10 Hz	25°C		0.47		
I_n	Equivalent input noise current		25°C		0.1		pA/ $\sqrt{\text{Hz}}$
B_1	Unity-gain bandwidth	See Figure 3	25°C		2.8		MHz
ϕ_m	Phase margin at unity gain	See Figure 3	25°C		52°		

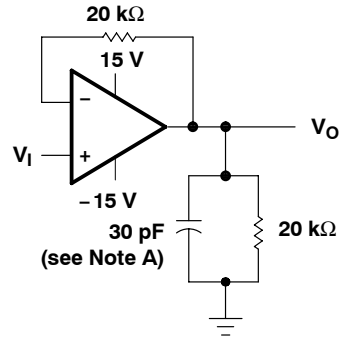
† Full range is -40°C to 125°C.



PARAMETER MEASUREMENT INFORMATION



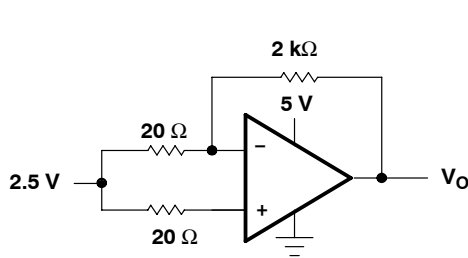
(a) SINGLE SUPPLY



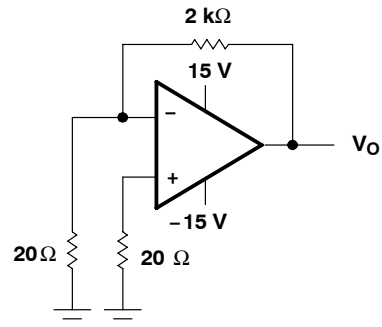
(b) SPLIT SUPPLY

NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

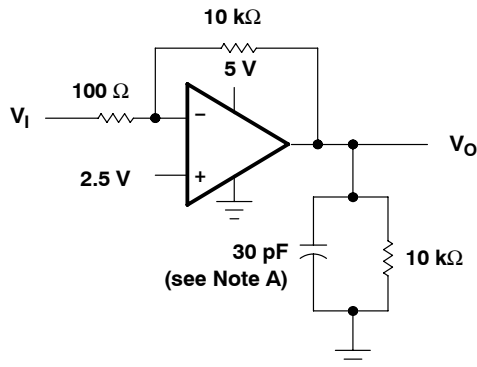


(a) SINGLE SUPPLY

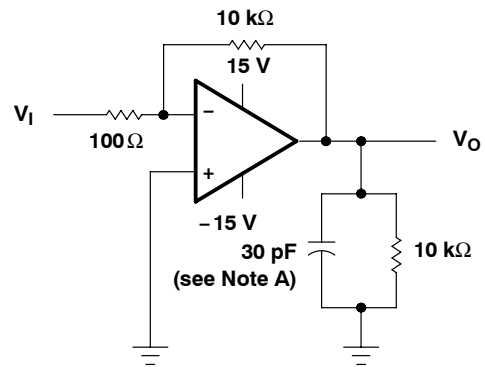


(b) SPLIT SUPPLY

Figure 2. Noise-Voltage Test Circuit



(a) SINGLE SUPPLY



(b) SPLIT SUPPLY

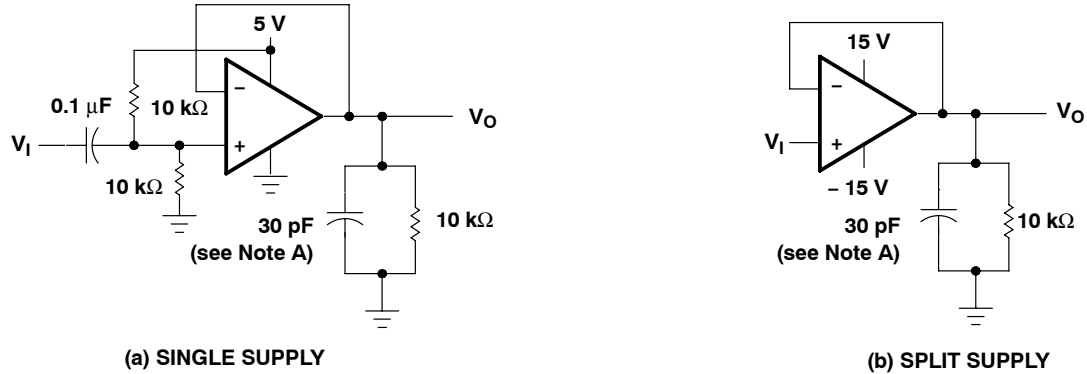
NOTE A: C_L includes fixture capacitance.

Figure 3. Unity-Gain Bandwidth and Phase-Margin Test Circuit

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PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 4. Small-Signal Pulse-Response Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

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Table of Graphs

		FIGURE	
V_{IO}	Input offset voltage	Distribution	5, 6, 7
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	8, 9, 10 11, 12, 13
I_I	Input current	vs Differential input voltage	14
V_{OM}	Maximum peak output voltage	vs Output current vs Free-air temperature	15, 16, 17 18
V_{OH}	High-level output voltage	vs High-level output current vs Free-air temperature	19, 20 21
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	22 23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	24, 25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26 27, 28, 29
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	30 – 33 34 – 37
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	38, 39, 40 41, 42, 43
CMRR	Common-mode rejection ratio	vs Frequency	44, 45, 46
SR	Slew rate	vs Free-air temperature	47, 48, 49
	Voltage-follower small-signal pulse response		50, 51
	Voltage-follower large-signal pulse response		52 – 57
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz 0.1 to 10 Hz	58 59
V_n	Equivalent input noise voltage	vs Frequency	60
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	61, 62 63, 64
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance vs Free-air temperature	65, 66 67, 68 69, 70
	Phase shift	vs Frequency	26



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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLE2021
INPUT OFFSET VOLTAGE**

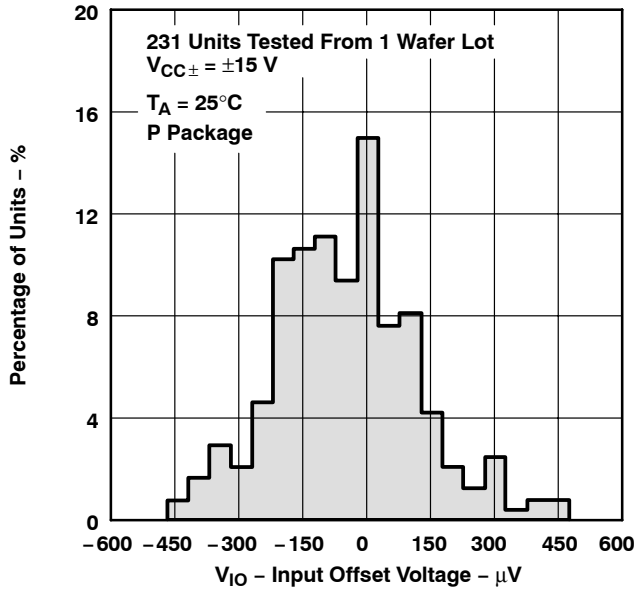


Figure 5

**DISTRIBUTION OF TLE2022
INPUT OFFSET VOLTAGE**

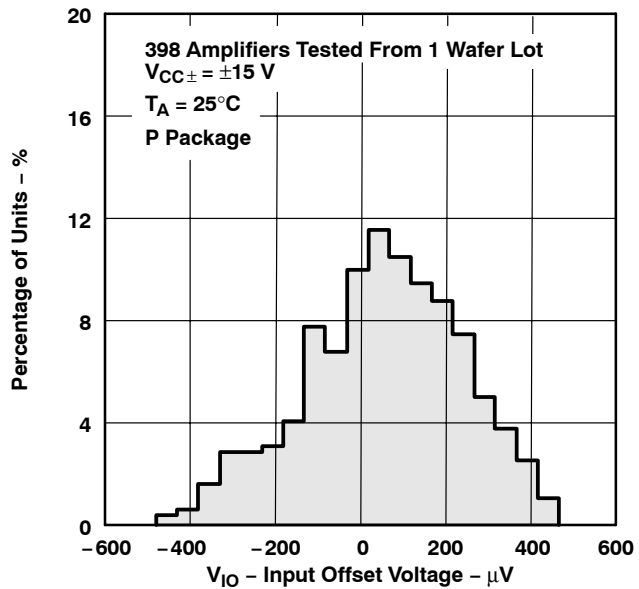


Figure 6

**DISTRIBUTION OF TLE2024
INPUT OFFSET VOLTAGE**

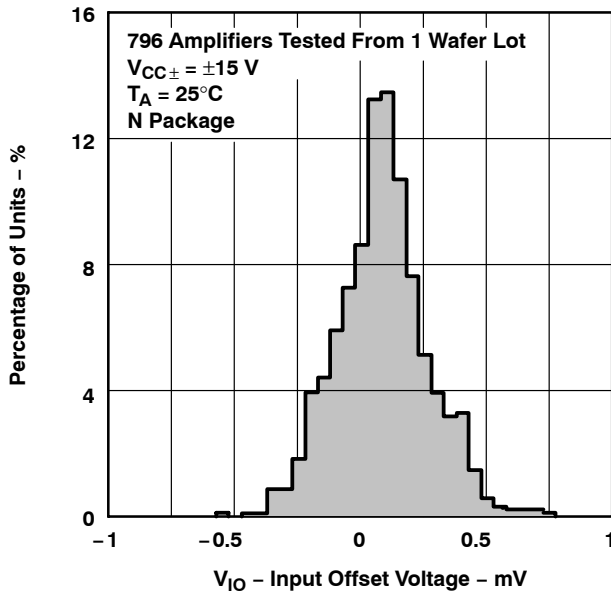


Figure 7

**TLE2021
INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

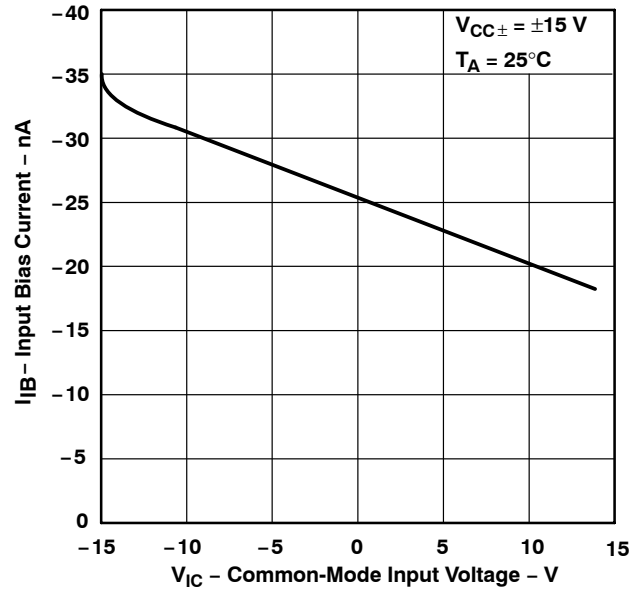
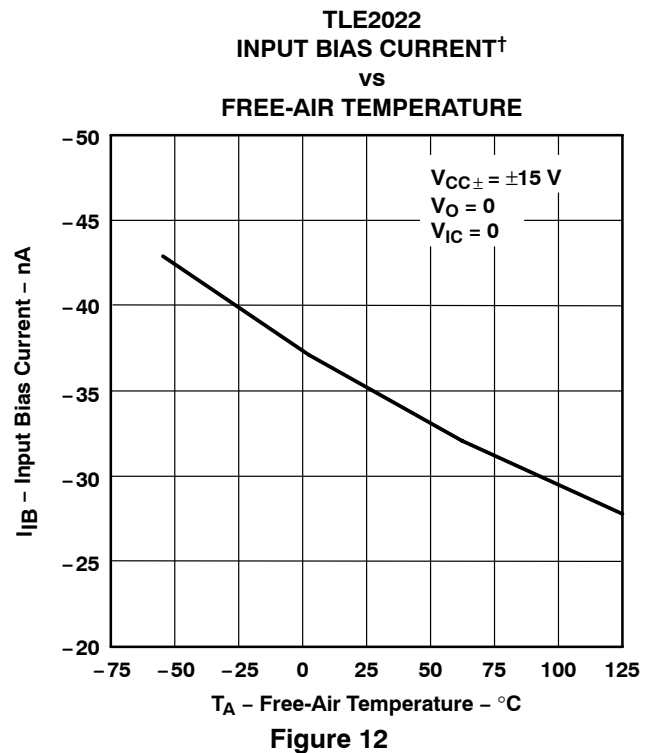
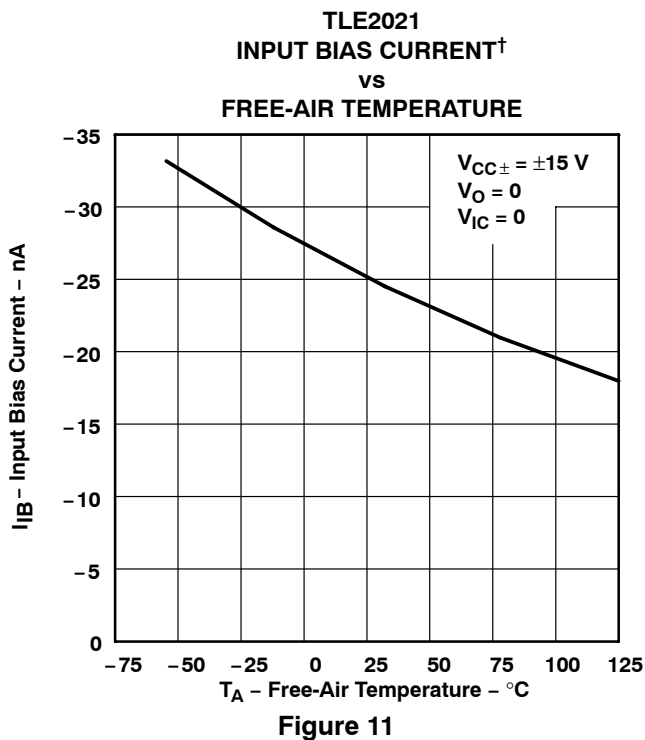
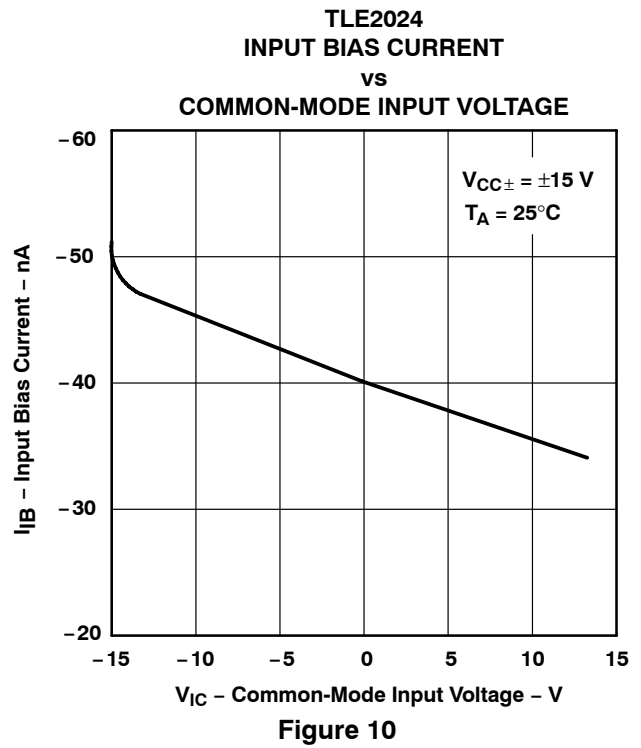
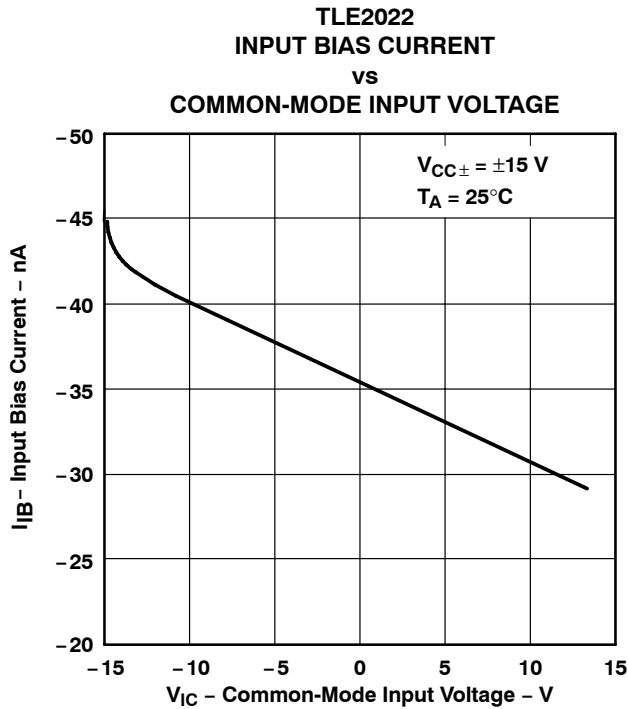


Figure 8

TYPICAL CHARACTERISTICS

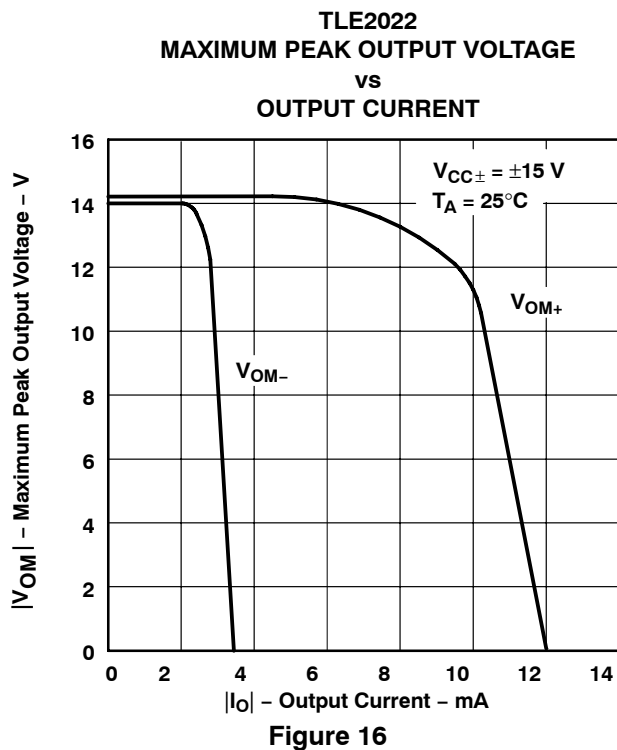
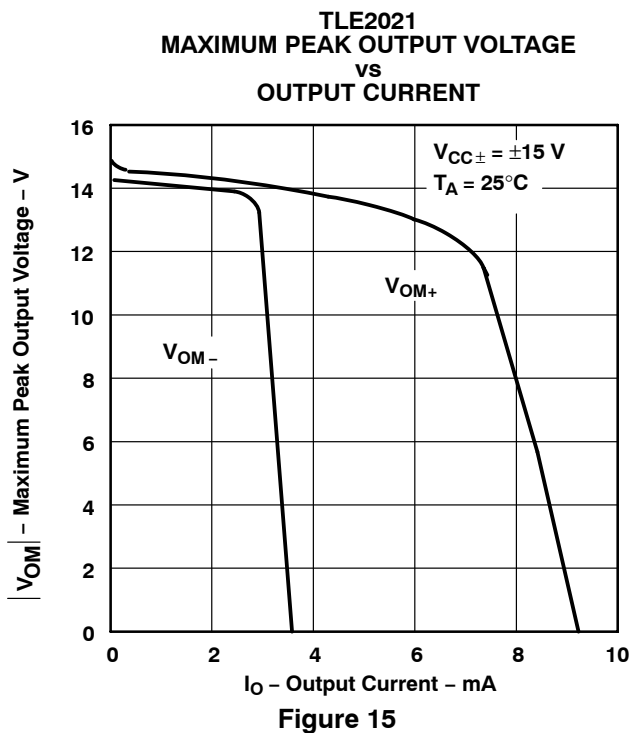
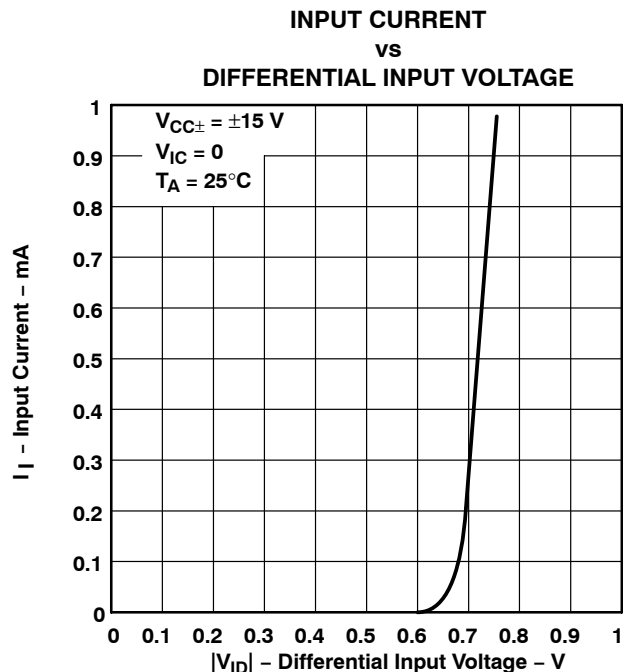
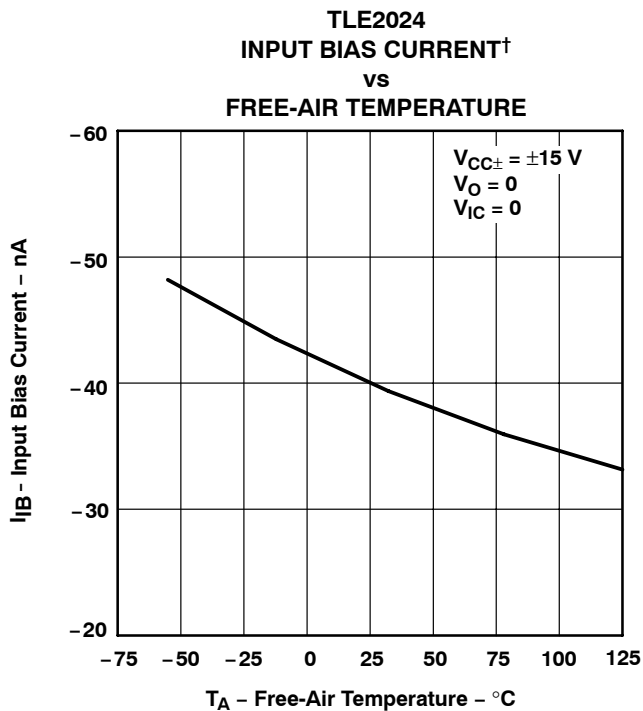


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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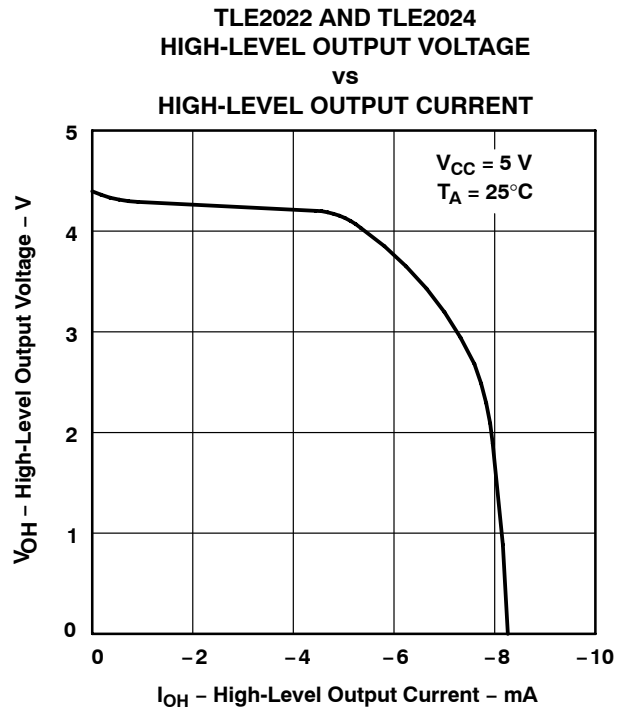
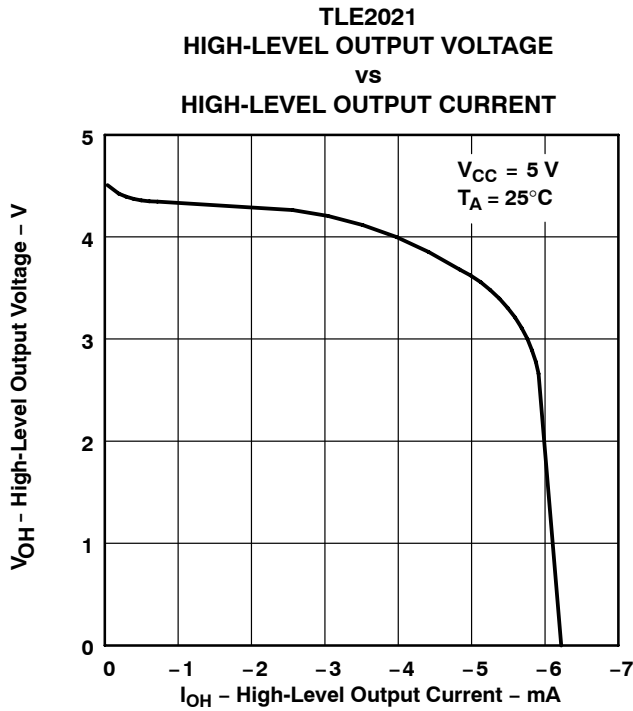
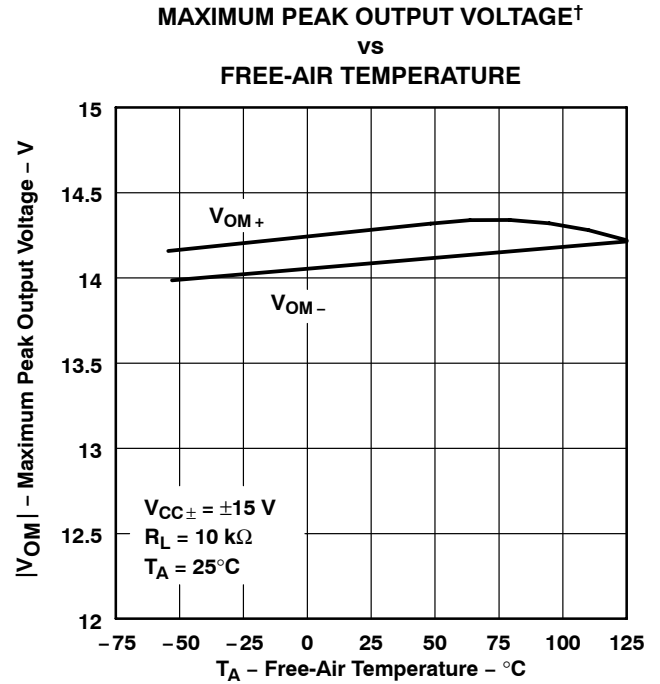
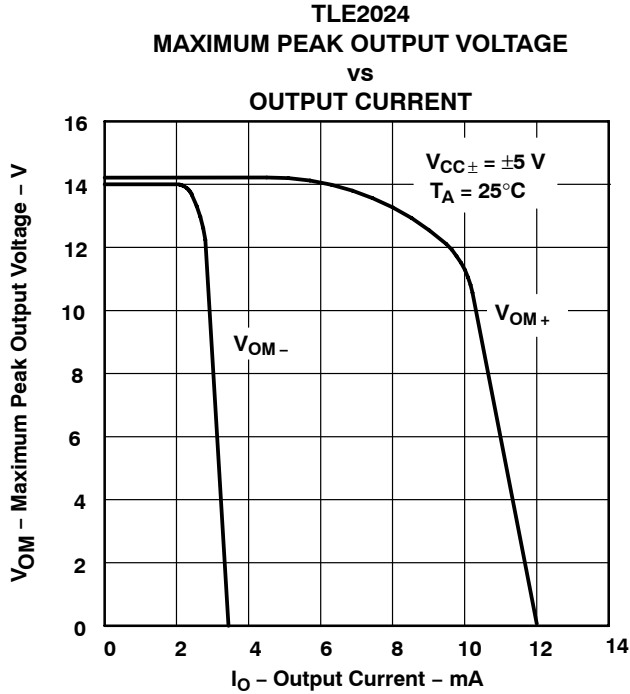
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TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

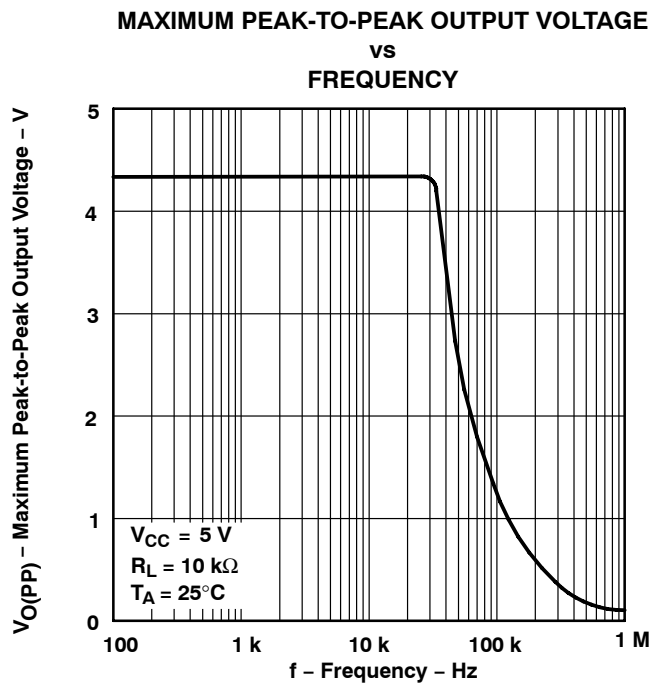
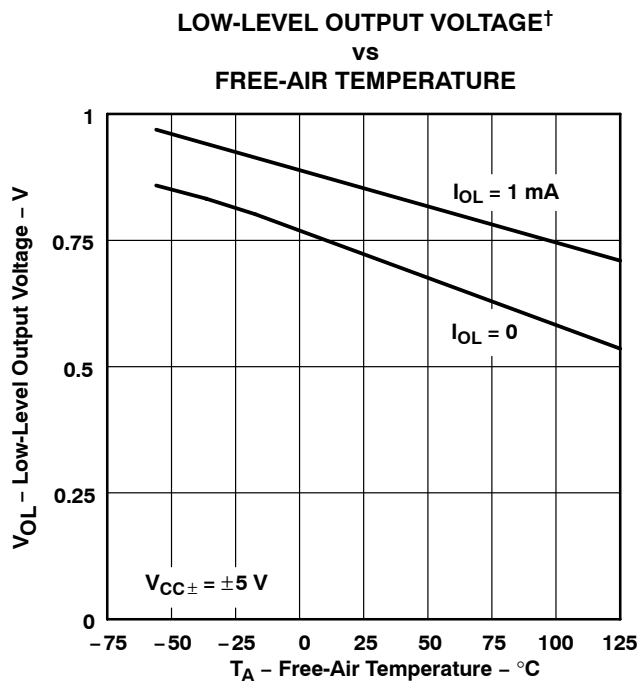
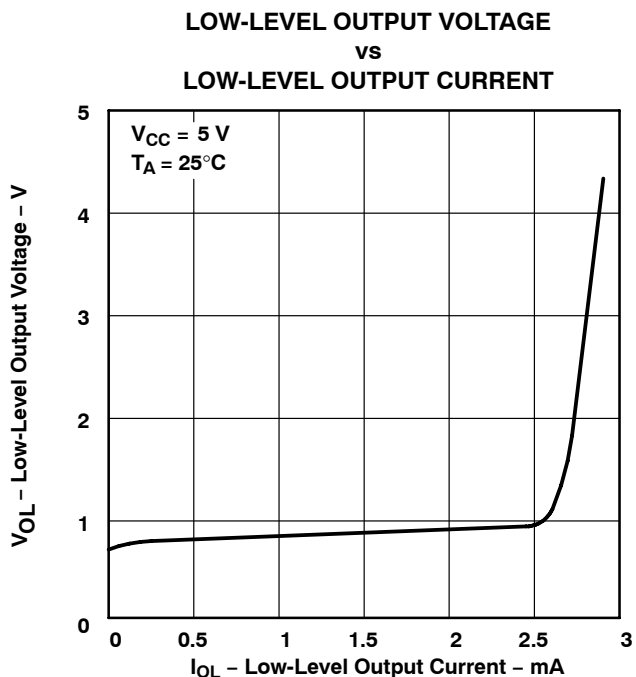
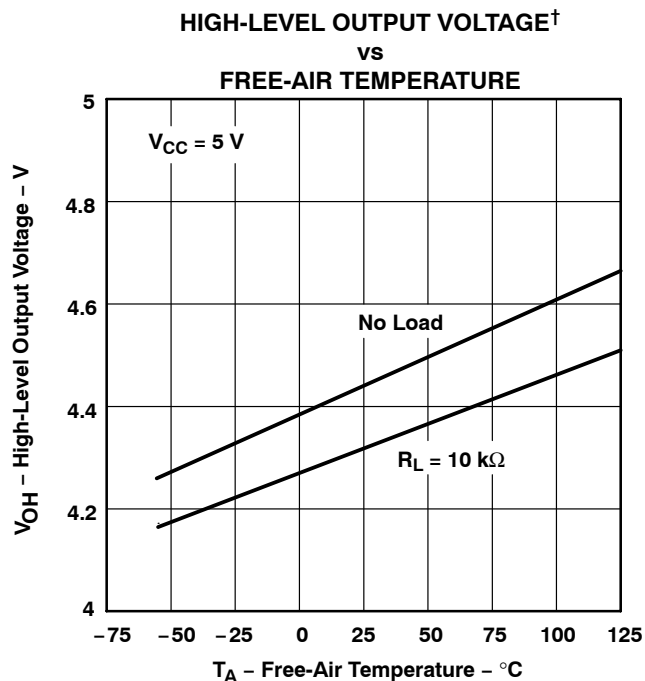


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY

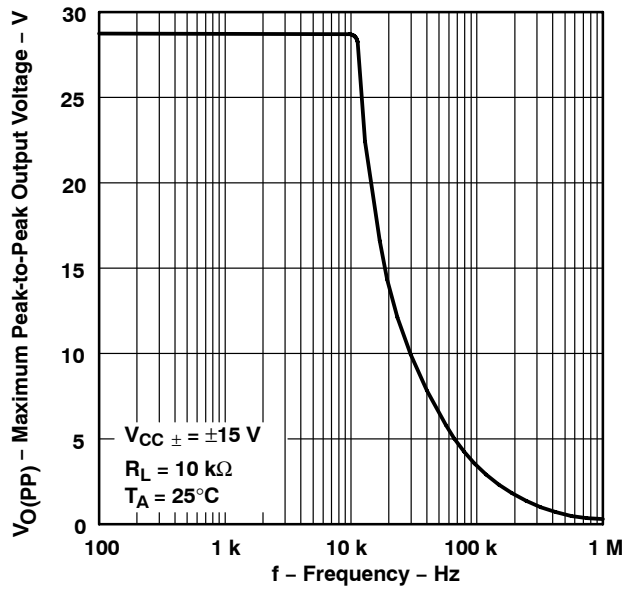


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE SHIFT
 vs
 FREQUENCY

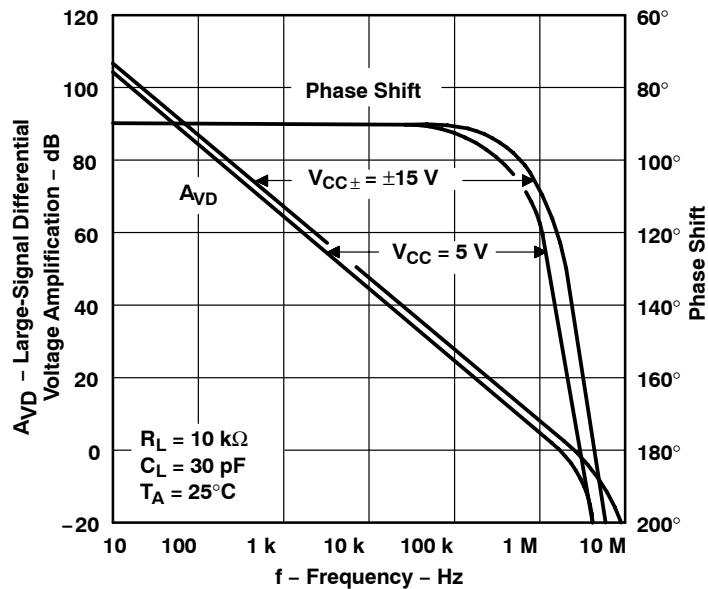


Figure 26

TLE202x-EP, TLE202xA-EP EXCALIBUR HIGH-SPEED LOW-POWER PRECISION OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

TLE2021
LARGE-SCALE DIFFERENTIAL VOLTAGE
AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

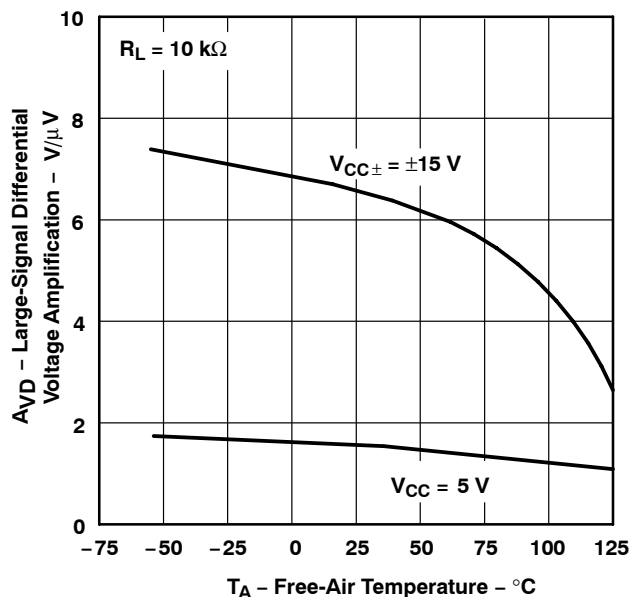


Figure 27

TLE2022
LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

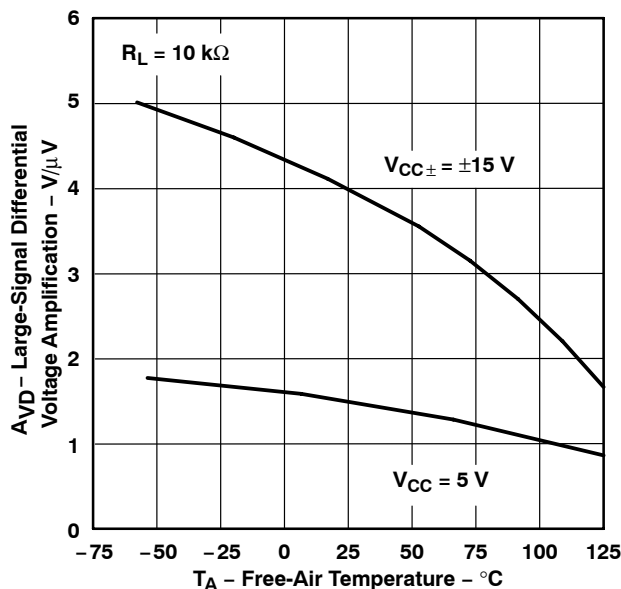


Figure 28

TLE2024
LARGE-SCALE DIFFERENTIAL VOLTAGE
AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

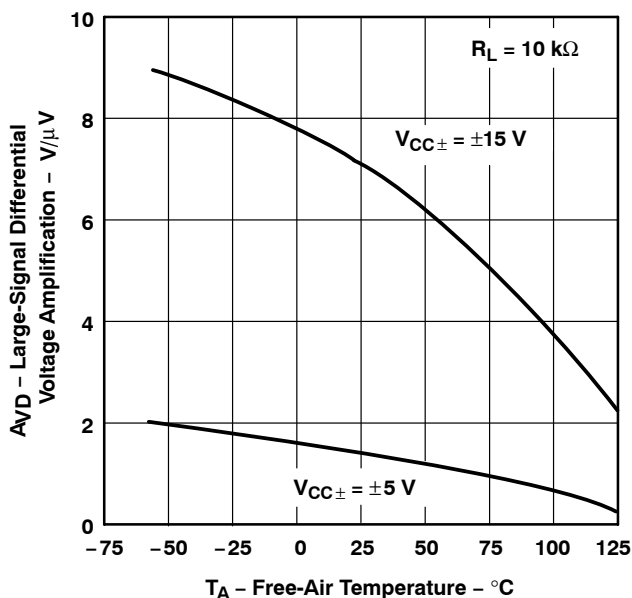


Figure 29

TLE2021
SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

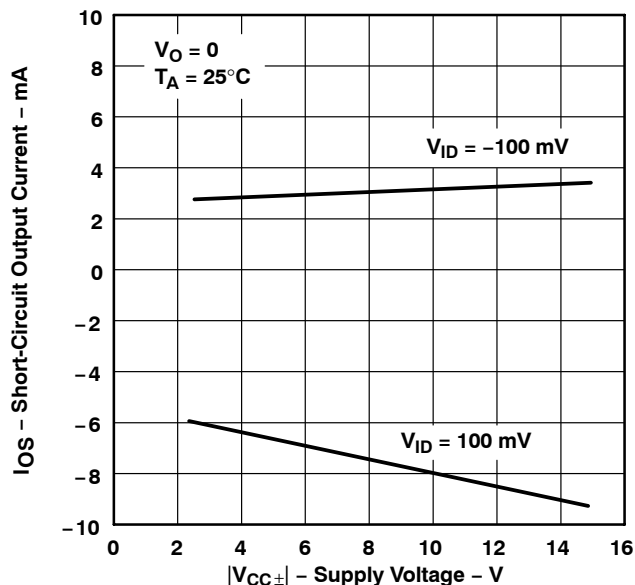
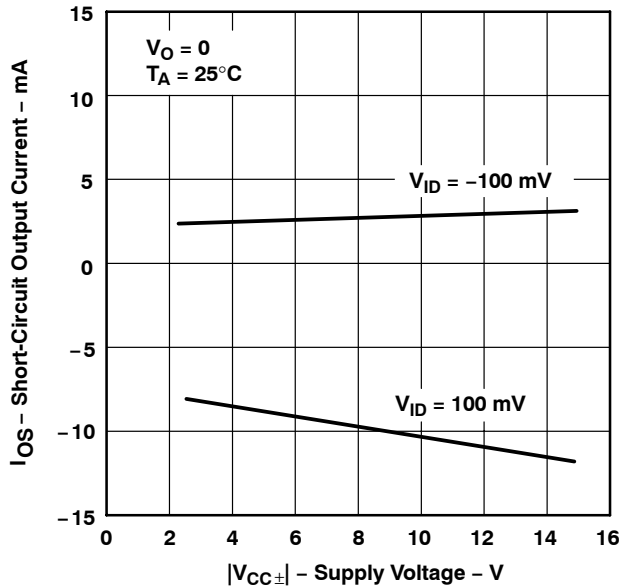


Figure 30

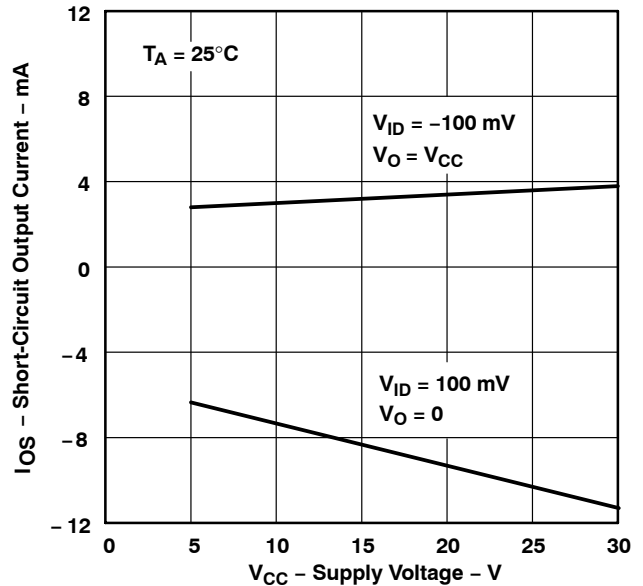
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

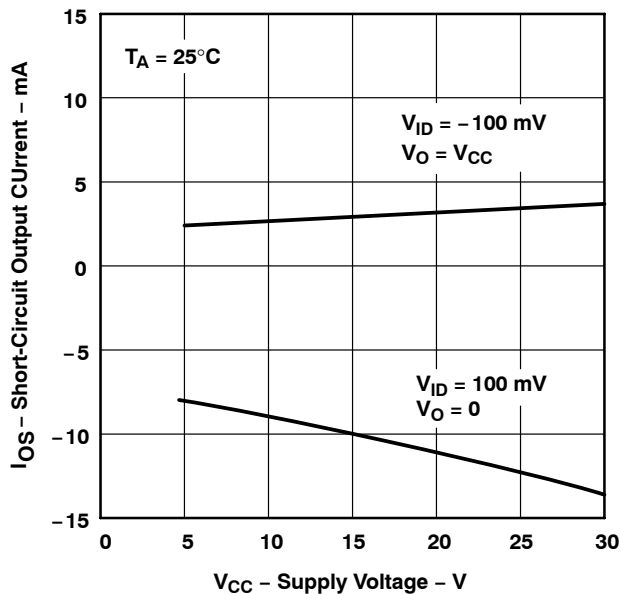
TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE



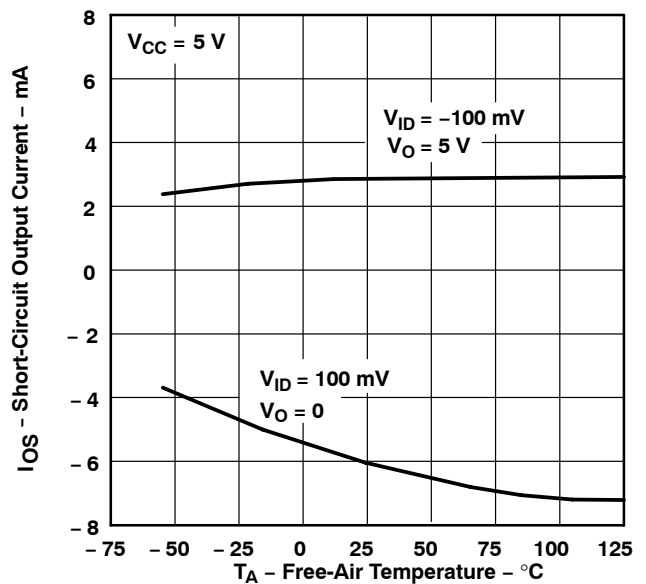
TLE2021
SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE



TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE



TLE2021
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

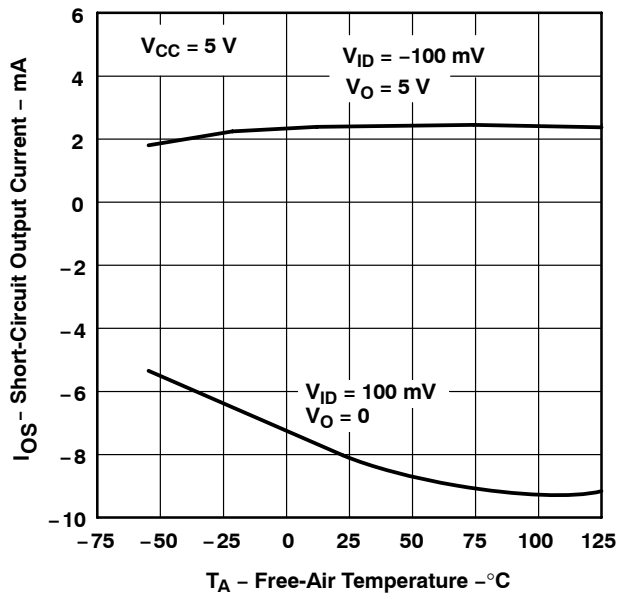


Figure 35

TLE2021
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

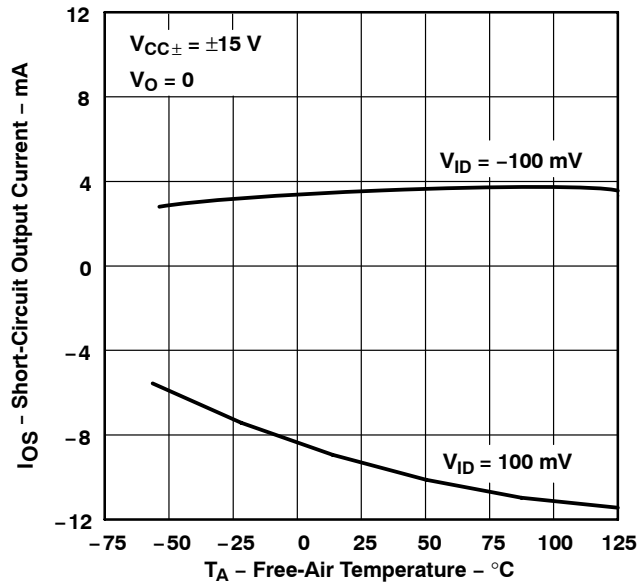


Figure 36

TLE2022 AND TLE2024
SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

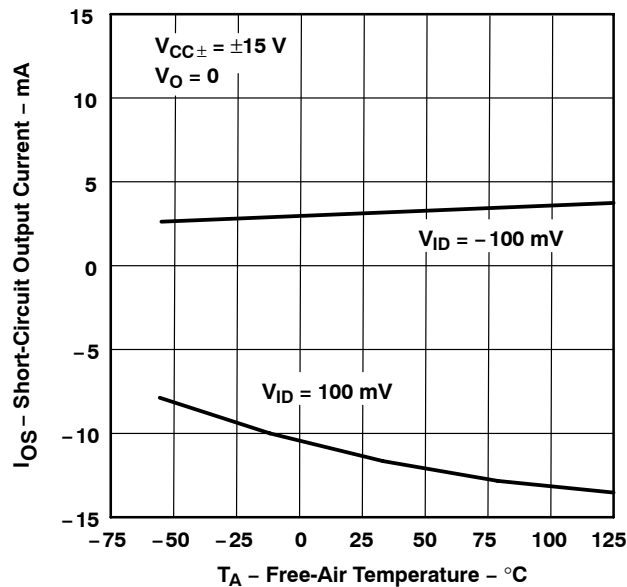


Figure 37

TLE2021
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

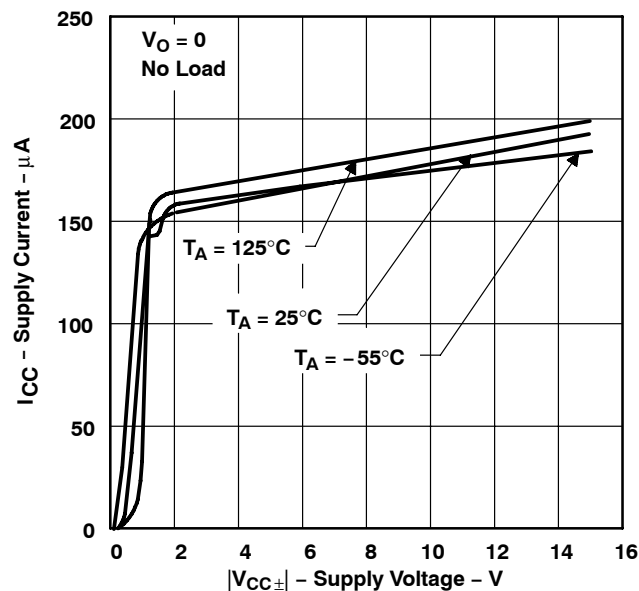


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

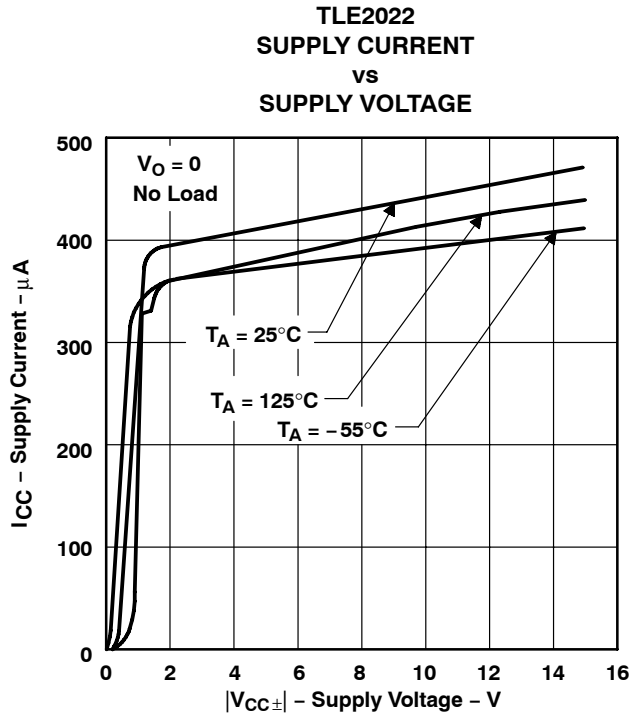


Figure 39

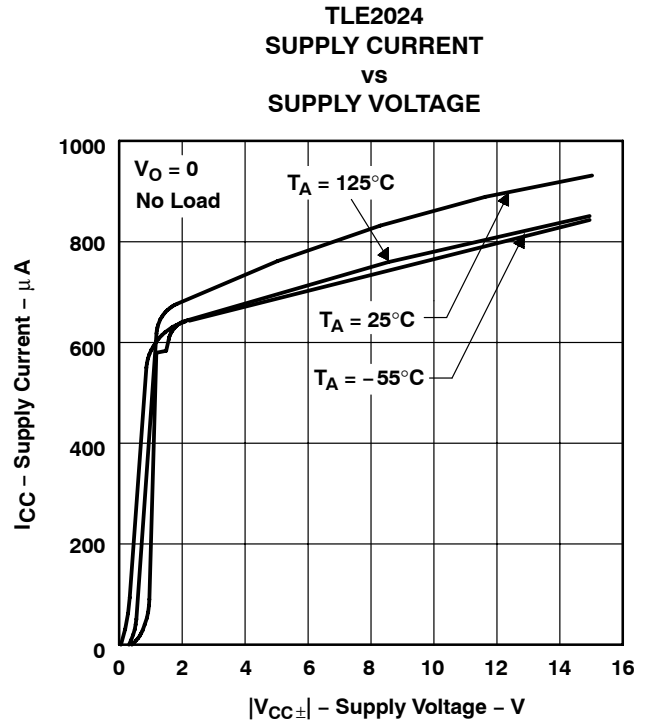


Figure 40

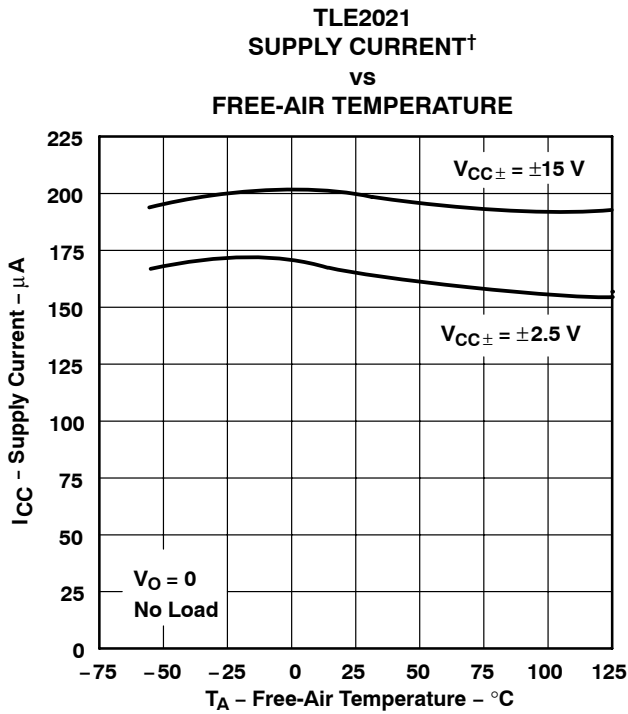


Figure 41

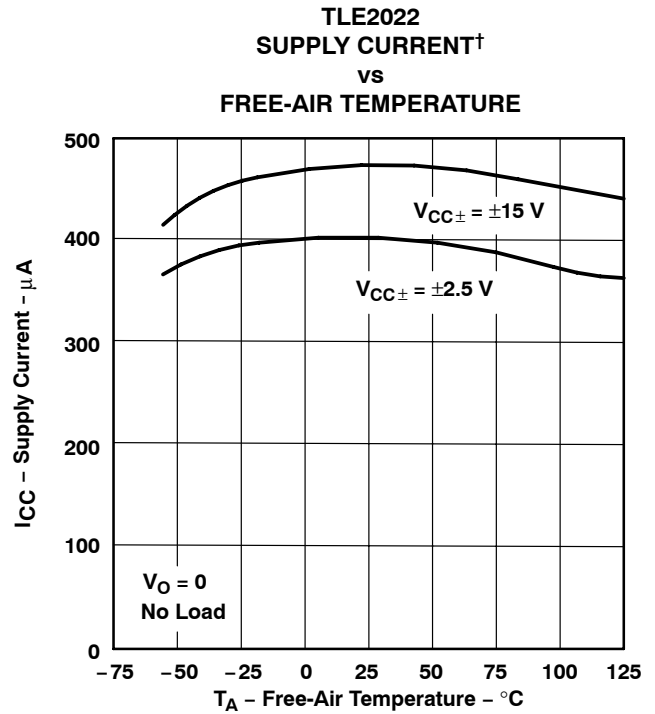


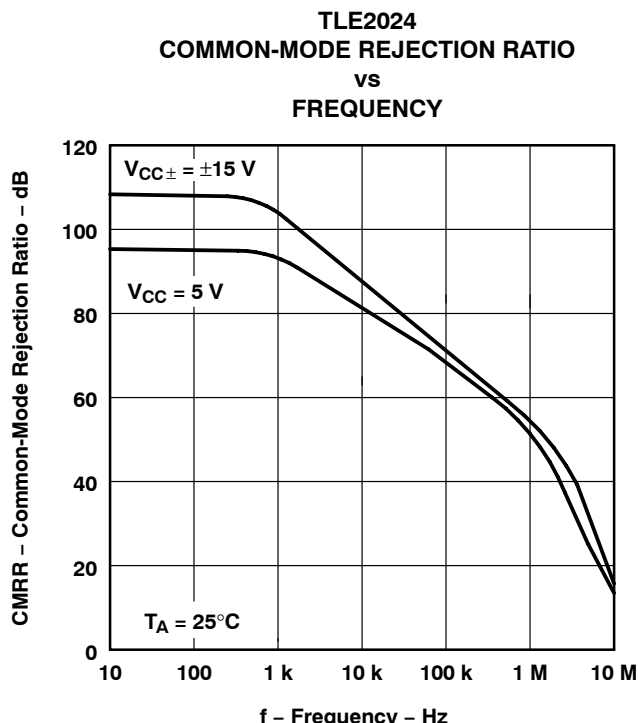
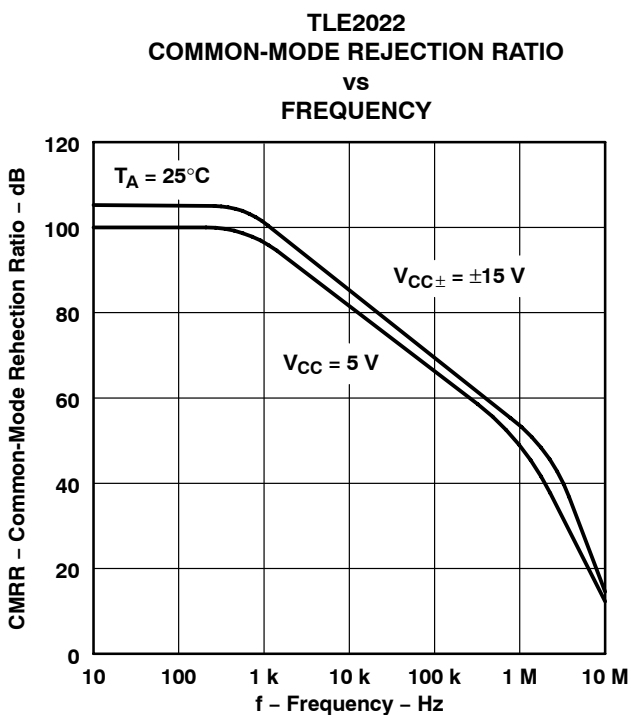
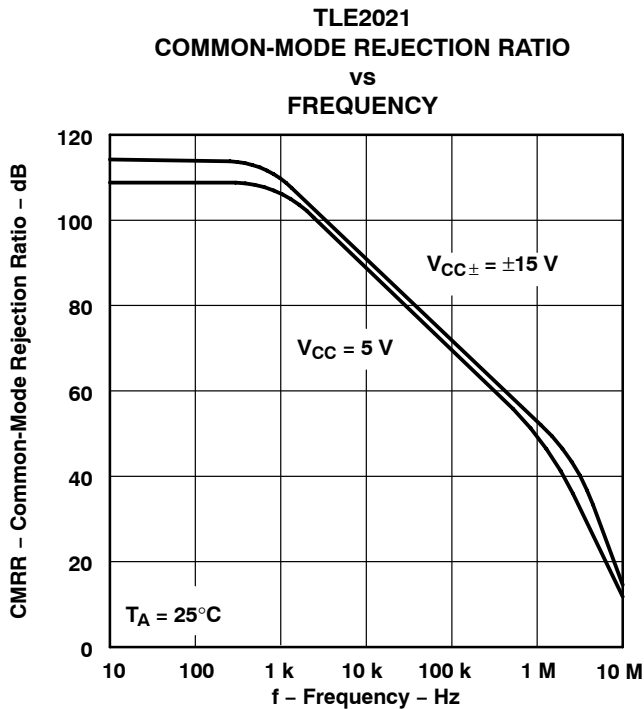
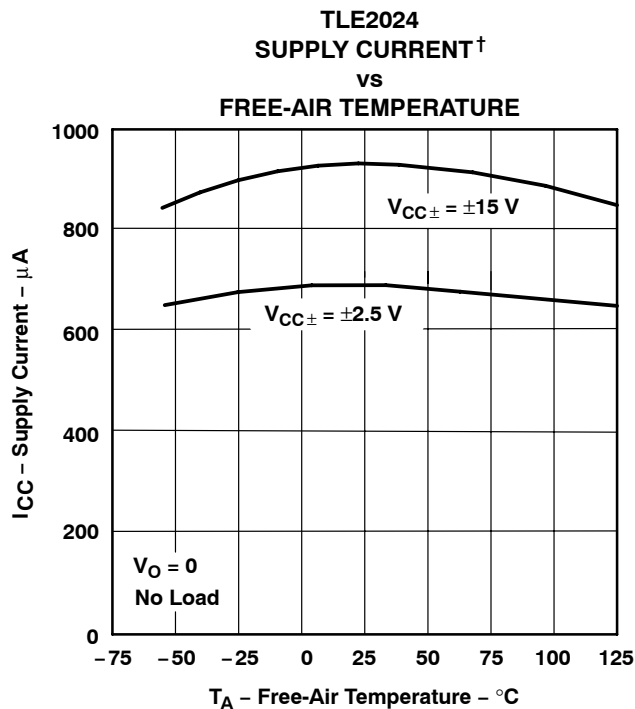
Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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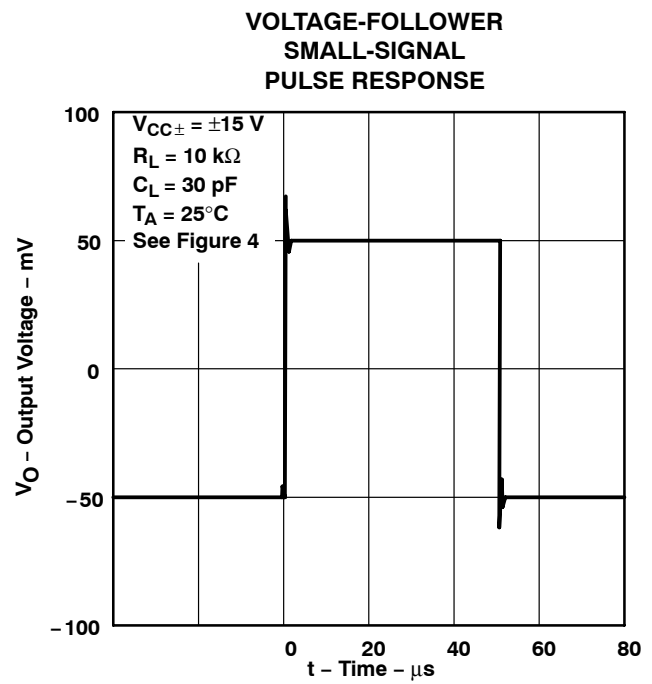
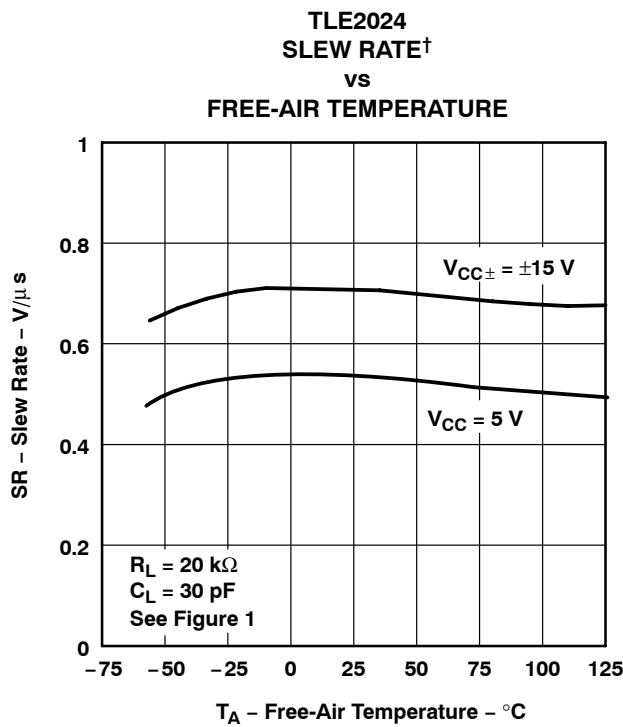
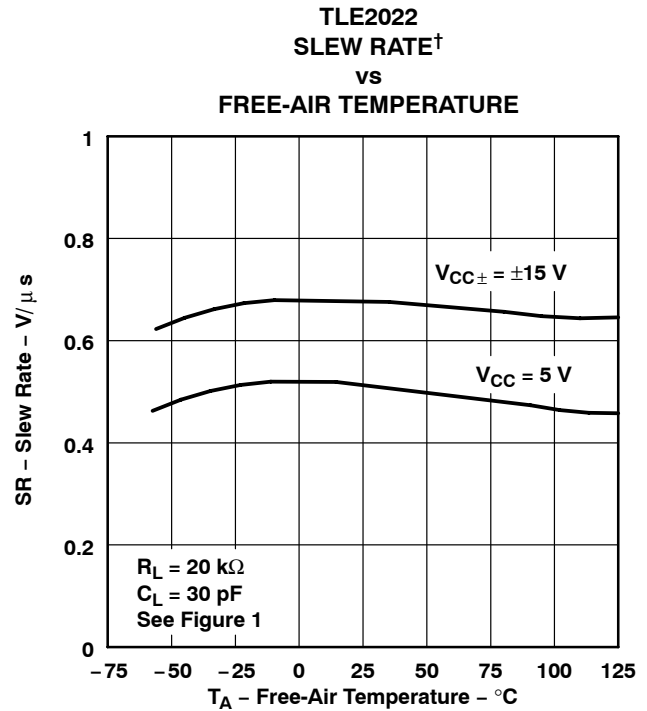
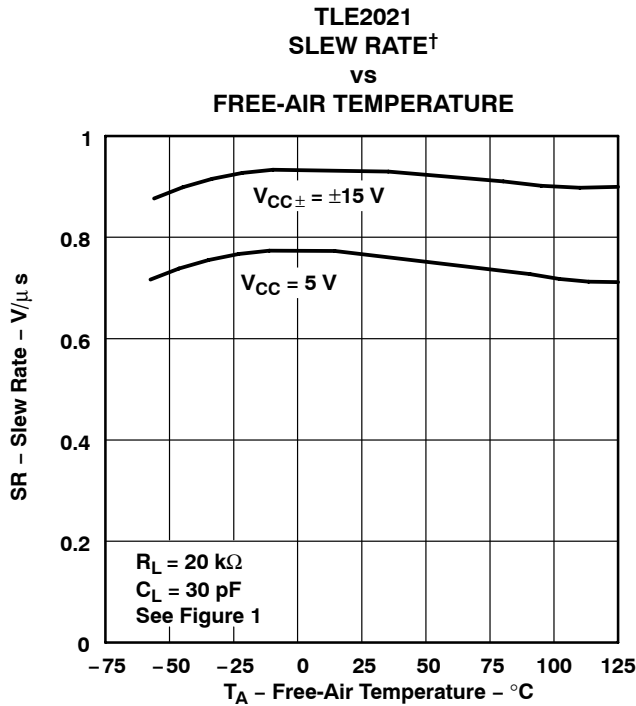
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TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER
 SMALL-SIGNAL
 PULSE RESPONSE**

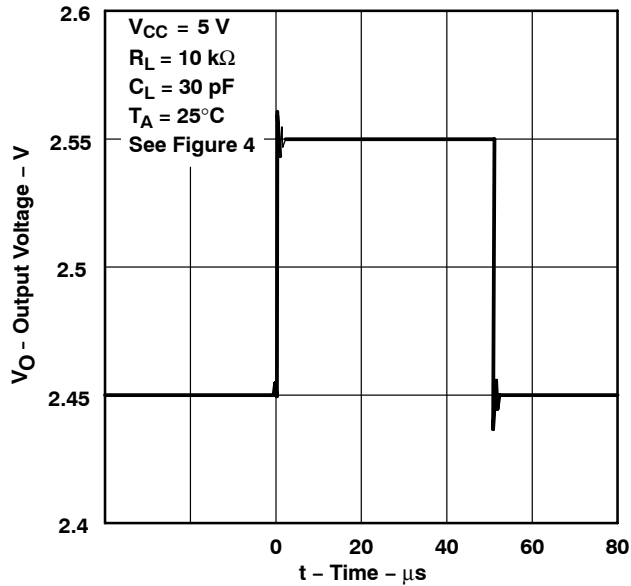


Figure 51

**TLE2021
 VOLTAGE-FOLLOWER LARGE-SIGNAL
 PULSE RESPONSE**

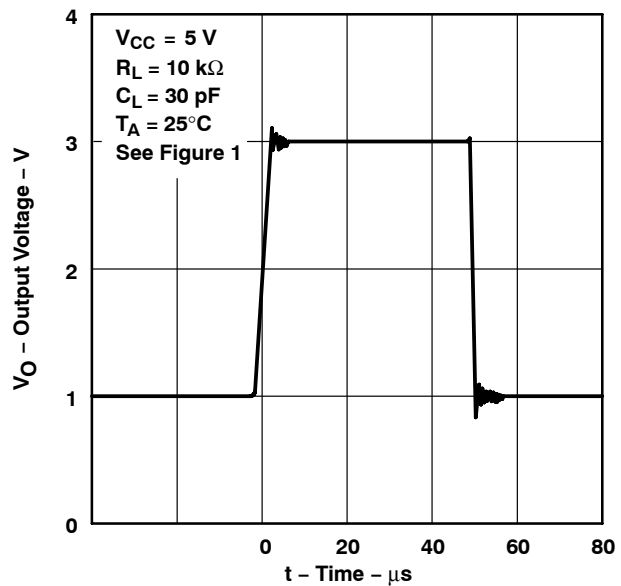


Figure 52

**TLE2022
 VOLTAGE-FOLLOWER LARGE-SIGNAL
 PULSE RESPONSE**

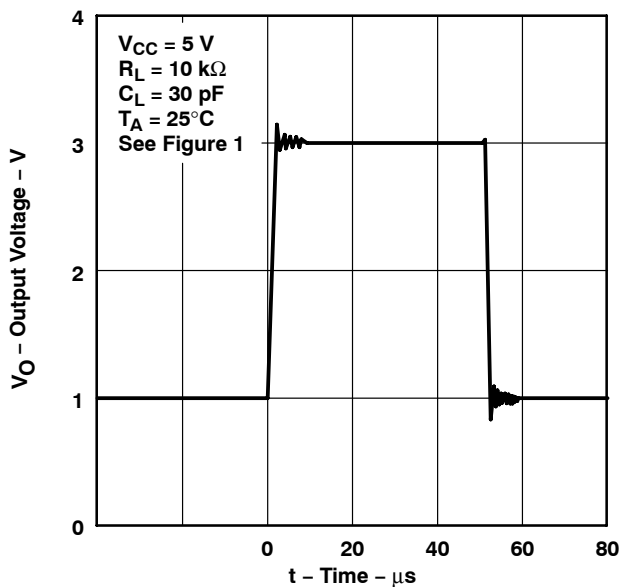


Figure 53

**TLE2024
 VOLTAGE-FOLLOWER LARGE-SCALE
 PULSE RESPONSE**

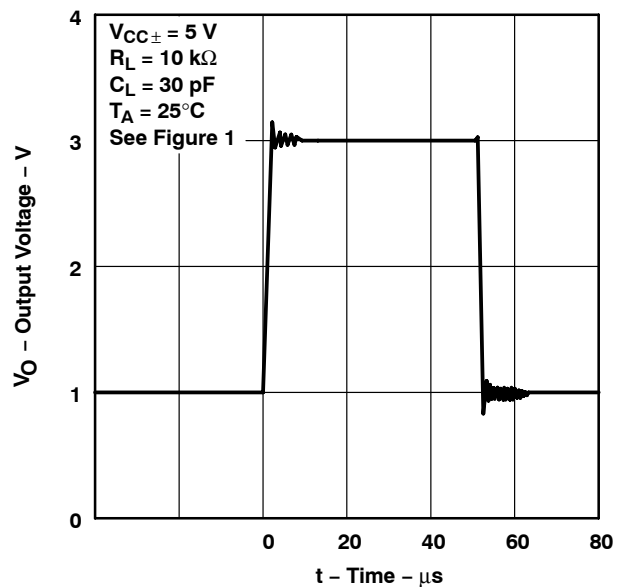
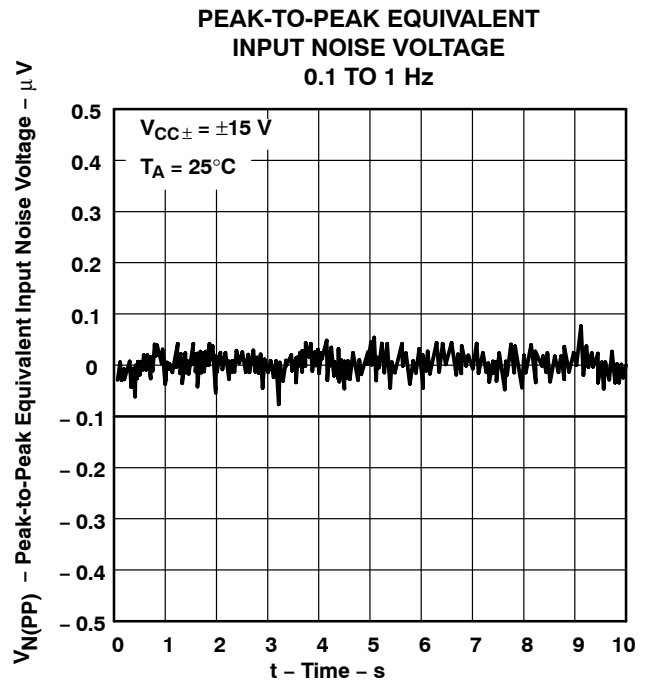
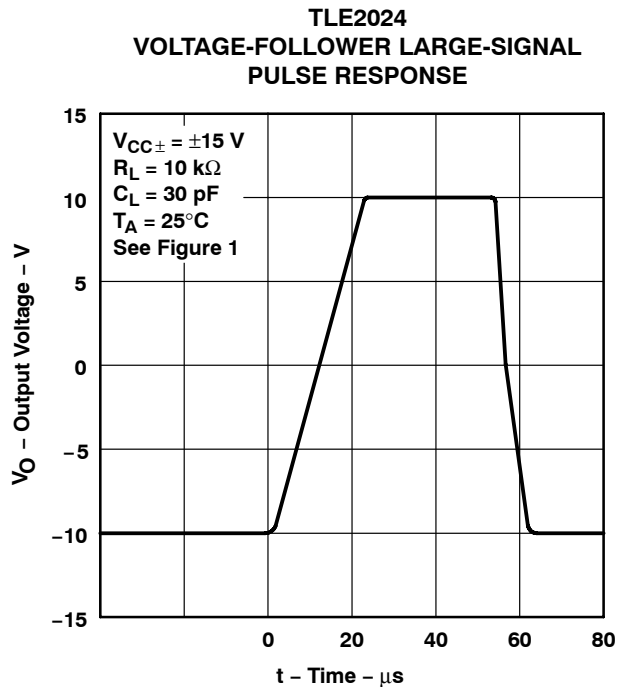
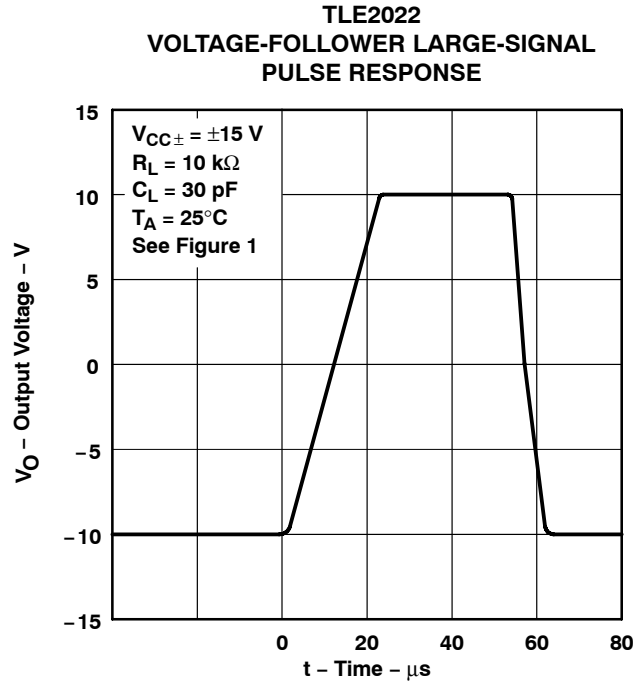
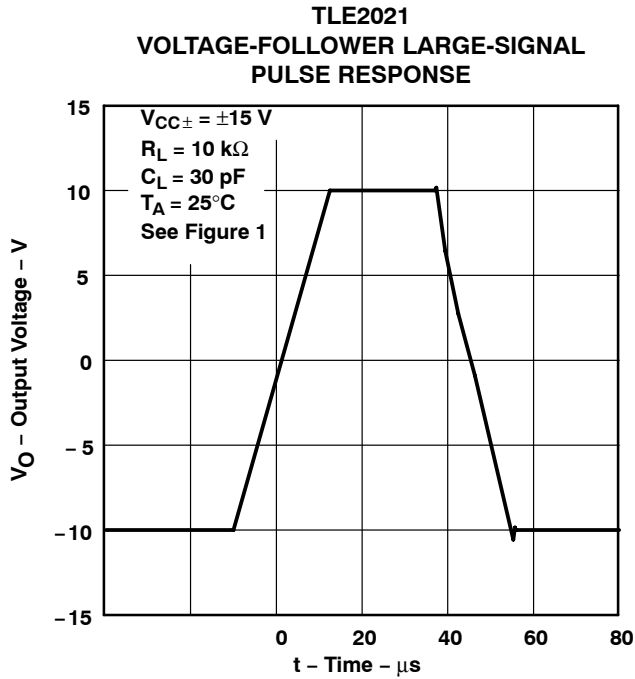


Figure 54



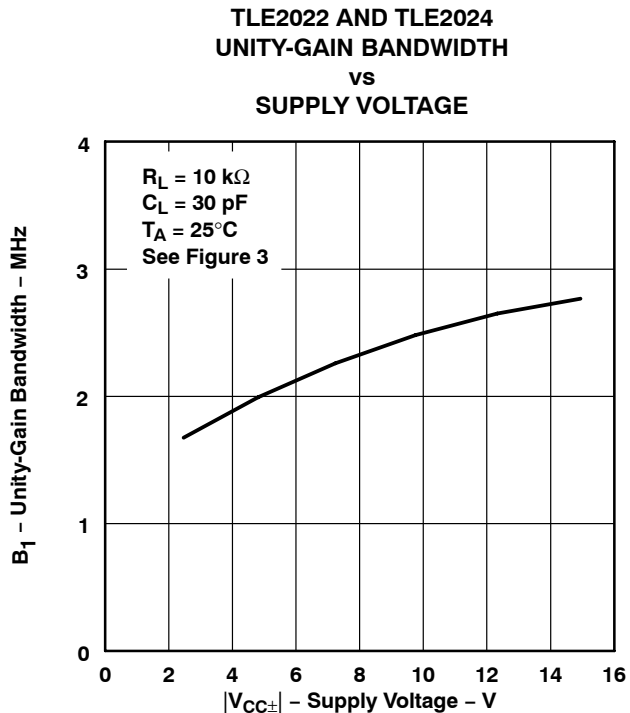
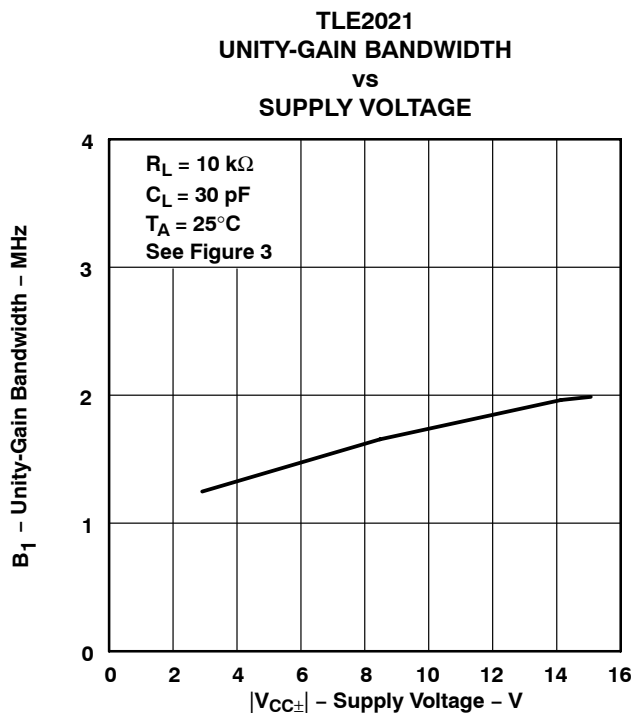
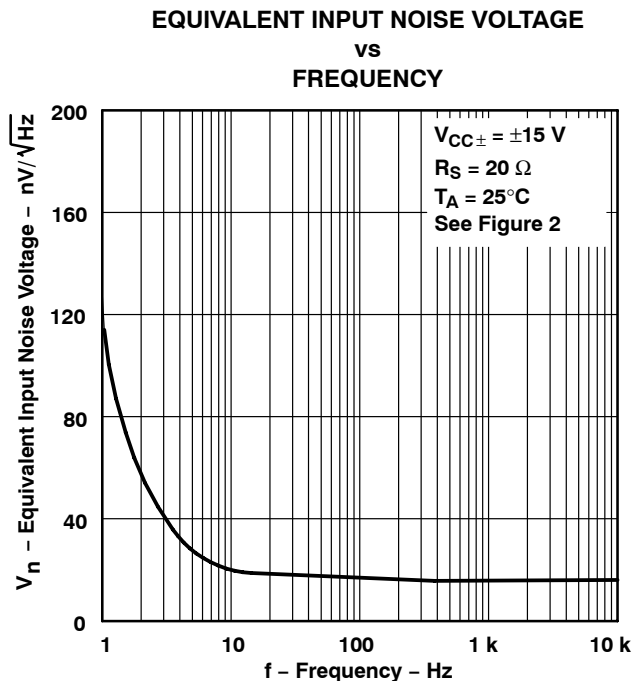
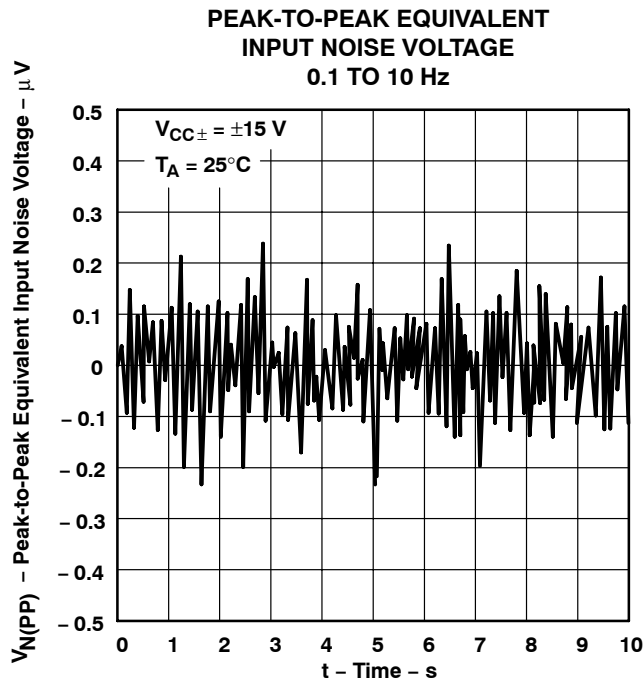
TYPICAL CHARACTERISTICS



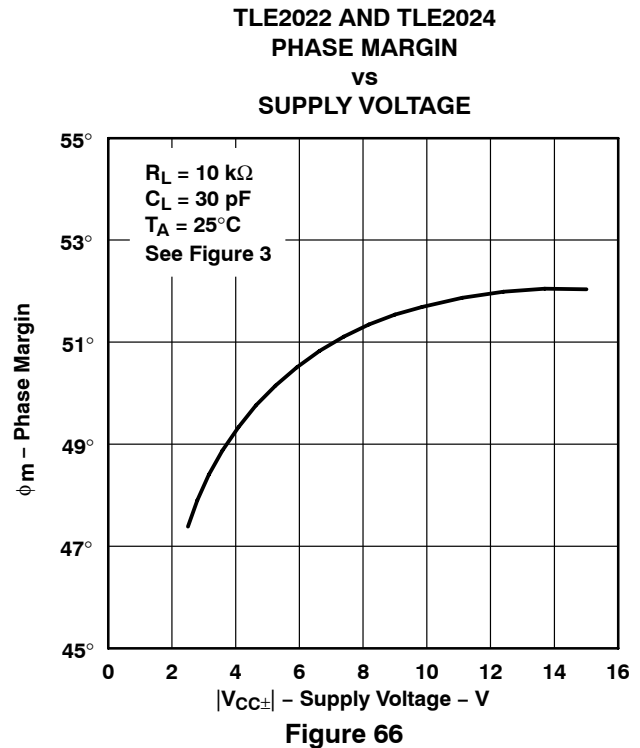
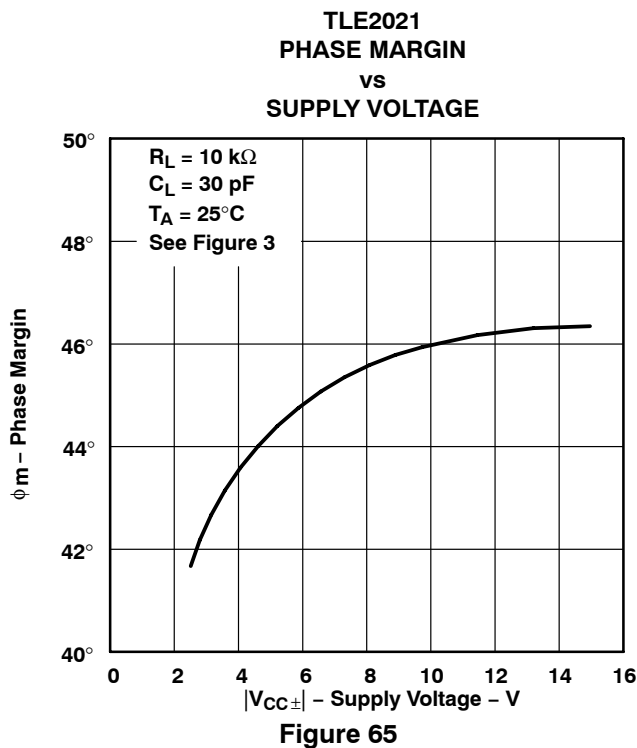
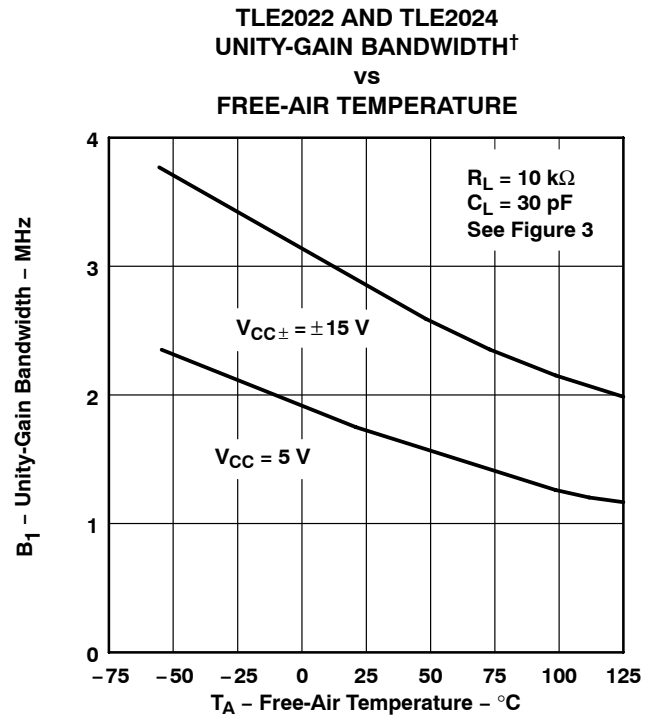
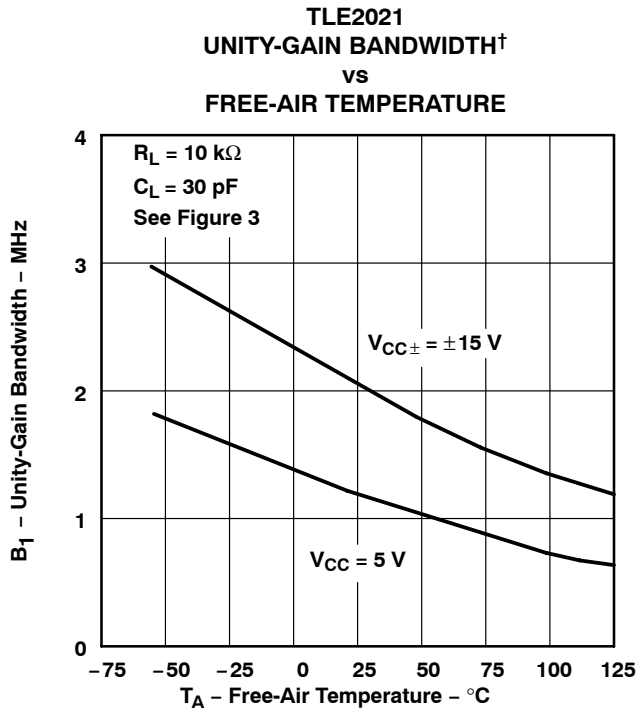
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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

**TLE2021
PHASE MARGIN
vs
LOAD CAPACITANCE**

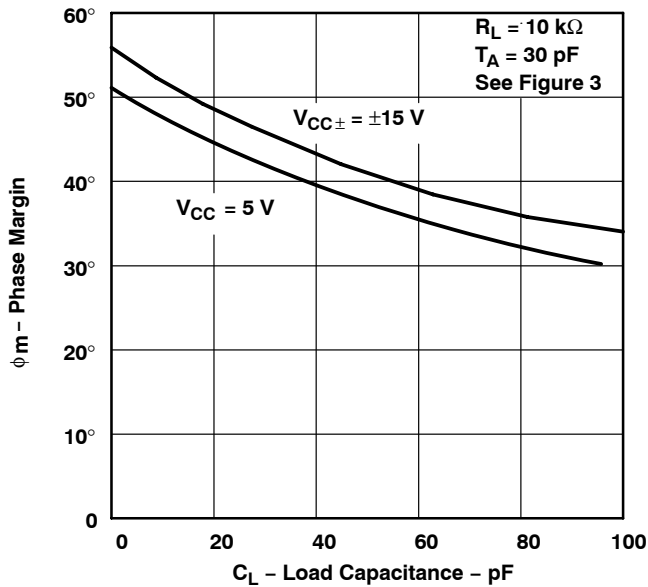


Figure 67

**TLE2022 AND TLE2024
PHASE MARGIN
vs
LOAD CAPACITANCE**

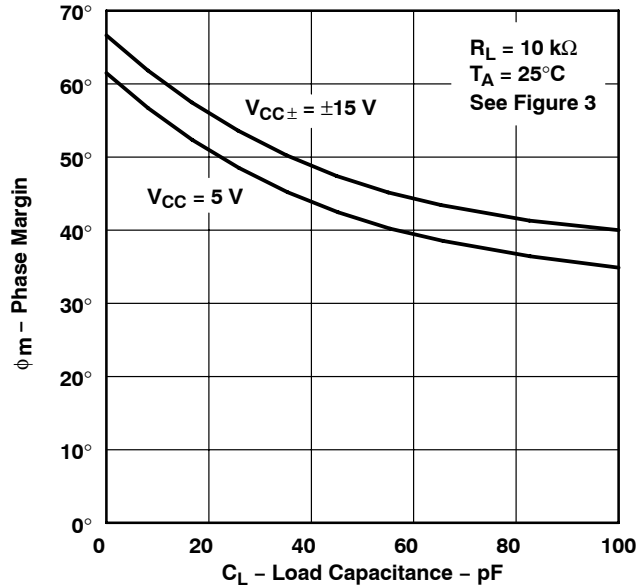


Figure 68

**TLE2021
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE**

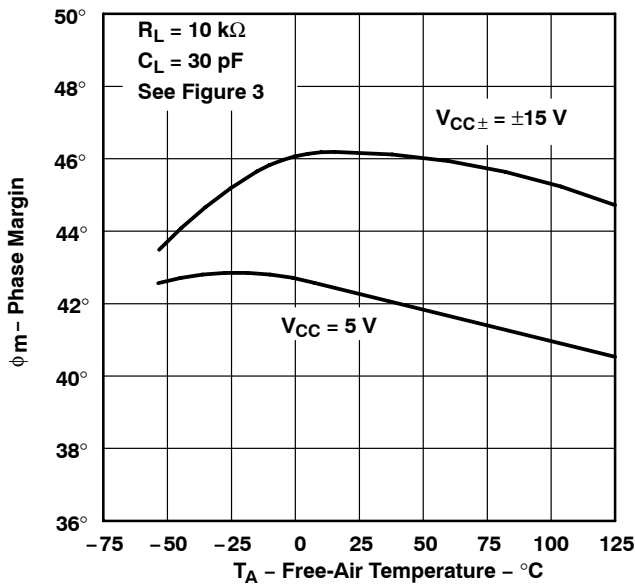


Figure 69

**TLE2022 AND TLE2024
PHASE MARGIN†
vs
FREE-AIR TEMPERATURE**

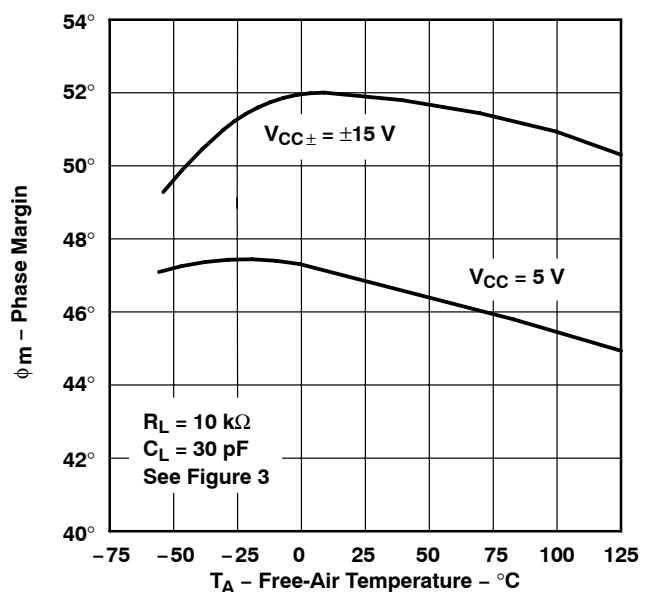


Figure 70

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

voltage-follower applications

The TLE202x circuitry includes input-protection diodes to limit the voltage across the input transistors; however, no provision is made in the circuit to limit the current if these diodes are forward biased. This condition can occur when the device is operated in the voltage-follower configuration and driven with a fast, large-signal pulse. It is recommended that a feedback resistor be used to limit the current to a maximum of 1 mA to prevent degradation of the device. This feedback resistor forms a pole with the input capacitance of the device. For feedback resistor values greater than 10 k Ω , this pole degrades the amplifier phase margin. This problem can be alleviated by adding a capacitor (20 pF to 50 pF) in parallel with the feedback resistor (see Figure 71).

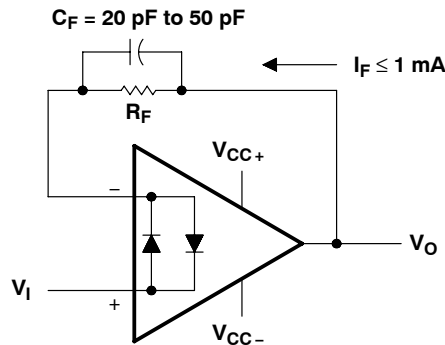


Figure 71. Voltage Follower

Input offset voltage nulling

The TLE202x series offers external null pins that further reduce the input offset voltage. The circuit in Figure 72 can be connected as shown if this feature is desired. When external nulling is not needed, the null pins may be left disconnected.

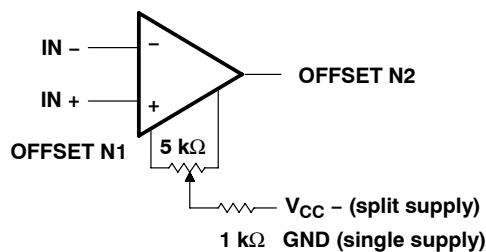


Figure 72. Input Offset Voltage Null Circuit

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*[™], the model generation software used with Microsim *PSpice*[™]. The Boyle macromodel (see Note 5) and subcircuit in Figure 73, Figure 74, and Figure 75 were generated using the TLE202x typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

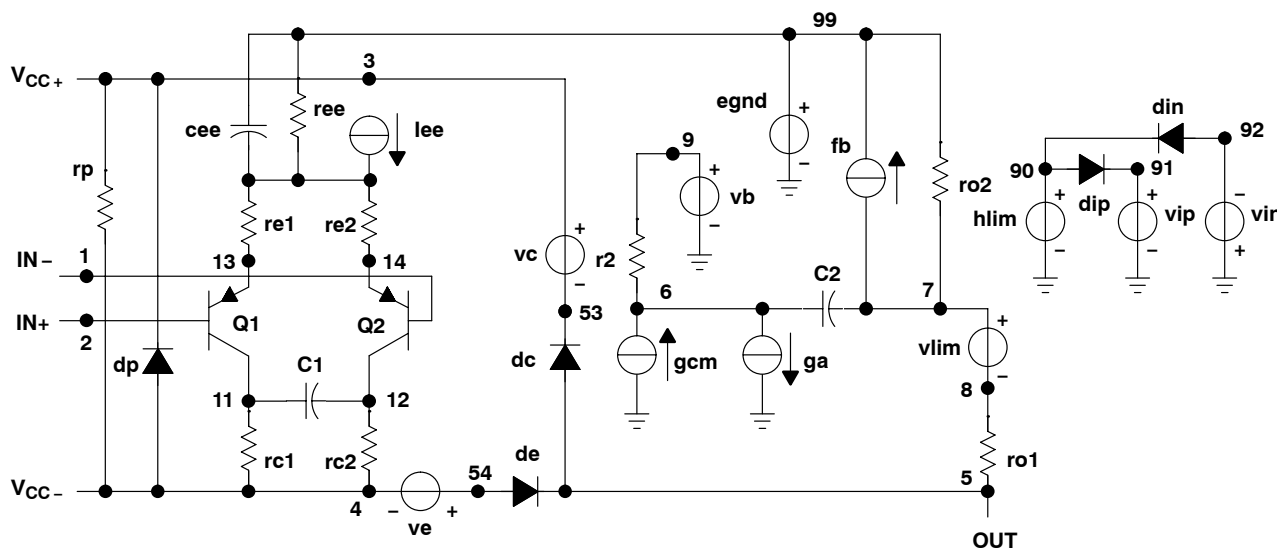


Figure 73. Boyle Subcircuit

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```
.SUBCKT TLE2021 1 2 3 4 5
*
c1 11 12 6.244E-12
c2 6 7 13.4E-12
c3 87 0 10.64E-9
cpsr 85 86 15.9E-9
dcm+ 81 82 dx
dcm- 83 81 dx
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
ecmr 84 99 (2 99) 1
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
epsr 85 0 poly(1) (3,4) -60E-6 2.0E-6
ense 89 2 poly(1) (88,0) 120E-6 1
fb 7 99 poly(6) vb vc ve vlp vln vpsr 0 547.3E6
+ -50E7 50E7 50E7 -50E7 547E6
ga 6 0 11 12 188.5E-6
gcm 0 6 10 99 335.2E-12
gpsr 85 86 (85,86) 100E-6
grc1 4 11 (4,11) 1.885E-4
grc2 4 12 (4,12) 1.885E-4
gre1 13 10 (13,10) 6.82E-4
gre2 14 10 (14,10) 6.82E-4
hlim 90 0 vlim 1k

hcmr 80 1 poly(2) vcm+ vcm- 0 1E2 1E2
irp 3 4 185E-6
iee 3 10 dc 15.67E-6
iio 2 0 2E-9
i1 88 0 1E-21
q1 11 89 13 qx
q2 12 80 14 qx
R2 6 9 100.0E3
rcm 84 81 1K
ree 10 99 14.76E6
rn1 87 0 2.55E8
rn2 87 88 11.67E3
ro1 8 5 62
ro2 7 99 63
vcm+ 82 99 13.3
vcm- 83 99 -14.6
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3.600
vln 0 92 dc 3.600
vpsr 0 86 dc 0
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=270)
.ends
```

Figure 74. Boyle Macromodel for the TLE2021

```
.SUBCKT TLE2022 1 2 3 4 5
*
c1 11 12 6.814E-12
c2 6 7 20.00E-12
dc 5 53 dx
de 54 5 dx
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
+ 45.47E6 -50E6 50E6 50E6 -50E6
ga 6 0 11 12 377.9E-6
gcm 0 6 10 99 7.84E-10
iee 3 10 DC 18.07E-6
hlim 90 0 vlim 1k
q1 11 2 13 qx
q2 12 1 14 qx
r2 6 9 100.0E3

rc1 4 11 2.842E3
rc2 4 12 2.842E3
ge1 13 10 (10,13) 31.299E-3
ge2 14 10 (10,14) 31.299E-3
ree 10 99 11.07E6
ro1 8 5 250
ro2 7 99 250
rp 3 4 137.2E3
vb 9 0 dc 0
vc 3 53 dc 1.300
ve 54 4 dc 1.500
vlim 7 8 dc 0
vlp 91 0 dc 3
vln 0 92 dc 3
.model dx d(is=800.0E-18)
.model qx pnp(is=800.0E-18 bf=257.1)
.ends
```

Figure 75. Boyle Macromodel for the TLE2022



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2021AQDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AE	Samples
TLE2021MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2021ME	Samples
TLE2021QDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021QE	Samples
TLE2022AQDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022AE	Samples
TLE2022QDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2022QE	Samples
TLE2024AQDWREP	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2024AE	Samples
TLE2024QDWREP	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2024QE	Samples
V62/04755-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2021AE	Samples
V62/04755-06YE	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2024QE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLE2021-EP, TLE2021A-EP, TLE2022-EP, TLE2022A-EP, TLE2024-EP, TLE2024A-EP :

- Catalog : [TLE2021](#), [TLE2021A](#), [TLE2022](#), [TLE2022A](#), [TLE2024](#), [TLE2024A](#)
- Automotive : [TLE2021-Q1](#), [TLE2021A-Q1](#), [TLE2022-Q1](#), [TLE2022A-Q1](#), [TLE2024-Q1](#)
- Military : [TLE2021M](#), [TLE2021AM](#), [TLE2022M](#), [TLE2022AM](#), [TLE2024M](#), [TLE2024AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2021AQDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2021QDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022AQDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2022QDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2024AQDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TLE2024QDWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2021AQDREP	SOIC	D	8	2500	340.5	336.1	25.0
TLE2021MDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLE2021QDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022AQDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLE2022QDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLE2024AQDWREP	SOIC	DW	16	2000	350.0	350.0	43.0
TLE2024QDWREP	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

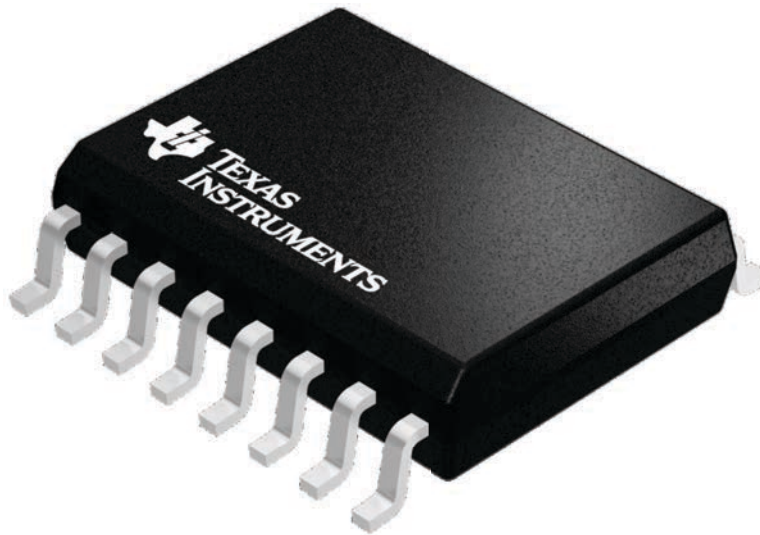
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

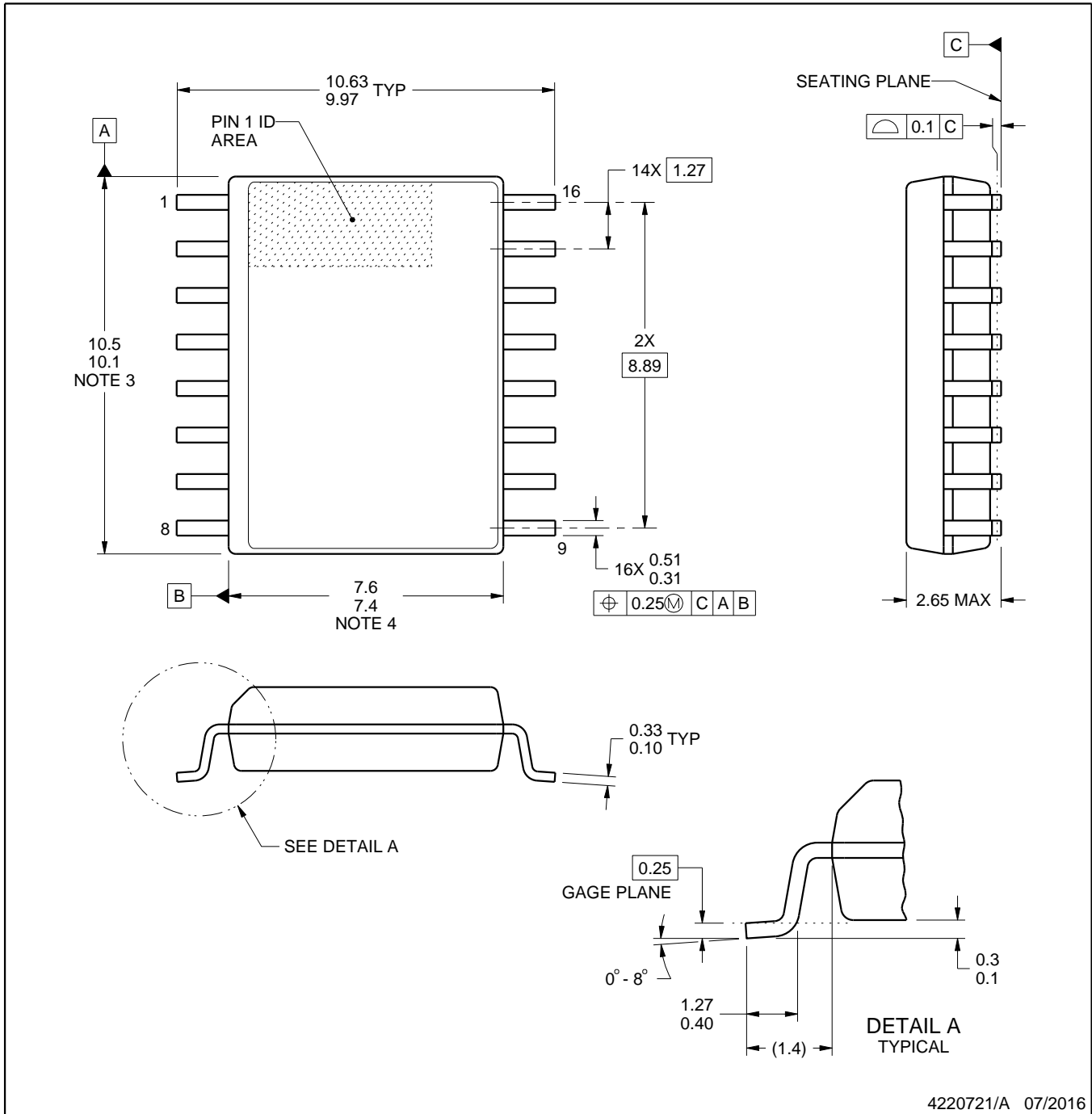


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

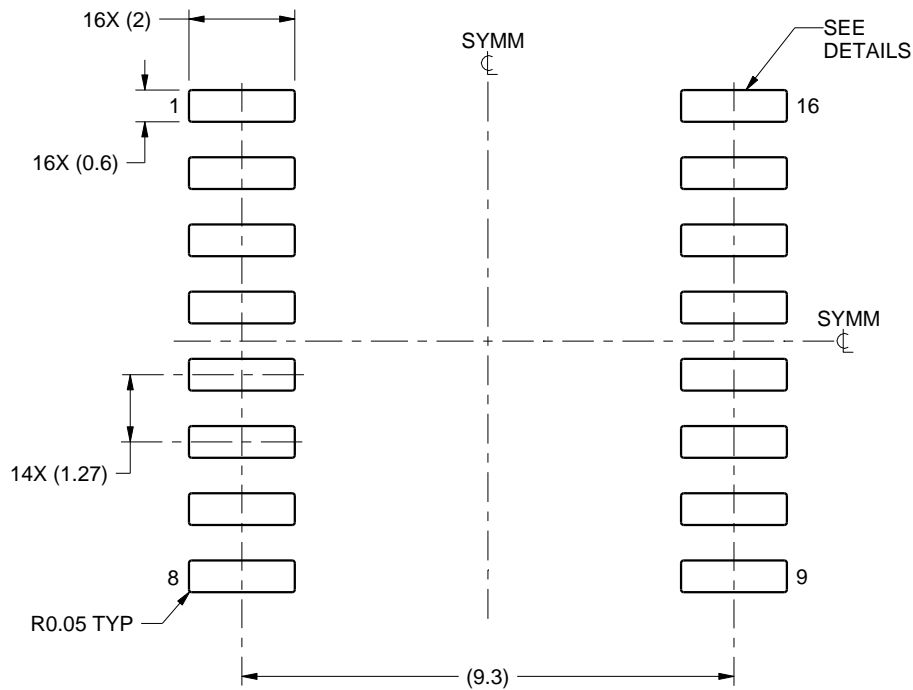
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

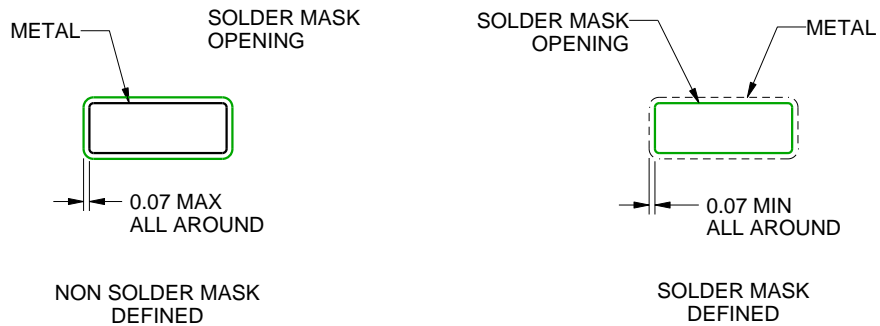
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

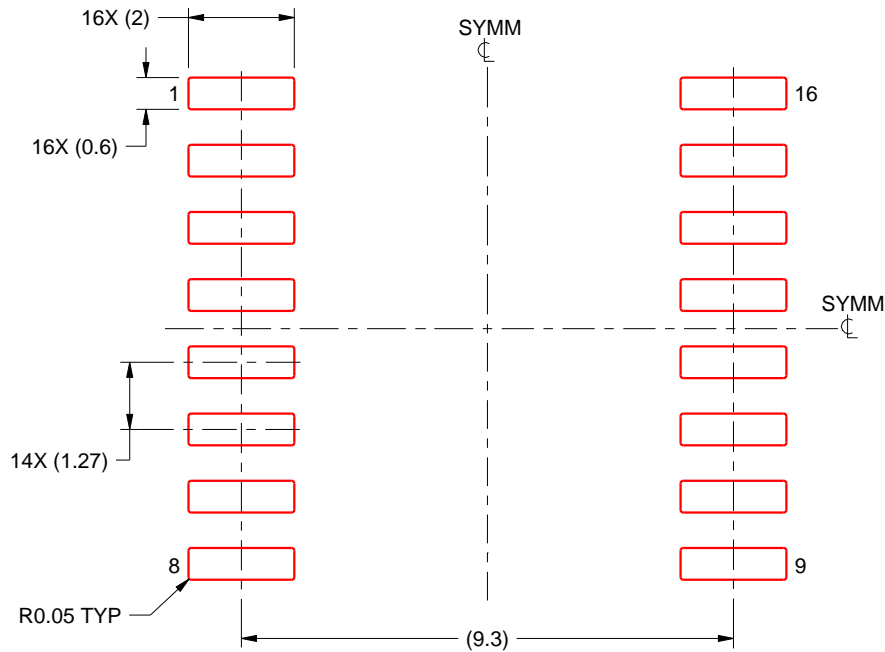
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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