TMUX7612-Q1 具有 1.8V 逻辑电平的汽车类 50V、低 RON、1:1 (SPST)、4 通道精密开关

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 125°C 的工作环境温度范围
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- 双电源电压范围：±4.5V 至 ±25 V
- 单电源电压范围：4.5V 至 50 V
- 精密性能：
  - 低导通电阻：1.35Ω（典型值）
  - 超低导通电阻平坦度：0.01Ω（典型值）
  - 大电流支持：300 mA（最大值）
  - 低导通漏电流：3.7pA（典型值），0.5nA（最大值）
  - 超低电荷注入：10pC（典型值）
- –40°C 至 +125°C 工作温度
- 轨到轨运行
- 双向运行
- 先断后合开关

2 应用

- OBDII CAN 切换
- 车载充电 (OBC)
- 高级驾驶辅助系统 (ADAS)
- ADAS 域控制器
- 远程信息处理控制单元
- 车身控制模块 (BCM)
- 车身电子装置和照明
- 电池管理系统
- HVAC 控制器模块

3 描述

TMUX7612-Q1 是互补金属氧化物半导体 (CMOS) 开关器件，具有四个独立可选的 1:1 单极单掷 (SPST) 开关通道。该器件支持单电源（4.5V 至 50 V）、双电源（±4.5V 至 ±25 V）或非对称电源（例如，V_{DD} = 37.5V，V_{SS} = -12 V）。TMUX7612-Q1 可支持源极 (Sx) 和漏极 (Dx) 引脚上 V_{SS} 到 V_{DD} 范围的双向模拟和数字信号。

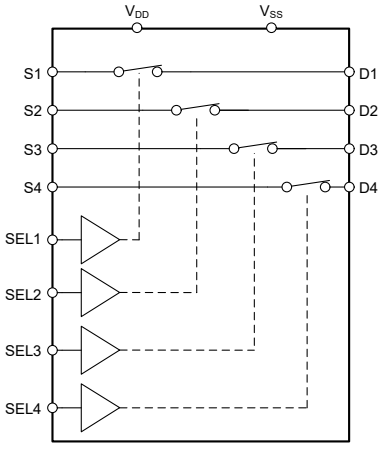
TMUX7612-Q1 的开关通过 SELx 引脚上适当的逻辑控制输入控制。TMUX7612-Q1 具有特殊架构，可实现超低电荷注入。这有助于防止器件的控制输入与模拟输出之间出现不必要的耦合，并减少交流噪声和失调电压误差。

TMUX7612-Q1 是精密开关和多路复用器系列器件，具有非常低的导通和关断漏电流，因此可用于高精度测量应用。

封装信息

器件型号	封装(1)	封装尺寸(2)
TMUX7612-Q1	PW（TSSOP，16）	5mm × 4.4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



TMUX7612-Q1
(SELx = Logic 1)

TMUX7612-Q1 方框图

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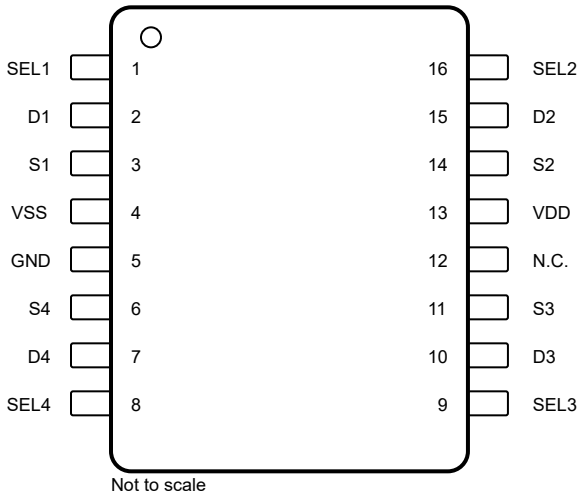
4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Pin Configuration and Functions



Not to scale

图 5-1. PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D1	2	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
D3	10	I/O	Drain pin 3. Can be an input or output.
D4	7	I/O	Drain pin 4. Can be an input or output.
GND	5	P	Ground (0 V) reference.
N.C.	12	—	No internal connection. Can be shorted to GND or left floating
S1	3	I/O	Source pin 1. Can be an input or output.
S2	14	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	6	I/O	Source pin 4. Can be an input or output.
SEL1	1	I	Logic control input 1, has internal pull-down resistor. Controls channel 1 state as provided in 表 7-1.
SEL2	16	I	Logic control input 2, has internal pull-down resistor. Controls channel 2 state as provided in 表 7-1.
SEL3	9	I	Logic control input 3, has internal pull-down resistor. Controls channel 3 state as provided in 表 7-1.
SEL4	8	I	Logic control input 4, has internal pull-down resistor. Controls channel 4 state as provided in 表 7-1.
VDD	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND
VSS	4	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND. In single-supply applications, this pin should be connected to ground.
Thermal Pad		—	The thermal exposed pad is connected internally. It is recommended that the pad be tied to VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		53	V
V_{DD}		–0.5	53	V
V_{SS}		–32	0.5	V
$V_{SEL} – V_{SS}$	Logic Supply Voltage	–0.5	53	V
I_{SEL}	Logic control input pin current (SEL pins)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation		1650	mW

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability,
functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX7612		UNIT
		RUM (QFN)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	4.5		50	V
V_{DD}	Positive power supply voltage	4.5		50	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
$V_{SEL} – V_{SS}$	Logic Supply Voltage	0		44	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (2)	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 50 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current Switch Pairs

CONTINUOUS CURRENT PER CHANNEL (I_{DC})			T_A = 25°C	T_A = 50°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS	Pins					
PW (TSSOP)	VSS to VDD -2.5 V	1 Channel	470	432	153	119	mA
		2 Channels	390	306	119	119	
		3 Channels	318	250	119	80	
		4 Channels	276	216	119	69	
RUM (QFN)	VSS to VDD -2.5 V	1 Channel	470	406	144	119	mA
		2 Channels	366	287	119	92	
		3 Channels	299	235	119	75	
		4 Channels	259	203	119	65	

6.6 Source or Drain Pulsed Current

Pulsed at 1 ms, 10% duty cycle

PULSED CURRENT PER CHANNEL (I_{DC})		T_A = 25°C	T_A = 50°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS					
PW (TSSOP)	VSS to VDD - 2.5 V	470	470	440	200	mA
RUM (QFN)	VSS to VDD - 2.5 V	470	470	410	190	mA

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6.7 Electrical Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 3 V to 9 V I_D = –10 mA	25°C		1.35	1.65	Ω
			–40°C to +85°C			2.15	
			–40°C to +125°C			2.45	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.1		Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 3 V to 9 V I_D = –10 mA	25°C		0.01		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.25	0.0035	0.25	nA
			–40°C to +50°C	–0.5		0.5	
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–12.5		12.5	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is off V_S = 1 V / 10 V V_D = 10 V / 1 V	25°C	–0.25	0.0027	0.25	nA
			–40°C to +50°C	–0.5		0.5	
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–12.5		12.5	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 12 V, V_{SS} = 0 V Switch state is on V_S = V_D = 1 V or 10 V	25°C	–0.5	0.0041	0.5	nA
			–40°C to +50°C	-0.6		0.6	
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–7		7	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 12 V, V_{SS} = 0 V All switches OFF	25°C		30	42	µA
			–40°C to +85°C			55	
			–40°C to +125°C			70	
I_{DD}	V_{DD} supply current	V_{DD} = 12 V, V_{SS} = 0 V All switches ON	25°C		400	500	µA
			–40°C to +85°C			525	
			–40°C to +125°C			550	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.8 Switching Characteristics (12 V Single Supply)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		2.2	2.5	µs
			–40°C to +85°C			3	µs
			–40°C to +125°C			3.5	µs
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF	25°C		1.8	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–70		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V	25°C		150		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, VBIAS = 6 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–60		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		43		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		43		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		37		pF

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6.9 Electrical Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10% GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		1.35	1.65	Ω
			–40°C to +85°C			2.15	
			–40°C to +125°C			2.45	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.1		Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.01		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.25	0.03	0.25	nA
			–40°C to +50°C	–0.5		0.5	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–12.5		12.5	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–0.25	0.03	0.25	nA
			–40°C to +50°C	–0.5		0.5	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–12.5		12.5	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–0.5	0.0037	0.5	nA
			–40°C to +50°C	-0.6		0.6	
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–7		7	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		35	50	µA
			–40°C to +85°C			60	
			–40°C to +125°C			75	
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		425	475	µA
			–40°C to +85°C			550	
			–40°C to +125°C			650	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches OFF	25°C		15	25	µA
			–40°C to +85°C			35	
			–40°C to +125°C			45	
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V All switches ON	25°C		340	400	µA
			–40°C to +85°C			425	
			–40°C to +125°C			450	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.10 Switching Characteristics (±15 V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.2	2.5	µs
			–40°C to +85°C			3	µs
			–40°C to +125°C			3.5	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.8	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		310		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–74		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–90		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–60		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		35		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		35		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		35		pF

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6.11 Electrical Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		1.35	1.65	Ω
			–40°C to +85°C			2.15	
			–40°C to +125°C			2.45	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.1		Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.01		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.25	0.012	0.25	nA
			–40°C to +50°C	-0.75		0.75	
			–40°C to +85°C	–1.1		1.1	
			–40°C to +125°C	–13.5		13.5	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–0.25	0.012	0.25	nA
			–40°C to +50°C	-0.75		0.75	
			–40°C to +85°C	–1.1		1.1	
			–40°C to +125°C	–13.5		13.5	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–0.75	0.0045	0.75	nA
			–40°C to +50°C	-1		1	
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–8.5		8.5	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		35	50	µA
			–40°C to +85°C			60	
			–40°C to +125°C			75	
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		425	475	µA
			–40°C to +85°C			550	
			–40°C to +125°C			650	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches OFF	25°C		15	25	µA
			–40°C to +85°C			35	
			–40°C to +125°C			45	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V All switches ON	25°C		340	400	µA
			–40°C to +85°C			425	
			–40°C to +125°C			450	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.12 Switching Characteristics (±20 V Dual Supply)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.2	2.5	µs
			–40°C to +85°C			2.9	µs
			–40°C to +125°C			3.2	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.8	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			2.8	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		320		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		-4		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–77		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V,	25°C		150		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–57		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		33		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		33		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0 V, f = 1 MHz	25°C		33		pF

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6.13 Electrical Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		1.35	1.65	Ω
			–40°C to +85°C			2.15	
			–40°C to +125°C			2.45	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.1		Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –7.5 V to 32.5 V I_D = –10 mA	25°C		0.01		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.75	0.021	0.75	nA
			–40°C to +50°C	–2.6		2.6	
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–18		18	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is off V_S = 32.5 V / –7.5 V V_D = –7.5 V / 32.5 V	25°C	–0.75	0.021	0.75	nA
			–40°C to +50°C	–2.6		2.6	
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–18		18	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 37.5 V, V_{SS} = -12.5 V Switch state is on V_S = V_D = 32.5 V or –7.5 V	25°C	-0.75	0.01	0.75	nA
			–40°C to +50°C	-1.2		1.2	
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–10		10	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		35	55	µA
			–40°C to +85°C			65	
			–40°C to +125°C			80	
I_{DD}	V_{DD} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		425	475	µA
			–40°C to +85°C			550	
			–40°C to +125°C			650	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches OFF	25°C		20	30	µA
			–40°C to +85°C			40	
			–40°C to +125°C			50	
I_{SS}	V_{SS} supply current	V_{DD} = 37.5 V, V_{SS} = -12.5 V All switches ON	25°C		340	400	µA
			–40°C to +85°C			425	
			–40°C to +125°C			450	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.14 Switching Characteristics (+37.5 V/–12.5 V Dual Supply)

V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V ±10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2.1	3	µs
			–40°C to +85°C			4	µs
			–40°C to +125°C			5.2	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.74	2	µs
			–40°C to +85°C			2.1	µs
			–40°C to +125°C			2.5	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		350		ns
			–40°C to +85°C	310			ns
			–40°C to +125°C	300			ns
Q_{INJ}	Charge injection	V_S = 12.5 V, C_L = 100 pF	25°C		6.5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–75		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 100 kHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V,	25°C		150		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 12.5 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–57		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		55		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		55		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 12.5 V, f = 1 MHz	25°C		35		pF

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6.15 Electrical Characteristics (48 V Single Supply)

V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V -10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V - 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 3 V to 45 V I_D = –10 mA	25°C		1.35	1.65	Ω
			–40°C to +85°C			2.15	
			–40°C to +125°C			2.45	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 3 V to 45 V I_D = –10 mA	25°C		0.1	0.18	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 3 V to 45 V I_D = –10 mA	25°C		0.01		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 24 V, I_S = –10 mA	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 48 V, V_{SS} = 0 V Switch state is off V_S = 44 V / 1 V V_D = 1 V / 44 V	25°C	–0.75	0.04	0.75	nA
			–40°C to +50°C	–3		3	
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–20		20	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 48 V, V_{SS} = 0 V Switch state is off V_S = 44 V / 1 V V_D = 1 V / 44 V	25°C	–0.75	0.04	0.75	nA
			–40°C to +50°C	–3		3	
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–20		20	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 48 V, V_{SS} = 0 V Switch state is on V_S = V_D = 44 V or 1 V	25°C	–1	0.4	1	nA
			–40°C to +50°C	-2.5		2.5	
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–11		11	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 48 V, V_{SS} = 0 V All switches OFF	25°C		35	55	µA
			–40°C to +85°C			65	µA
			–40°C to +125°C			80	µA
I_{DD}	V_{DD} supply current	V_{DD} = 48 V, V_{SS} = 0 V All switches ON	25°C		425	475	µA
			–40°C to +85°C			550	µA
			–40°C to +125°C			650	µA
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 48 V, V_{SS} = 0 V All switches OFF	25°C		20	30	µA
			–40°C to +85°C			40	µA
			–40°C to +125°C			50	µA
I_{SS}	V_{SS} supply current	V_{DD} = 48 V, V_{SS} = 0 V All switches ON	25°C		340	400	µA
			–40°C to +85°C			425	µA
			–40°C to +125°C			450	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.16 Switching Characteristics (48 V Single Supply)

V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V ±10%, GND = 0 V (unless otherwise noted)
V_{DD} = +37.5 V ± 10%, V_{SS} = –12.5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		2	3	µs
			–40°C to +85°C			4	µs
			–40°C to +125°C			5.2	µs
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF	25°C		1.75	2	µs
			–40°C to +85°C			2.25	µs
			–40°C to +125°C			2.5	µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		325		ns
			–40°C to +85°C	280			ns
			–40°C to +125°C	270			ns
Q_{INJ}	Charge injection	V_S = 24 V, C_L = 100 pF	25°C		16		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V, f = 100 kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V, f = 1 MHz	25°C		–71		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V, f = 100 kHz	25°C		–105		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V, f = 1 MHz	25°C		–100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V,	25°C		150		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS},VBIAS = 6 V, f = 1 MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		–57		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 24 V, V_{BIAS} = 24 V R_L = 110 Ω , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.005		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		55		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		55		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 6 V, f = 1 MHz	25°C		35		pF

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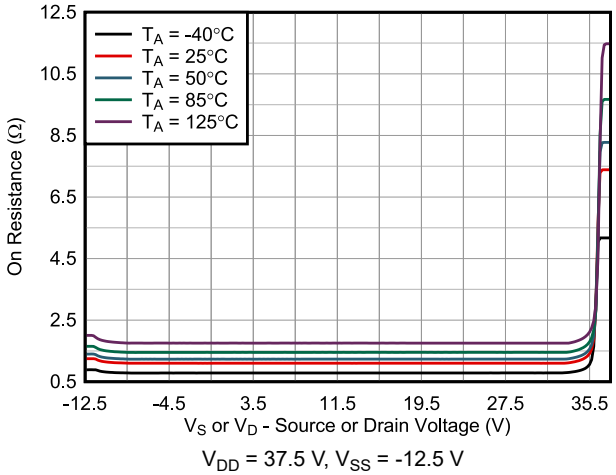
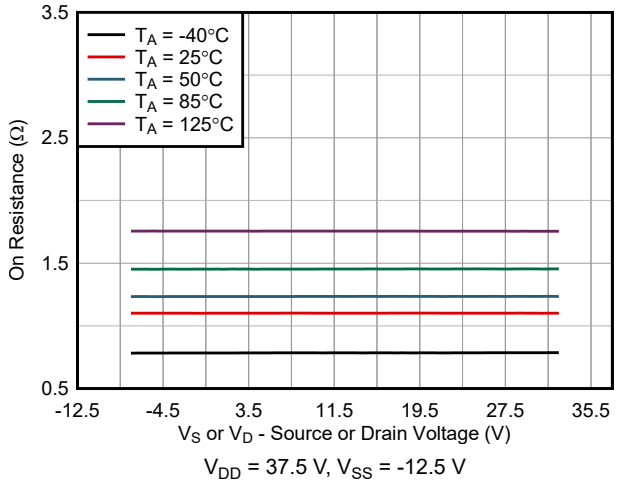
6.17 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



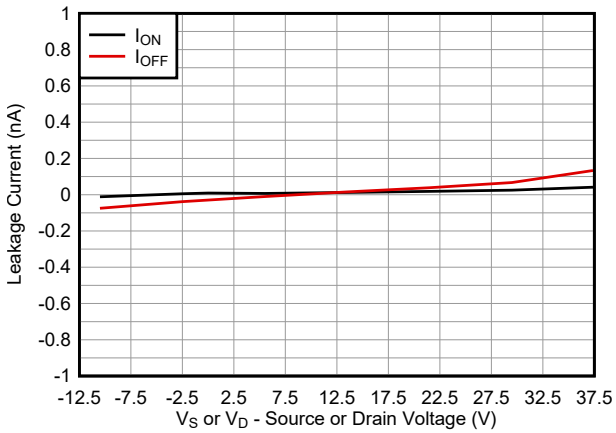
V_{DD} = 37.5 V, V_{SS} = -12.5 V

图 6-1. On-Resistance vs Source or Drain Voltage



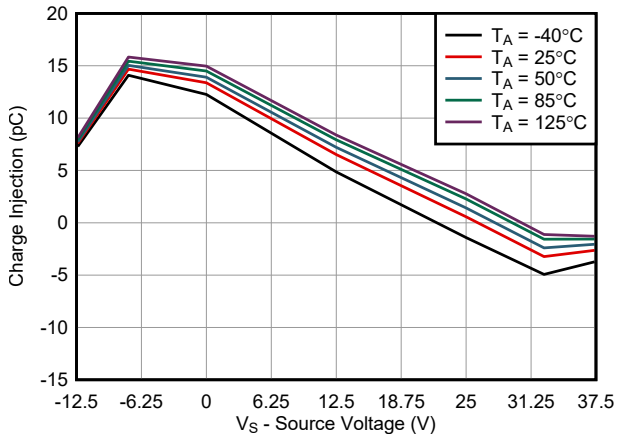
V_{DD} = 37.5 V, V_{SS} = -12.5 V

图 6-2. On-Resistance vs Source or Drain Voltage



V_{DD} = 37.5 V, V_{SS} = -12.5 V

图 6-3. Leakage Current vs Bias Voltage



V_{DD} = 37.5 V, V_{SS} = -12.5 V

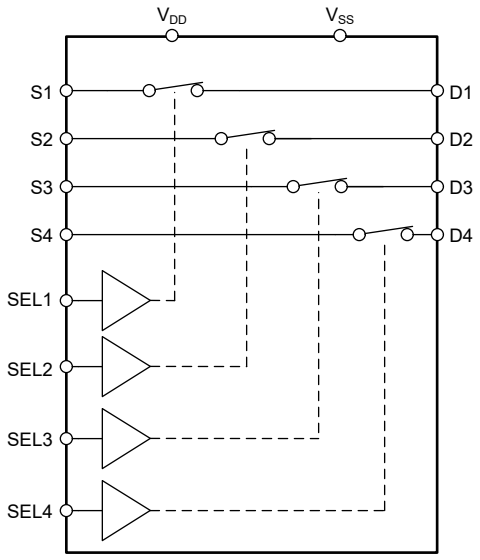
图 6-4. Charge Injection vs Source Voltage

7 Detailed Description

7.1 Overview

TMUX7612-Q1 is a 1:1 (SPST), 4-channel switch. This device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 37.5 V, V_{SS} = –12 V.

7.2 Functional Block Diagram



TMUX7612-Q1
(SELx = Logic 1)

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX7612-Q1 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX7612-Q1 ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX7612-Q1 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX7612-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

7.3.4 Flat On-Resistance

The TMUX7612-Q1 is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in precision applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

This architecture also keeps RON the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5 V above VSS to 5 V below VDD. As long as this headroom is maintained, the TMUX7612-Q1 exhibits an extremely linear response.

ADVANCE INFORMATION

7.3.5 Power-Up Sequence Free

The TMUX7612-Q1 supports any power up sequencing. With the supply rails (VDD and VSS), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

7.3.6 Ultra-Low Charge Injection

The TMUX7612-Q1 contains specialized architecture to significantly reduce charge injection, which is consistent across supply and bias conditions. The result is a dramatic drop in AC noise when switching compared to other low on-resistance multiplexers or switches.

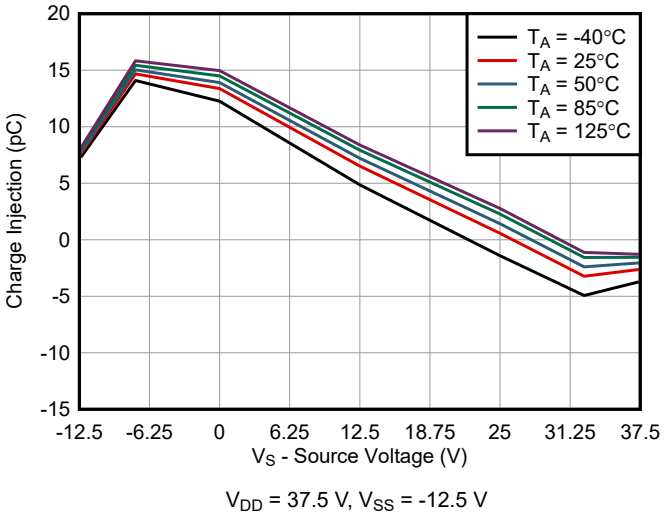


图 7-1. Charge Injection vs Source Voltage

7.3.7 Ultra-Low Leakage Current

The TMUX7612-Q1 provides extremely low on-leakage and off-leakage currents. This device is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. 图 7-2 shows typical leakage currents of the TMUX7612-Q1 devices versus source or drain voltage at V_{DD} = 32.5 V, V_{SS} = -12.5 V and 50°C. The typical performance seen here is less than 0.2 nA at 50°C, which enables the TMUX7612-Q1 to be used in a wide array of precision applications.

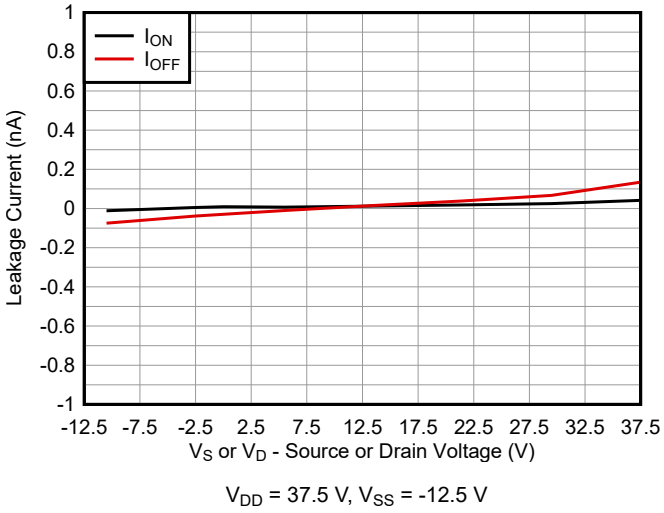


图 7-2. Leakage Current at 50°C vs Bias Voltage

7.4 Device Functional Modes

The TMUX7612-Q1 has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins operate down to 1.8 V logic and can be as high as 44 V.

The TMUX7612-Q1 devices can be operated without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors.

7.4.1 Truth Tables

表 7-1 provides the truth table for TMUX7612-Q1.

表 7-1. TMUX7612-Q1 Truth Table

SEL x (1)	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1) x denotes 1, 2, 3, or 4 for the corresponding channel.

ADVANCE INFORMATION

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX7612-Q1 is a part of the precision switches and multiplexers family of devices. The device operates with dual supplies (±4.5 V to ±25 V), a single supply (4.5 V to 50 V), or asymmetric supplies (such as V_{DD} = 37.5 V, V_{SS} = –12.5 V), and offers a true rail-to-rail input and output signal range. The TMUX7612-Q1 offers a low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX7612-Q1 a great option for high-performance and high-voltage industrial applications.

8.1.1 Typical Application – MEMs Lidar Switching

One example to take advantage of TMUX7612-Q1 precision performance is the implementation of MEMs (Microelectromechanical systems) based LIDAR for ADAS systems .

LIDAR is often used in automotive systems to provide driver feedback on surroundings at a high spatial resolution. To achieve a 360° view, the LIDAR system will often be rotated while scanning. This solution; however, requires expensive and bulky mechanical components. One alternative to this mechanical solution is an electromechanical equivalent in the form of MEMs modules. These MEMs modules control the angle of many tiny mirrors based on an input analog voltage. The angle can be swept across overlapping MEMs modules to scan the environment and capture a full view. Additionally, to move the laser in 2 dimensions cascading mirrors are needed. To help maximize the MEMs modules, a switch can be placed in series with the MEMs controller to control the path of the tilt angle analog output. Each switch on the TMUX7612-Q1 can be controlled independently, so this solution has a high level of flexibility and can be optimized and expanded based on the number MEMs modules needed in the system.

MEMs systems are particularly susceptible to SNR issues. Since the tilt angle is controlled by an input analog voltage, any small error in this voltage could cause an improper angle and result in erroneous data. A low R_{ON} switch like the TMUX7612-Q1 with low leakage current (3.7 pA typical) reduces potential voltage offsets.

These LIDAR systems often have asymmetric supplies. It is possible that the positive and negative supply rails are +12 V and -30 V respectively. Additionally, in an automotive system, these supply rails can vary dramatically to as much as +6 V and -32 V. The TMUX7612-Q1 is well equipped to handle these supply situations. Not only can it operate with asymmetric supplies, the TMUX7612-Q1 can operate down to a +4.5 V minimum positive supply.

ADVANCE INFORMATION

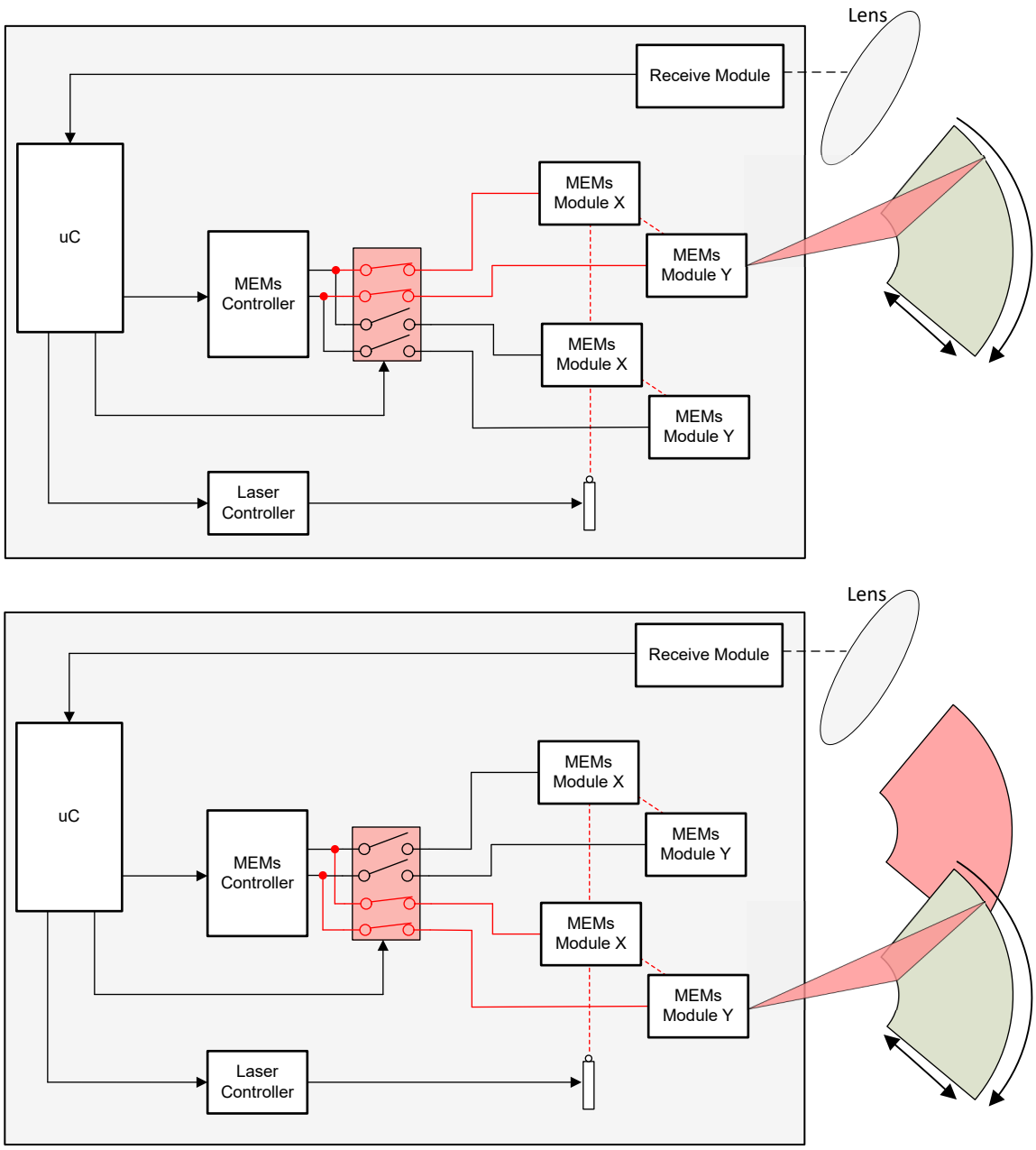


图 8-1. MEMs Module Switching for LIDAR

8.2 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	6 V to 12 V
Supply (V_{SS})	- 32 V to - 30V
Input / Output signal range	V_{SS} to V_{DD}(Rail-to-Rail)
Control logic thresholds	1.8 V compatible

ADVANCE INFORMATION

ADVANCE INFORMATION

8.3 Detailed Design Procedure

The application shown in *MEMs Module Switching for LIDAR* demonstrates how to incorporate the TMUX7612-Q1 switch to expand the system MEMs module density without adding additional lasers, lenses, or controllers. The tilt angle analog control is passed through the switch to the MEMs modules. The angles can then be swept in the X and Y direction. Once the sweeps are complete, the TMUX7612-Q1 will switch to the next set of modules and repeat this process until a full image of the environment is obtained. This device can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX7612-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pins have an internal pull-down resistor to prevent floating input logic. The TMUX7612-Q1 supports asymmetric supply rails within a 50 V differential, and down to 4.5 V on the positive supply. For this design, the signal range must stay within the supply rails of the device.

8.4 Application Curve

TMUX7612-Q1 has excellent linearity, leakage, and charge injection performance making them an excellent choice to minimize noise and offset errors for precision applications and very low current range measurements.

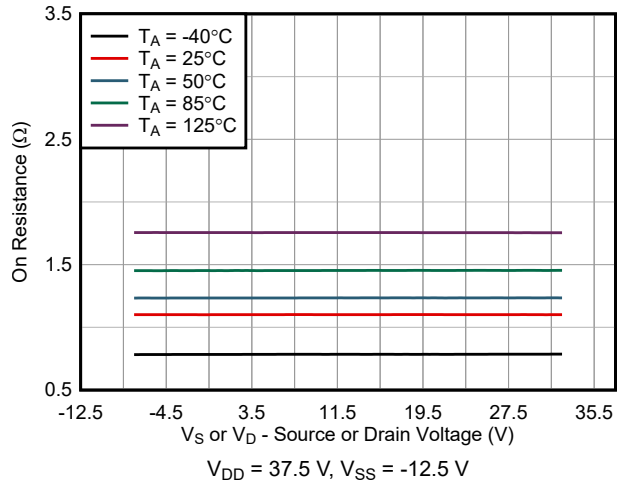


图 8-2. On-Resistance vs Source or Drain Voltage

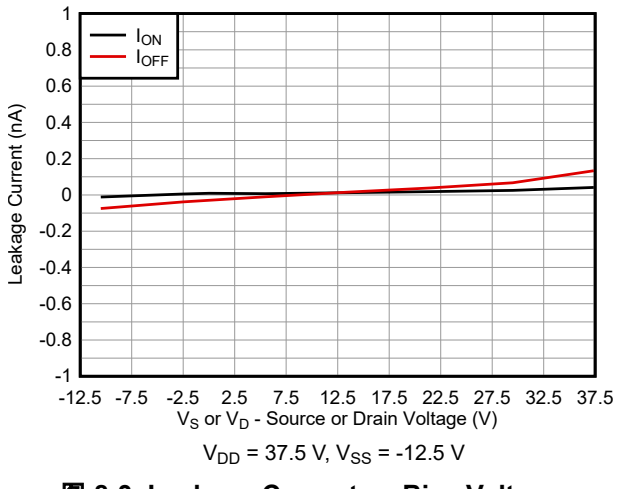


图 8-3. Leakage Current vs Bias Voltage

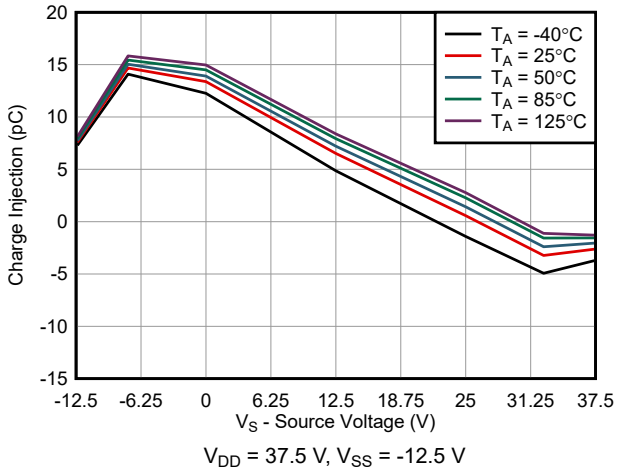


图 8-4. Charge Injection vs Source Voltage

8.5 Power Supply Recommendations

The TMUX7612-Q1 device operates across a wide supply range of ±4.5 V to ±25 V (4.5 V to 50 V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always make sure a solid ground (GND) connection is established before supplies are ramped.

8.6 Layout

8.6.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-5 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

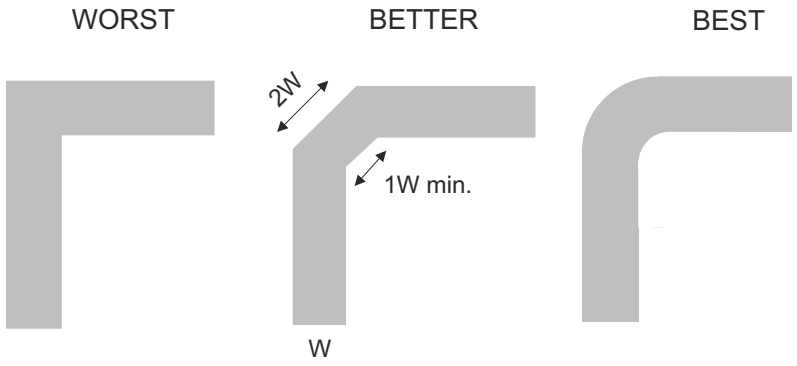


图 8-5. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 8-6 shows an example of a PCB layout with the TMUX7612-Q1.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

ADVANCE INFORMATION

8.6.2 Layout Example

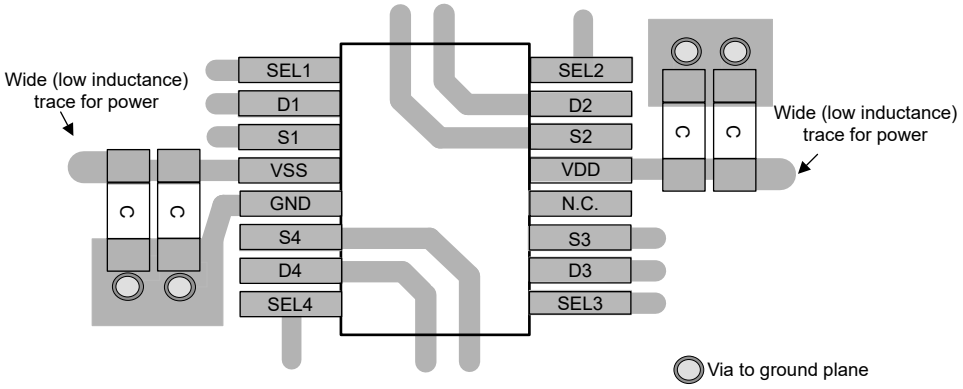


图 8-6. TMUX7612-Q1 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

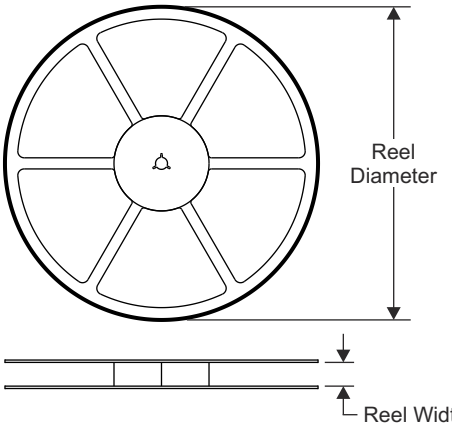
10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

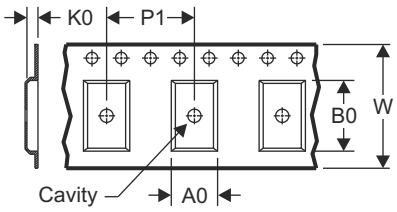
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

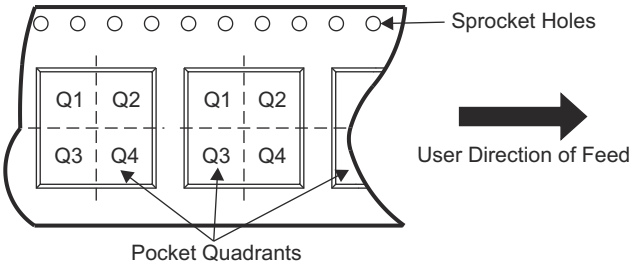


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

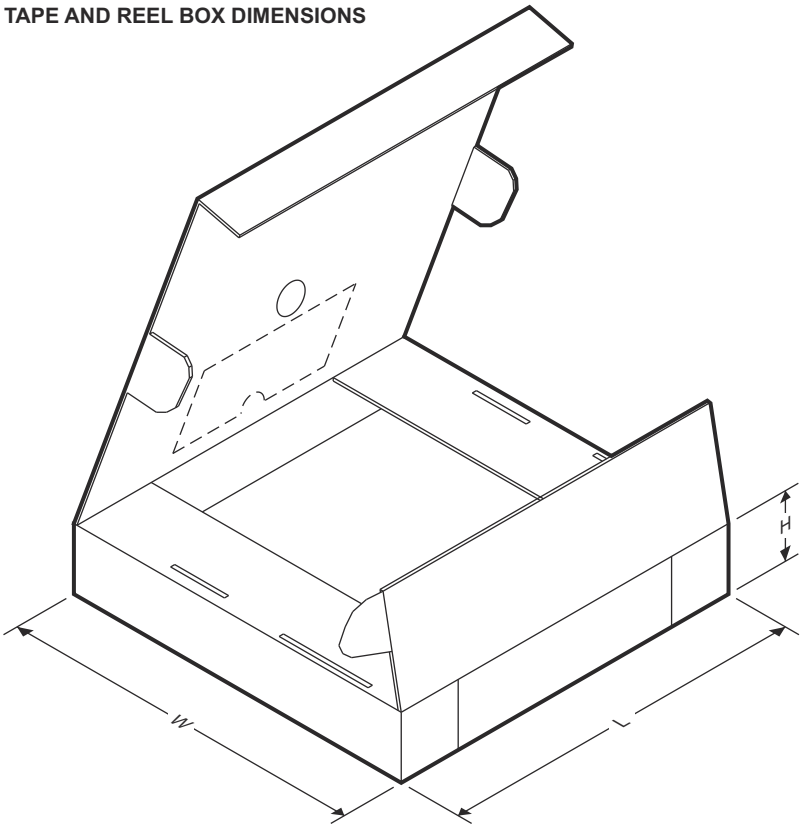
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTMUX7612QPWR	TSSOP	PW	16	3000	330	12.4	6.90	5.60	1.60	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTMUX7612QPWR	TSSOP	PW	16	3000	367	367	35

ADVANCE INFORMATION

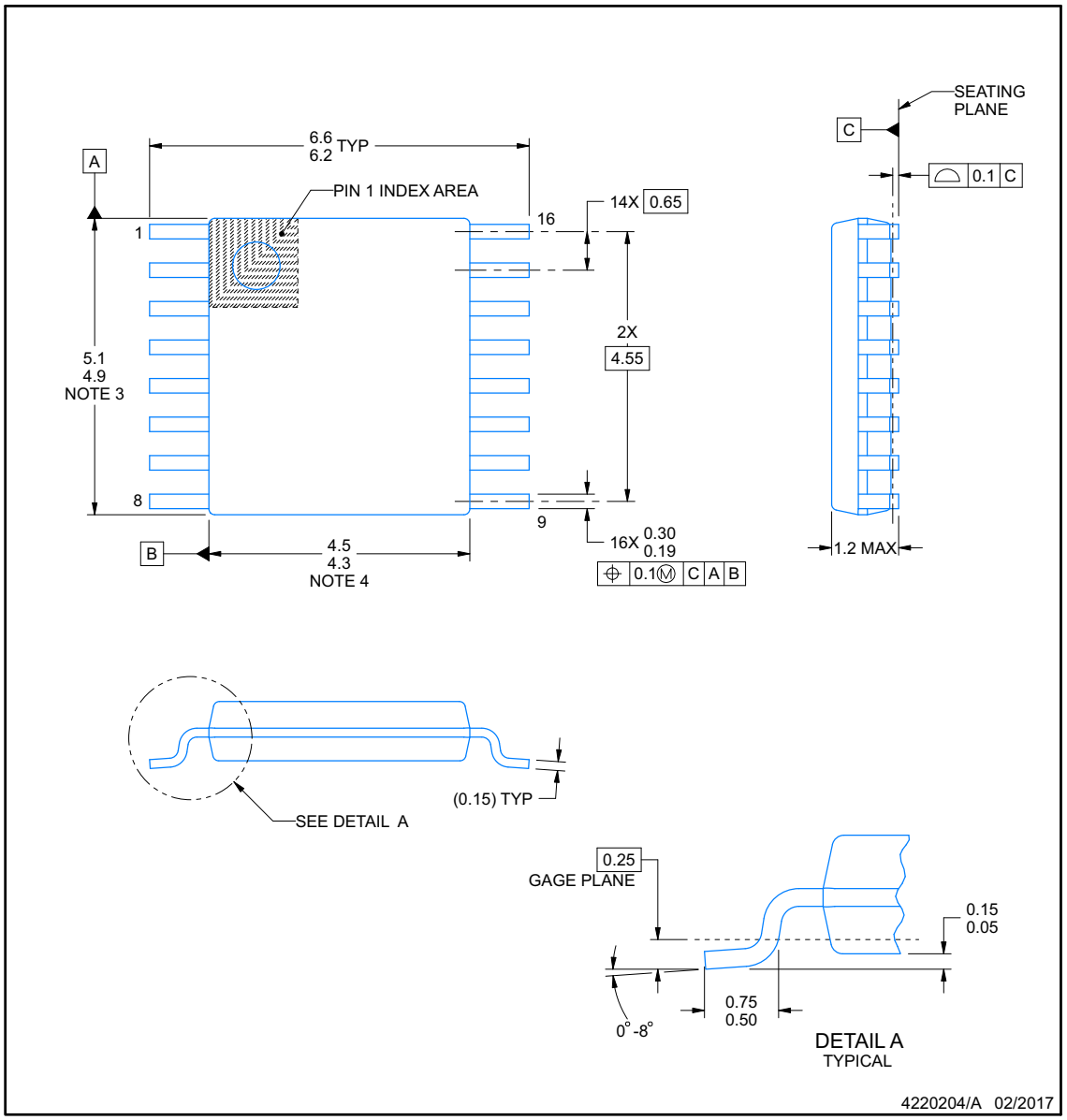
ADVANCE INFORMATION

10.2 Mechanical Data

PACKAGE OUTLINE

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

TEXAS INSTRUMENTS
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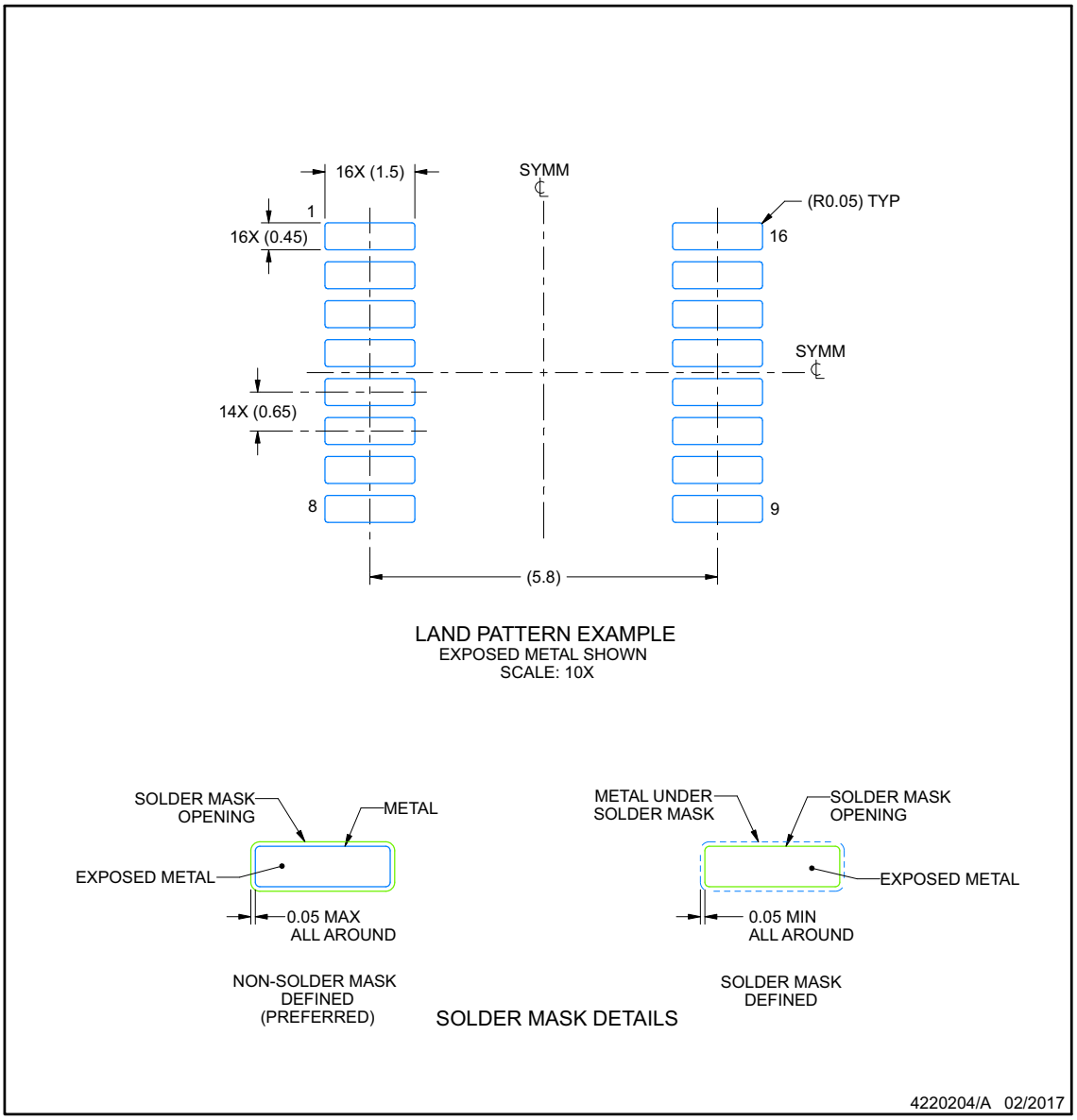
EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

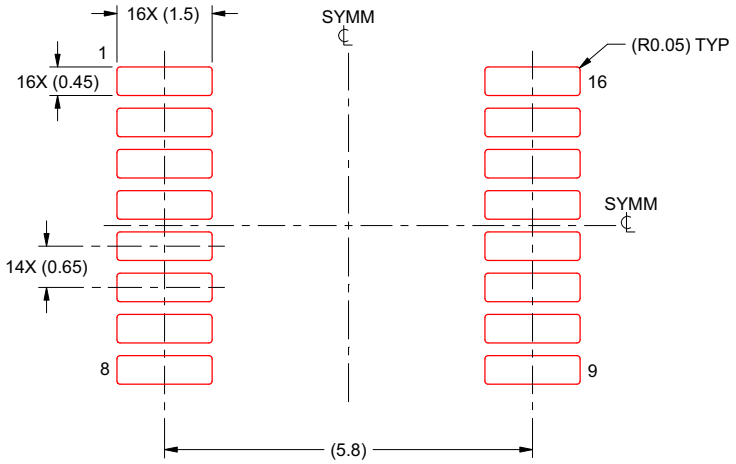
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX7612PWRQ1	ACTIVE	TSSOP	PW	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

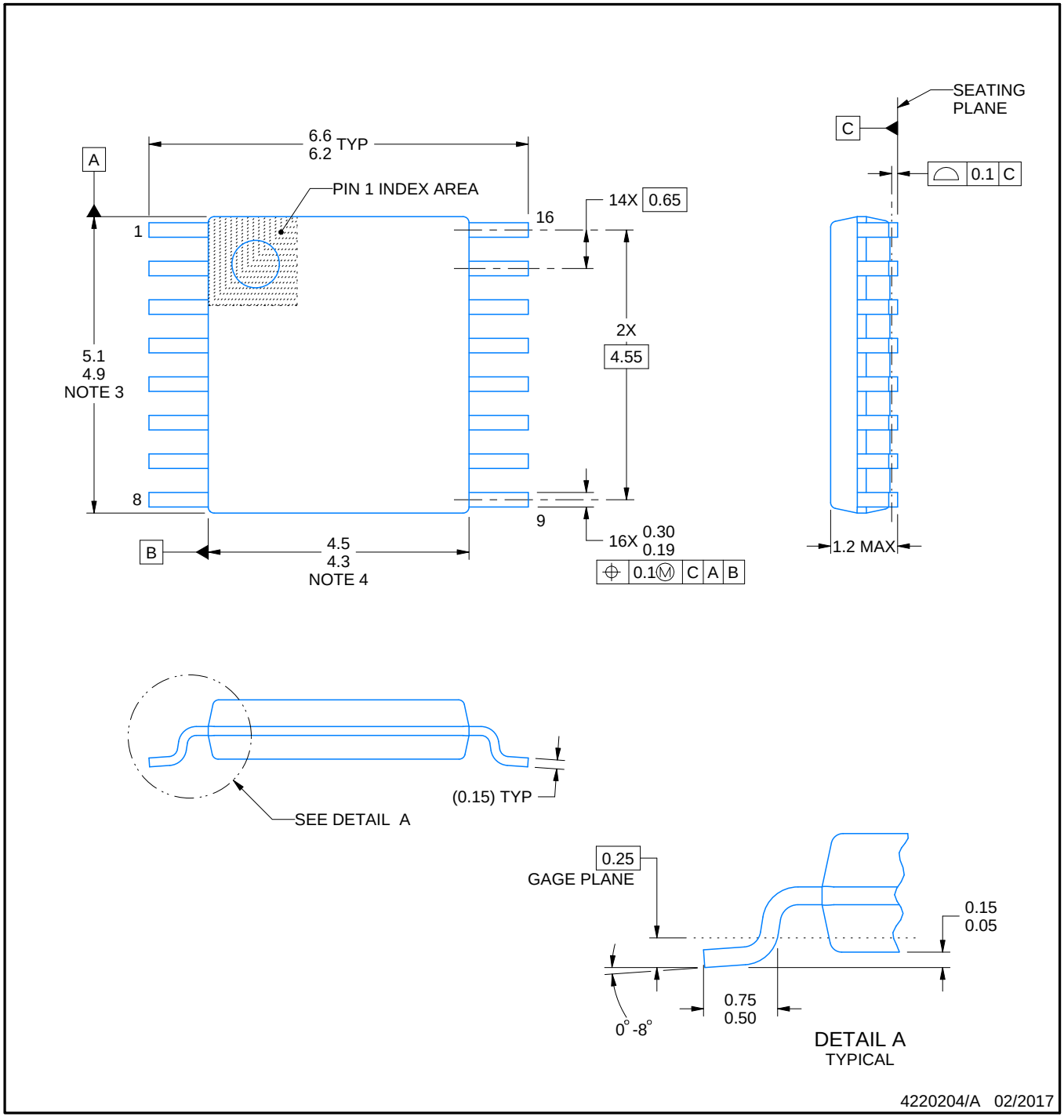
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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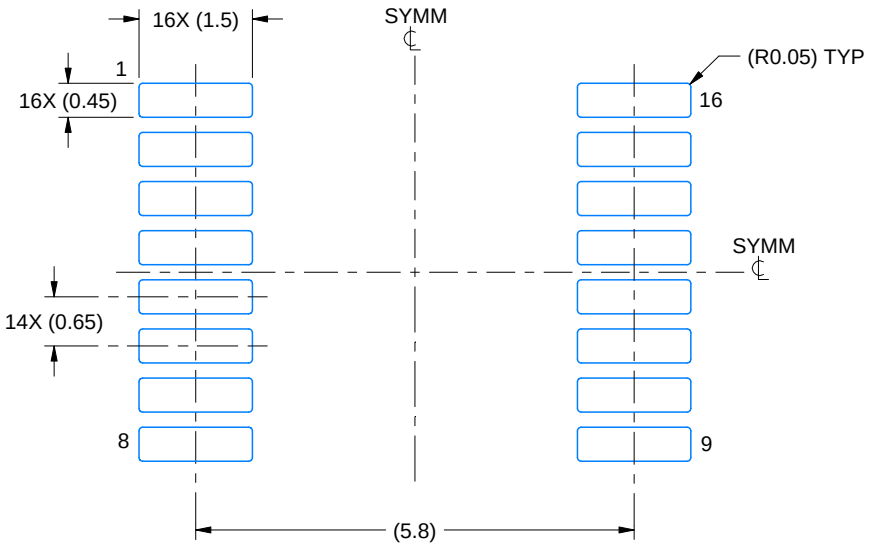
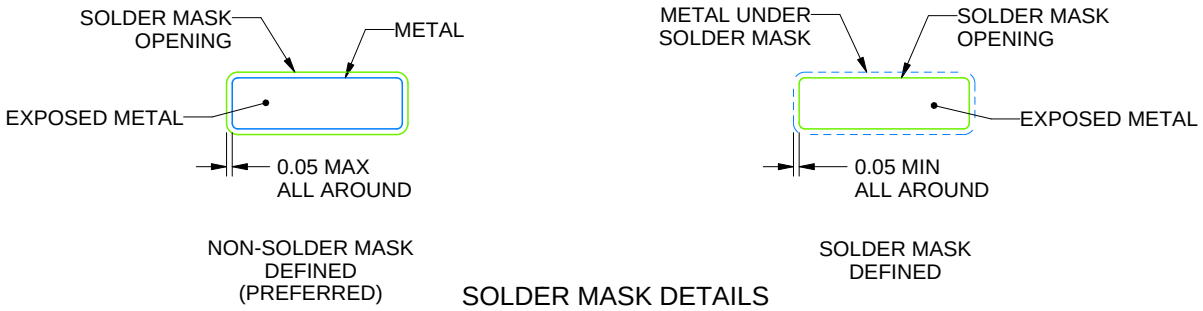
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

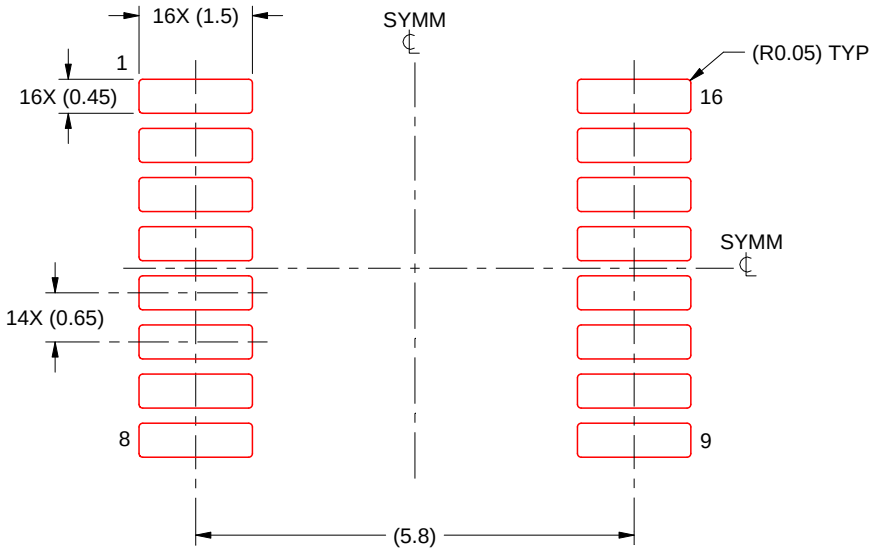


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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