TPD1E01B04 适用于 USB Type-C 和 Thunderbolt 3 的单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±15kV 接触放电
  - ±17kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2.5A (8/20μs)
- IO 电容：
  - 0.18pF（典型值）
  - 0.2pF（最大值）
- 直流击穿电压：6.4V（典型值）
- 超低泄漏电流：10nA（最大值）
- 低静电放电 (ESD) 钳位电压：16A 传输线路脉冲 (TLP) 时为 15V
- 低插入损耗：26.9GHz（–3dB 带宽）
- 支持速率高达 20Gbps 的高速接口
- 工业温度范围：-40°C 至 +125°C
- 超小型 0201 封装

2 应用

- 终端设备
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - 电视和监视器
  - USB 软件狗
  - 扩展坞
- 接口
  - USB Type-C
  - Thunderbolt 3
  - USB 3.1 第 2 代
  - 高清多媒体接口 (HDMI) 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3

3 说明

TPD1E01B04 是一款适用于 USB Type-C 和 Thunderbolt 3 电路保护的双向 TVS ESD 保护二极管阵列。TPD1E01B04 的额定 ESD 冲击消散值等于 IEC 61000-4-2（4 级）国际标准中规定的最高水平。

此器件 特有 一个 0.18pF（典型值）IO 电容，适用于保护速率高达 20Gbps 的高速接口（例如 USB 3.1 Gen2 和 Thunderbolt 3）。低动态电阻和低钳位电压可针对瞬变事件提供系统级保护。

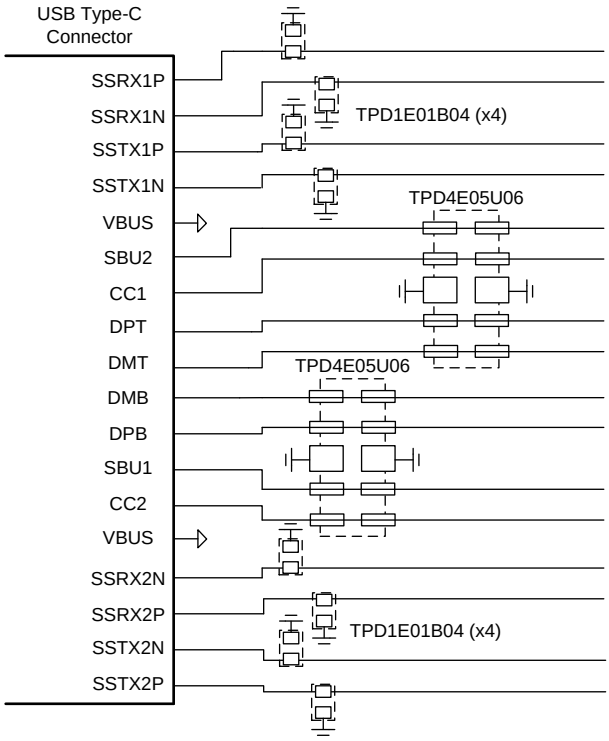
TPD1E01B04 采用符合工业标准的 0201 (DPL) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E01B04	X2SON (2)	0.60mm x 0.30mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2016) to Revision B **Page**

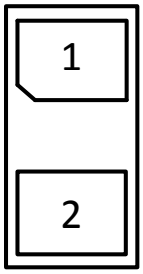
- 更改了*Electrical Characteristics*表。更新了 V_{HOLD} 限值 ... 1

Changes from Original (March 2016) to Revision A **Page**

- 器件状态从*产品预览*改为*量产数据* ... 1

5 Pin Configuration and Functions

DPL Package
2-Pin X2SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs)		27	W
	IEC 61000-4-5 current (t_p - 8/20 µs)		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		IEC 61000-4-2 air-gap discharge	±17000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E01B04 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	582	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	264.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	394.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	394.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to IO pin			–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	5.9	6.5	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		7		V
		I_{PP} = 5 A, TLP, from IO to GND		9.2		
		I_{PP} = 16 A, TLP, from IO to GND		15		
		I_{PP} = 1 A, TLP, from GND to IO		7		
		I_{PP} = 5 A, TLP, from GND to IO		9.2		
		I_{PP} = 16 A, TLP, from GND to IO		15		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.57		Ω
		GND to IO		0.57		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND T_A = 25°C		0.18	0.20	pF

6.7 Typical Characteristics

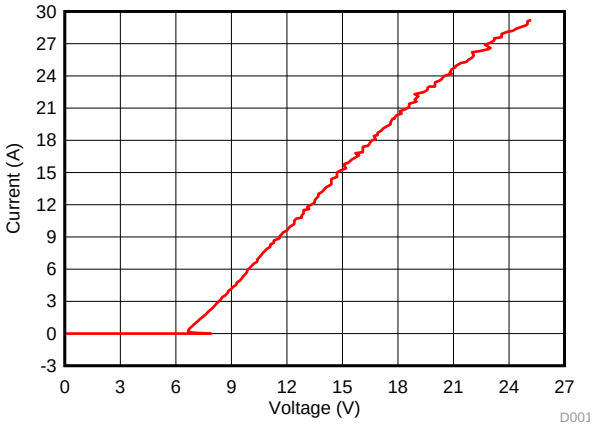


Figure 1. Positive TLP Curve

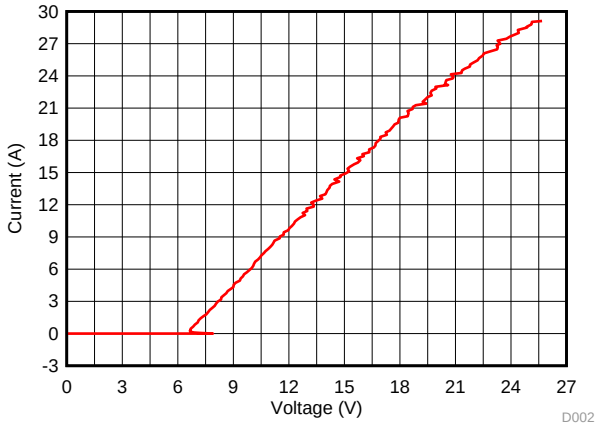


Figure 2. Negative TLP Curve

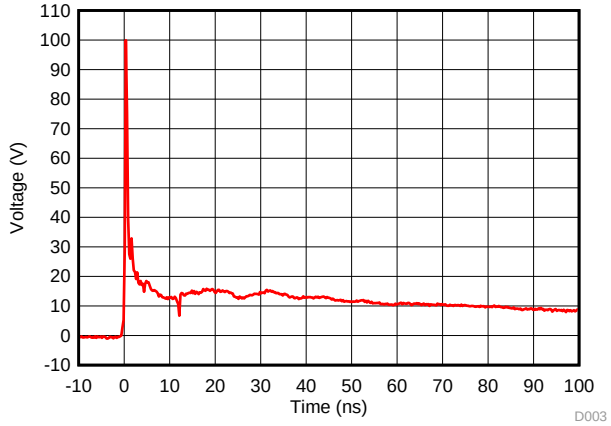


Figure 3. 8-kV IEC Waveform

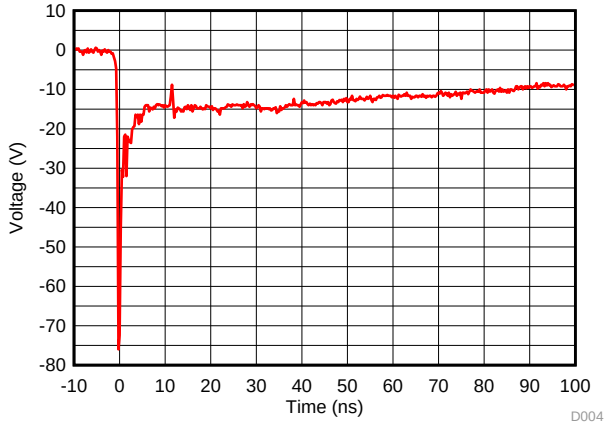


Figure 4. –8-kV IEC Waveform

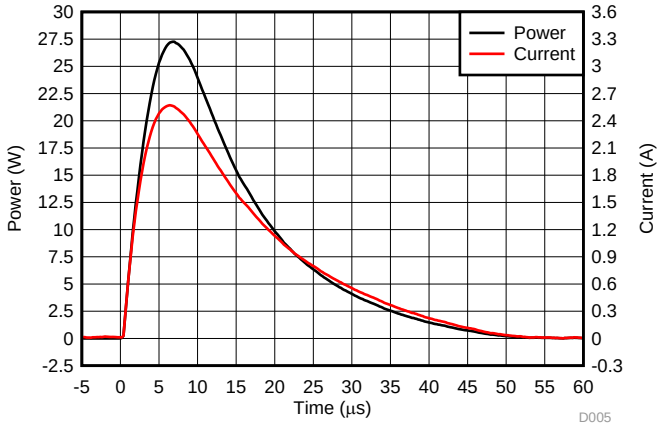


Figure 5. Surge Curve (t_p = 8/20µs), IO pin to GND

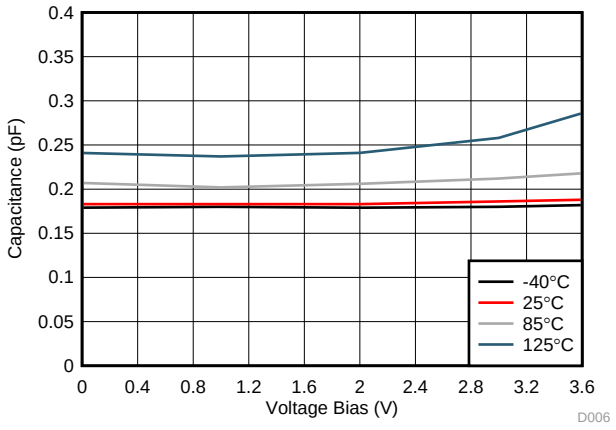


Figure 6. Capacitance vs. Bias Voltage

Typical Characteristics (continued)

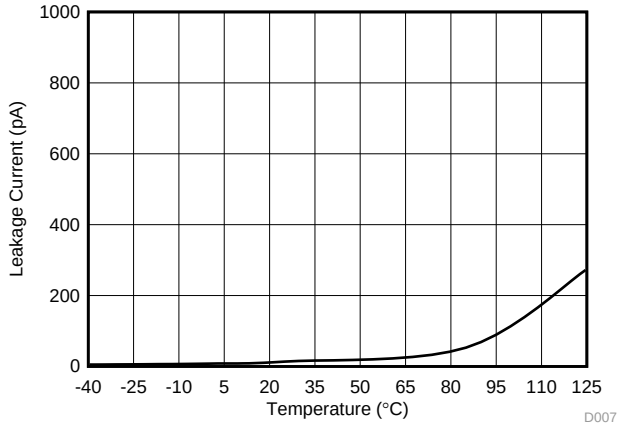


Figure 7. Leakage Current vs. Temperature

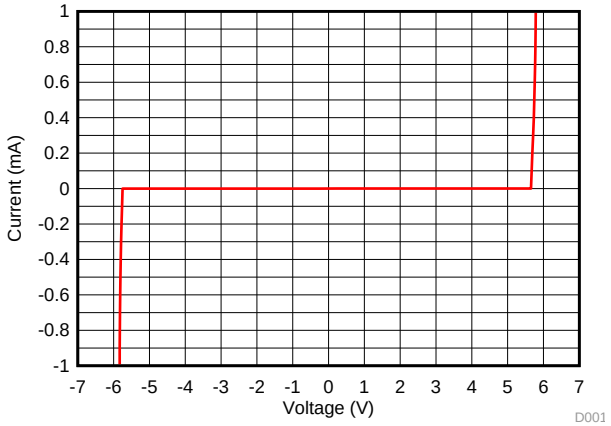


Figure 8. DC Voltage Sweep I-V Curve

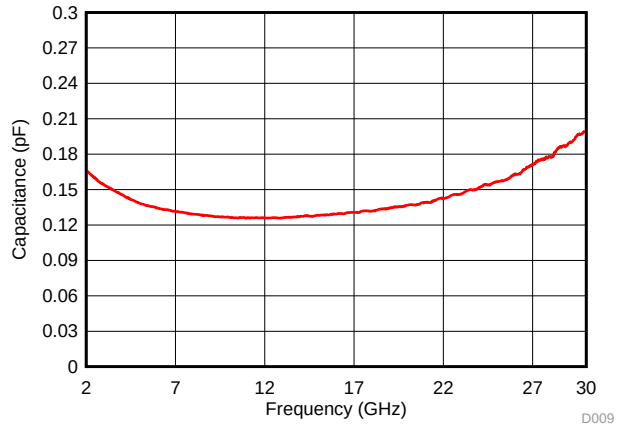


Figure 9. Capacitance vs. Frequency

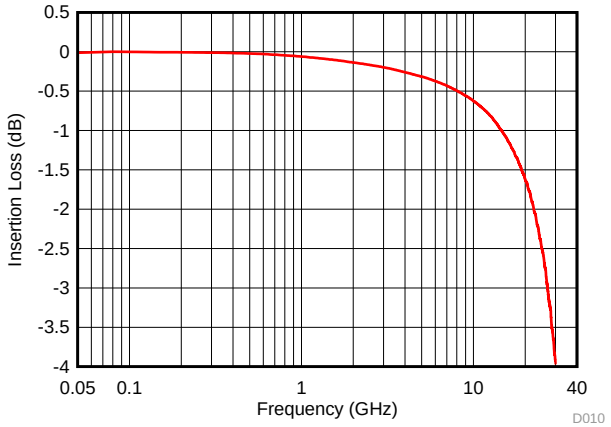


Figure 10. Insertion Loss

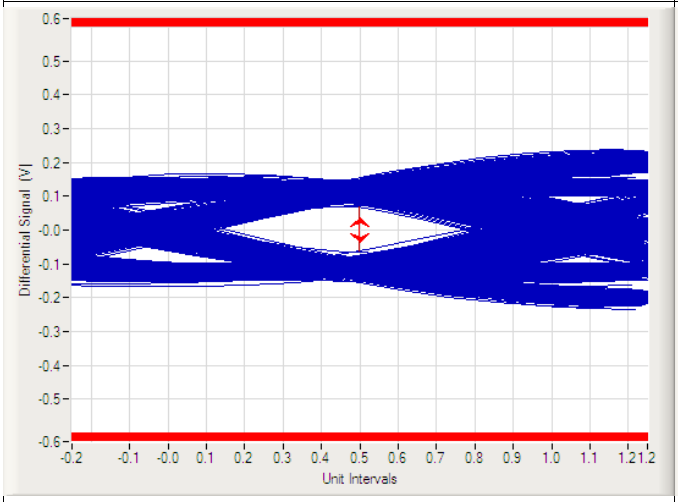


Figure 11. USB3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

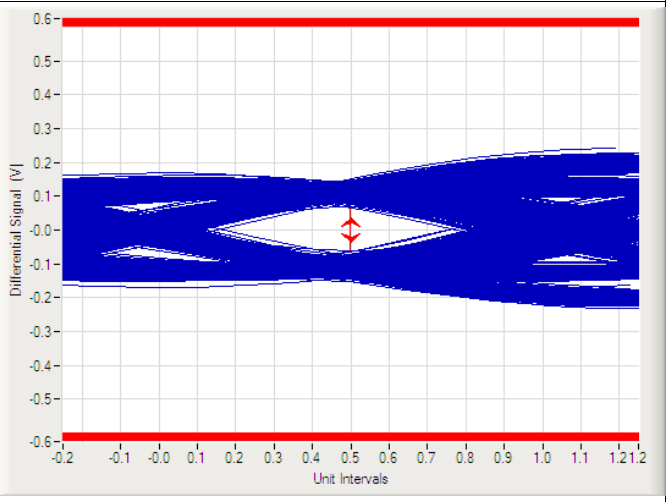


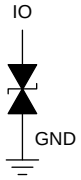
Figure 12. USB3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04)

7 Detailed Description

7.1 Overview

The TPD1E01B04 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins including Thunderbolt 3. The low capacitance allows for extremely low losses even at RF frequencies such as USB 3.1 Gen 2, Thunderbolt 3, or antenna applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and ±17-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 27 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.18 pF (typical) and 0.20 pF (maximum). This device supports data rates up to 20 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V (typical). This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±2.5 V

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.2 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 20 Gbps, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

Feature Description (continued)

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E01B04 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E01B04 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E01B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

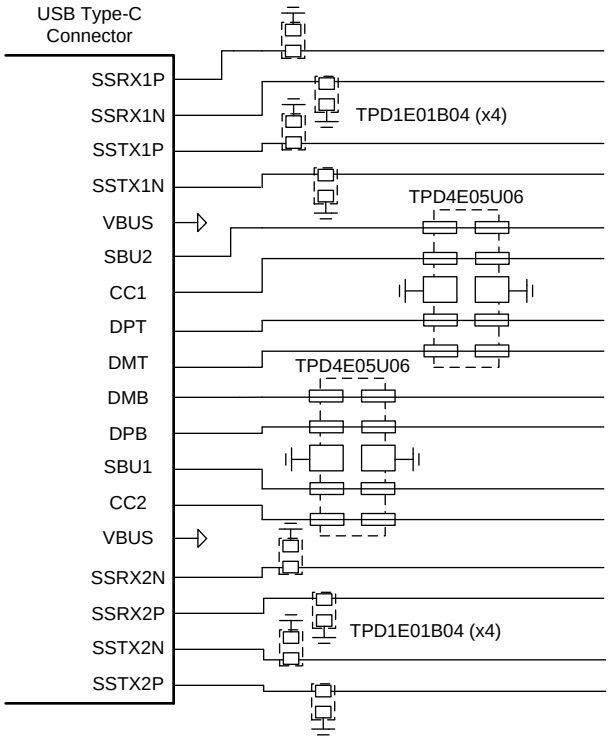


Figure 13. USB Type-C for Thunderbolt 3 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E01B04 devices and two TPD4E05U06 devices are being used in a USB Type-C for Thunderbolt 3 application. This provides a complete ESD protection scheme.

Given the Thunderbolt 3 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on superspeed Lines	0 V to 3.6 V
Operating frequency on superspeed Lines	up to 10 GHz
Signal range on CC, SBU, and DP/DM Lines	0 V to 5 V

Typical Application (continued)

Table 1. Design Parameters (continued)

DESIGN PARAMETER	VALUE
Operating frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E01B04 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP-DM lines.

8.2.2.2 Operating Frequency

The TPD1E01B04 has a 0.18 pF (typical) capacitance, which supports the Thunderbolt 3 data rates of 20 Gbps. The TPD4E05U06 has a 0.5-pF (typical) capacitance, which easily supports the CC, SBU, and DP-DM data rates.

8.2.3 Application Curves

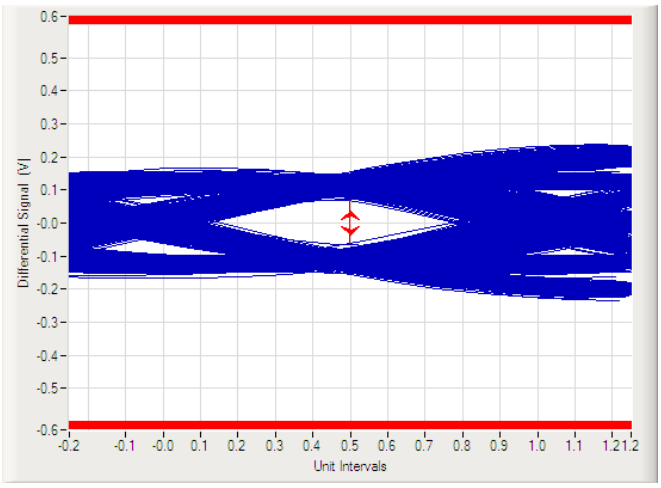


Figure 14. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

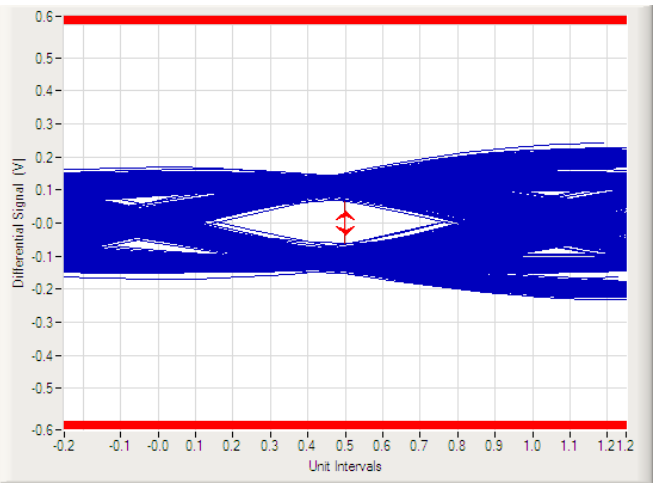


Figure 15. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04)

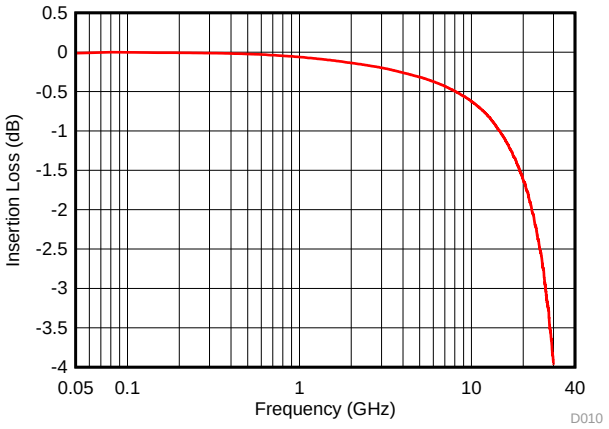


Figure 16. Insertion Loss

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

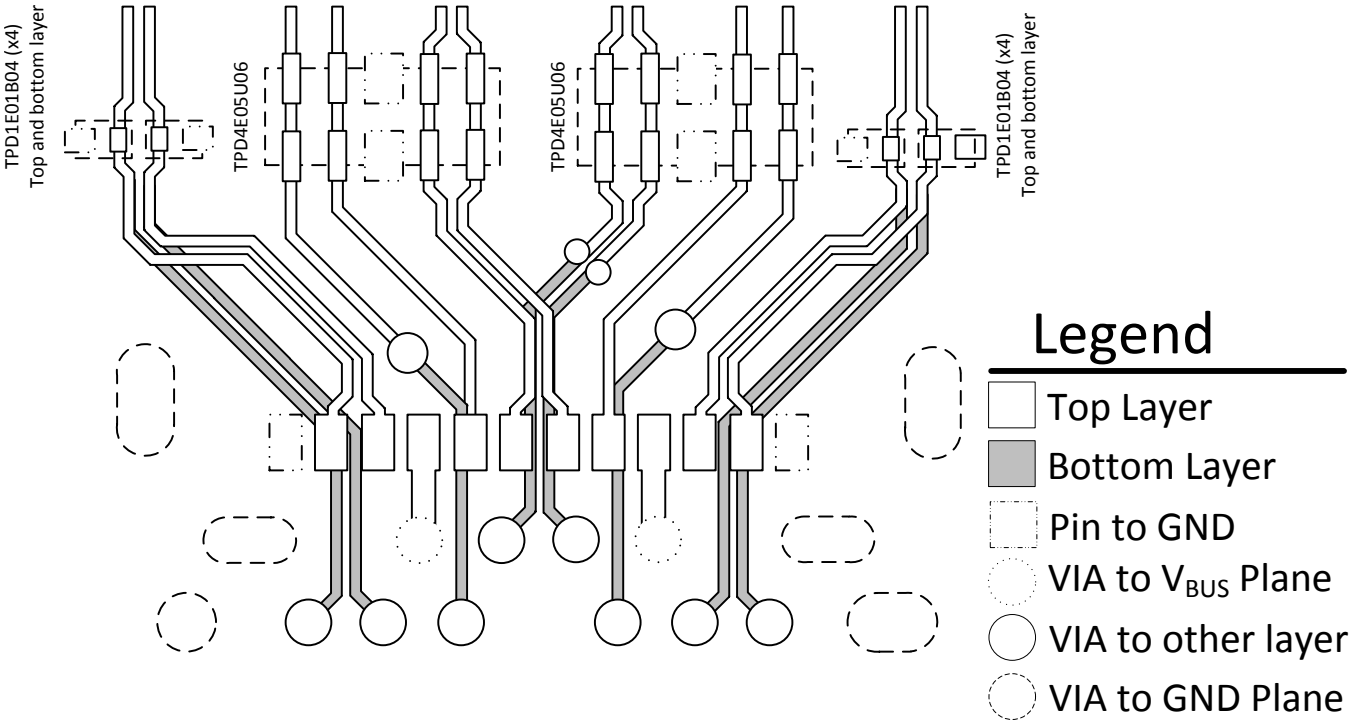


Figure 17. USB Type-C Mid-Mount, Hybrid Connector ESD Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

用户指南《TPD1E01B04 评估模块》，SLVUAN5

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E01B04DPLR	ACTIVE	X2SON	DPL	2	15000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TPD1E01B04DPLT	ACTIVE	X2SON	DPL	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TPD1E01B04DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5C	Samples
TPD1E01B04DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPD1E01B04 :

- Automotive : TPD1E01B04-Q1

NOTE: Qualified Version Definitions:

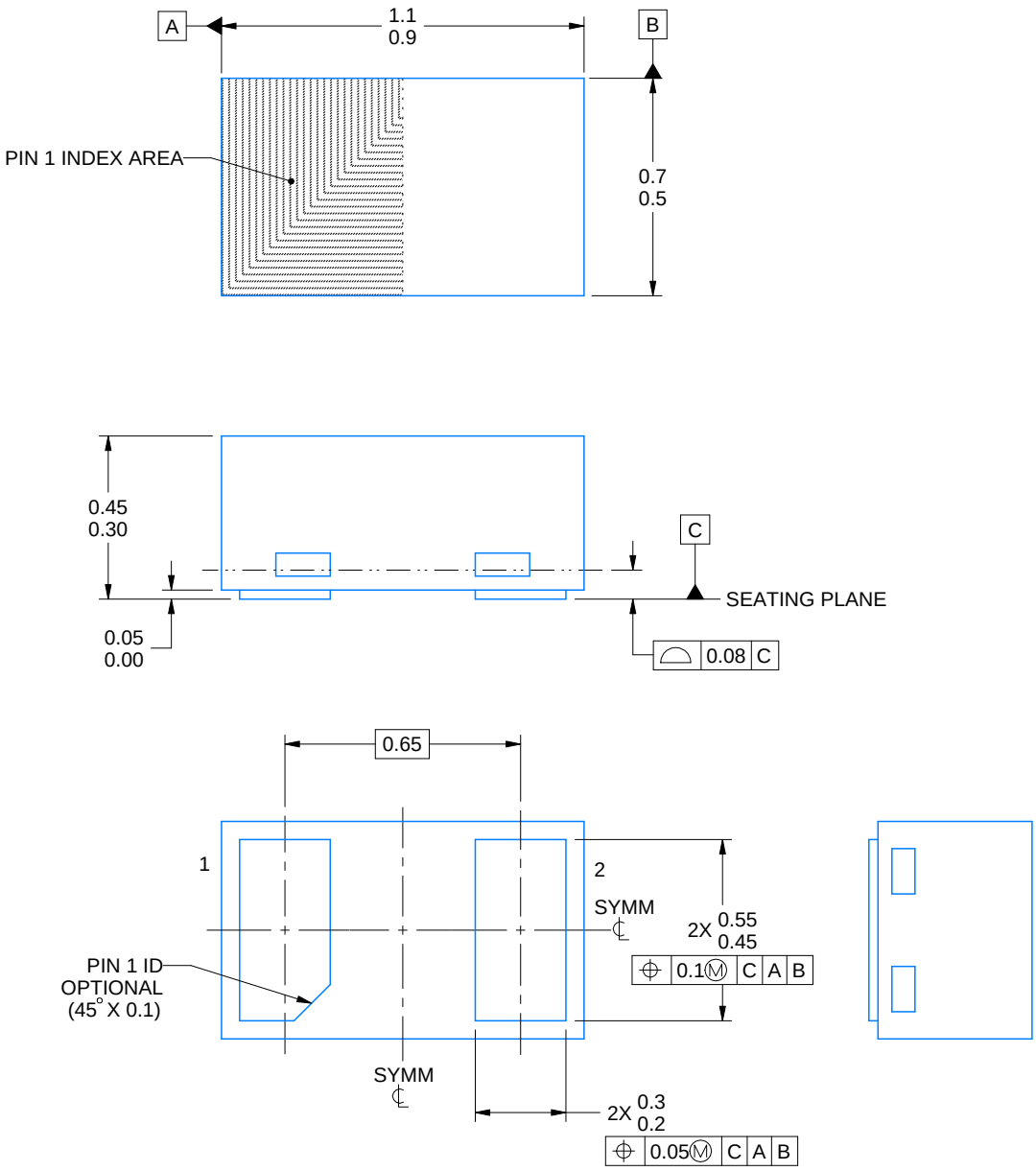
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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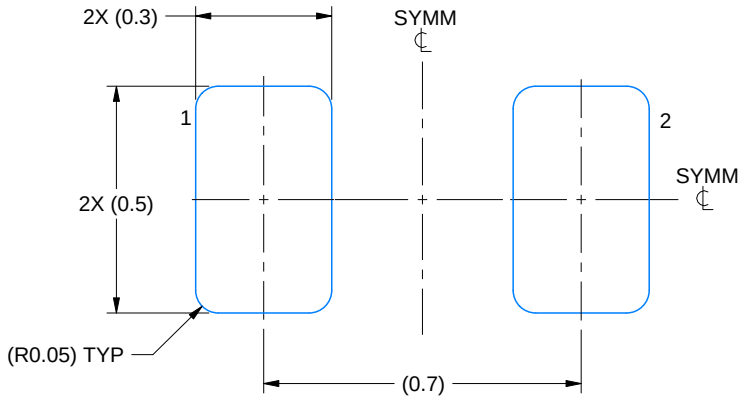
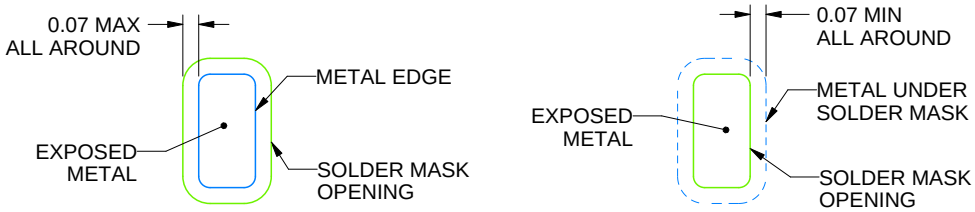
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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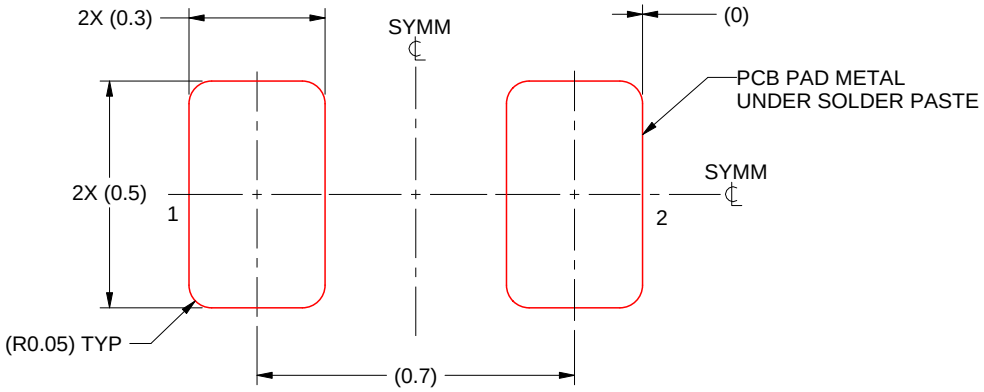
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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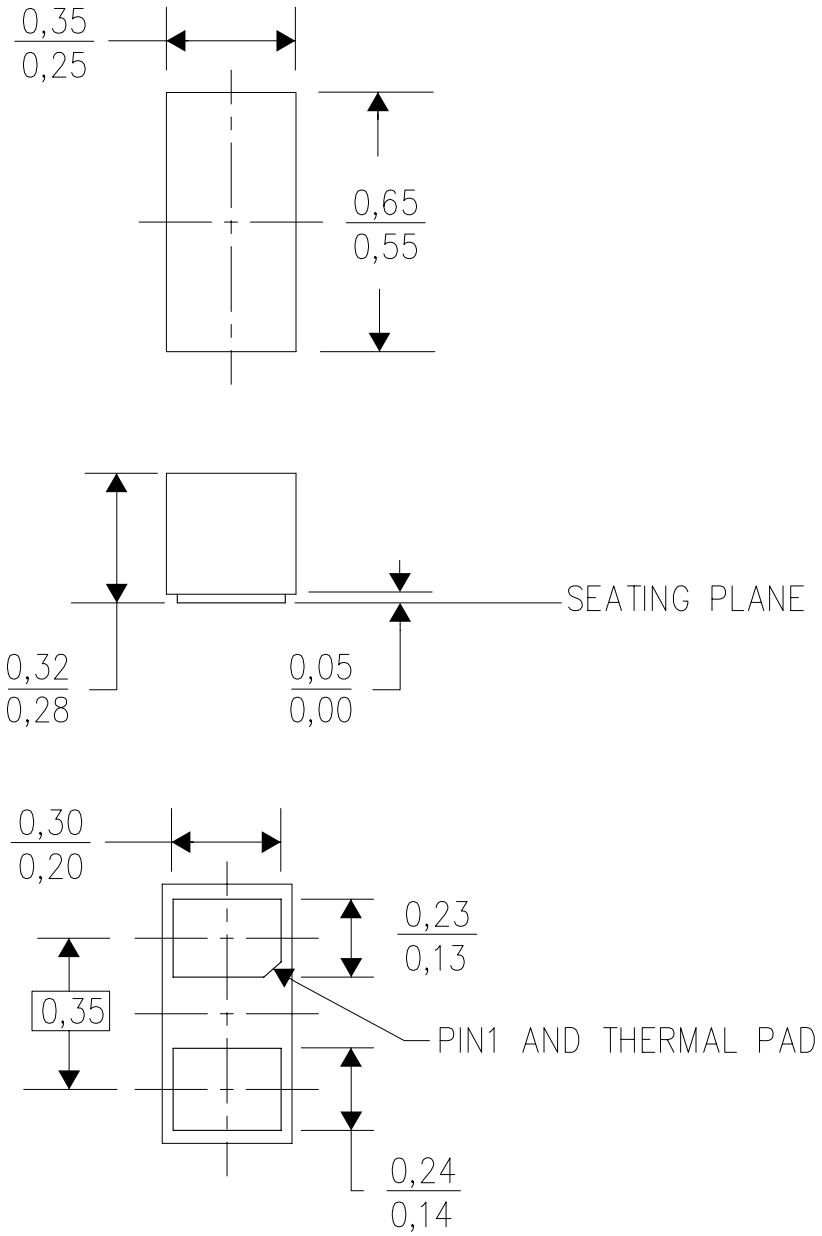
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

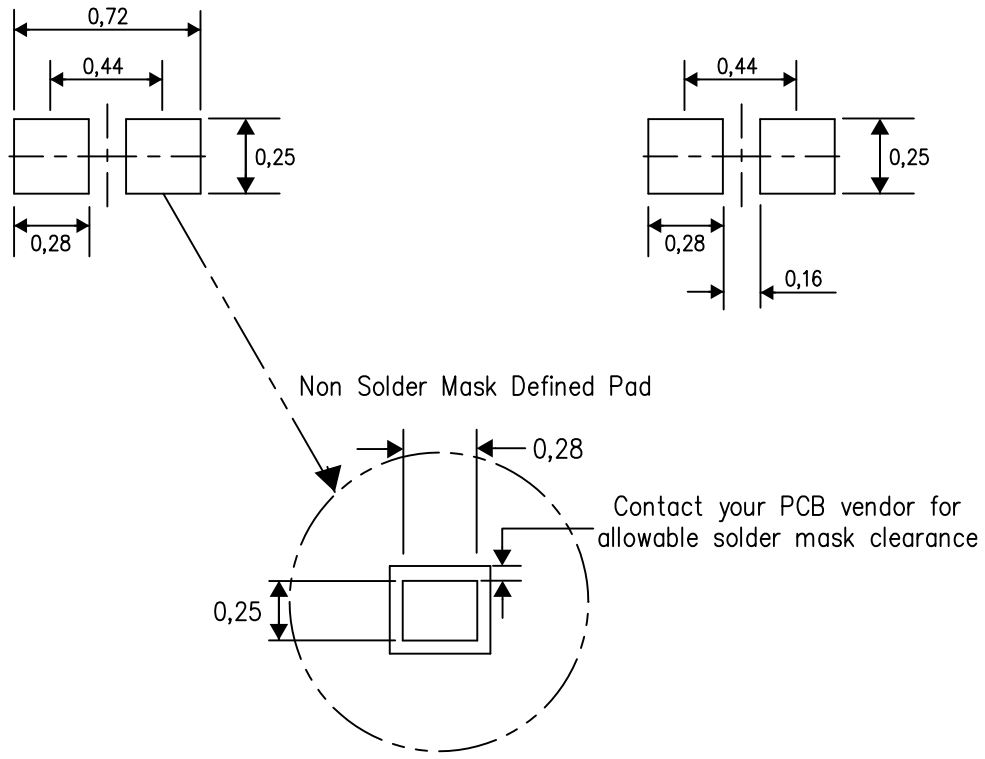


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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