用于 SuperSpeed（速率高达 6Gbps）接口的 TPDxE05U06-Q1 1 通道和 4 通道 ESD 保护二极管

1 特性

- 符合 AEC-Q101
  - 人体放电模型 (HBM) 分类等级 H3B
  - 充电器件模型 (CDM) 分类等级 C5
  - 器件温度范围：–40°C 至 +125°C
- IEC 61000-4-2 4 级 ESD 保护（请参阅 *ESD Ratings—IEC Specification* 表）
  - ±12kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 2.5A (8/20μs)
- I/O 电容 0.42pF 至 0.5pF（典型值）
- 直流击穿电压 6.4V（最小值）
- 超低漏电流 10nA（最大值）
- 低 ESD 钳位电压（在 5A TLP 下为 14V）
- 简易直通路由封装

2 应用

- 终端设备
  - 音响主机
  - 后座娱乐系统
  - 远程信息处理
  - USB 集线器
  - 导航模块
  - 媒体接口
- 接口
  - USB 2.0
  - USB 3.0
  - HDMI 1.4/2.0
  - 低压差分信令 (LVDS)
  - DisplayPort
  - SIM 卡

3 说明

TPDxE05U06-Q1 是一系列具有超低电容的单向瞬态电压抑制器 (TVS) 静电放电 (ESD) 保护二极管。这些器件旨在耗散那些高于 IEC61000-4-2 4 级国际标准中规定的最高水平的 ESD 冲击。超低负载电容特性使得这些器件非常适合保护任何高达 6Gbps 的高速 信号应用。

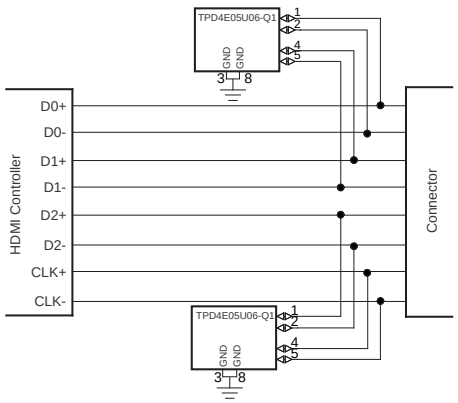
这些器件还具有未经过汽车认证的型号：TPDxE05U06。

器件信息(1)

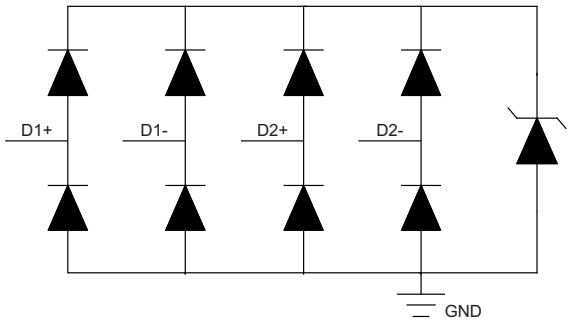
器件型号	封装	封装尺寸（标称值）
TPD4E05U06-Q1	USON (10)	2.50mm x 1.00mm
TPD1E05U06-Q1	X1SON (2)	0.60mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

TPD4E05U06-Q1 简化原理图



TPD4E05U06-Q1 框图



目录

4 修订历史记录

Changes from Revision A (August 2014) to Revision B **Page**

- 添加了 1 通道 (TPD1E05U06-Q1) 封装 ... 1
- Added DPY package information in *Thermal Information* table ... 4
- Added DPY package Dynamic resistance in *Electrical Characteristics* table ... 5
- Added DPY package Line capacitance in *Electrical Characteristics* table ... 5

Changes from Revision B (August 2016) to Revision C **Page**

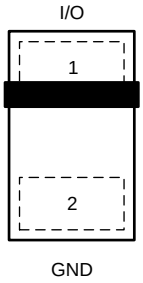
- 已更改 在*引脚配置和功能* 部分中添加了 DPY 封装引脚配置 ... 1

Changes from Original (August 2014) to Revision A **Page**

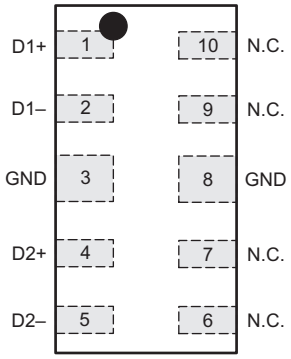
- 在“特性”中添加了内容（请参阅 *ESD Ratings—IEC Specification* 表）：IEC 61000-4-2 4 级 ESD 保护 ... 1

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



DQA Package
10-Pin USON
Top View



Pin Functions TPD1E05U06-Q1 DPY

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	I/O	I/O	ESD Protected Channel(1)
2	GND	Ground	Ground; Connect to ground

(1) Place as close to the connector as possible.

Pin Functions TPD4E05U06-Q1 DQA

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	D1+	I/O	ESD Protected Channel(1)
2	D1–	I/O	ESD Protected Channel(1)
4	D2+	I/O	ESD Protected Channel(1)
5	D2–	I/O	ESD Protected Channel(1)
6, 7, 9, 10	NC	NC	Not Connected; Used for optional straight-through routing. Can be left floating or grounded
3, 8	GND	Ground	Ground; Connect to ground

(1) Place as close to the connector as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Current (tp – 8/20 µs)		2.5	A
	IEC 61000-4-5 Power (tp – 8/20 µs) - TPD4E05U06-Q1 (3)		40	W
	IEC 61000-4-5 Power (tp – 8/20 µs) - TPD1E05U06-Q1 (3)		30	W
T_A	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25°C

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM), per AEC Q100-002 (2)	±8000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V(ESD)	Electrostatic Discharge	IEC 61000-4-2 contact discharge - TPD4E05U06-Q1 (1)	±12000	V
		IEC 61000-4-2 contact discharge - TPD1E05U06-Q1	±12000	
		IEC 61000-4-2 air-gap discharge	±15000	

(1) Measured at 25°C, per IEC 61000.4.2 Ed. 2.0 Section 7.2.4.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC (1)		TPD1E05U06-Q1 DPY (X1SON) 2 PINS	TPD4E05U06-Q1 DQA (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	697.3	327	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	471	189.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	575.9	257.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	175.7	60.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	575.1	257	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT – OUTPUT RESISTANCE								
V_{RWM}	Reverse stand-off voltage		I_{IO} < 10 µA				5.5	V
V_{BR}	Break-down voltage		I_{IO} = 1 mA		6.4		8.7	V
V_{CLAMP}	Clamp voltage		I_{PP} = 1 A, TLP, from I/O to GND (1)			10		V
			I_{PP} = 5 A, TLP, from I/O to GND (1)			14		
			I_{PP} = 1 A, TLP, from GND to I/O (1)			3		
			I_{PP} = 5 A, TLP, from GND to I/O (1)			7.5		
I_{LEAK}	Leakage current		V_{IO} = 2.5 V			1	10	nA
R_{DYN}	Dynamic resistance	DPY package	I/O to GND (2)			0.8		Ω
			GND to I/O (2)			0.7		
		DQA package	I/O to GND (2)			0.96		
			GND to I/O (2)			0.9		
CAPACITANCE								
C_L	Line capacitance		V_{IO} = 2.5 V, f = 1 MHz, I/O to GND	TPD1E05U06-Q1 DPY package		0.42		pF
				TPD4E05U06-Q1 DQA package		0.5		
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of input capacitance		GND Pin = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, Channel x pin to GND – channel y pin to GND			0.05	0.08	pF
C_{CROSS}	Channel to channel input capacitance		GND Pin = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins			0.04	0.08	pF

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 5 A and I = 10 A.

6.7 Typical Characteristics

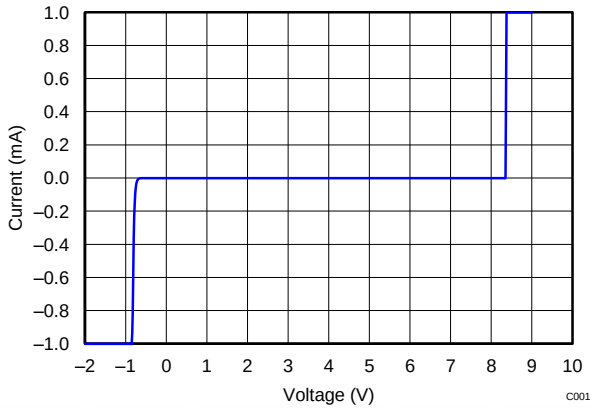


Figure 1. Current vs Voltage
Current vs Voltage DC Voltage Sweep I-V Curve

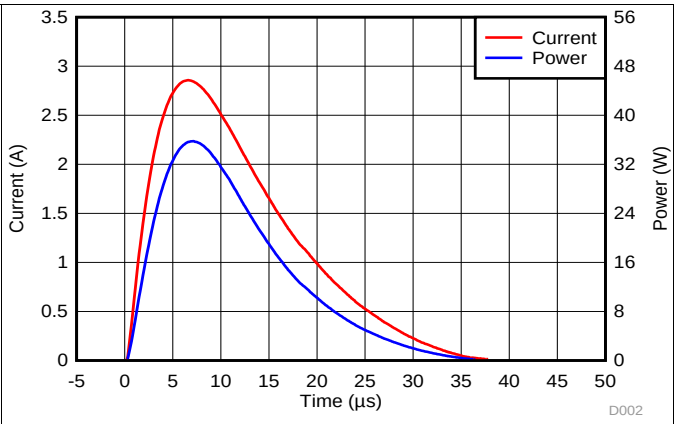


Figure 2. Current and Power vs Time
Surge Curve (tp = 8/20 µs), Pin I/O to GND

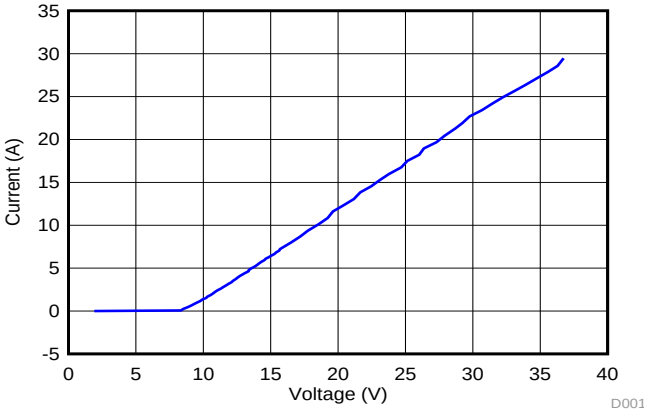


Figure 3. Current vs Voltage
Positive TLP Plot I/O to GND

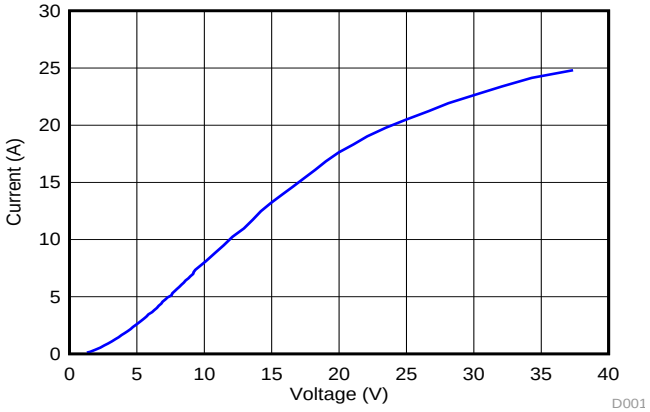


Figure 4. Current vs Voltage
Negative TLP Plot I/O to GND

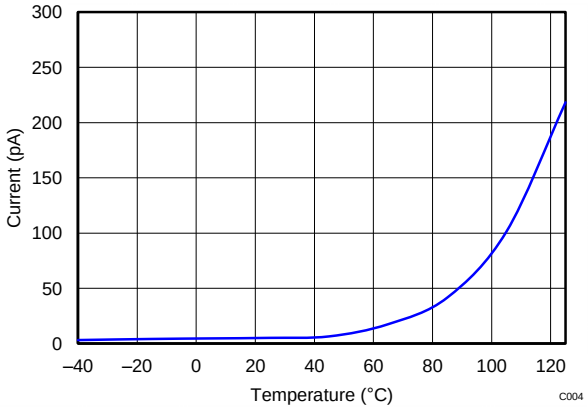


Figure 5. Leakage Current vs Temperature

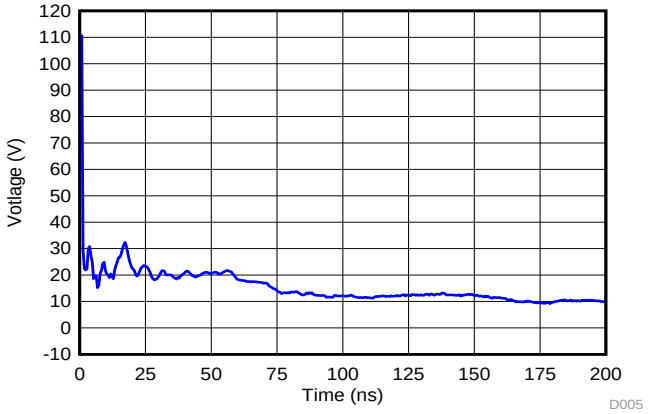


Figure 6. Voltage vs Time 8-kV IEC Waveform

Typical Characteristics (continued)

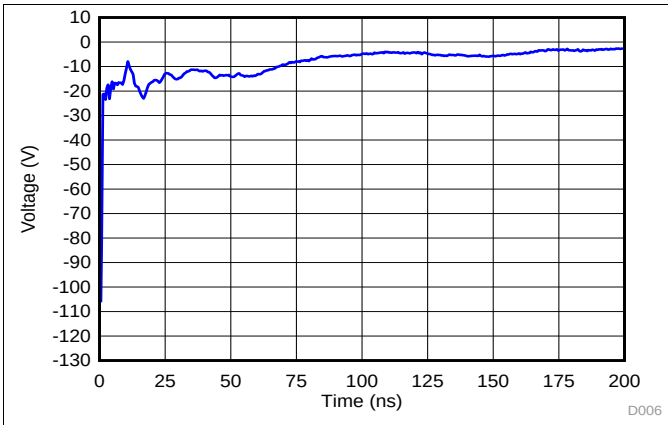


Figure 7. Voltage vs Time –8-kV IEC Waveform

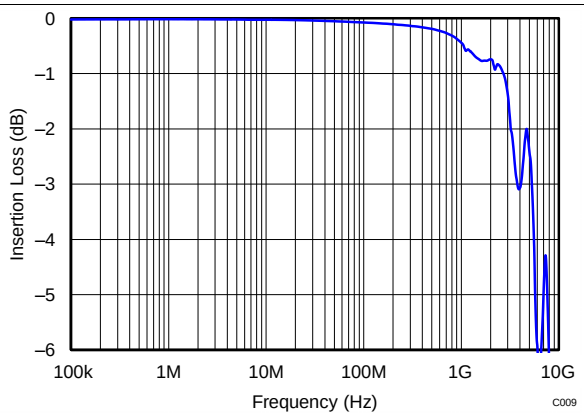


Figure 8. Insertion Loss vs Frequency

7 Detailed Description

7.1 Overview

The TPDxE05U06-Q1 is a family of unidirectional TVS ESD protection diode arrays with ultra-low capacitance between 0.42 pF and 0.5 pF. They are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard (12-kV contact, 15-kV air gap). The ultra-low loading capacitance makes them ideal for protecting any high-speed signal applications up to 6 Gbps.

7.2 Functional Block Diagram

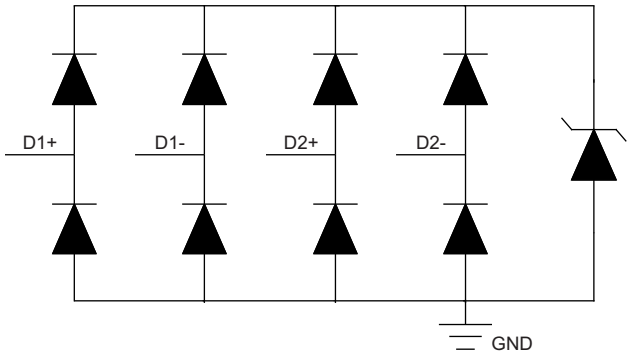


Figure 9. TPD4E05U06-Q1 Block Diagram

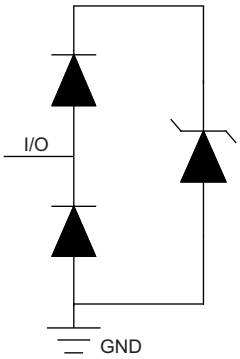


Figure 10. TPD1E05U06-Q1 Block Diagram

7.3 Feature Description

7.3.1 AEC-Q101 Qualification

These devices are qualified to AEC-Q101 standards. They pass HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and are qualified to operate from –40°C to +125°C.

7.3.2 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

Feature Description (continued)

7.3.4 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.5 I/O Capacitance

The capacitance between each I/O pin to ground is 0.5 pF. These capacitances support data rates up to 5 Gbps.

7.3.6 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.4 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5 V.

7.3.7 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

7.3.8 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (I_{PP} = 1 A).

7.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPDxE05U06-Q1 are passive integrated circuits that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06-Q1 (usually within 10s of nano-seconds) the devices reverts to passive.

8 Application and Implementation

8.1 Application Information

The TPD4E05U06-Q1 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

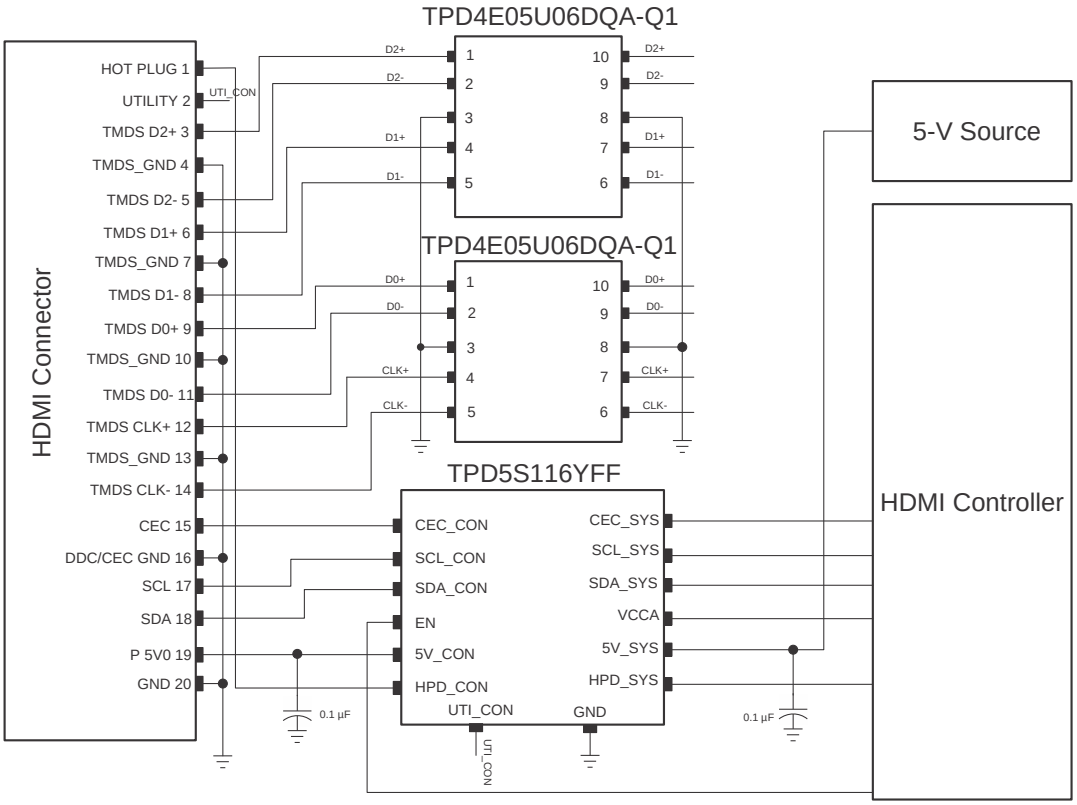


Figure 11. HDMI 1.4 Application

8.2.1 Design Requirements

For this design example, two TPD4E05U06-Q1 devices, and a TPD5S116 are being used in an HDMI 1.4 application. This provides a complete port protection scheme.

Given the HDMI 1.4 application, the parameters in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 2, 4, or 5	0 V to 5 V
Operating frequency	1.7 GHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06-Q1 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E05U06-Q1 has a capacitance of 0.5 pF (Typical), supporting HDMI 1.4 data rates.

8.2.3 Application Curve

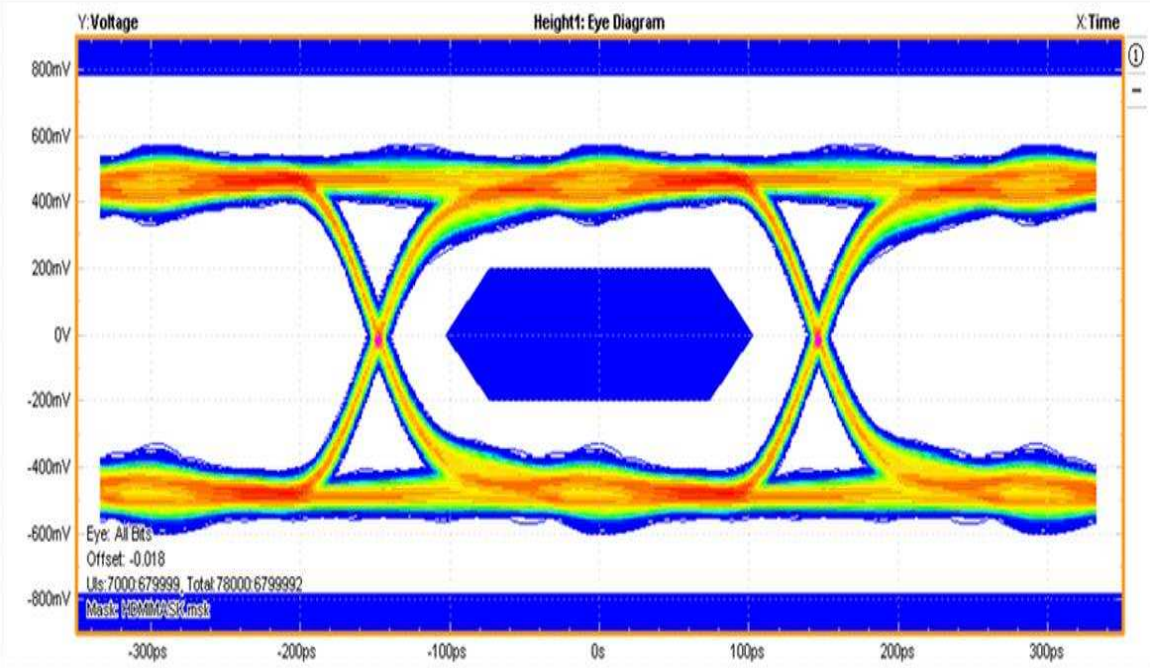


Figure 12. 3.4 Gbps HDMI Eye Diagram

9 Layout

9.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

9.2 Layout Example

This application is typical of an HDMI 1.4 layout.

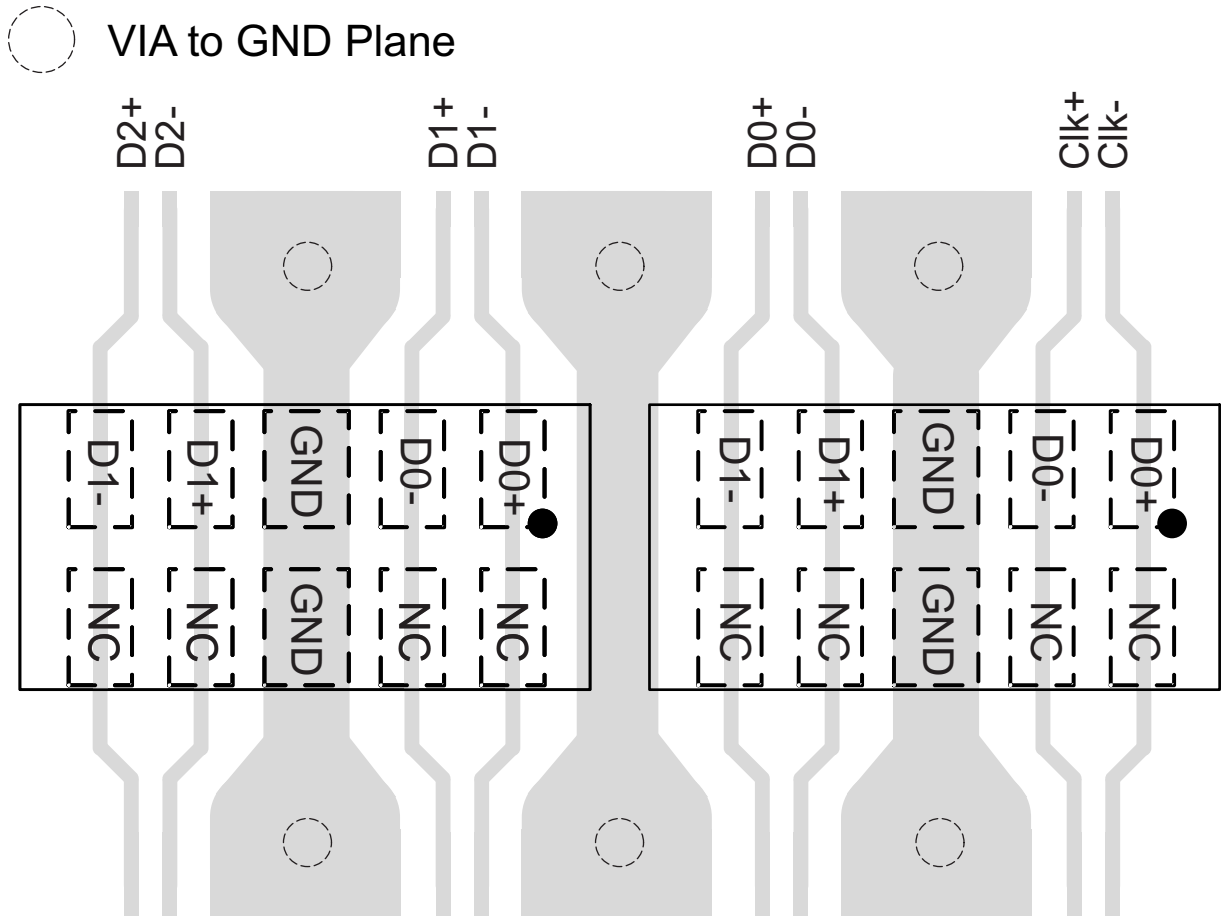


Figure 13. TPD4E05U06-Q1 Layout

10 器件和文档支持

10.1 文档支持

10.1.1 相关文档

请参阅如下相关文档：

- *《TPD1E05U06-Q1 评估模块用户指南》*
- *阅读和理解 ESD 保护数据表*
- *《ESD 布局指南》*
- *《TPD4E05U06DQA GUI 用户指南》*

10.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPD4E05U06-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPD1E05U06-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

10.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

10.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06QDPYRQ1	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4O	Samples
TPD4E05U06QDQARQ1	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(BRH, CQ1)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

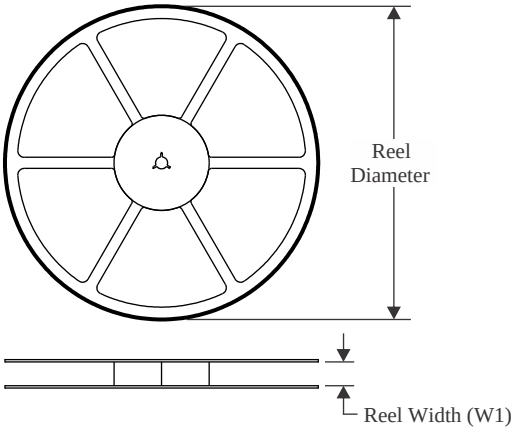
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

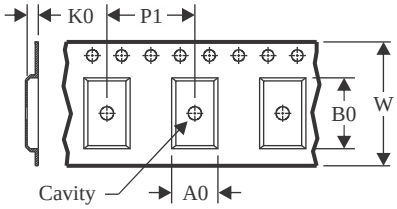
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

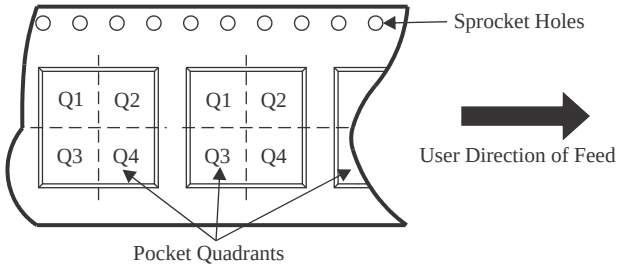


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

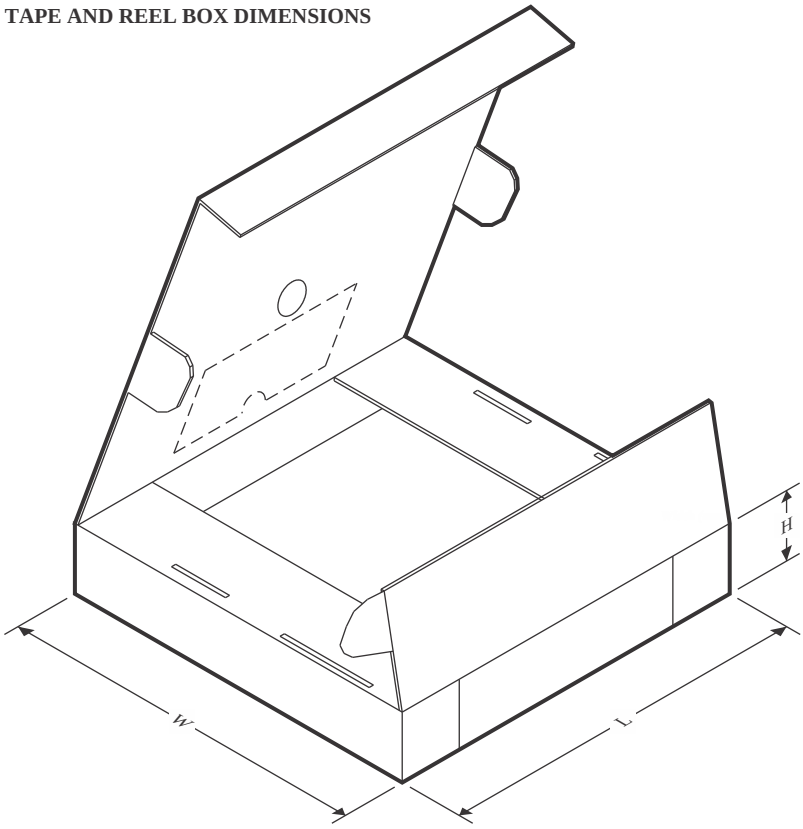
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06QDPYRQ1	X1SON	DPY	2	10000	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1
TPD4E05U06QDQARQ1	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1
TPD4E05U06QDQARQ1	USON	DQA	10	3000	180.0	8.4	1.3	2.83	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06QDPYRQ1	X1SON	DPY	2	10000	189.0	185.0	36.0
TPD4E05U06QDQARQ1	USON	DQA	10	3000	189.0	185.0	36.0
TPD4E05U06QDQARQ1	USON	DQA	10	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

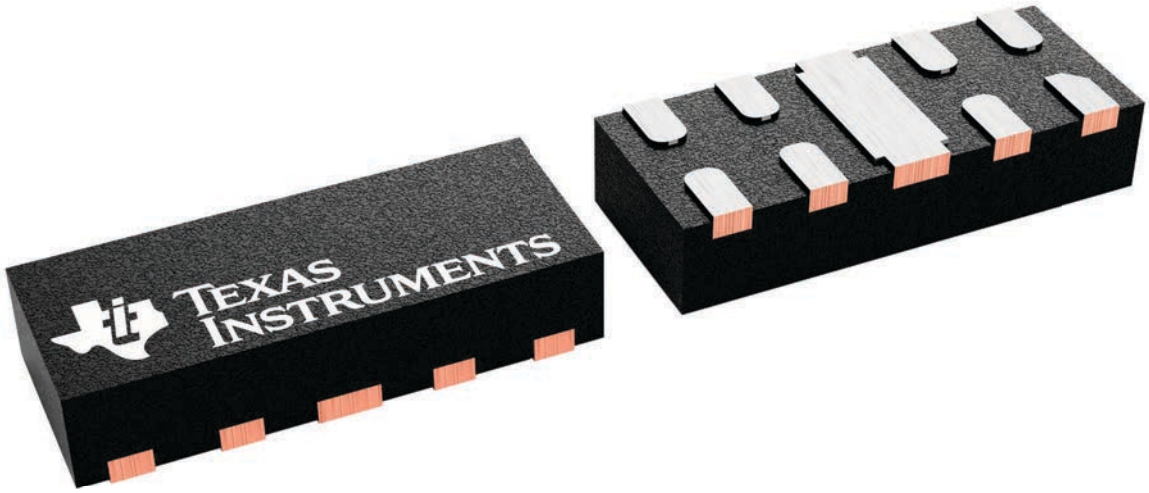
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



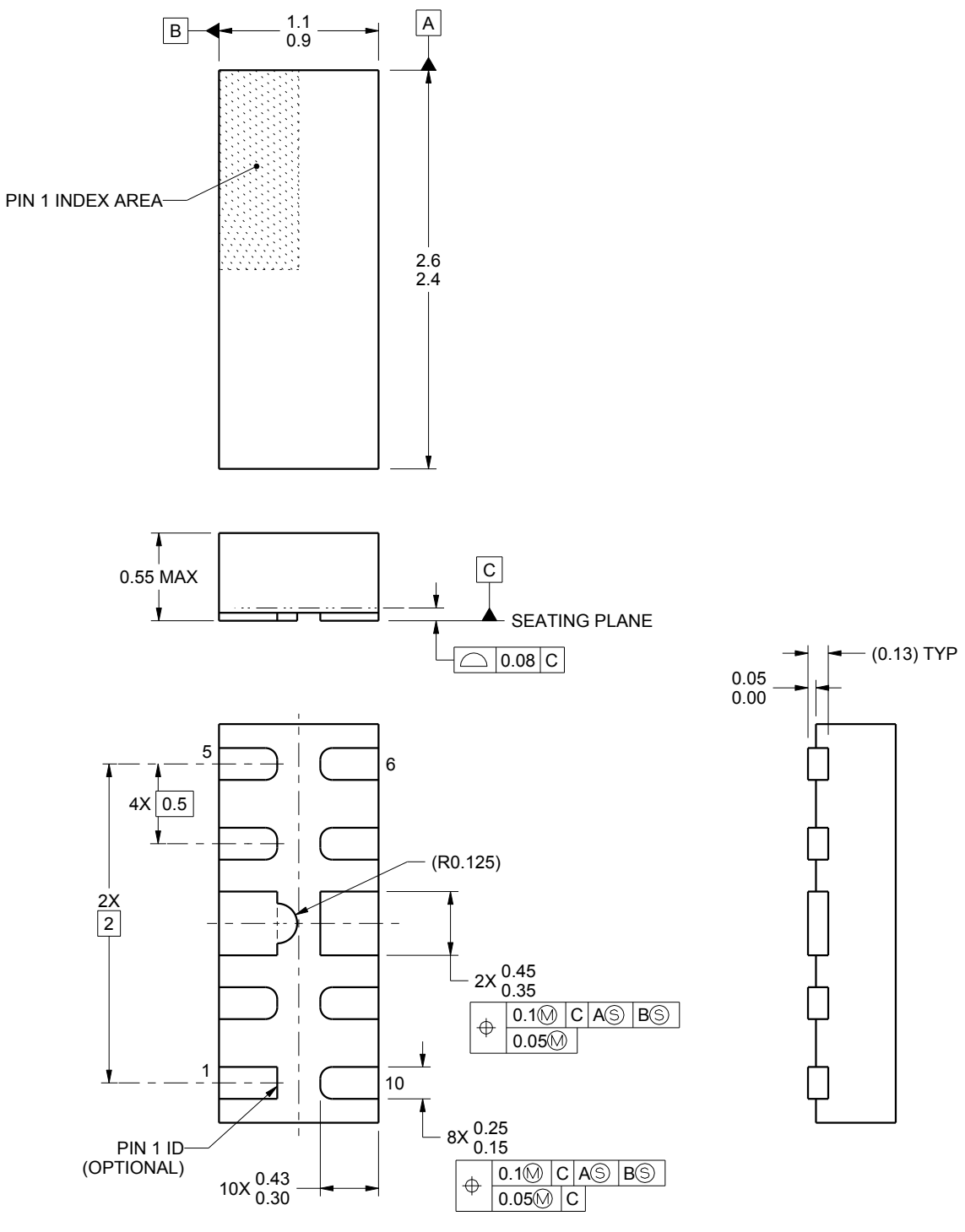
4230320/A

PACKAGE OUTLINE

DQA0010A

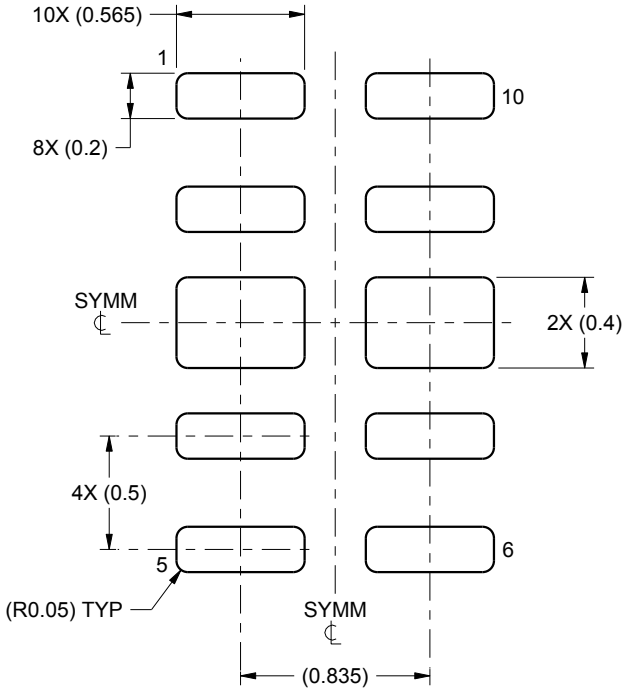
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

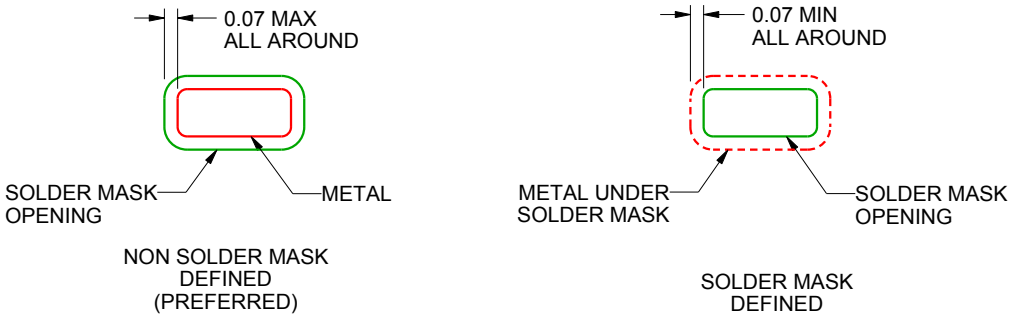


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

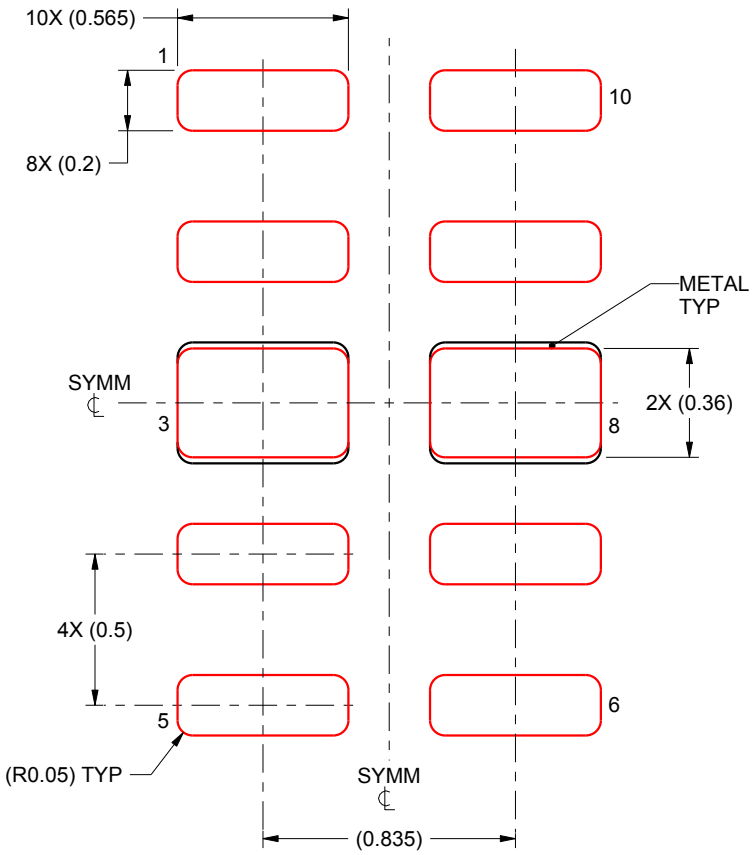
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

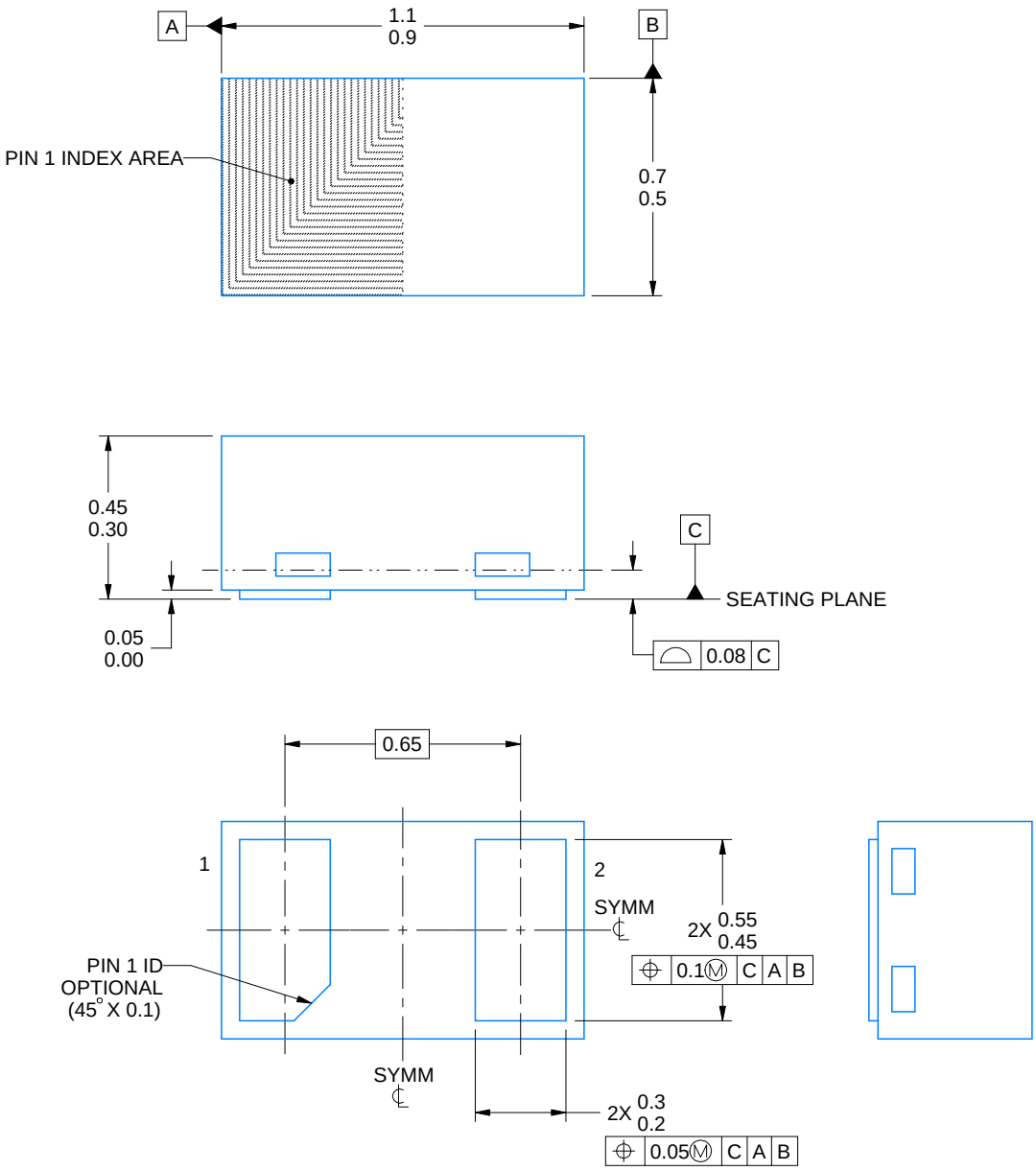
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

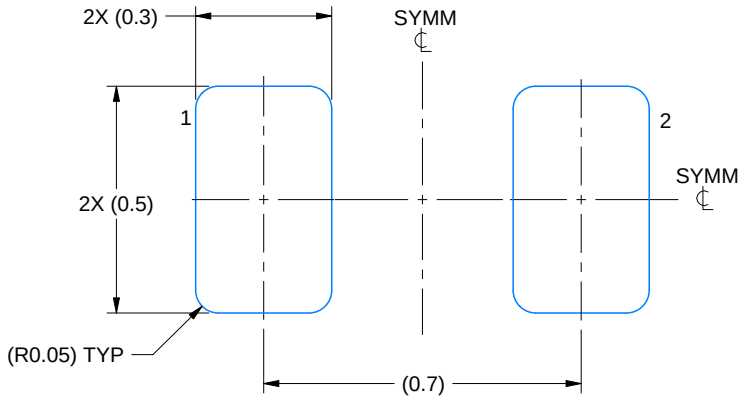
PLASTIC SMALL OUTLINE - NO LEAD



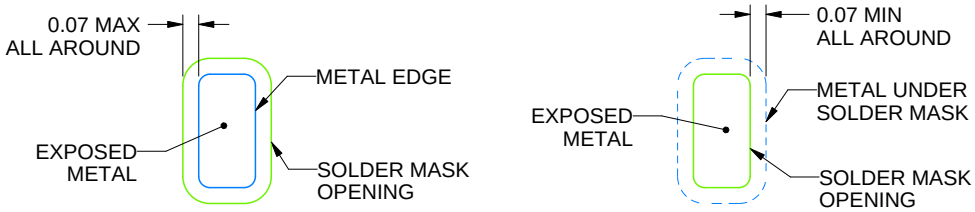
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

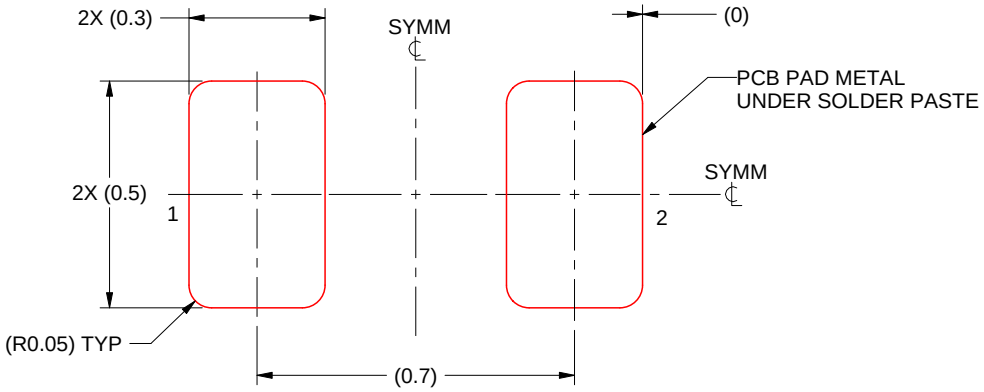


SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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