TPD4E1U06 四通道、高速 ESD 保护器件

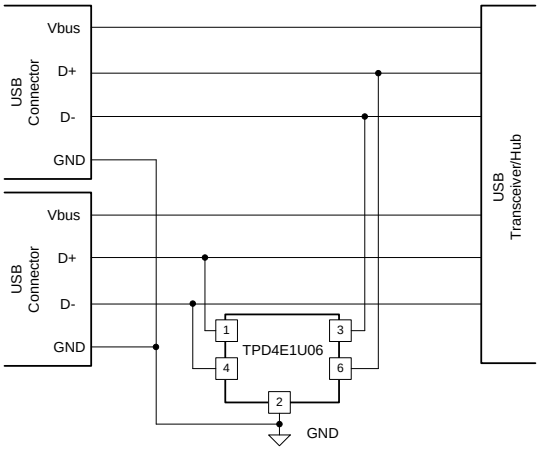
1 特性

- IEC 61000-4-2 4 级 ESD 保护
  - ±15kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 3A (8/20μs)
- IO 电容：0.8pF（典型值）
- 直流击穿电压：6.5V（最小值）
- 超低泄漏电流：10nA（最大值）
- 低 ESD 钳位电压
- 工业温度范围：-40°C 至 +125°C
- 小型、易于布线的 DCK 和 DBV 封装

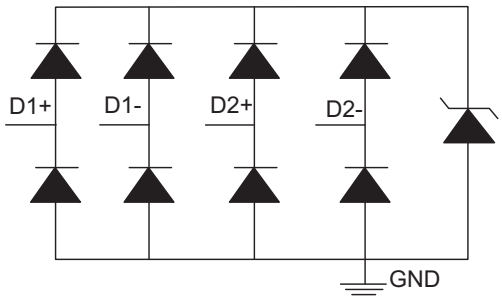
2 应用

- USB 2.0
- 以太网
- 高清多媒体接口 (HDMI) 控制线路
- 移动产业处理器接口 (MIPI) 总线
- 低压差分信令 (LVDS)
- SATA

LP38690 的



电路原理图



3 说明

TPD4E1U06 是一款基于四通道单向瞬态电压抑制器 (TVS) 的静电放电 (ESD) 保护二极管，具有超低电容。该器件的 ESD 冲击消散值高于 IEC 61000-4-2 国际标准规定的最高水平。其 0.8pF 的线路电容使其广泛适用于各类 应用的输出电流传感电阻器和运算放大器而得以实现。典型应用领域包括 HDMI、USB2.0、MHL 和 DisplayPort。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD4E1U06DCK	SC70	2.00mm × 1.25mm
TPD4E1U06DBV	SOT-23	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (October 2014) to Revision D — **Page**

- Updated DCK and DBV Pinout image ... 3
- Added 61000-4-5 spec to *Absolute Maximum Ratings* table ... 4
- Added *IEC 61000-4-5 Surge Protection* section ... 8
- Added *IEC 61000-4-4 EFT Protection* section ... 8

Changes from Revision B (February 2013) to Revision C — **Page**

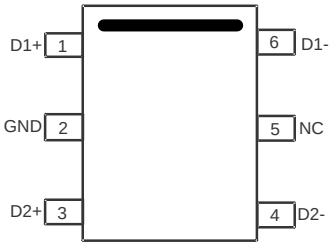
- 已添加 *引脚配置和功能*部分，*处理额定值*表，*特性 说明* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision A (December 2012) to Revision B — **Page**

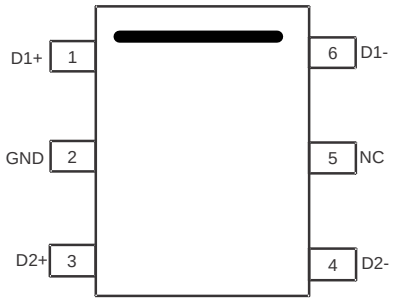
- Added C_{CROSS} data for DBV package ... 5

5 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D1+	1	I/O	ESD protected channel. Connect to data line as close to the connector as possible
D1–	6	I/O	
D2–	4	I/O	
D2+	3	I/O	
GND	2	GND	Ground. Connect to ground
NC	5	I/O	No connect. Can be left floating, grounded, or connected to VCC

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	IEC 61000-4-4 EFT protection (5/50 ns)		80	A
I_{PP}	IEC 61000-4-5 surge protection (8/20 μs) peak pulse current		3	A
P_{PP}	IEC 61000-4-5 surge protection (8/20 μs) peak pulse power		45	W
	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–65	115	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact ESD	±15000	V
		IEC 61000-4-2 air-gap ESD	±15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD4E1U06		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.3	274.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.1	113.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	57.3	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.9	75.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, tp = 8/20 µs, from I/O to GND(1)			11		V
		I_{PP} = 3 A, tp = 8/20 µs, from I/O to GND(1)			15		V
R_{DYN}	Dynamic resistance	Pin x to GND pin(2)			1.0		Ω
		GND to pin x			0.6		
C_L	Line capacitance	f = 1 MHz, V_{BIAS} = 2.5 V, 25°C			0.8	1	pF
C_{CROSS}	Channel to channel input capacitance	Pin 2 = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins	DCK package		0.006	0.015	pF
			DBV package		0.01	0.025	
$\Delta C_{IO-TO-GND}$	Variation of channel input capacitance	Pin 2 = 0 V , f = 1 MHz, V_{BIAS} = 2.5 V, channel_x pin to ground – channel_y pin to ground			0.025	0.07	pF
V_{BR}	Break-down voltage, IO to GND	I_{IO} = 1 mA		6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			1	10	nA

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A.

6.7 Typical Characteristics

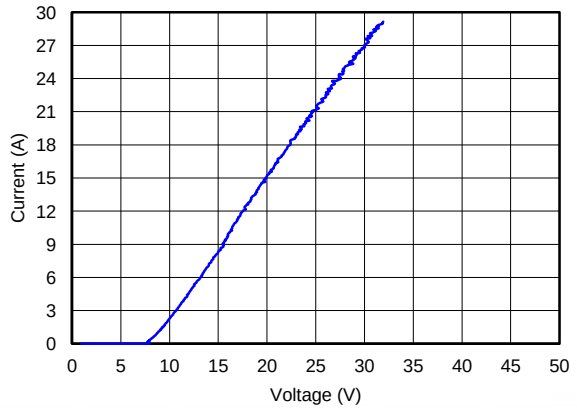


Figure 1. TLP, Data to GND

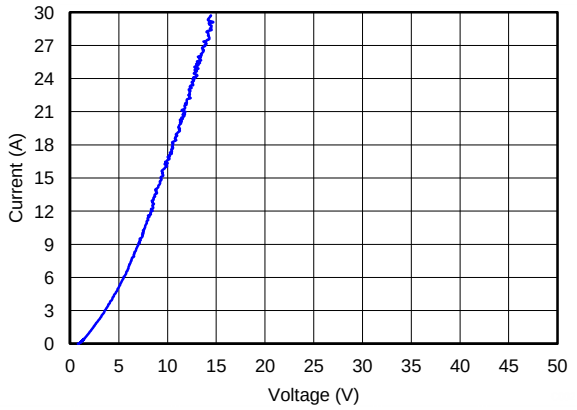


Figure 2. TLP, GND to Data

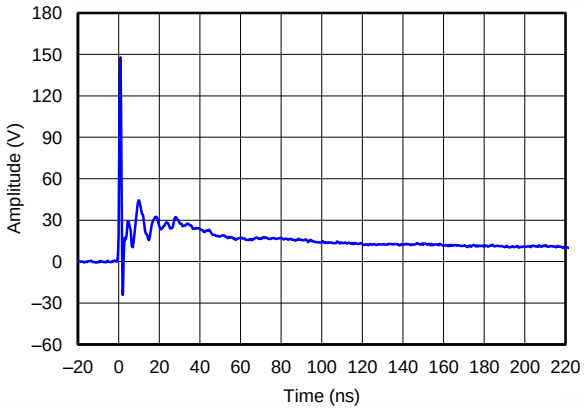


Figure 3. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

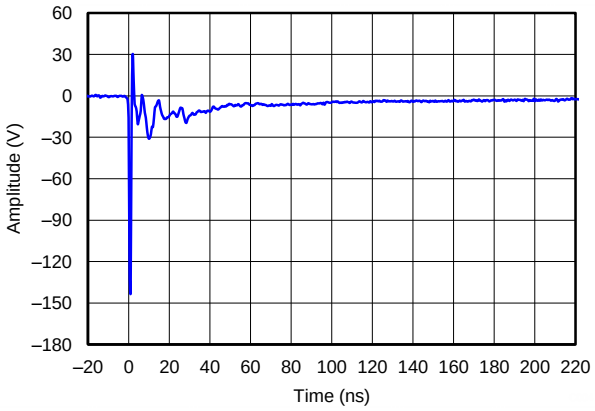


Figure 4. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

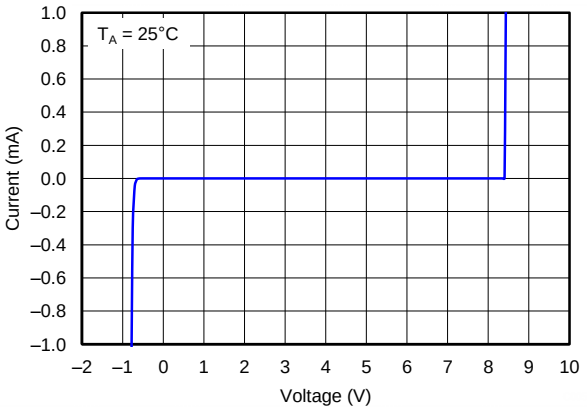


Figure 5. Diode Curve

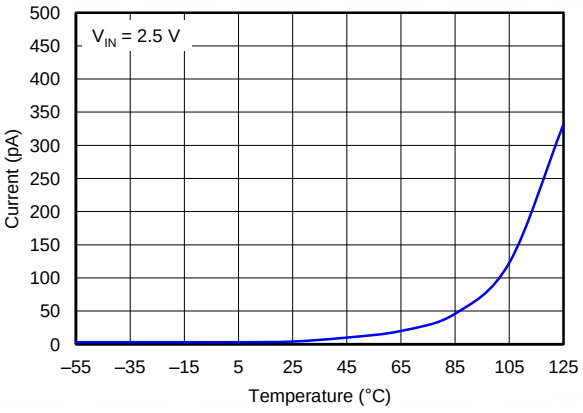


Figure 6. I_{LEAK} vs Temperature

Typical Characteristics (continued)

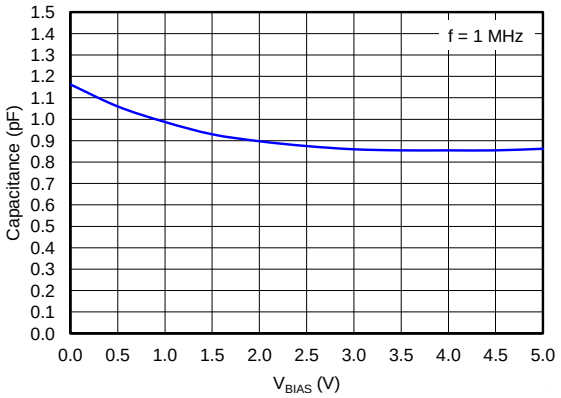


Figure 7. Capacitance Across V_{BIAS}

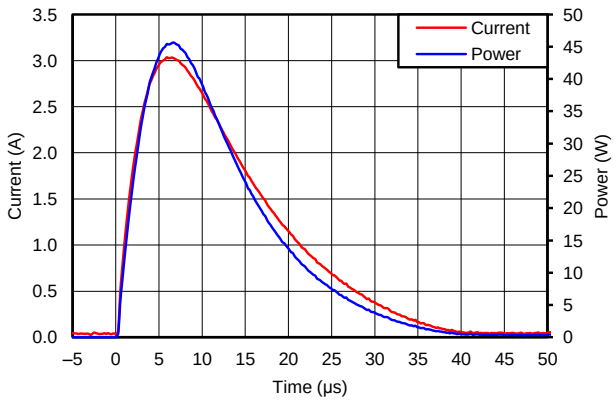


Figure 8. Surge Curve (tp = 8/20 µs), Pin IO to GND

7 Detailed Description

7.1 Overview

The TPD4E1U06 is a quad channel unidirectional TVS ESD protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort. Its 0.8-pF line capacitance makes it suitable for a wide range of applications.

7.2 Functional Block Diagram

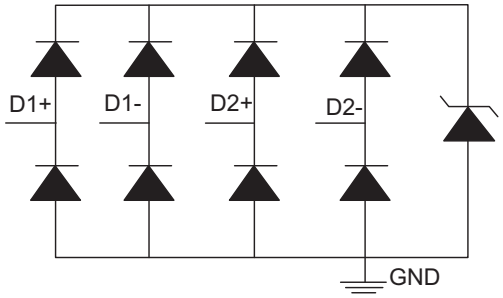


Figure 9. Circuit Schematic Diagram

7.3 Feature Description

7.3.1 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and air. An ESD/surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3 A and 45 W (8/20-μs waveform). An ESD-surge clamp diverts this current to ground.

7.3.3 IEC 61000-4-4 EFT Protection

The IO pins can withstand an electrical fast transient burst of up to 80 A (5/50-ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.8 pF.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 11 V (I_{PP} = 1 A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

Feature Description (continued)

7.3.9 Small, Easy-to-Route Packages

The layout of this device makes it simple to add protection to the design. Industry standard packages allow for easy additions to the board and easy layout.

7.4 Device Functional Modes

The TPD4E1U06 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the forward diode drop. During ESD events, voltages as high as ±15 kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1U06 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E1U06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

For this design example, one TPD4E1U06 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.

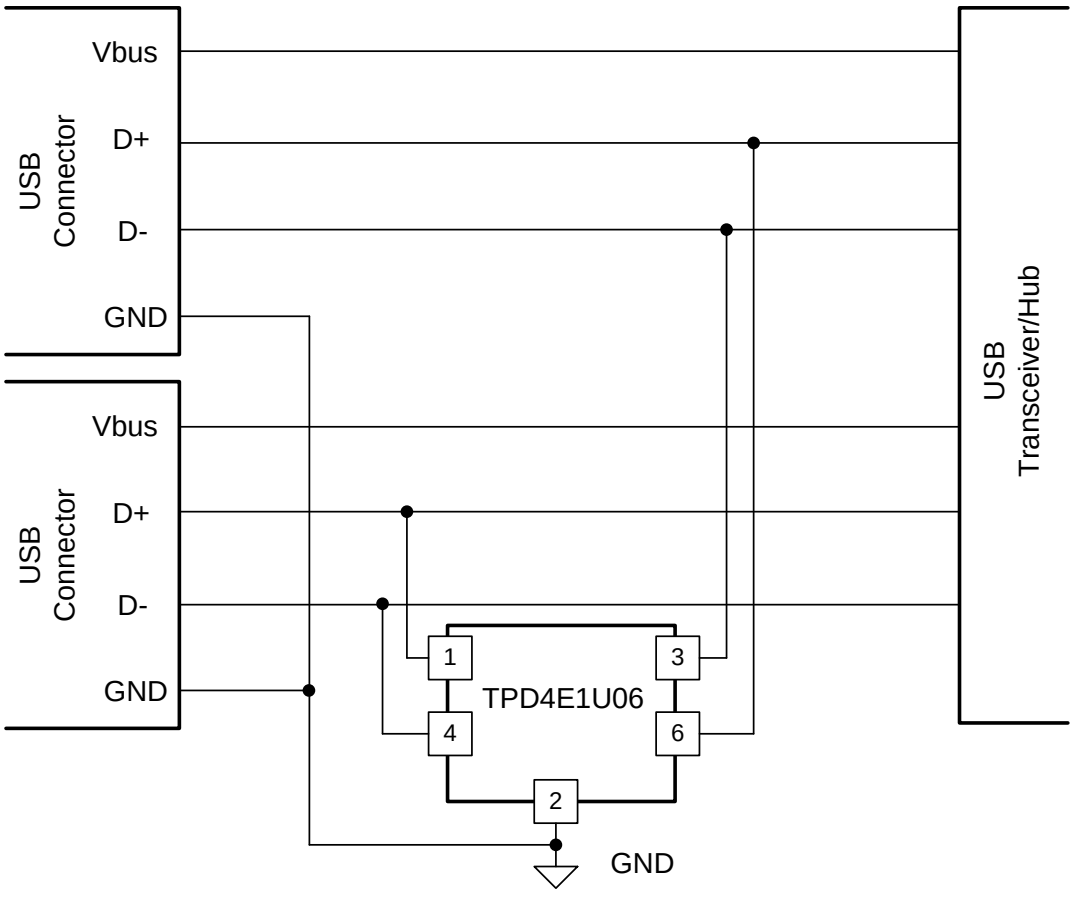


Figure 10. Dual USB 2.0 Application

Typical Application (continued)

8.2.1 Design Requirements

Given the USB 2.0 application, the parameters in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 3, 4, or 6	0 V to 5 V
Operating frequency	240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range on Pins 1, 3, 4, or 6

The TPD4E1U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O supports a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E1U06 has a capacitance of 0.8 pF (typical), supporting USB 2.0 data rates.

8.2.3 Application Curve

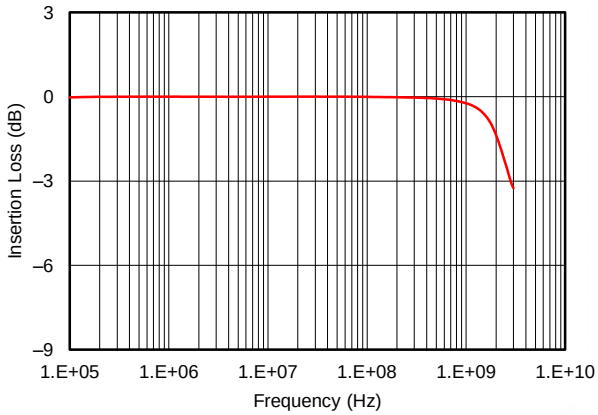


Figure 11. Insertion Loss Graph

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

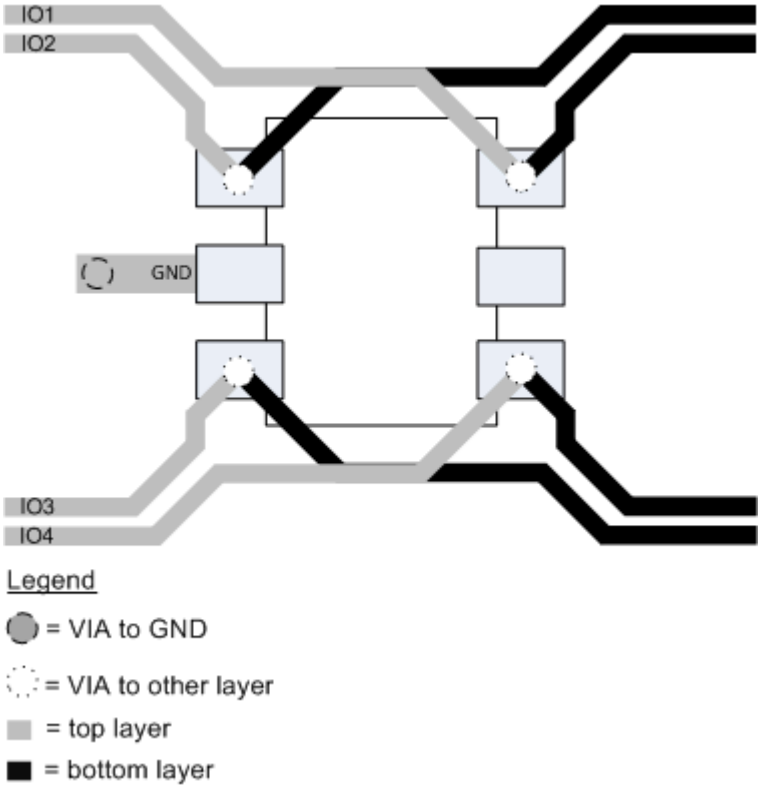


Figure 12. PCB Layout Recommendation

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *阅读和理解 ESD 保护数据表*
- *《ESD 布局指南》*
- *TTPD4E1U06DCK EVM 用户指南*
- *TPD4E1U06DBV EVM 用户指南*

11.2 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹。单击右上角的*"提醒我" (Alert me)* 按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查看任意已修订文档的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E1U06DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(NG4, NG4P)	Samples
TPD4E1U06DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BP6, BP8, BPI) (BPP, BPP, BPS)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

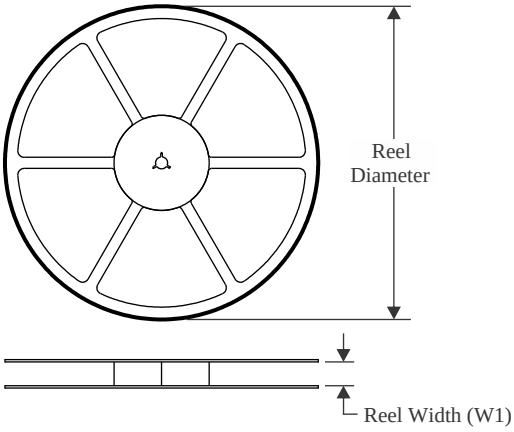
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

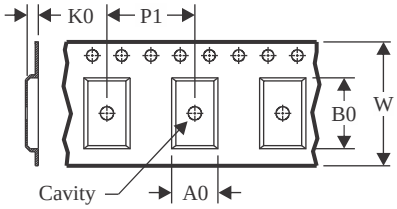
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

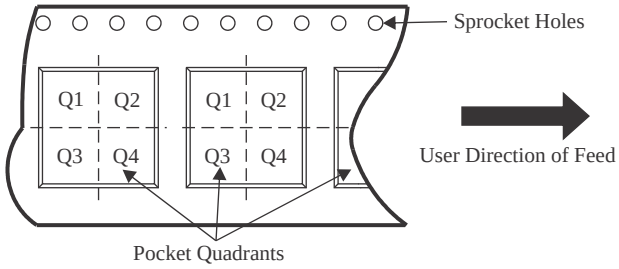


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

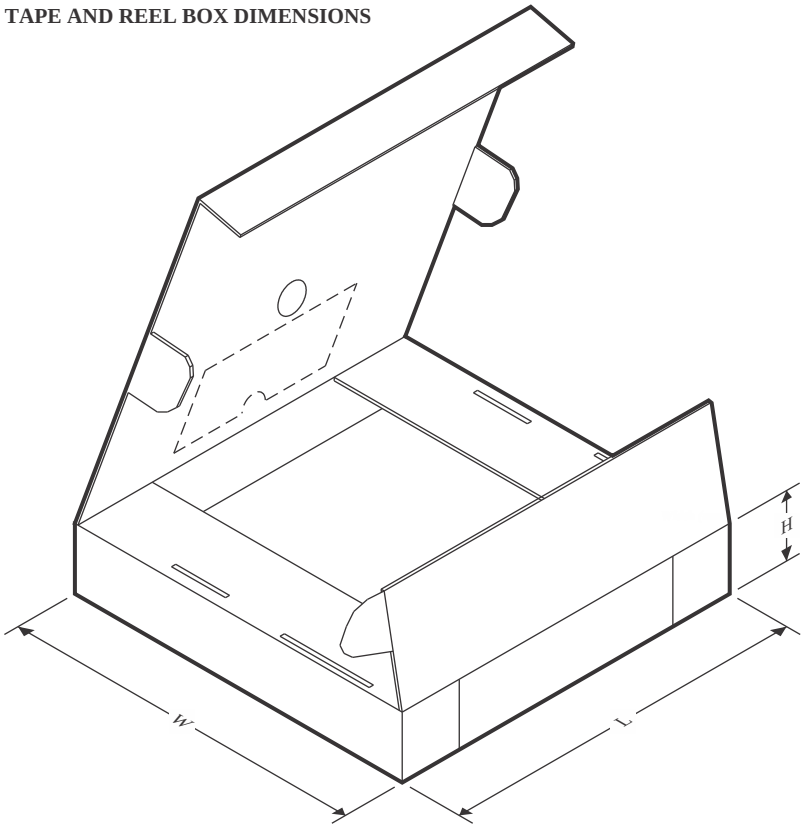
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E1U06DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPD4E1U06DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPD4E1U06DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

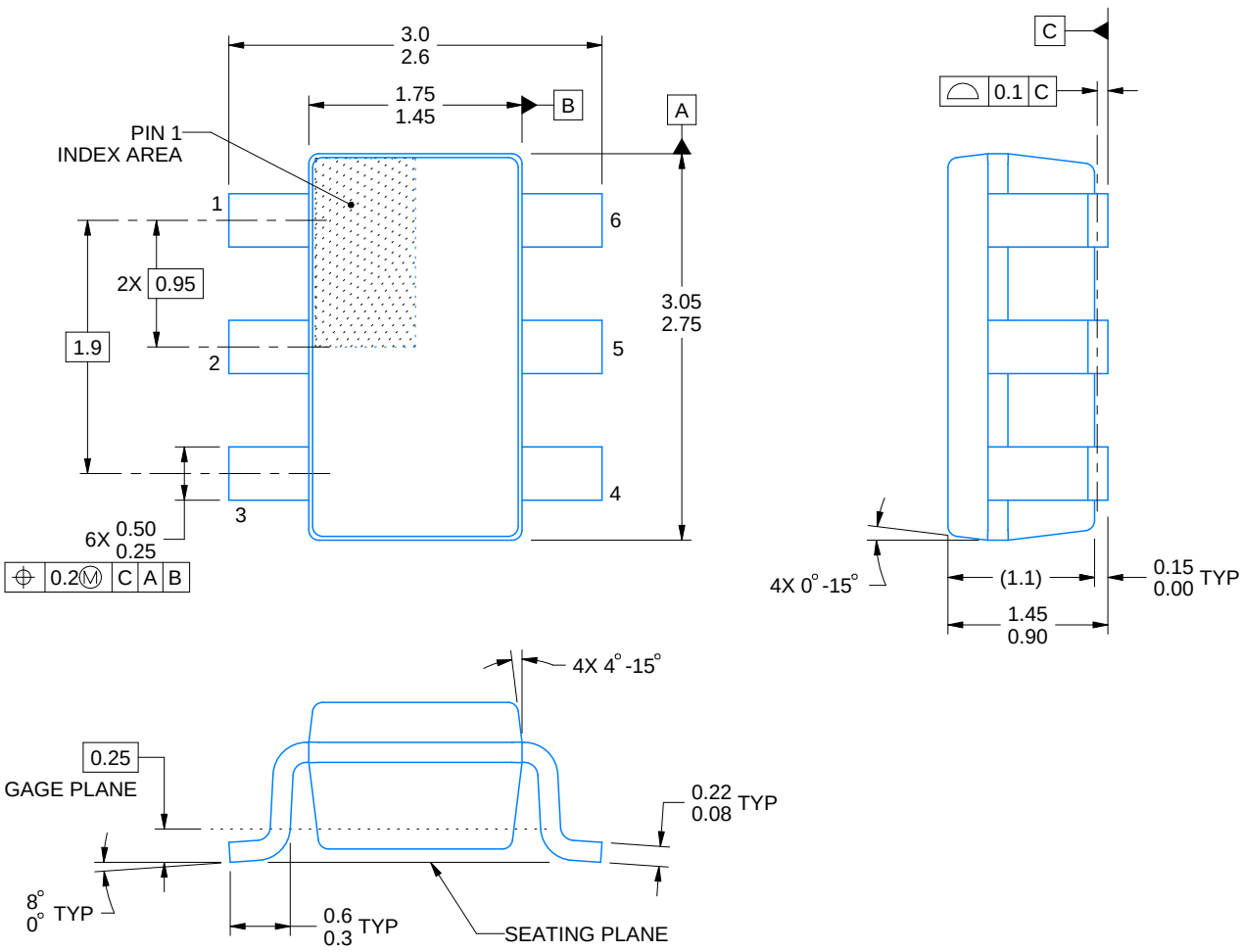
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E1U06DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPD4E1U06DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPD4E1U06DCKR	SC70	DCK	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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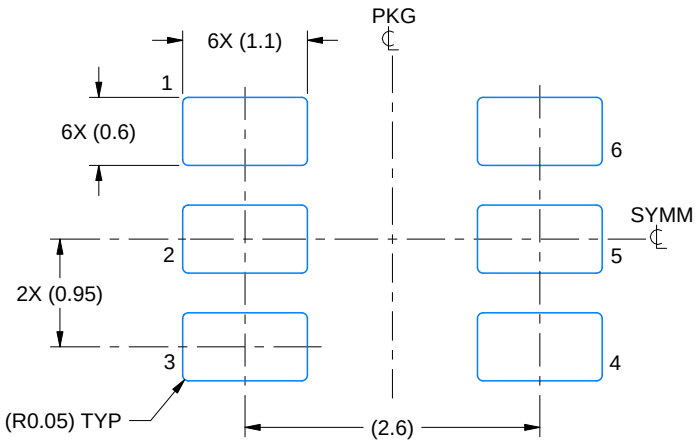
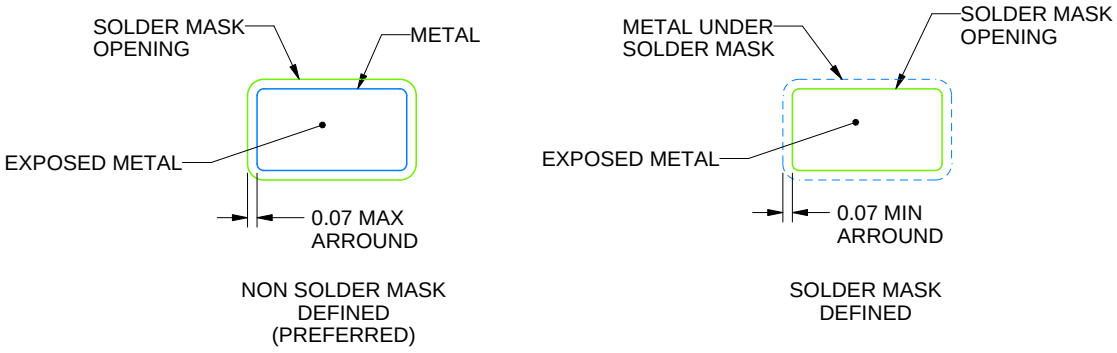
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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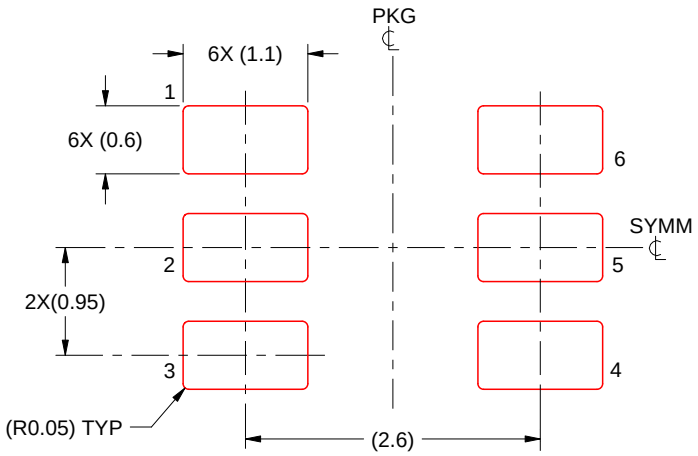
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

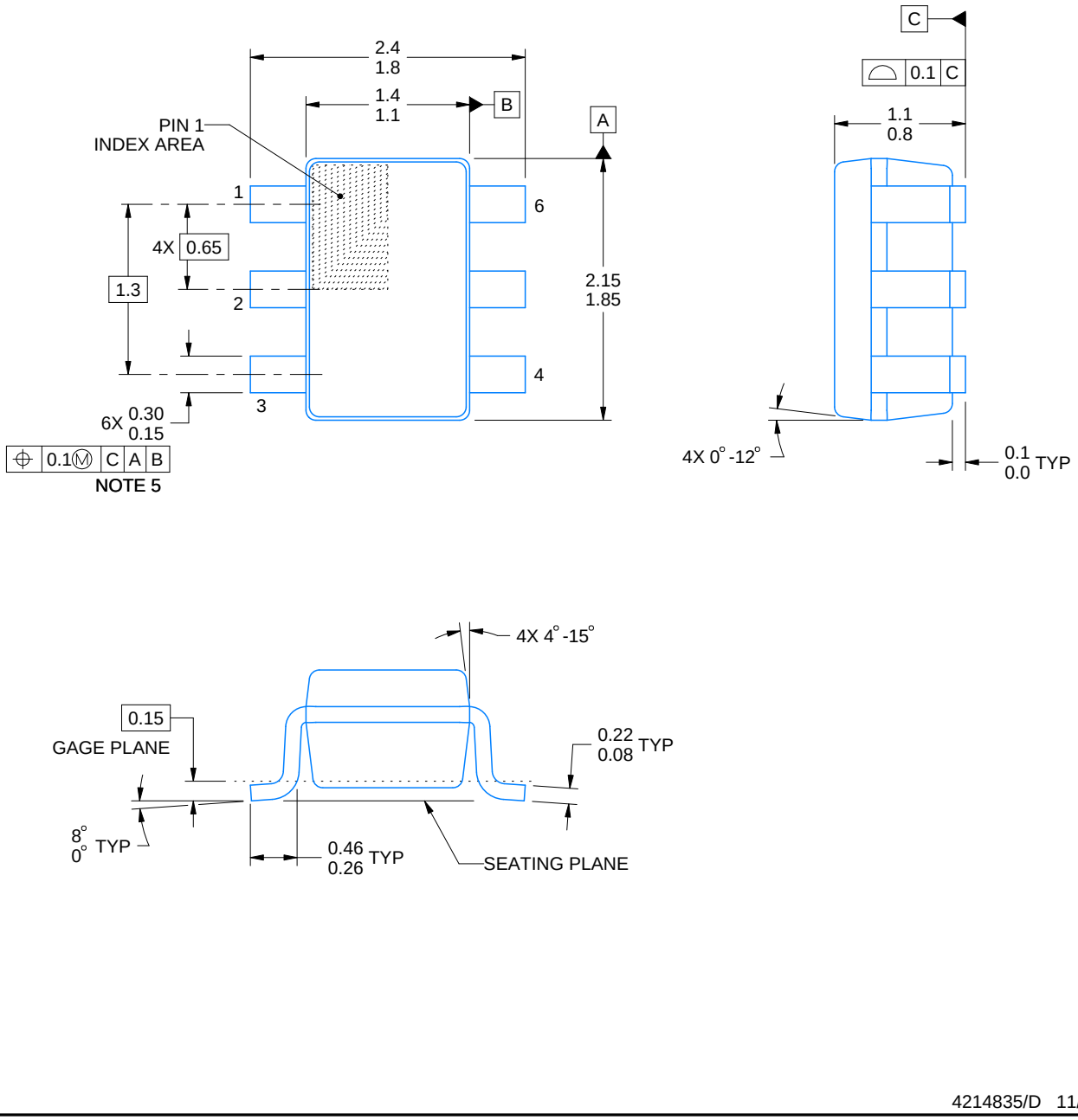
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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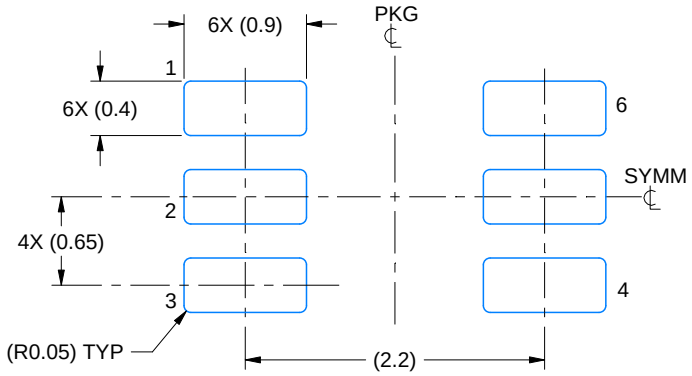
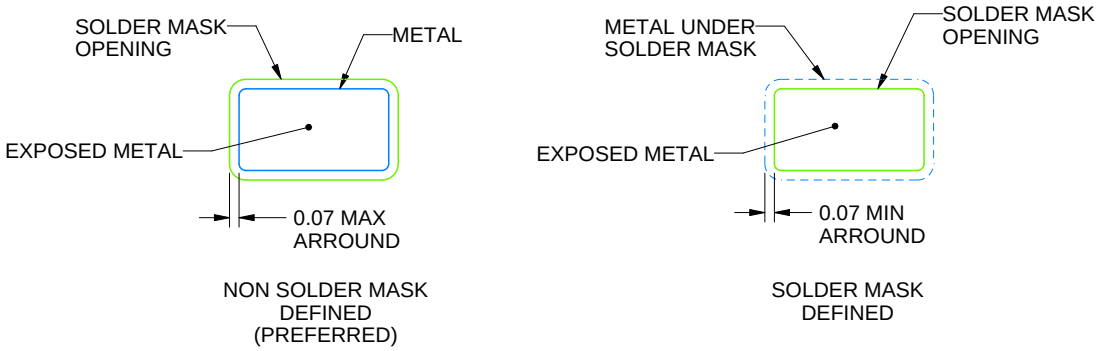
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

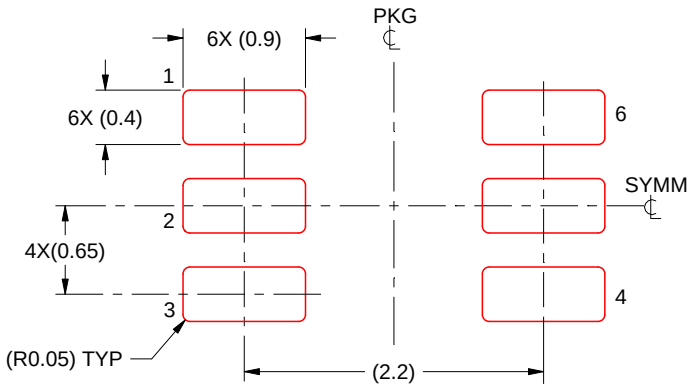


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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