

## TPD6E004 适用于高速数据接口的 低电容、6 通道、±15kV ESD 保护阵列

### 1 特性

- ESD 保护性能超过 JESD 规范要求：
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC 61000-4-2 接触放电
  - ±12kV IEC 61000-4-2 空气间隙放电
- 1.6pF 低 I/O 电容
- 电源电压范围为 0.9V 至 5.5V
- 6 通道器件
- 节省空间的 UQFN (RSE) 封装

### 2 应用

- USB
- 以太网™
- FireWire™
- 视频
- 手机
- SVGA 视频连接
- 血糖仪

### 3 说明

TPD6E004 器件是一款低电容、±15kV ESD 保护二极管阵列，设计用于保护连接到通信线路的敏感电子元件。每个通道包含一对二极管，用于将 ESD 电流脉冲引导至 V<sub>CC</sub> 或 GND。TPD6E004 可针对高达 ±15kV 的人体放电模型 (HBM) ESD 脉冲、±8kV 接触 ESD 和 ±12kV 空气间隙 ESD (如 IEC 61000-4-2 中所规定) 提供保护。该器件每通道具有 1.6pF 的电容典型值，因此非常适用于高速数据 I/O 接口。

TPD6E004 器件采用 RSE 封装，额定工作温度范围为 -40°C 至 +85°C。

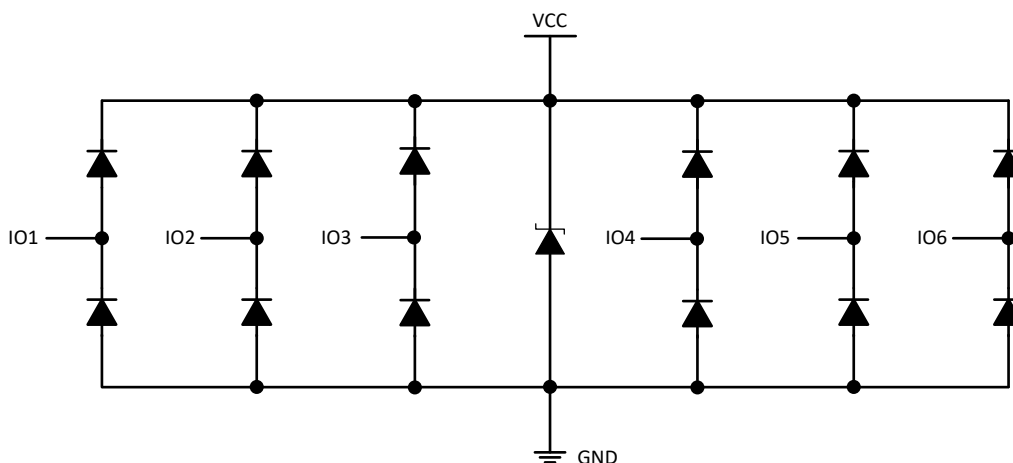
TPD6E004 器件采用 6 通道 ESD 结构，专为 USB、以太网和 FireWire 应用而设计。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
TPD6E004	RSE (UQFN, 8)	1.5mm x 1.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。



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功能方框图



## Table of Contents

<b>1 特性</b> .....	1	7.3 Feature Description.....	6
<b>2 应用</b> .....	1	7.4 Device Functional Modes.....	6
<b>3 说明</b> .....	1	<b>8 Application and Implementation</b> .....	7
<b>4 Revision History</b> .....	2	8.1 Application Information.....	7
<b>5 Pin Configuration and Functions</b> .....	3	8.2 Typical Application.....	7
<b>6 Specifications</b> .....	4	8.3 Power Supply Recommendations.....	9
6.1 Absolute Maximum Ratings <sup>(1)</sup> .....	4	8.4 Layout.....	9
6.2 ESD Ratings.....	4	<b>9 Device and Documentation Support</b> .....	11
6.3 ESD Ratings - Surge Protection.....	4	9.1 Documentation Support.....	11
6.4 Recommended Operating Conditions.....	4	9.2 支持资源.....	11
6.5 Thermal Information.....	4	9.3 Trademarks.....	11
6.6 Electrical Characteristics.....	5	9.4 静电放电警告.....	11
6.7 Typical Characteristics.....	5	9.5 术语表.....	11
<b>7 Detailed Description</b> .....	6	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	11
7.1 Overview.....	6		
7.2 Functional Block Diagram.....	6		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision B (February 2016) to Revision C (July 2023) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式..... 1
- 更新了封装信息表以包含封装引线尺寸..... 1

### Changes from Revision A (February 2008) to Revision B (February 2016) Page

- 添加了器件信息表、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。..... 1

## 5 Pin Configuration and Functions

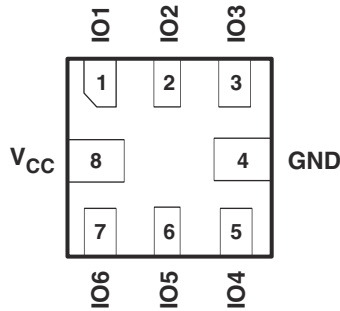


图 5-1. RSE Package, 8-Pin UQFN (Bottom View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO1	1	I/O	ESD-protected channel
IO2	2	I/O	ESD-protected channel
IO3	3	I/O	ESD-protected channel
GND	4	GND	Ground
IO4	5	I/O	ESD-protected channel
IO5	6	I/O	ESD-protected channel
IO6	7	I/O	ESD-protected channel
V <sub>CC</sub>	8	PWR	Power-supply input. Bypass V <sub>CC</sub> to GND with a 0.1- μ F ceramic capacitor.

(1) I = input, O = output, GND = ground, PWR = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Operating voltage for pin VCC	- 0.3	5.5	V
V <sub>I/O</sub>	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6	- 0.3	V <sub>CC</sub> + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)	220	°C
		Vapor phase (60 s)	215	
	Lead temperature (soldering, 10 s)		300	°C
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±15000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - Surge Protection

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000 V
		IEC 61000-4-2 air-gap discharge	

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C
V <sub>CC</sub>	Operating voltage for pin VCC	0.9	5.5	V
V <sub>I/O</sub>	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6	0	Minimum of: (5.8, V <sub>CC</sub> )	V

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD6E004	UNIT
		RSE (UQFN)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	138.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	74.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	43.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.6 Electrical Characteristics

$V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{CC}$ Supply voltage		0.9		5.5	V
$I_{CC}$ Supply current				500	nA
$V_F$ Diode forward voltage	$I_F = 1\text{ mA}$		0.8		V
$I_l$ Channel leakage current			$\pm 1$		nA
$V_{BR}$ Break-down voltage	$I_l = 10\ \mu\text{A}$	6		8	V
$C_{I/O}$ Channel input capacitance	$V_{CC} = 5\text{ V}$ , bias of $V_{CC}/2$ , $f = 10\text{ MHz}$		1.6	2	pF

(1) Typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

### 6.7 Typical Characteristics

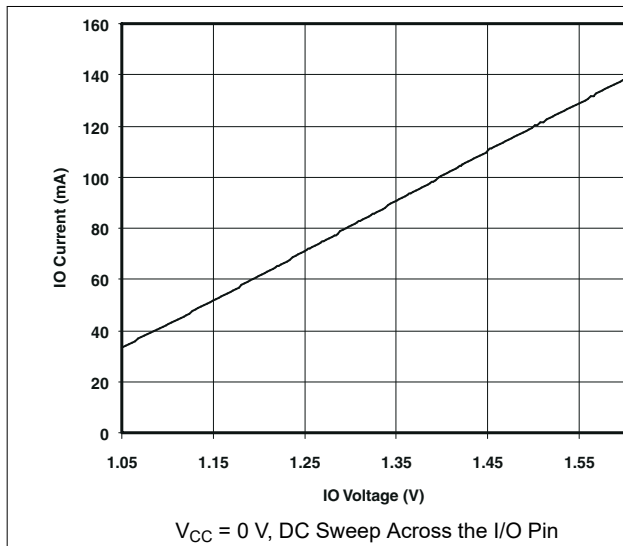


图 6-1. Forward Diode Voltage (Upper Clamp Diode)

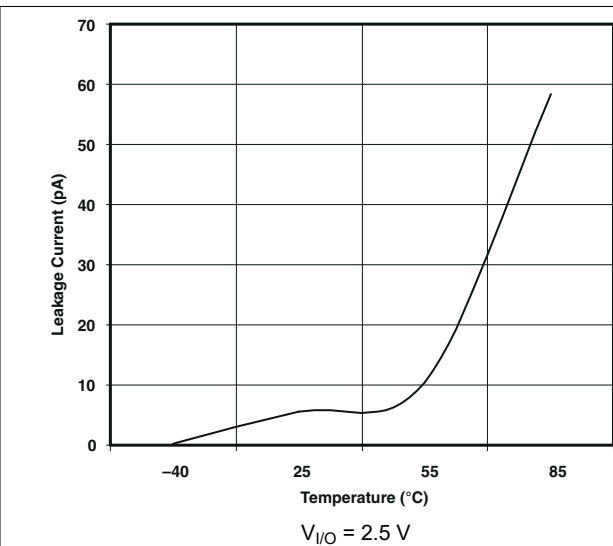


图 6-2. Leakage Current vs Temperature

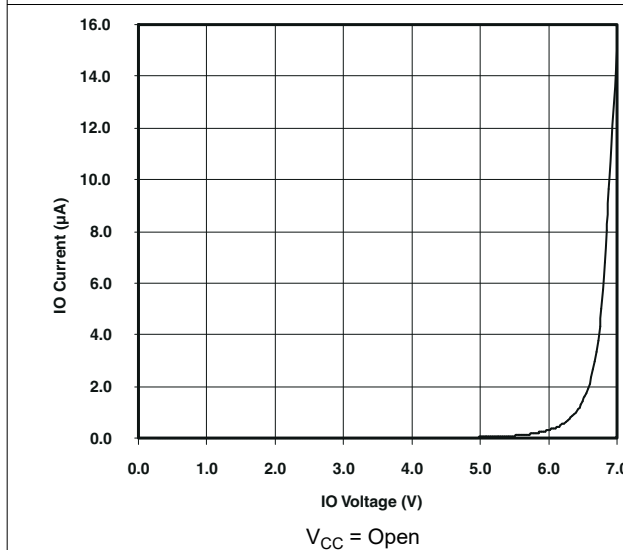


图 6-3. Reverse Diode Curve Current I/O to GND

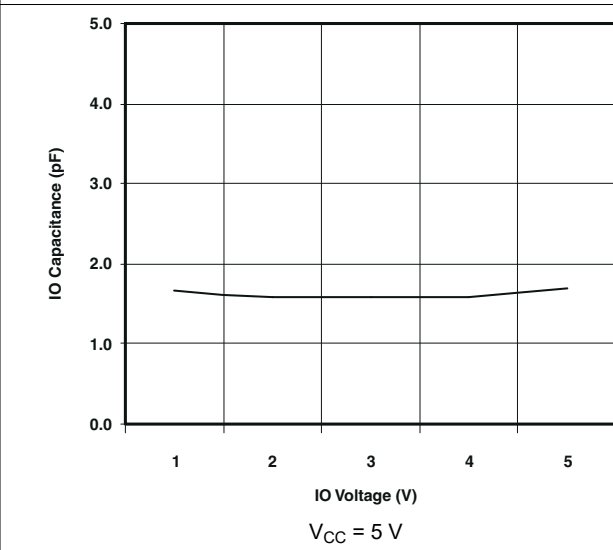


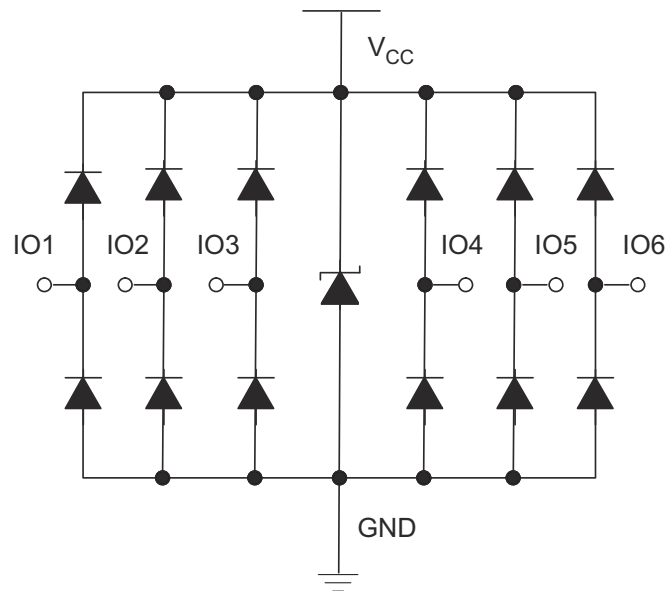
图 6-4. I/O Capacitance vs Input Voltage

## 7 Detailed Description

### 7.1 Overview

The TPD6E004 device is a six-channel TVS protection diode array. The TPD6E004 is rated to dissipate ESD strikes of  $\pm 8$ -kV contact and  $\pm 12$ -kV air-gap, as specified in the IEC 61000-4-2 international standard. This device has 1.6-pF capacitance per I/O channel, making it an excellent choice for use in high-speed data I/O interfaces.

### 7.2 Functional Block Diagram



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图 7-1. Logic Block Diagram

### 7.3 Feature Description

The TPD6E004 is a TVS that provides ESD protection for up to six channels, withstanding up to  $\pm 8$ -kV contact and  $\pm 12$ -kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any I/O pin of the TPD6E004. The small footprint is an excellent choice for applications where space-saving designs are important.

### 7.4 Device Functional Modes

The TPD6E004 device is a passive integrated circuit that triggers when voltages are above  $V_{BR}$  or below the diodes  $V_F$  of approximately  $-0.8$  V. During ESD events, voltages as high as  $\pm 8$ -kV contact and  $\pm 12$ -kV air-gap ESD can be directed to ground through the internal diodes. When the voltages on the protected line fall below the trigger levels of TPD6E004 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.

## 8 Application and Implementation

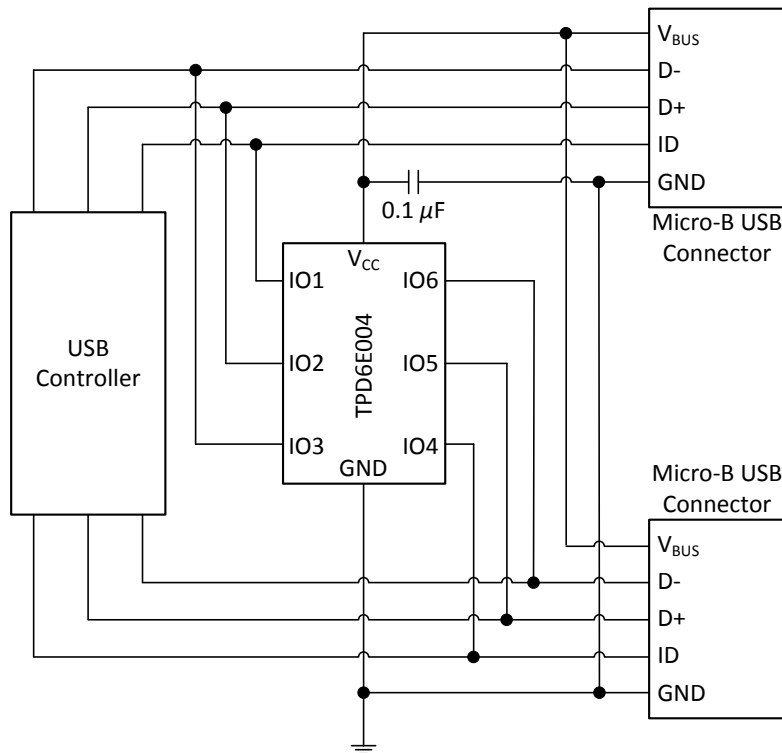
### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The TPD6E004 device is a TVS diode array typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected integrated circuit (IC). The triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level for the protected IC.

### 8.2 Typical Application



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图 8-1. Two-Port Micro-B USB 2.0 Application

### 8.2.1 Design Requirements

For this design example, a single TPD6E004 is used to protect all the pins of two USB 2.0 Micro-B connectors. 表 8-1 lists the design parameters for the USB application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, IO4, IO5 and IO6	0 V to 3.6 V
Signal voltage range on V <sub>CC</sub>	0 V to 5.5 V
Operating Frequency	240 MHz

### 8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD6E004 ESD solution offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. The TPD6E004 is designed to protect the core circuitry and allow the system to function properly in the event of an ESD strike. For proper operation, the [Layout Guidelines](#) and following design guidelines must be followed:

1. Place the TPD6E004 solution close to the connectors. This allows the TPD6E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1- $\mu$ F capacitor very close to the V<sub>CC</sub> pin. This limits any momentary voltage surge at the I/O pin during the ESD strike event.
3. Ensure that there is enough metallization for the V<sub>CC</sub> and GND loop. During normal operation, the TPD6E004 consumes only  $\mu$ A of leakage current, but during an ESD event, V<sub>CC</sub> and GND may see 15-A to 30-A of current, depending on the ESD level. A sufficient current path enables the safe discharge of all the energy associated with the ESD strike.
4. Leave any unused I/O pins floating. In this example of protecting two Micro-B USB ports, none of the I/O pins are left unused.
5. The V<sub>CC</sub> pin can be connected in two different ways:
  - a. If the V<sub>CC</sub> pin is connected to the system power supply, then the TPD6E004 works as a transient suppressor for any signal swing above V<sub>CC</sub> + V<sub>F</sub>. TI recommends a 0.1- $\mu$ F capacitor on the device V<sub>CC</sub> pin for ESD bypass.
  - b. If the V<sub>CC</sub> pin is not connected to the system power supply, then the TPD6E004 can tolerate a higher signal swing in the range of up to 5.8 V.

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备注

A 0.1- $\mu$ F capacitor is still recommended at the V<sub>CC</sub> pin for ESD bypass.

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### 8.2.3 Application Curve

图 8-2 is a capture of the voltage clamping waveform of the TPD6E004 during a +8-kV contact IEC 61000-4-2 ESD strike.



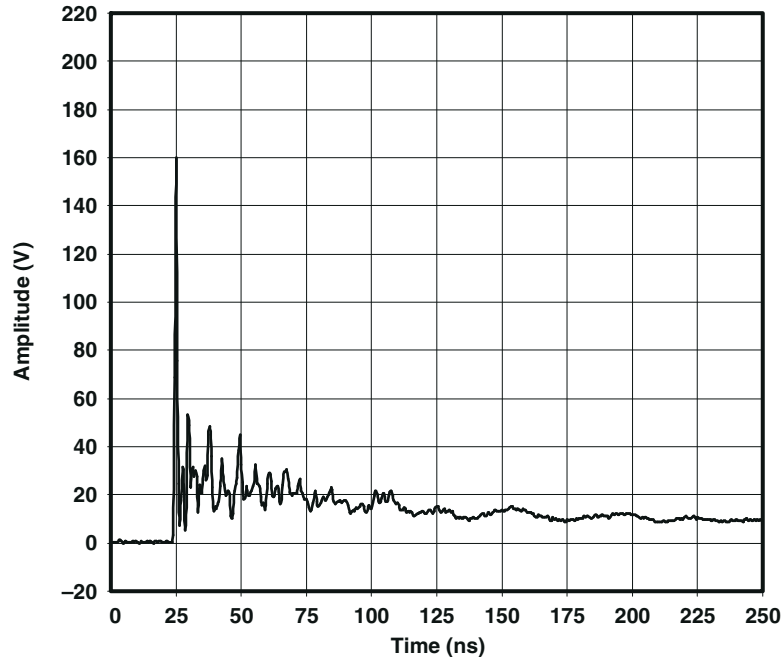


图 8-2. IEC 61000-4-2 +8-kV Contact ESD Clamping Waveform

### 8.3 Power Supply Recommendations

The TPD6E004 device is a passive ESD protection device, so there is no need to power it. Do not violate the maximum voltage specifications for each pin.







### 8.4 Layout

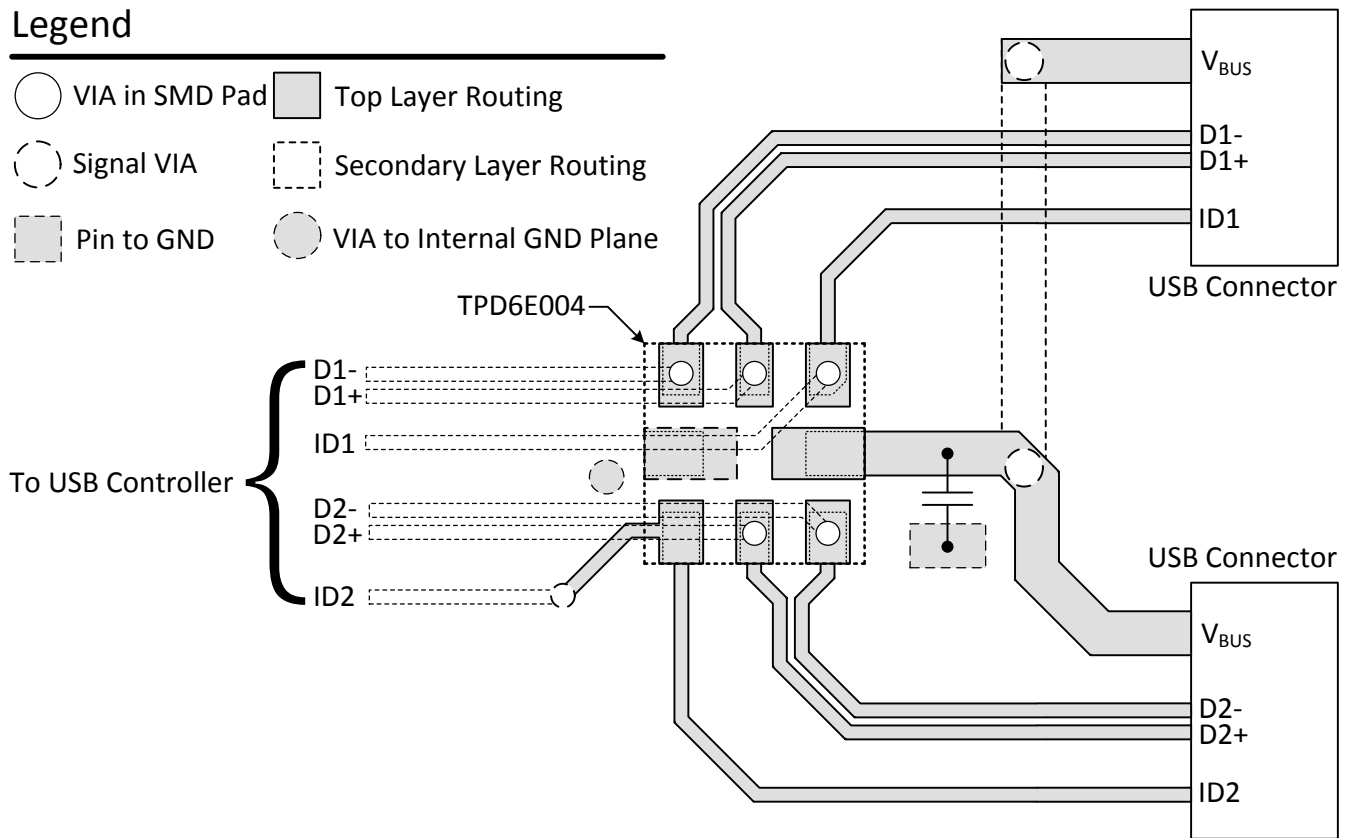
#### 8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any corners less than 135° on the protected traces between the TVS and the connector. Best practice is using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Connect the ground pin to a same layer ground pour which is connected to an internal ground plane with a via. Place the via very near the ground pin.

### 8.4.2 Layout Example

#### Legend

-  VIA in SMD Pad
-  Signal VIA
-  Pin to GND
-  Top Layer Routing
-  Secondary Layer Routing
-  VIA to Internal GND Plane



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图 8-3. TPD6E004 Layout Example for Two USB 2.0 Micro-B Connectors

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Reading and Understanding an ESD Protection Data Sheet](#)
- Texas Instrument, [ESD Protection Layout Guide](#)

### 9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 9.3 Trademarks

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FireWire™ is a trademark of Apple Inc.

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### 9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD6E004RSER	ACTIVE	UQFN	RSE	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

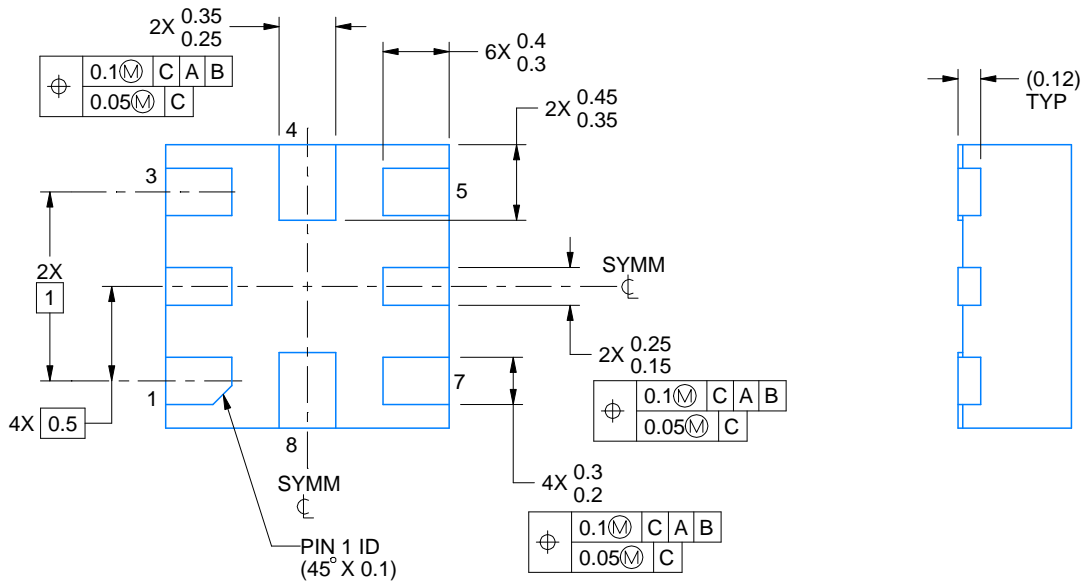
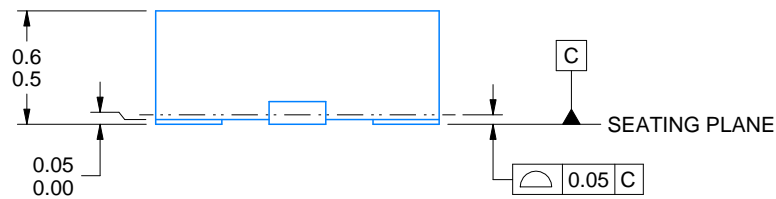
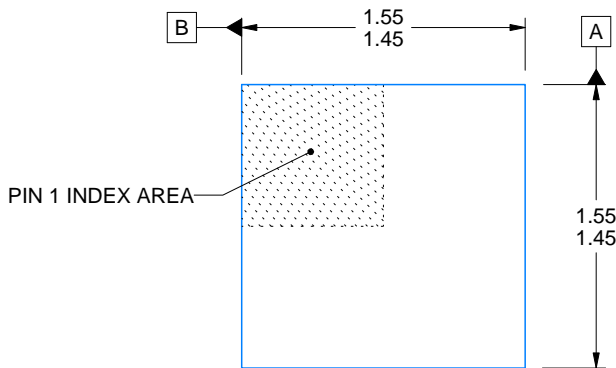
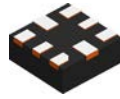

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6E004RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6E004RSER	UQFN	RSE	8	3000	184.0	184.0	19.0



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NOTES:

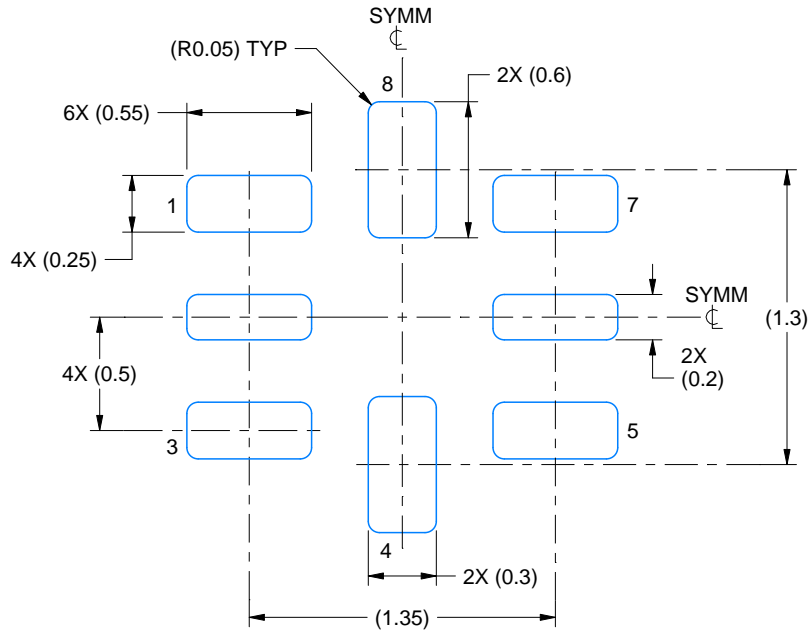
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

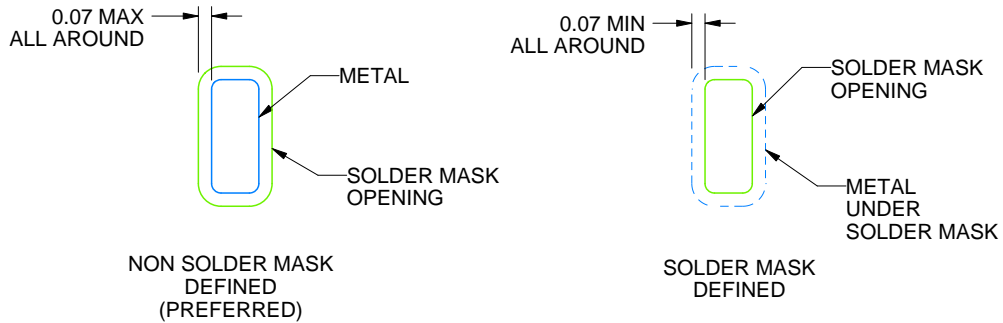
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

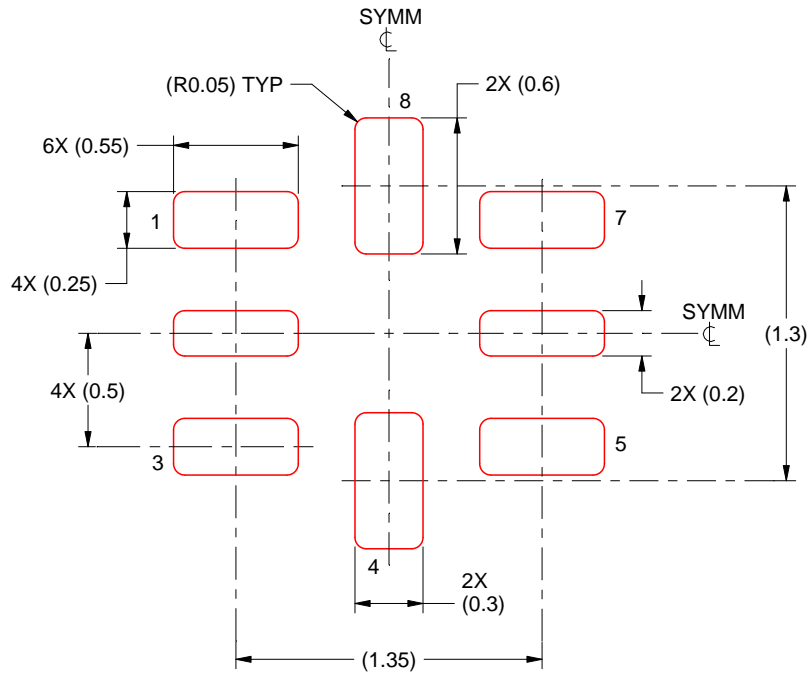


# EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICKNESS  
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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