

TPS22994 具有通用输入输出 (GPIO) 和 I²C 控制功能的四通道负载开关

1 特性

- 输入电压：1.0V 至 3.6V
- 低导通状态电阻 ($V_{BIAS} = 7.2V$)
 - $V_{IN} = 3.3V$ 时, $R_{ON} = 41m\Omega$
 - $V_{IN} = 1.8V$ 时, $R_{ON} = 41m\Omega$
 - $V_{IN} = 1.5V$ 时, $R_{ON} = 41m\Omega$
 - $V_{IN} = 1.0V$ 时, $R_{ON} = 41m\Omega$
- V_{BIAS} 电压范围：2.7V 至 17.2V
 - 适合于 1S/2S/3S/4S 锂离子电池拓扑结构
- 每通道持续电流最大为 1A
- 静态电流
 - 单通道 $< 12\mu A$
 - 全部四通道 $< 22\mu A$
- 关断电流（全部四通道） $< 7\mu A$
- 四个 1.2V 兼容 GPIO 控制输入
- I²C 配置（每通道）
 - 开/关控制
 - 可编程转换率控制（5 个选项）
 - 可编程接通延迟（4 个选项）
 - 可编程输出放电（4 个选项）
- I²C SwitchALL™ 用于多通道/多芯片控制的命令
- 四方扁平无引线 (QFN)-20 封装，3mm x 3mm，高度 0.75mm

2 应用

- 超薄个人电脑
- 笔记本电脑
- 平板电脑
- 服务器
- 一体机

3 说明

TPS22994 是一款多通道、低 R_{ON} 负载开关，此开关具有用户可编程特性。此器件包括四个 N 通道属氧化物半导体场效应晶体管 (MOSFET)，能够在 1.0V 至 3.6V 输入电压范围内运行。由于开关可通过 I²C 控制，因此非常适用于 GPIO 有限的处理器。

TPS22994 器件的上升时间受到内部控制以避免浪涌电流。TPS22994 具有五个可编程转换率选项、四个接通延迟选项和四个快速输出放电 (QOD) 电阻选项。

此器件的通道可由 GPIO 或 I²C 控制。缺省运行模式为通过 ONx 端子的 GPIO 控制。I²C 从地址端子可接至高电平或低电平，以分配 7 个唯一的器件地址。

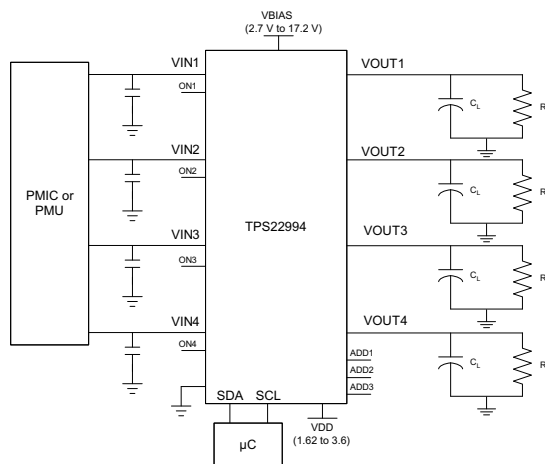
TPS22994 采用节省空间的 RUK 封装（焊球间距 0.4mm），并可在 -40°C 至 85°C 的自然通风温度范围内运行。

器件信息⁽¹⁾

部件号	封装	封装尺寸（标称值）
TPS22994	WQFN (20)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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5 修订历史记录

Changes from Revision A (September 2014) to Revision B	Page
• Updated MAX limits in the Electrical Characteristics table.	6
• Updated Detailed Design Procedure for Parallel Channels Application.	30

Changes from Original (August 2014) to Revision A	Page
• 初始发布的完整版数据表	1

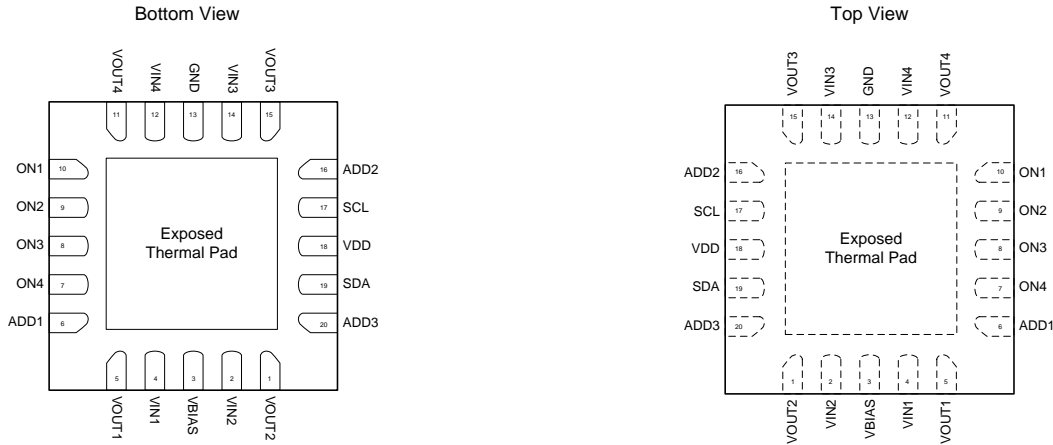
6 Device Comparison Table

TPS22994	
R_{ON} TYPICAL AT 3.3 V (V_{BIAS} = 7.2 V)	41 mΩ
RISE TIME ⁽¹⁾	Programmable
ON DELAY ⁽¹⁾	Programmable
QUICK OUTPUT DISCHARGE ^{(1) (2)}	Programmable
MAXIMUM OUTPUT CURRENT (per channel)	1 A
GPIO ENABLE	Active High
OPERATING TEMP	–40°C to 85°C

(1) See [Application Information](#) section.

(2) This feature discharges output of the switch to GND through an internal resistor, preventing the output from floating. See Application information section.

7 Pin Configuration and Functions



Pin Functions

Pin		I/O	DESCRIPTION
NO.	NAME		
Exposed Thermal Pad		-	Exposed thermal pad for thermal relief. Tie to GND.
1	VOUT2	O	Channel 2 output.
2	VIN2	I	Channel 2 input.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.7 V to 17.2 V. See the Applications and Implementation section.
4	VIN1	I	Channel 1 input.
5	VOUT1	O	Channel 1 output.
6	ADD1	I	Device address pin. Tie high or low. Do not leave floating. See the Applications and Implementation section.
7	ON4	I	Active high channel 4 control input. Do not leave floating.
8	ON3	I	Active high channel 3 control input. Do not leave floating.
9	ON2	I	Active high channel 2 control input. Do not leave floating.
10	ON1	I	Active high channel 1 control input. Do not leave floating.
11	VOUT4	O	Channel 4 output.
12	VIN4	I	Channel 4 input.
13	GND	-	Device ground.
14	VIN3	I	Channel 3 input.
15	VOUT3	O	Channel 3 output.
16	ADD2	I	Device address pin. Tie high or low. See the Applications and Implementation section.
17	SCL	I	Serial clock input.
18	VDD	I	I ² C device supply input. Tie this pin to the I ² C SCL/SDA pull-up voltage. See the Applications and Implementation section.
19	SDA	I/O	Serial data input/output.
20	ADD3	I	Device address pin. Tie high or low. See the Applications and Implementation section.

8 Specifications

8.1 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{INx}	Input voltage for VIN1, VIN2, VIN3, VIN4	For V _{BIAS} < 4.6 V	1.0	(V _{BIAS} – 1 V)
		For V _{BIAS} ≥ 4.6 V	1.0	3.6
V _{BIAS}	Supply voltage for VBIAS	2.7	17.2	V
V _{DD}	Supply voltage for VDD	1.62	3.6	V
V _{ADDx}	Input voltage for ADD1, ADD2, ADD3	0	V _{DD}	V
V _{ONx}	Input voltage for ON1, ON2, ON3, ON4	0	5	V
V _{OUTx}	Output voltage for VOUT1, VOUT2, VOUT3, VOUT4	0	V _{INx}	V
C _{INx}	Input capacitor on VIN1, VIN2, VIN3, VIN4	1 ⁽¹⁾		μF

(1) Refer to application section.

8.2 Absolute Maximum Ratings⁽¹⁾

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT ⁽²⁾
		MIN	MAX	
V _{INx}	Input voltage for VIN1, VIN2, VIN3, VIN4	–0.3	4	V
V _{BIAS}	Supply voltage for VBIAS	–0.3	20	V
V _{OUTx}	Output voltage for VOUT1, VOUT2, VOUT3, VOUT4	–0.3	4	V
V _{DD} , V _{SCL} , V _{SDA} , V _{ADDx}	Input voltage for VDD, SCL, SDA, ADD1, ADD2, ADD3	–0.3	4	V
V _{ONx}	Input voltage for ON1, ON2, ON3, ON4	–0.3	6	V
I _{MAX}	Maximum continuous switch current per channel		1	A
T _A	Operating free-air temperature ⁽³⁾	–40	85	°C
T _J	Maximum junction temperature		125	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C

- Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to network ground pin.
- In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A(max)} = T_{J(max)} – (θ_{JA} × P_{D(max)})

8.3 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature	–65	150	°C
ESD ⁽¹⁾	Electrostatic discharge protection	Human-Body Model (HBM) ⁽²⁾	–2000	2000
		Charged-Device Model (CDM) ⁽³⁾	–500	500

- Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

8.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		TPS22994	
		RUK	UNIT
		20 PINS	
Θ_{JA}	Junction-to-ambient thermal resistance	46	°C/W
$\Theta_{JC(top)}$	Junction-to-case(top) thermal resistance	50	
Θ_{JB}	Junction-to-board thermal resistance	18	
Ψ_{JT}	Junction-to-top characterization parameter	0.7	
Ψ_{JB}	Junction-to-board characterization parameter	18	
$\Theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	4.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

8.5 Electrical Characteristics

The specification applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full) (unless otherwise noted). Typical values are for $T_A = 25^{\circ}\text{C}$. $V_{BIAS} = 7.2\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES CURRENTS AND LEAKAGES								
$I_{Q, VBIAS}$	Quiescent current for VBIAS (all four channels)	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1,2,3,4} = \text{lower of } (V_{BIAS}-1\text{ V}) \text{ or } 3.6\text{ V}$, $V_{ON1,2,3,4} = 3.6\text{ V}$, $V_{DD} = 0\text{ V}$	$V_{BIAS} = 2.7\text{ V}$	Full	18.3	27.6	μA	
			$V_{BIAS} = 3.3\text{ V}$		18.9	28.6		
			$V_{BIAS} = 4.5\text{ V}$		19.4	29.9		
			$V_{BIAS} = 5.2\text{ V}$		19.9	30.3		
			$V_{BIAS} = 7.2\text{ V}$		21.1	33.6		
			$V_{BIAS} = 10.8\text{ V}$		21.2	34.8		
			$V_{BIAS} = 12.6\text{ V}$		21.2	35.0		
			$V_{BIAS} = 17.2\text{ V}$		21.2	35.7		
	Quiescent current for VBIAS (single channel)	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1} = \text{lower of } (V_{BIAS}-1\text{ V}) \text{ or } 3.6\text{ V}$, $V_{ON1} = 3.6\text{ V}$, $V_{IN2,3,4} = V_{ON2,3,4} = 0\text{ V}$, $V_{DD} = 0\text{ V}$	$V_{BIAS} = 2.7\text{ V}$	Full	8.3	16.6	μA	
			$V_{BIAS} = 3.3\text{ V}$		8.8	17.6		
			$V_{BIAS} = 4.5\text{ V}$		9.5	18.9		
			$V_{BIAS} = 5.2\text{ V}$		9.9	19.6		
			$V_{BIAS} = 7.2\text{ V}$		11.3	22.5		
			$V_{BIAS} = 10.8\text{ V}$		11.7	23.6		
$V_{BIAS} = 12.6\text{ V}$			11.7		23.8			
$V_{BIAS} = 17.2\text{ V}$			11.9		24.4			
$I_{Q, VDD}$	Quiescent current for VDD	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1,2,3,4} = V_{ON1,2,3,4} = 3.6\text{ V}$, $f_{SCL} = 0\text{ Hz}$	$V_{DD} = 1.8\text{ V}$	Full	0.6	1.1	μA	
$V_{DD} = 3.6\text{ V}$	1.2	1.9						
$I_{DYN, VDD}$	Average dynamic current for VDD during I ² C communication	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1,2,3,4} = V_{ON1,2,3,4} = 3.6\text{ V}$, $f_{SCL} = 1\text{ MHz}$	$V_{DD} = 1.8\text{ V}$	Full	7.7	μA		
			$V_{DD} = 3.6\text{ V}$		19.0			
$I_{DYN, VBIAS}$	Average dynamic current for VBIAS (all four channels) during I ² C communication	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1,2,3,4} = \text{lower of } (V_{BIAS}-1\text{ V}) \text{ or } 3.6\text{ V}$, $V_{ON1,2,3,4} = 3.6\text{ V}$, $f_{SCL} = 1\text{ MHz}$	$V_{BIAS} = 3.3\text{ V}$	Full	65.0	μA		
			$V_{BIAS} = 5.2\text{ V}$		66.9			
			$V_{BIAS} = 7.2\text{ V}$		68.4			
			$V_{BIAS} = 10.8\text{ V}$		68.5			
			$V_{BIAS} = 12.6\text{ V}$		68.6			
			$V_{BIAS} = 17.2\text{ V}$		69.1			
	Average dynamic current for VBIAS (single channel) during I ² C communication	$I_{OUT1,2,3,4} = 0\text{ A}$, $V_{IN1,2,3,4} = \text{lower of } (V_{BIAS}-1\text{ V}) \text{ or } 3.6\text{ V}$, $V_{ON1,2,3,4} = 3.6\text{ V}$, $V_{IN2,3,4} = V_{ON2,3,4} = 0\text{ V}$, $f_{SCL} = 1\text{ MHz}$	$V_{BIAS} = 3.3\text{ V}$	Full	48.0	μA		
			$V_{BIAS} = 5.2\text{ V}$		58.2			
			$V_{BIAS} = 7.2\text{ V}$		58.9			
			$V_{BIAS} = 10.8\text{ V}$		60.2			
			$V_{BIAS} = 12.6\text{ V}$		60.2			
			$V_{BIAS} = 17.2\text{ V}$		60.7			

Electrical Characteristics (continued)

The specification applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full) (unless otherwise noted). Typical values are for $T_A = 25^{\circ}\text{C}$. $V_{\text{BIAS}} = 7.2\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT	
$I_{\text{SD, VBIAS}}$	Shutdown current for VBIAS (all four channels)	$V_{\text{ON}1,2,3,4} = 0\text{ V}$, $V_{\text{OUT}1,2,3,4} = 0\text{ V}$, $V_{\text{DD}} = 3.6\text{ V}$, $V_{\text{BIAS}} = 17.2\text{ V}$	Full		6.5	12.8	μA	
$I_{\text{SD, VDD}}$	Shutdown current for VDD	$V_{\text{ON}1,2,3,4} = 0\text{ V}$, $V_{\text{OUT}1,2,3,4} = 0\text{ V}$, $V_{\text{DD}} = 3.6\text{ V}$	Full		1.2	1.9	μA	
$I_{\text{SD, VINx}}$	Shutdown current for VINx	$V_{\text{ONx}} = 0\text{ V}$, $V_{\text{OUTx}} = 0\text{ V}$, $V_{\text{DD}} = 3.6\text{ V}$	Full		$V_{\text{INx}} = 3.6\text{ V}$	1.0	μA	
					$V_{\text{INx}} = 3.3\text{ V}$	1.0		
					$V_{\text{INx}} = 1.8\text{ V}$	0.5		
					$V_{\text{INx}} = 1.5\text{ V}$	0.5		
					$V_{\text{INx}} = 1.0\text{ V}$	0.5		
I_{ONx}	Leakage current for ONx	$V_{\text{ONx}} = 5\text{ V}$	Full		0.003	0.1	μA	
I_{ADDx}	Leakage current for ADDx	$V_{\text{ADDx}} = 3.6\text{ V}$	Full		0.002	0.2	μA	
I_{SCL}	Leakage current for SCL	$V_{\text{SCL}} = 3.6\text{ V}$	Full		0.002	0.2	μA	
I_{SDA}	Leakage current for SDA	$V_{\text{SDA}} = 3.6\text{ V}$	Full		0.002	0.2	μA	
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance	$V_{\text{BIAS}} = 7.2\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C	$V_{\text{IN}} = 3.3\text{ V}$	40.6	50.3	$\text{m}\Omega$	
				Full		58.5		
			25°C	$V_{\text{IN}} = 2.5\text{ V}$	40.5	50.2	$\text{m}\Omega$	
				Full		58.5		
			25°C	$V_{\text{IN}} = 1.8\text{ V}$	40.5	50.1	$\text{m}\Omega$	
				Full		58.5		
			25°C	$V_{\text{IN}} = 1.5\text{ V}$	40.5	50.1	$\text{m}\Omega$	
				Full		58.5		
			25°C	$V_{\text{IN}} = 1.0\text{ V}$	40.5	49.9	$\text{m}\Omega$	
				Full		58.5		
			$V_{\text{BIAS}} = 5.2\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C	$V_{\text{IN}} = 3.3\text{ V}$	60.4	64.0	$\text{m}\Omega$
					Full		71.0	
		25°C		$V_{\text{IN}} = 2.5\text{ V}$	44.7	53.1	$\text{m}\Omega$	
				Full		65.2		
		25°C		$V_{\text{IN}} = 1.8\text{ V}$	41.5	50.3	$\text{m}\Omega$	
				Full		60.9		
		25°C		$V_{\text{IN}} = 1.5\text{ V}$	40.8	50.3	$\text{m}\Omega$	
				Full		60.5		
		25°C		$V_{\text{IN}} = 1.0\text{ V}$	40.6	50.1	$\text{m}\Omega$	
				Full		60.3		
		$V_{\text{BIAS}} = 3.3\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$		25°C	$V_{\text{IN}} = 2.3\text{ V}$	114.2	166.0	$\text{m}\Omega$
					Full		175.0	
			25°C	$V_{\text{IN}} = 1.8\text{ V}$	64.2	85.9	$\text{m}\Omega$	
				Full		94.4		
25°C	$V_{\text{IN}} = 1.5\text{ V}$		55.4	69.5	$\text{m}\Omega$			
	Full			81.0				
25°C	$V_{\text{IN}} = 1.0\text{ V}$		48.0	57.9	$\text{m}\Omega$			
	Full			70.0				
R_{PD}	Output pulldown resistance	$V_{\text{IN}} = 3.3\text{ V}$, $V_{\text{ON}} = 0\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, QOD[1:0] = 00	25°C	93	Ω			
		$V_{\text{IN}} = 3.3\text{ V}$, $V_{\text{ON}} = 0\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, QOD[1:0] = 01	25°C	470				
		$V_{\text{IN}} = 3.3\text{ V}$, $V_{\text{ON}} = 0\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, QOD[1:0] = 10	25°C	940				
		$V_{\text{IN}} = 3.3\text{ V}$, $V_{\text{ON}} = 0\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, QOD[1:0] = 11		No QOD				

Electrical Characteristics (continued)

The specification applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ (Full) (unless otherwise noted). Typical values are for $T_A = 25^{\circ}\text{C}$. $V_{\text{BIAS}} = 7.2\text{ V}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
THRESHOLD CHARACTERISTICS							
$V_{\text{IH, ADDx}}$	High-level input voltage for ADDx		Full	$0.7 \times V_{\text{DD}}$			V
$V_{\text{IL, ADDx}}$	Low-level input voltage for ADDx		Full		$0.3 \times V_{\text{DD}}$		V
$V_{\text{IH, ONx}}$	High-level input voltage for ONx		Full	1.05		5	V
$V_{\text{IL, ONx}}$	Low-level input voltage for ONx		Full	0		0.4	V
$V_{\text{HYS, ONx}}$	Hysteresis for ONx	$V_{\text{BIAS}} = 2.7\text{ V}$	25°C		107		mV
		$V_{\text{BIAS}} = 5.2\text{ V}$			105		
		$V_{\text{BIAS}} = 7.2\text{ V}$			107		
		$V_{\text{BIAS}} = 10.8\text{ V}$			108		
		$V_{\text{BIAS}} = 12.6\text{ V}$			109		
		$V_{\text{BIAS}} = 17.2\text{ V}$			108		
I²C CHARACTERISTICS							
$f_{\text{SCL}}^{(1)}$	Clock frequency		Full			1	MHz
$t_{\text{SU, SDA}}^{(1)}$	Setup time for SDA	$f_{\text{SCL}} = 1\text{ MHz}$ (fast mode plus)	Full	50			ns
$t_{\text{HD, SDA}}^{(1)}$	Hold time for SDA		Full	0			ns
$I_{\text{OL, SDA}}$	SDA output low current	$V_{\text{OL, SDA}} = 0.4\text{ V}$	25°C		8		mA
$V_{\text{IH, SDA}}$	High-level input voltage for SDA		Full	$0.7 \times V_{\text{DD}}$		V_{DD}	V
$V_{\text{IH, SCL}}$	High-level input voltage for SCL		Full	$0.7 \times V_{\text{DD}}$		V_{DD}	V
$V_{\text{IL, SDA}}$	Low-level input voltage for SDA		Full	0		$0.3 \times V_{\text{DD}}$	V
$V_{\text{IL, SCL}}$	Low-level input voltage for SCL		Full	0		$0.3 \times V_{\text{DD}}$	V

(1) Parameter verified by design.

8.6 Switching Characteristics, $V_{BIAS} = 7.2\text{ V}$

Values below are typical values at $T_A = 25^\circ\text{C}$. $V_{BIAS} = 7.2\text{V}$ (unless otherwise noted).

PARAMETER	TEST CONDITION	VIN VOLTAGE				UNIT	
		3.3 V	1.8 V	1.5 V	1.0 V		
t_{ON} VOUTx turn-on time	$V_{BIAS} = 7.2\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	Slew rate[4:2] = 000	10.2	10.0	9.9	9.9	μs
		Slew rate[4:2] = 001	220	159	147	124	
		Slew rate[4:2] = 010	380	274	252	213	
		Slew rate[4:2] = 011	674	486	446	377	
		Slew rate[4:2] = 100	1334	967	888	749	
t_{OFF} VOUTx turn-off time	$V_{BIAS} = 7.2\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	2.5	2.5	2.5	2.5	μs	
t_R VOUTx rise time	$V_{BIAS} = 7.2\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	Slew rate[4:2] = 000	1.4	0.9	0.8	0.7	μs
		Slew rate[4:2] = 001	271	178	158	125	
		Slew rate[4:2] = 010	471	309	275	218	
		Slew rate[4:2] = 011	835	549	489	390	
		Slew rate[4:2] = 100	1674	1096	976	774	
t_F VOUTx fall time	$V_{BIAS} = 7.2\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	2.3	2.3	2.3	2.3	μs	
t_D VOUTx ON delay time	$V_{BIAS} = 7.2\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, Slew rate[6:5] = 000	ON delay[4:2] = 00	9.6	9.6	9.6	9.6	μs
		ON delay[4:2] = 01	87	87	87	87	
		ON delay[4:2] = 10	295	295	295	295	
		ON delay[4:2] = 11	846	846	846	846	

8.7 Switching Characteristics, $V_{BIAS} = 3.3\text{ V}$

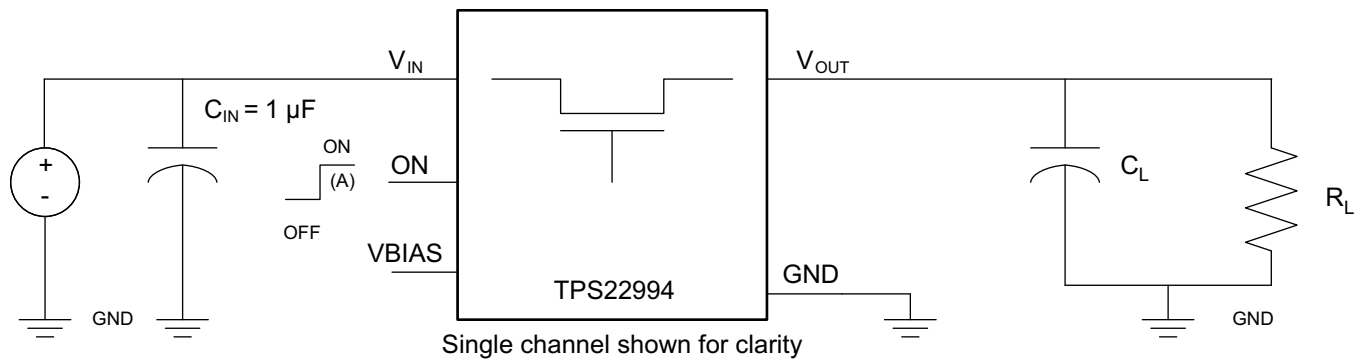
Values below are typical values at $T_A = 25^\circ\text{C}$. $V_{BIAS} = 3.3\text{ V}$ (unless otherwise noted).

PARAMETER	TEST CONDITION	VIN VOLTAGE			UNIT	
		1.8V	1.5V	1.0V		
t_{ON} VOUTx turn-on time	$V_{BIAS} = 3.3\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	Slew rate[4:2] = 000	8.4	8.3	8.1	μs
		Slew rate[4:2] = 001	165	152	129	
		Slew rate[4:2] = 010	283	260	221	
		Slew rate[4:2] = 011	502	460	389	
		Slew rate[4:2] = 100	997	915	773	
t_{OFF} VOUTx turn-off time	$V_{BIAS} = 3.3\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	2.5	2.6	2.8	μs	
t_R VOUTx rise time	$V_{BIAS} = 3.3\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	Slew rate[4:2] = 000	2.8	2.4	1.8	μs
		Slew rate[4:2] = 001	184	163	128	
		Slew rate[4:2] = 010	318	283	224	
		Slew rate[4:2] = 011	565	501	398	
		Slew rate[4:2] = 100	1126	1002	791	
t_F VOUTx fall time	$V_{BIAS} = 3.3\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, $ON\text{-delay}[6:5] = 00$	2.2	2.2	2.1	μs	
t_D VOUTx ON delay time	$V_{BIAS} = 3.3\text{ V}$, $R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $QOD[1:0] = 10$, Slew rate[6:5] = 000	ON delay[4:2] = 00	7.3	7.3	7.3	μs
		ON delay[4:2] = 01	89	89	89	
		ON delay[4:2] = 10	296	296	296	
		ON delay[4:2] = 11	846	846	846	

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- A. Rise and fall times of the control signal is 100 ns.
- B. All switching measurements are done using GPIO control only.

Figure 1. Test Circuit

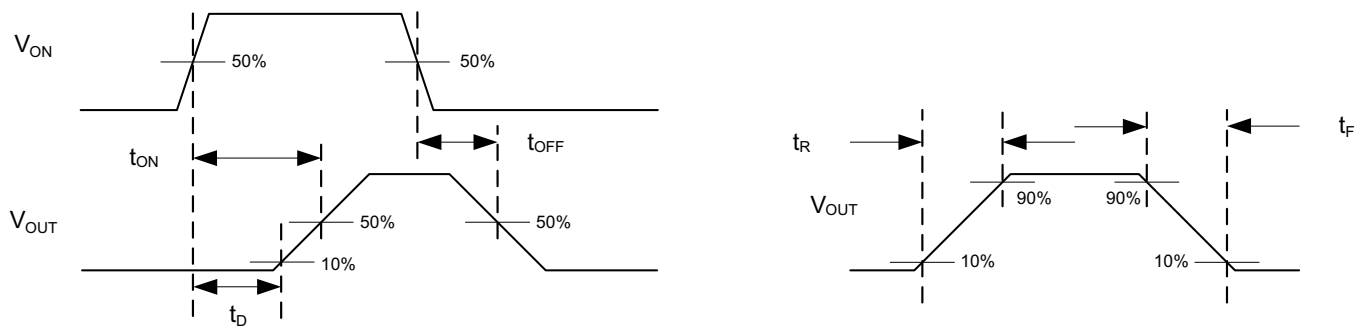


Figure 2. t_{ON}/t_{OFF} Waveforms

8.8 Typical Characteristics

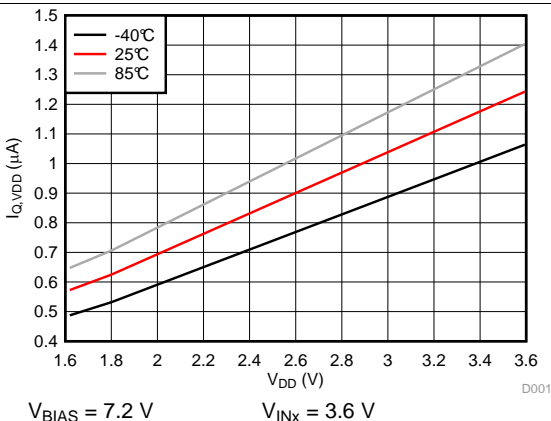


Figure 3. $I_{Q,VDD}$ vs. V_{DD}

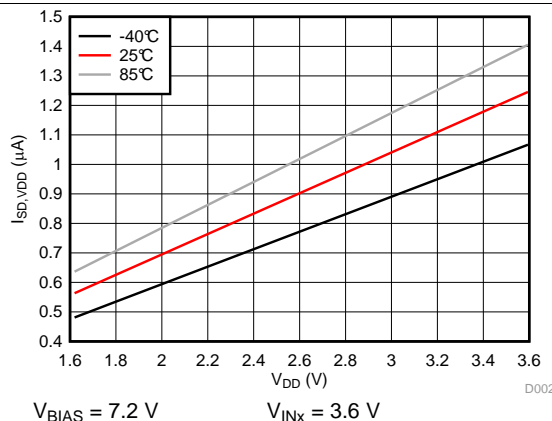


Figure 4. $I_{SD,VDD}$ vs. V_{DD}

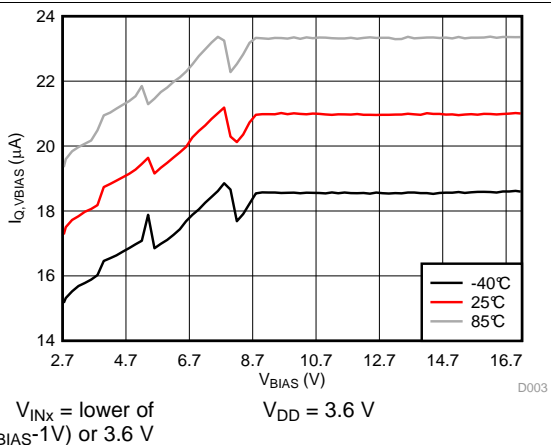


Figure 5. $I_{Q,VBIAS}$ vs. V_{BIAS} (all channels)

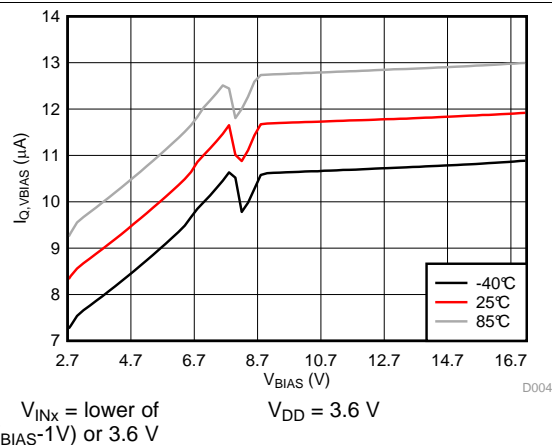


Figure 6. $I_{Q,VBIAS}$ vs. V_{BIAS} (single channel)

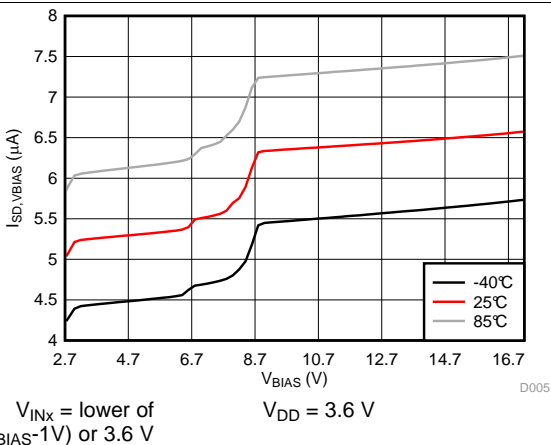


Figure 7. $I_{SD,VBIAS}$ vs. V_{BIAS}

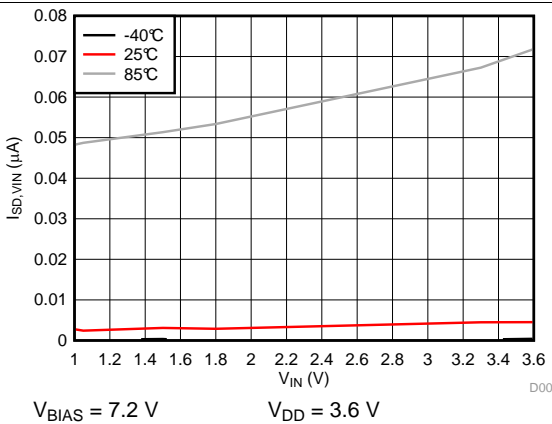


Figure 8. $I_{SD,VIN}$ vs. V_{IN}

Typical Characteristics (continued)

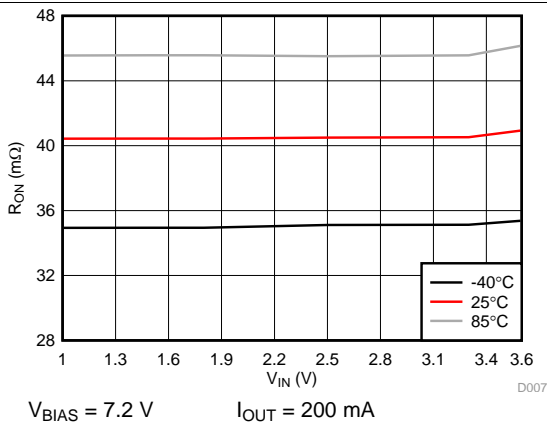


Figure 9. R_{ON} vs. V_{IN}

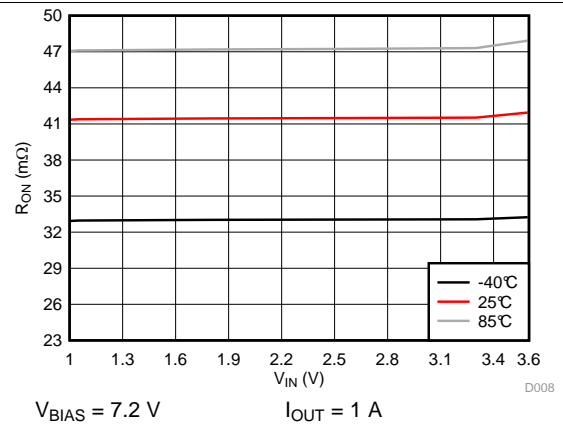


Figure 10. R_{ON} vs. V_{IN} (single channel)

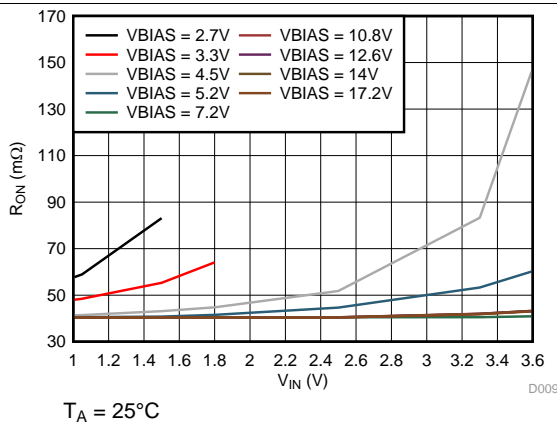


Figure 11. R_{ON} vs. V_{IN}

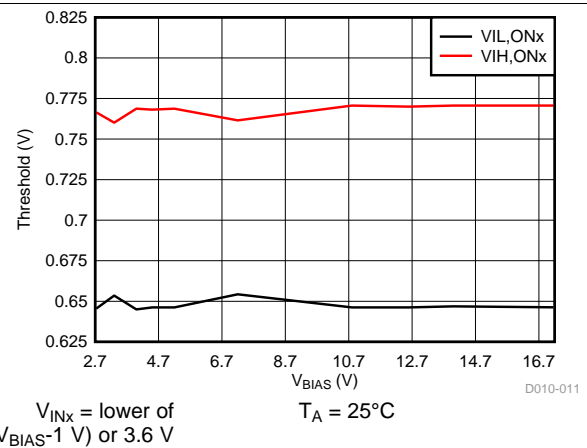


Figure 12. V_{IH}/V_{IL} for ONx vs. V_{BIAS}

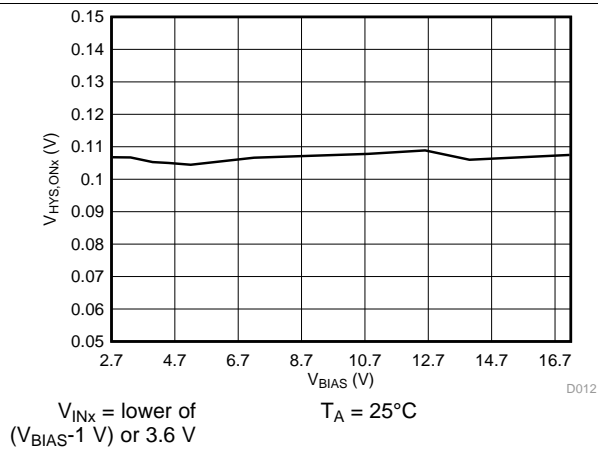


Figure 13. $V_{HYS, ONx}$ vs. V_{BIAS}

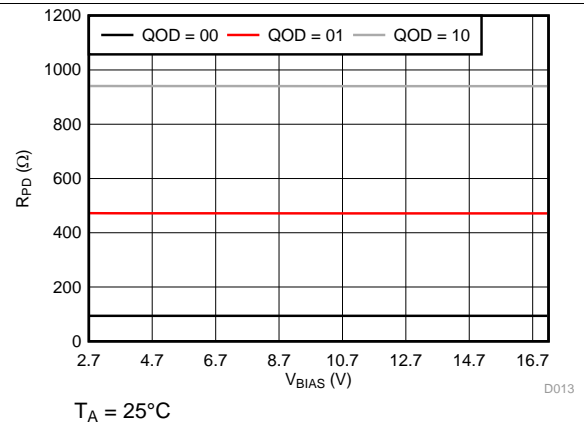


Figure 14. R_{PD} vs. V_{BIAS}

Typical Characteristics (continued)

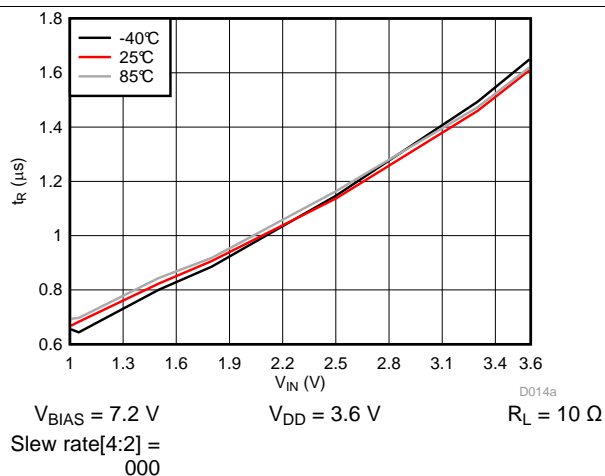


Figure 15. t_R vs. V_{IN}

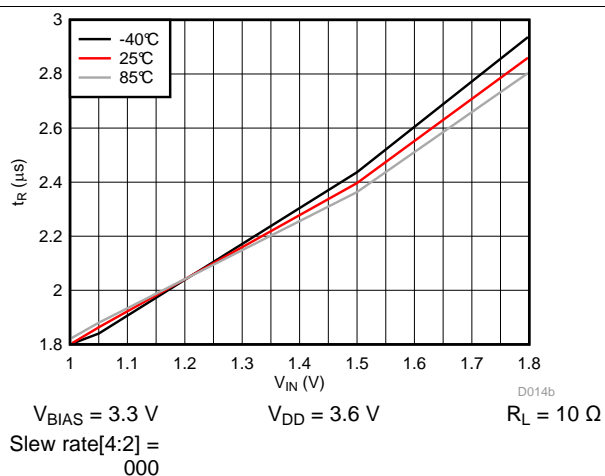


Figure 16. t_R vs. V_{IN}

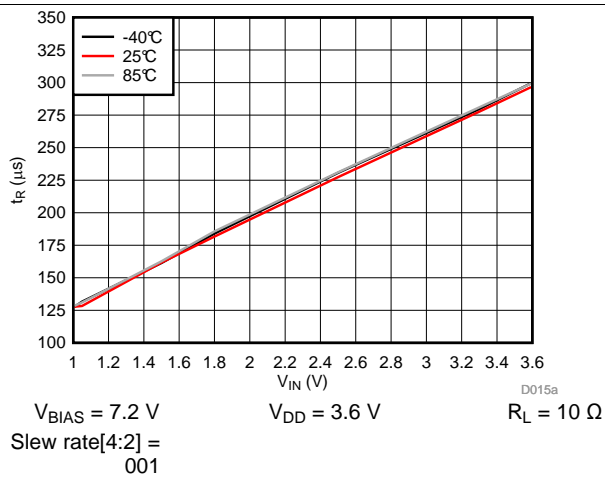


Figure 17. t_R vs. V_{IN}

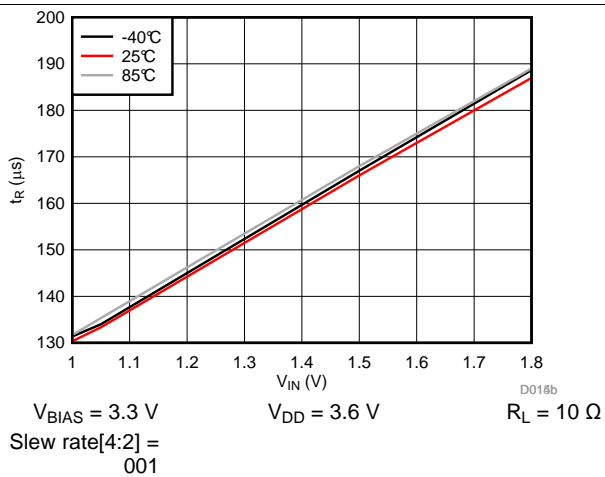


Figure 18. t_R vs. V_{IN}

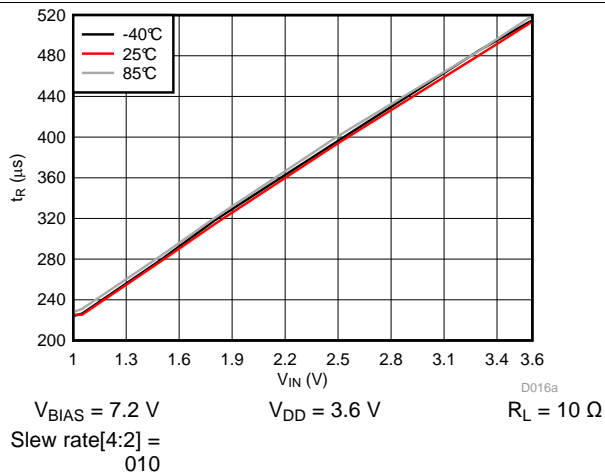


Figure 19. t_R vs. V_{IN}

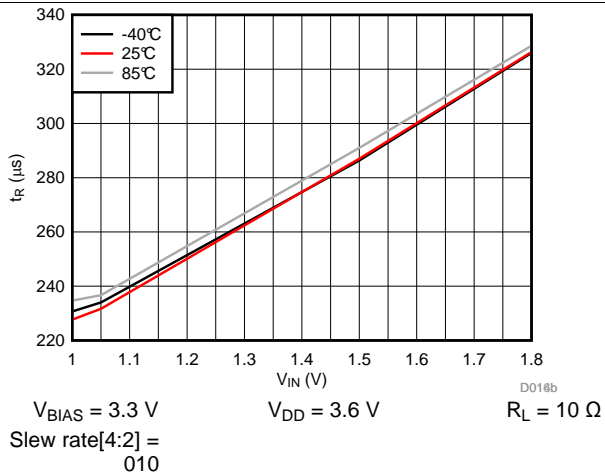


Figure 20. t_R vs. V_{IN}

Typical Characteristics (continued)

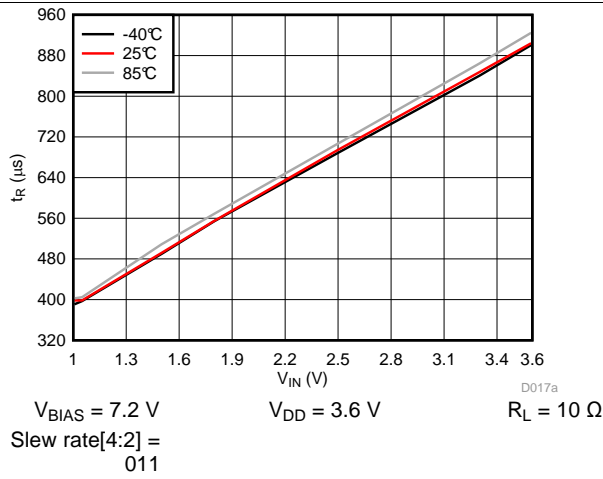


Figure 21. t_R vs. V_{IN}

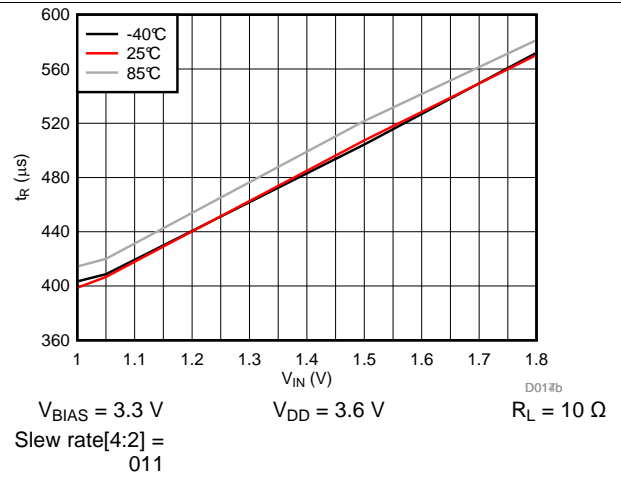


Figure 22. t_R vs. V_{IN}

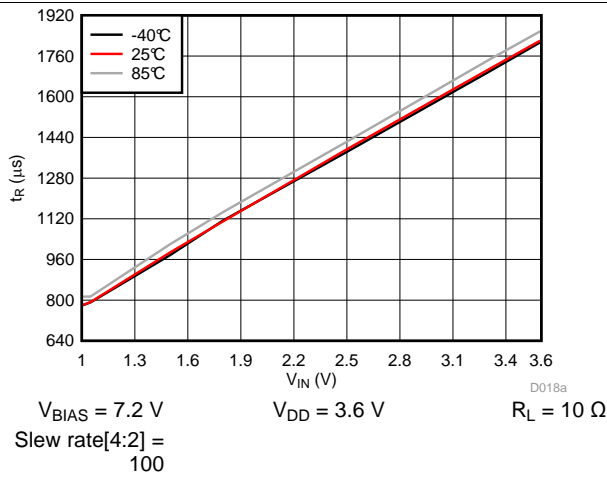


Figure 23. t_R vs. V_{IN}

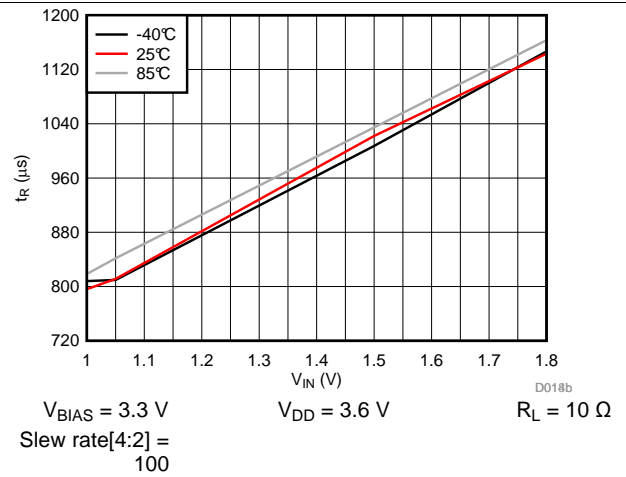


Figure 24. t_R vs. V_{IN}

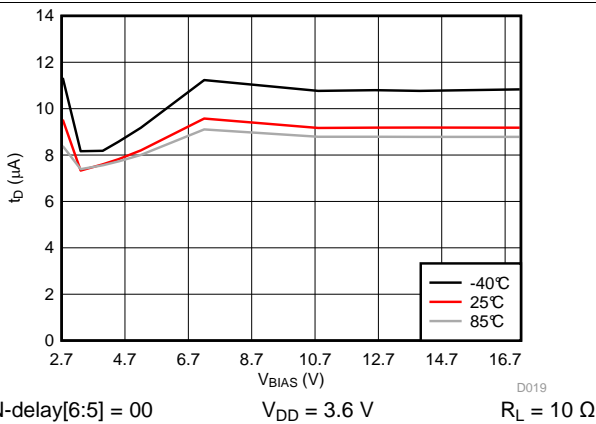


Figure 25. t_D vs. V_{BIAS}

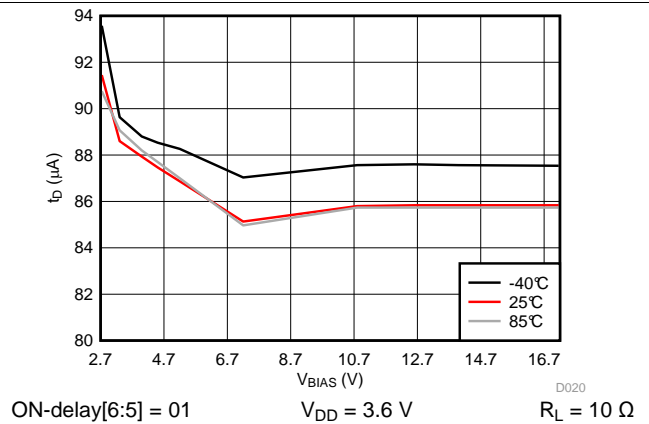


Figure 26. t_D vs. V_{BIAS}

Typical Characteristics (continued)

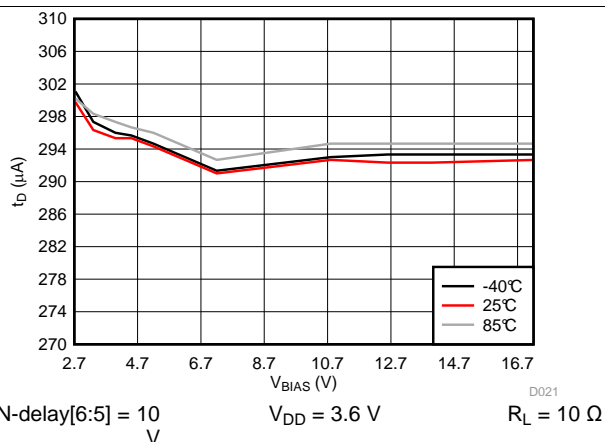


Figure 27. t_D vs. V_{BIAS}

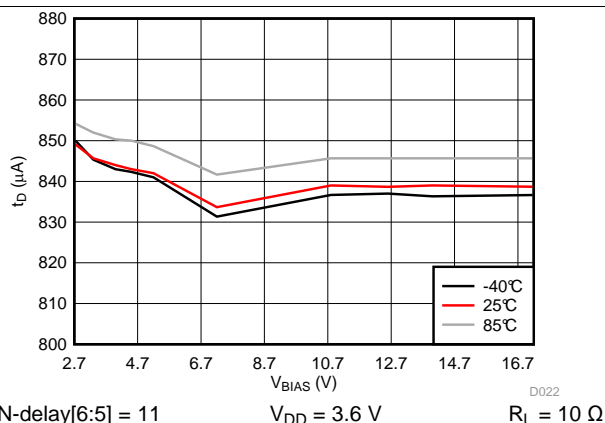


Figure 28. t_D vs. V_{BIAS}

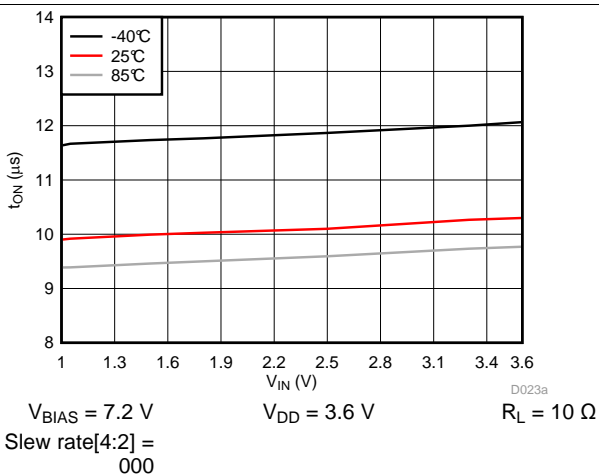


Figure 29. t_{ON} vs. V_{IN}

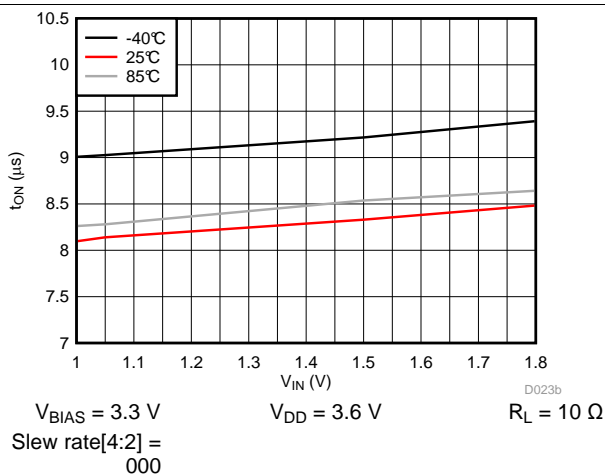


Figure 30. t_{ON} vs. V_{IN}

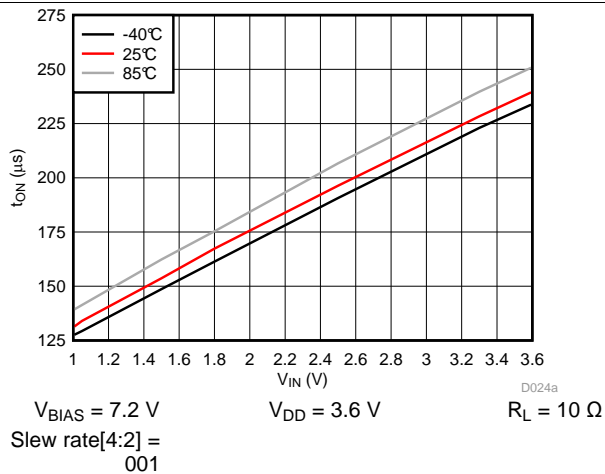


Figure 31. t_{ON} vs. V_{IN}

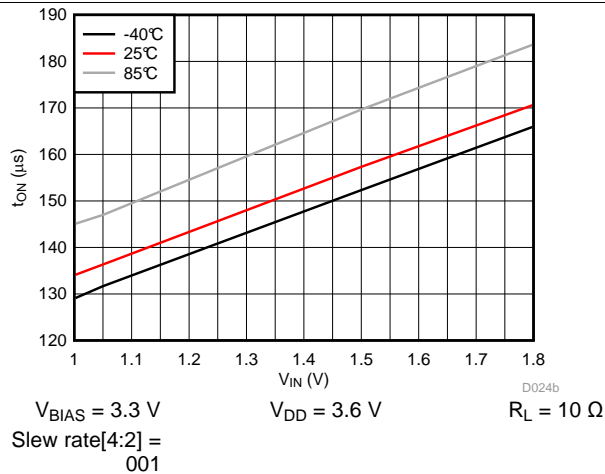


Figure 32. t_{ON} vs. V_{IN}

Typical Characteristics (continued)

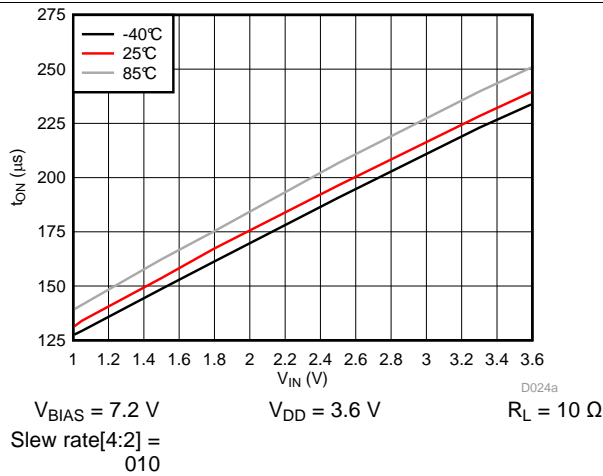


Figure 33. t_{ON} vs. V_{IN}

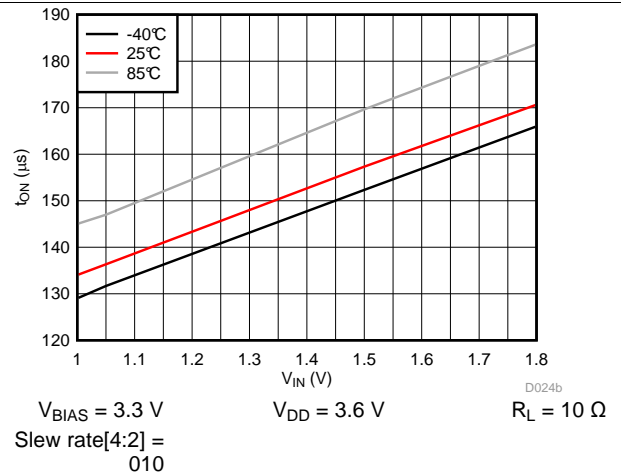


Figure 34. t_{ON} vs. V_{IN}

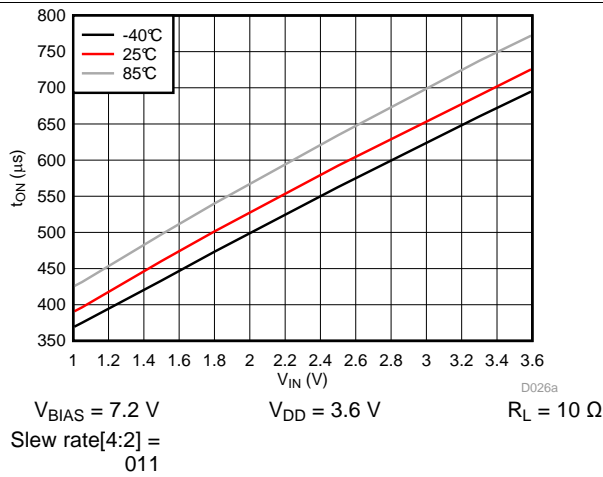


Figure 35. t_{ON} vs. V_{IN}

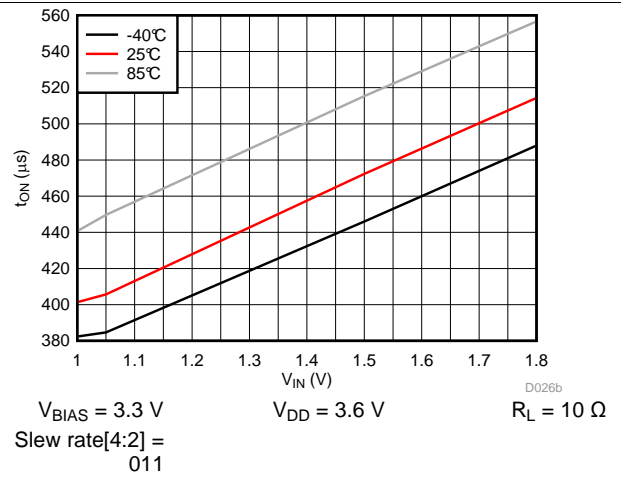


Figure 36. t_{ON} vs. V_{IN}

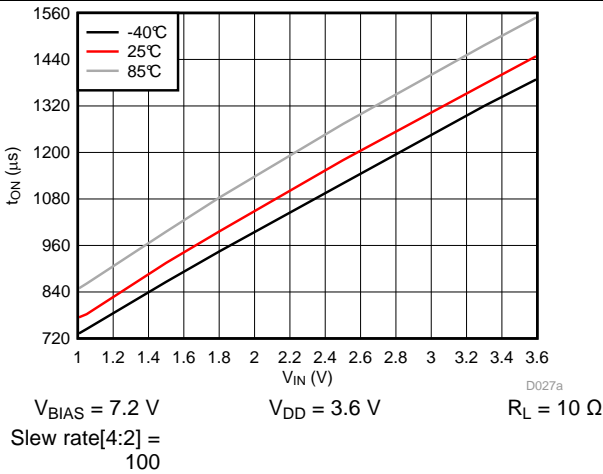


Figure 37. t_{ON} vs. V_{IN}

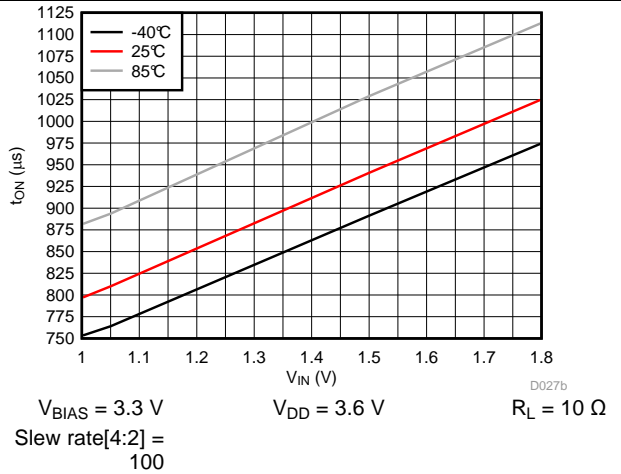


Figure 38. t_{ON} vs. V_{IN}

Typical Characteristics (continued)

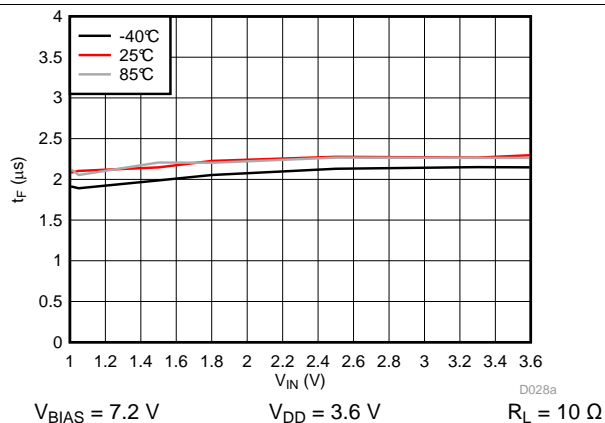


Figure 39. t_F vs. V_{IN}

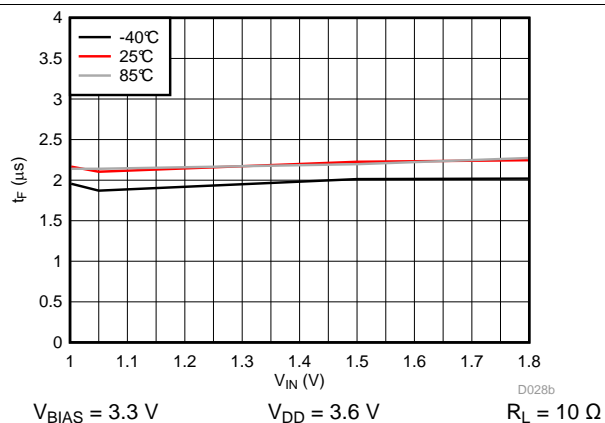


Figure 40. t_F vs. V_{IN}

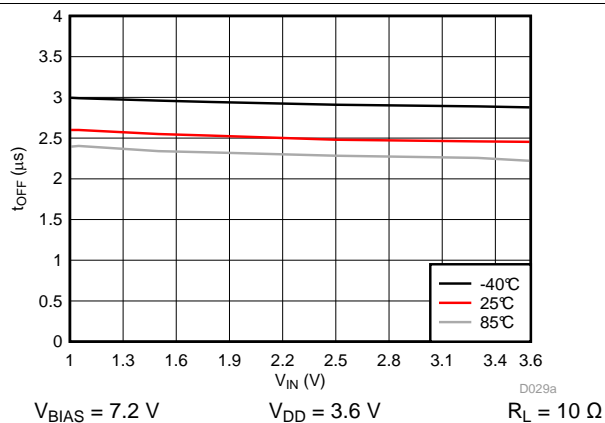


Figure 41. t_{OFF} vs. V_{IN}

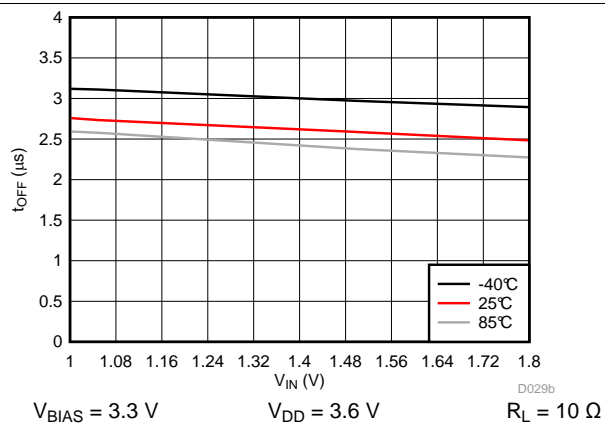


Figure 42. t_{OFF} vs. V_{IN}

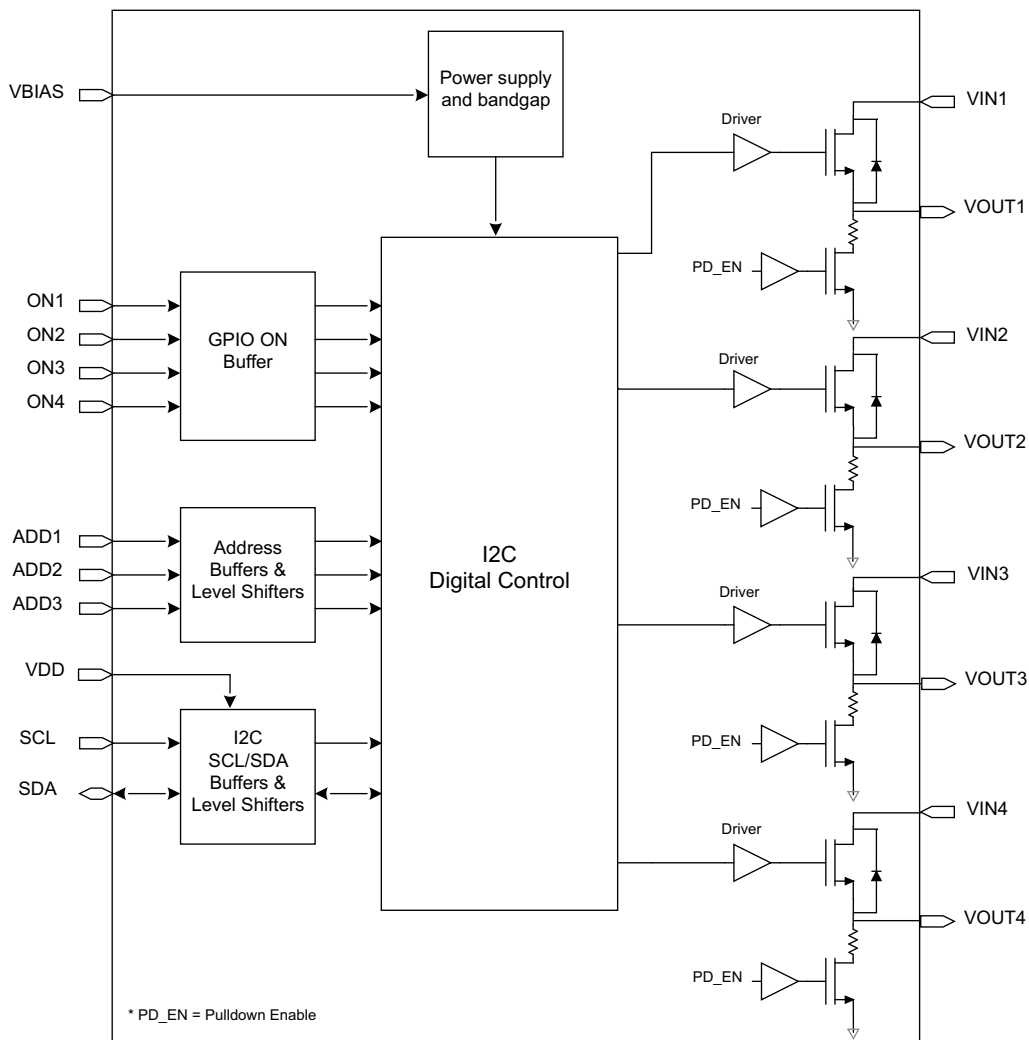
9 Detailed Description

9.1 Overview

The TPS22994 is a GPIO controllable and I²C programmable, quad-channel load switch. The device comes in a 20-pin QFN package and is designed to handle up to 3.6 V and 1 A per channel (per VINx/VOUTx). The VBIAS pin of the device is designed to interface directly with battery voltages or adapter input voltages as high as 17.2 V. To increase efficiency during standby power, the device implements each channel with an N-channel MOSFET without the use of a chargepump. This allows the quiescent current (I_{Q,VBIAS}) to be much lower than traditional GPIO-based load switches, thus increasing efficiency during standby.

The TPS22994 can be programmed via standard I²C commands. This allows the user to select between 5 slew rates, 4 on-delays, and 4 quick output discharge (QOD) options. The combination of these options allows the user to program the power sequencing for downstream modules via software. Each individual channel can also be controlled (enabling and disabling channels only) via GPIO when I²C communication is not present. The TPS22994 contains a special function called SwitchALL™ that allows multiple devices (either the TPS22993 or TPS22994) to be enabled or disabled synchronously via a single I²C command, allowing the user to switch system power states synchronously.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Operating Frequency

The TPS22994 is designed to be compatible with fast-mode plus and operate up to 1 MHz clock frequency for bus communication. The device is also compatible with standard-mode (100 kHz) and fast-mode (400 kHz). This device can reside on the same bus as high-speed mode (3.4MHz) devices, but the device is not designed for I²C commands for frequencies greater than 1 MHz. See table below for characteristics of the fast-mode plus, fast-mode, and standard-mode bus speeds.

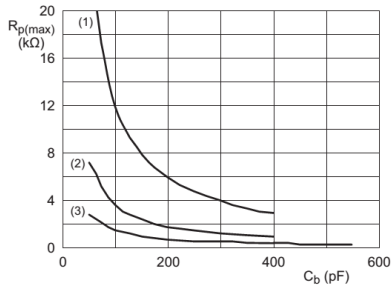
Table 1. I²C Interface Timing Requirements⁽¹⁾

PARAMETER		STANDARD MODE I ² C BUS		FAST MODE I ² C BUS		FAST MODE PLUS (FM+) I ² C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{scl}	I ² C clock frequency	0	100	0	400	0	1000	kHz
t _{sch}	I ² C clock high time	4		0.6		0.26		µs
t _{scl}	I ² C clock low time	4.7		1.3		0.5		µs
t _{sp}	I ² C spike time		50		50		50	ns
t _{sds}	I ² C serial data setup time	250		100		50		ns
t _{sdh}	I ² C serial data hold time	0		0		0		ns
t _{icr}	I ² C input rise time		1000	20	300		120	ns
t _{buf}	I ² C bus free time between Stop and Start	4.7		1.3		0.5		µs
t _{sts}	I ² C Start or repeater Start condition setup time	4.7		0.6		0.26		µs
t _{sth}	I ² C Start or repeater Start condition hold time	4		0.6		0.26		µs
t _{sps}	I ² C Stop condition setup time	4		0.6		0.26		µs
t _{vd(data)}	Valid data time; SCL low to SDA output valid		3.45	0.3	0.9		0.45	µs
t _{vd(ack)}	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		3.45	0.3	0.9		0.45	µs

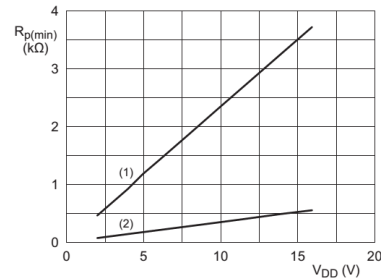
(1) over operating free-air temperature range (unless otherwise noted)

9.3.2 SDA/SCL Pin Configuration

The SDA and SCL pins of the device operate use an open-drain configuration, and therefore, need pull up resistors to communicate on the I²C bus. The graph below shows recommended values for max pull-up resistors (R_P) and bus capacitances (C_b) to ensure proper bus communications. The SDA and SCL pins should be pulled up to VDD through an appropriately sized R_P based on the graphs below.



- (1) Standard-mode
- (2) Fast-mode
- (3) Fast-mode Plus



- (1) Fast-mode and Standard-mode
- (2) Fast-mode Plus

9.3.3 Address (ADDx) Pin Configuration

The TPS22994 can be configured with an unique I²C slave addresses by using the ADDx pins. There are 3 ADDx pins that can be tied high to VDD or low to GND (independent of each other) to get up to 7 different slave addresses. The ADDx pins should be tied to GND if the I²C functionality of the device is not to be used. External pull-up resistors for the ADDx are optional as the ADDx inputs are high impedance. The following table shows the ADDx pin tie-offs with their associated slave addresses (assuming an eight bit word, where the LSB is the read/write bit and the device address bits are the 7 MSB bits) :

Hex Address	ADD3	ADD2	ADD1
E0/E1	GND	GND	GND
E2/E3	GND	GND	VDD
E4/E5	GND	VDD	GND
E6/E7	GND	VDD	VDD
E8/E9	VDD	GND	GND
EA/EB	VDD	GND	VDD
EC/ED	VDD	VDD	GND
EE	Invalid unique device address. This address is the SwitchALL™ address.		

9.3.4 On-Delay Control

Using the I²C interface, the configuration register for each channel can be set for different ON delays for power sequencing. The typical options for delay are as follows (see [Switching Characteristics](#), $V_{BIAS} = 7.2\text{ V}$ table):

- 00 = 11 μs delay (default register value)
- 01 = 105 μs delay
- 10 = 330 μs delay
- 11 = 950 μs delay

It is not recommended to change the delay value for the duration of the delay that is programmed when the channel is enabled (except for ON-delay setting of '00' which requires a minimum of 100 μs wait time before changing the setting). This could result in erratic behavior where the output could toggle unintentionally but would eventually recover by the end of the delay time programmed at the time of channel enable.

9.3.5 Slew Rate Control

Using the I²C interface, the configuration register for each channel can be set for different slew rates for inrush current control and power sequencing. The typical options for slew rate are as follows (see [Switching Characteristics](#) table for VOUTx rise times):

- 000 = 1 μ s/V
- 001 = 150 μ s/V
- 010 = 250 μ s/V
- 011 = 460 μ s/V (default register value)
- 100 = 890 μ s/V
- 101 = invalid slew rate
- 110 = invalid slew rate
- 111 = reserved

9.3.6 Quick Output Discharge (QOD) Control

Using the I²C interface, the configuration register for each channel can be set for different output discharge resistors. The typical options for QOD are as follows (see Electrical Characteristics table):

- 00 = 110 Ω
- 01 = 490 Ω
- 10 = 951 Ω (default register value)
- 11 = No QOD (high impedance)

9.3.7 Mode Registers

Using the I²C interface, the mode registers can be programmed to the desired on/off status for each channel. The contents of these registers are copied over to the control registers when a SwitchALL™ command is issued, allowing all channels of the device to transition to their desired output states synchronously. See the I²C Protocol section and the Application Scenario section for more information on how to use the mode registers in conjunction with the SwitchALL™ command.

9.3.8 SwitchALL™ Command

I²C controlled channels can respond to a common slave address. This feature allows multiple load switches on the same I²C bus to respond simultaneously. The SwitchALL™ address is EEh. During a SwitchALL™ command, the lower four bits (bits 0 through 3) of the mode register is copied to the lower four bits (bits 0 through 3) of the control register. The mode register to be invoked is referenced in the body of the SwitchALL™ command. The structure of the SwitchALL™ command is as follows (as shown in Figure 43): <start><SwitchALL™ addr><mode addr><stop>. See the I²C Protocol section and the Application Scenario section for more information on how to use the SwitchALL™ command in conjunction with the mode registers.

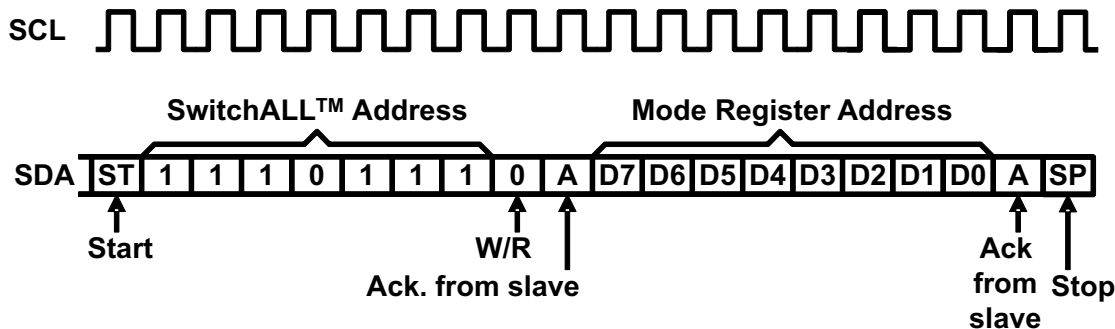


Figure 43. Composition of SwitchALL™ Command

9.3.9 V_{DD} Supply For I²C Operation

The SDA and SCL pins of the device must be pulled up to the VDD voltage of the device for proper I²C bus communication. See [Recommended Operating Conditions](#) for VDD operating range.

9.3.10 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop. For the fastest slew rate setting of the device, a C_{IN} to C_L ratio of at least 100 to 1 is recommended to avoid excessive voltage drop.

9.3.11 Output Capacitor (Optional)

Due to the integrated body diode of the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. For the fastest slew rate setting of the device, a C_{IN} to C_L ratio of at least 100 to 1 is recommended to minimize V_{IN} dip caused by inrush currents during startup.

9.3.12 I²C Protocol

The following section will cover the standard I²C protocol used in the TPS22994. In the I²C protocol, the following basic blocks are present in every command (except for the SwitchALL™ command):

- Start/stop bit – marks the beginning and end of each command.
- Slave address – the unique address of the slave device.
- Sub address – this includes the register address and the auto-increment bit.
- Data byte – data being written to the register. Eight bits must always be transferred even if a single bit is being written or read.
- Auto-increment bit – setting this bit to ‘1’ turns on the auto-increment functionality; setting this bit to ‘0’ turns off the auto-increment functionality.
- Write/read bit – this bit signifies if the command being sent will result in reading from a register or writing to a register. Setting this bit to ‘0’ signifies a write, and setting this bit to ‘1’ signifies a read.
- Acknowledge bit – this bit signifies if the master or slave has received the preceding data byte.

9.3.12.1 Start and Stop Bit

In the I²C protocol, all commands contain a START bit and a STOP bit. A START bit, defined by high to low transition on the SDA line while SCL is high, marks the beginning of a command. A STOP bit, defined by low to high transition on the SDA line while SCL is high, marks the end of a command. The START and STOP bits are generated by the master device on the I²C bus. The START bit indicates to other devices that the bus is busy, and some time after the STOP bit the bus is assumed to be free.

9.3.12.2 Auto-increment Bit

The auto-increment feature in the I²C protocol allows users to read from and write to consecutive registers in fewer clock cycles. Since the register addresses are consecutive, this eliminates the need to resend the register address. The I²C core of the device automatically increments the register address pointer by one when the auto-increment bit is set to ‘1’. When this bit is set to ‘0’, the auto-increment functionality is disabled.

9.3.12.3 Write Command

During the write command, the write/read bit is set to ‘0’, signifying that the register in question will be written to. [Figure 44](#) the composition of the write protocol to a *single* register:

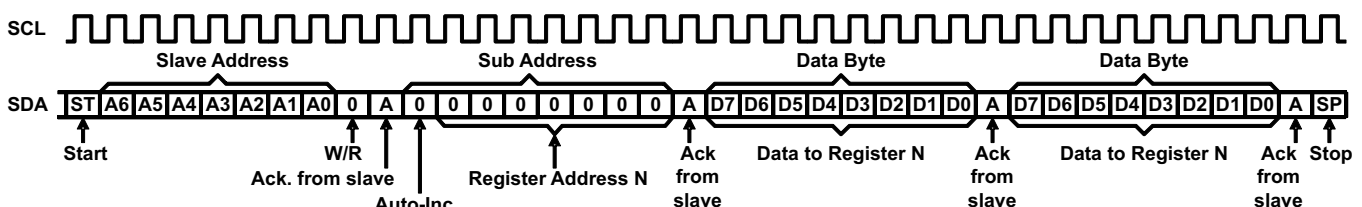


Figure 44. Data Write to a Single Register

Number of clock cycles for single register write: 29

If multiple consecutive registers must be written to, a short-hand version of the write command can be used. Using the auto-increment functionality of I²C, the device will increment the register address after each byte. Figure 45 shows the composition of the write protocol to multiple consecutive registers:

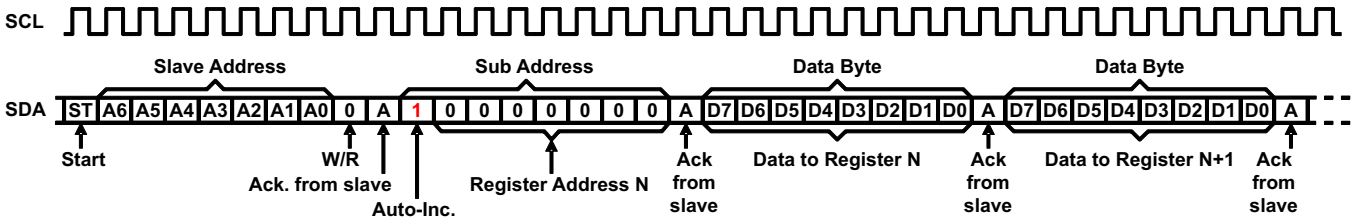


Figure 45. Data Write to Consecutive Registers

Number of clock cycles for consecutive register write: 20 + (Number of registers) x 9

The write command is always ended with a STOP bit after the desired registers have been written to. If multiple non-consecutive registers must be written to, then the format in Figure 44 must be followed.

9.3.12.4 Read Command

During the read command, the write/read bit is set to '1', signifying that the register in question will be read from. However, a read protocol includes a “dummy” write sequence to ensure that the memory pointer in the device is pointing to the correct register that will be read. Failure to precede the read command with a write command may result in a read from a random register. Figure 46 shows the composition of the read protocol to a single register:

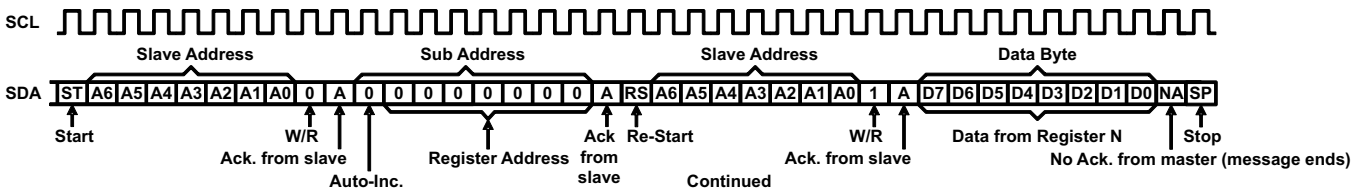


Figure 46. Data Read to a Single Register

Number of clock cycles for single register read: 39

If multiple registers must be read from, a short-hand version of the read command can be used. Using the auto-increment functionality of I²C, the device will increment the register address after each byte. Figure 47 shows the composition of the read protocol to multiple consecutive registers:

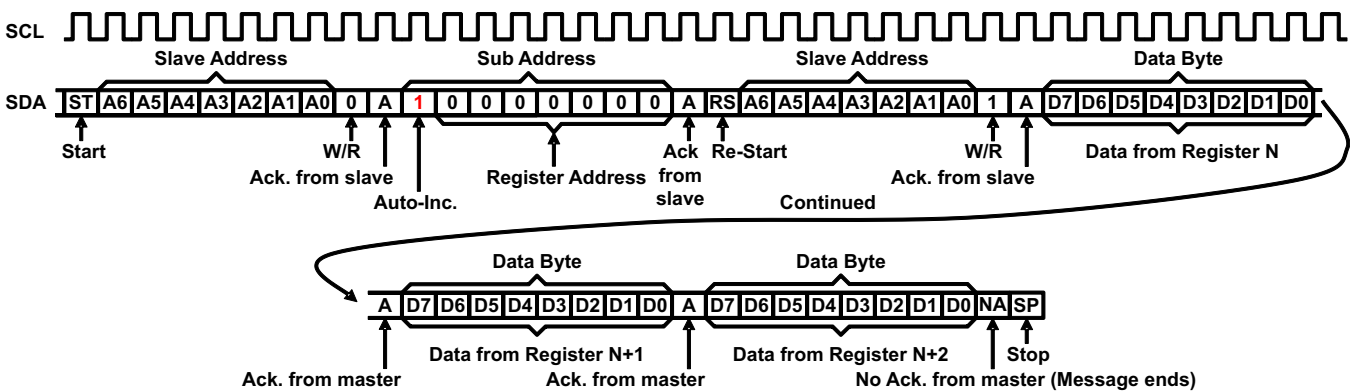


Figure 47. Data Read to Consecutive Registers

Number of clock cycles for consecutive register write: 30 + (Number of registers) x 9

The read command is always ended with a STOP bit after the desired registers have been read from. If multiple non-consecutive registers must be read from, then the format in [Figure 46](#) must be followed.

9.3.12.5 SwitchALL™ Command

The SwitchALL™ command allows multiple devices in the same I²C bus to respond synchronously to the same command from the master. Every TPS22994 device has a shared address which allows for multiple devices to respond or execute a pre-determined action with a single command. [Figure 48](#) shows the composition of the SwitchALL™ command:

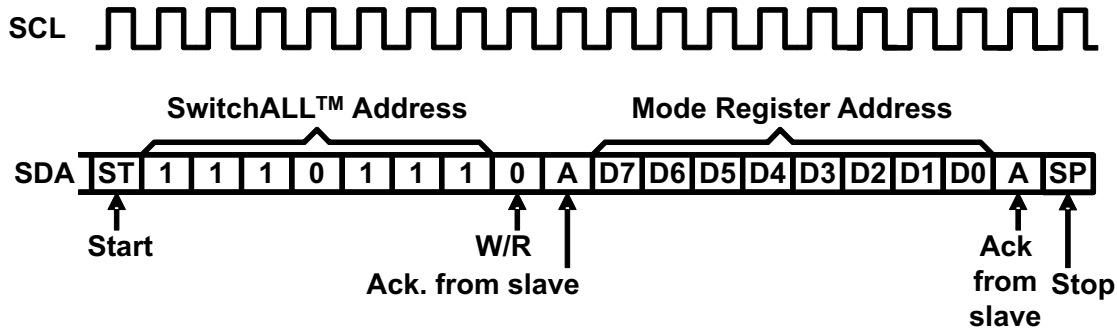


Figure 48. SwitchALL™ Command Structure

Number of clock cycles for a SwitchALL™ command: 20

9.4 Device Functional Modes

9.4.1 I²C Control

When power is applied to VBIAS, the device comes up in its default mode of GPIO operation where the channel outputs can be controlled solely via the ON pins. At any time, if SDA and SCL are present and valid, the device can be configured to be controlled via I²C (if in GPIO control) or GPIO (if in I²C control).

The control register (address **05h**) can be configured for GPIO or I²C enable on a per channel basis.

9.4.2 GPIO Control

There are four ON pins to enable/disable the four channels. Each ON pin controls the state of the switch by default upon power up. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher voltage GPIO.

9.5 Register Map

Configuration registers (default register values shown below)

Channel 1 configuration register (Address: **01h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 2 configuration register (Address: **02h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 3 configuration register (Address: **03h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 4 configuration register (Address: **04h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Control register (default register values shown below)

Control register (Address: **05h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I ² C ch 4	GPIO/I ² C ch 3	GPIO/I ² C ch 2	GPIO/I ² C ch 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Mode registers (default register values shown below)

Mode1 (Address: **06h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode2 (Address: **07h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode3 (Address: **08h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

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Mode4 (Address: 09h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode5 (Address: 0Ah)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode6 (Address: 0Bh)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode7 (Address: 0Ch)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode8 (Address: 0Dh)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode9 (Address: 0Eh)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode10 (Address: 0Fh)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode11 (Address: 10h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode12 (Address: 11h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section will cover applications of I²C in the TPS22994. Registers discussed here are specific to the TPS22994.

10.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-μF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop. For the fastest slew rate setting of the device, a C_{IN} to C_L ratio of at least 100 to 1 is recommended to avoid excessive voltage drop.

10.1.2 Output Capacitor (Optional)

Due to the integrated body diode of the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. For the fastest slew rate setting of the device, a C_{IN} to C_L ratio of at least 100 to 1 is recommended to minimize V_{IN} dip caused by inrush currents during startup.

10.1.3 Switch from GPIO Control to I²C Control (and vice versa)

The TPS22994 can be switched from GPIO control to I²C (and vice versa) mode by writing to the control register of the device. Each device has a single control register and is located at register address 05h. The register's composition is as follows:

Control register (Address: 05h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I ² C CH 4	GPIO/I ² C CH 3	GPIO/I ² C CH 2	GPIO/I ² C CH 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Figure 49. Control Register Composition

The higher four bits of the control register dictates if the device is in GPIO control (bit set to '0') or I²C control (bit set to '1'). The transition from GPIO control to I²C control can be made with a single write command to the control register. See [Figure 44](#) for the composition of a single write command. It is recommended that the channel of interest is transitioned from GPIO control to I²C control with the first write command and followed by a second write command to enable the channel via I²C control. This will ensure a smooth transition from GPIO control to I²C control.

10.1.4 Configuration of Configuration Registers

The TPS22994 contains four configuration registers (one for each channel) and are located at register addresses 01h through 04h. The register's composition is as follows (single channel shown for clarity):

Channel 1 configuration register (Address: 01h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	0	1	0

Figure 50. Configuration Register Composition

10.1.4.1 Single Register Configuration

A single configuration register can be written to using the write command sequence shown in Figure 44.

Multiple register writes to non-consecutive registers is treated as multiple single register writes and follows the same write command as that of a single register write as shown in Figure 44.

10.1.4.2 Multi-register Configuration (Consecutive Registers)

Multiple consecutive configuration registers can be written to using the write command sequence shown in Figure 45.

10.1.5 Configuration of Mode Registers

The TPS22994 contains twelve mode registers located at register addresses 06h through 11h. These mode registers allow the user to turn-on or turn-off multiple channels in a single TPS22994 or multiple channels spanning multiple TPS22994 devices with a single SwitchALL™ command.

For example, an application may have multiple power states (e.g. sleep, active, idle, etc.) as shown in Figure 51.

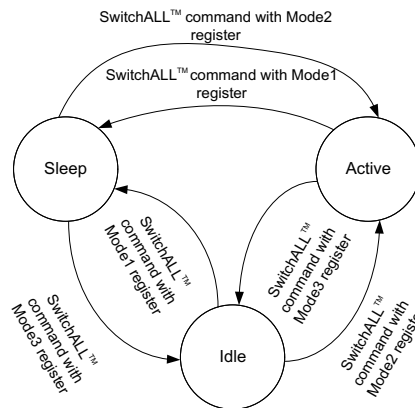


Figure 51. Application Example of Power States

In each of the different power states, different combinations of channels may be on or off. Each power state may be associated with a single mode register (Mode1, Mode2, etc.) across multiple TPS22994 as shown in Table 2. For example, with 7 quad-channel devices, up to 28 rails can be enabled/disabled with a single SwitchALL™ command.

Table 2. Application Example of State of Each Channel in Multiple TPS22994 in Different Power States

Mode Register	Power State	Load Switch #1				Load Switch #2				Load Switch #N			
		Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4
Mode1	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
Mode2	Active	On	On	On	On	On	Off	On	Off	On	Off	On	Off
Mode3	Idle	On	Off	On	Off	On	On	On	On	On	On	On	On

The contents of the lower four bits of the mode register is copied into the lower four bits of the control register during an SwitchALL™ command. The address of the mode register to be copied is specified in the SwitchALL™ command (see Figure 48 for the structure of the SwitchALL™ command). By executing a SwitchALL™ command, the application will apply the different on/off combinations for the various power states with a single command rather than having to turn on/off each channel individually by re-configuring the control register. This reduces the latency and allows the application to control multiple channels synchronously. The example above shows the application using three mode registers, but the TPS22994 contains twelve mode registers, allowing for up to twelve power states.

The mode register's composition is as follows (single mode register shown for clarity):

Mode1 (Address: 06h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Figure 52. Mode Register Composition

The lower four bits of the mode registers are copied into the lower four bits of the control register during an all-call command.

10.1.6 Turn-on/Turn-off of Channels

By default upon power up VBIAS, all the channels of the TPS22994 are controlled via the ONx pins. Using the I²C interface, each channel be controlled via I²C control as well. The channels of the TPS22994 can also be switched on or off by writing to the control register of the device. Each device has a single control register and is located at register address 05h. The register's composition is as follows:

Control Register (Address: 05h)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I ² C CH 4	GPIO/I ² C CH 3	GPIO/I ² C CH 2	GPIO/I ² C CH 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Figure 53. Control Register Composition

The lower four bits of the control register dictate if the channels of the device are off (bit set to '0') or on (bit set to '1') during I²C control. The transition from off to on can be made with a single write command to the control register. See Figure 44 for the composition of a single write command.

10.2 Typical Application

10.2.1 Tying Multiple Channels in Parallel

Two or more channels of the device can be tied in parallel for applications that require lower R_{ON} and/or more continuous current. Tying two channels in parallel will result in half of the R_{ON} and two times the I_{MAX} capability. Tying three channels in parallel will result in one-third of the R_{ON} and three times the I_{MAX} capability. Tying four channels in parallel will result in one-fourth of the R_{ON} and four times the I_{MAX} capability. For the channels that are tied in parallel, it is recommended that the ONx pins be tied together for synchronous control of the channels when in GPIO control. In I²C control, all four channels can be enabled or disabled synchronously by writing to the control register of the device. [Figure 54](#) shows an application example of tying all four channels in parallel.

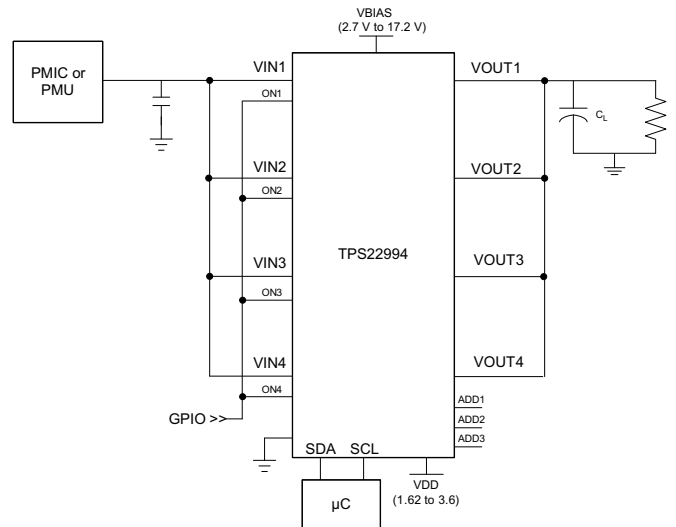


Figure 54. Parallel Channels

10.2.1.1 Design Requirements

Refer to [Design Requirements](#).

10.2.1.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#).

The only difference between single channel and multiple channels in parallel is the resulting R_{ON} and voltage drop from VINx to VOUTx. Thus, the design procedure is identical to [Detailed Design Procedure](#). The VINx to VOUTx voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN conditions of the device. Refer to the R_{ON} specification of the device in the [Electrical Characteristics](#) table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use the following equation to calculate the VINx to VOUTx voltage drop:

$$\Delta V = I_{LOAD} \times (R_{ON}/K) \quad (1)$$

Where:

ΔV = voltage drop from VINx to VOUTx

I_{LOAD} = load current

R_{ON} = On-resistance of the device for a specific V_{IN}

K = number of channels in parallel (2, 3, or 4)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification per channel of the device is not violated.

10.2.1.3 Application Curves

Refer to [Application Curves](#).

Typical Application (continued)

10.2.2 Cold Boot Programming of All Registers

Since the TPS22994 has a digital core with volatile memory, upon power cycle of the VBIAS pin, the registers will revert back to their default values (see register map for default values). Therefore, the application must reprogram the configuration registers, control register, and mode registers if non-default values are desired. The TPS22994 contains 17 programmable registers (4 configuration registers, 1 control register, 12 mode registers) in total.

During cold boot when the microcontroller and the I²C bus is not yet up and running, the channels of the TPS22994 can still be enabled via GPIO control. One method to achieve this is to tie the ONx pin to the respective VINx pin for the channels that need to turn on by default during cold boot. With this method, when VINx is applied to the TPS22994, the channel will be enabled as well. Once the I²C bus is active, the channel can be switched over to I²C control to be disabled. See Figure 55 for an example of how the ONx pins can be tied to VINx for default enable during cold boot.

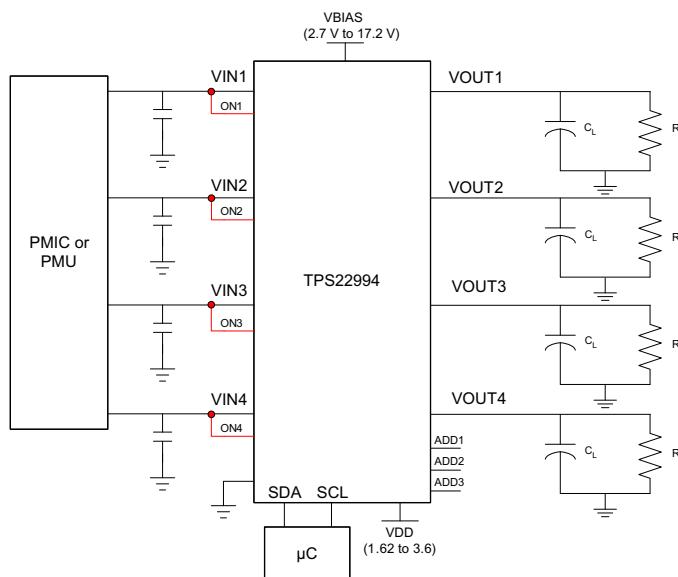


Figure 55. Cold Boot Programming

10.2.2.1 Design Requirements

Refer to [Design Requirements](#).

10.2.2.2 Detailed Design Procedure

Refer to [Design Requirements](#).

10.2.2.3 Application Curves

Refer to [Application Curves](#).

Typical Application (continued)

10.2.3 Power Sequencing Without I²C

It is also possible to power sequence the channels of the device during a cold boot when there is no I²C bus present for control. One method to accomplish this is to tie the VOUT of one channel to the ON pin of the next channel in the sequence. For example, if the desired power up sequence is VOUT3, VOUT1, VOUT2, and VOUT4 (in that order), then the device can be configured for GPIO control as shown in Figure 56. The device will power up with default slew rate, ON-delay, and QOD values as specified in the register map.

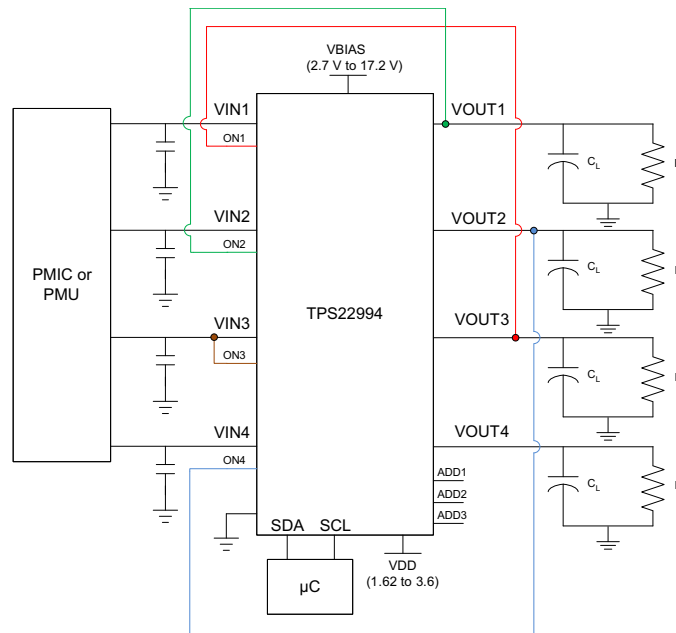


Figure 56. Power Sequencing Without I²C Schematic

10.2.3.1 Design Requirements

10.2.3.1.1 Reading From the Registers

Reading any register from the TPS22994 follows the same standard I²C read protocol as outlined in the I²C Protocol section of this datasheet.

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
V_{INx}	3.3 V
Load Current	1 A

10.2.3.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{INx} voltage
- Load Current

10.2.3.2.1 VIN to VOUT Voltage Drop

The VINx to VOUTx voltage drop in the device is determined by the RON of the device and the load current. The RON of the device depends upon the VIN conditions of the device. Refer to the RON specification of the device in the *Electrical Characteristics* table of this datasheet. Once the RON of the device is determined based upon the VINx conditions, use Equation 2 to calculate the VINx to VOUTx voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \tag{2}$$

Where:

ΔV = voltage drop from VINx to VOUTx

I_{LOAD} = load current

R_{ON} = On-resistance of the device for a specific VIN

An appropriate ILOAD must be chosen such that the IMAX specification of the device is not violated.

10.2.3.2.2 Inrush Current

To determine how much inrush current will be caused by the CL capacitor, use Equation 3:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \tag{3}$$

Where:

IINRUSH = amount of inrush caused by CL

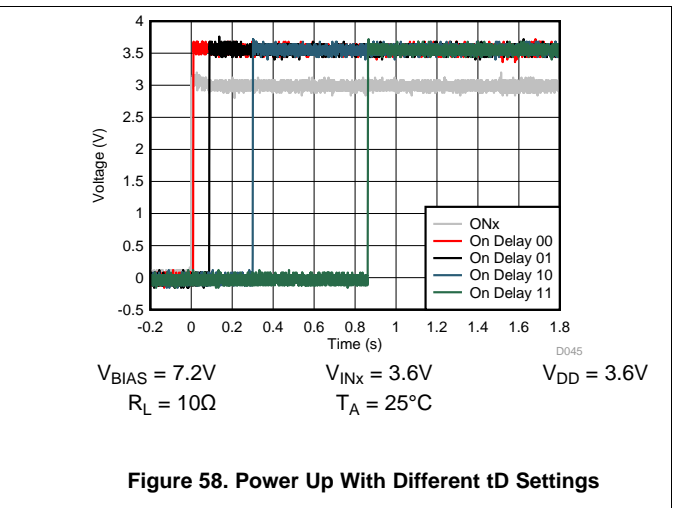
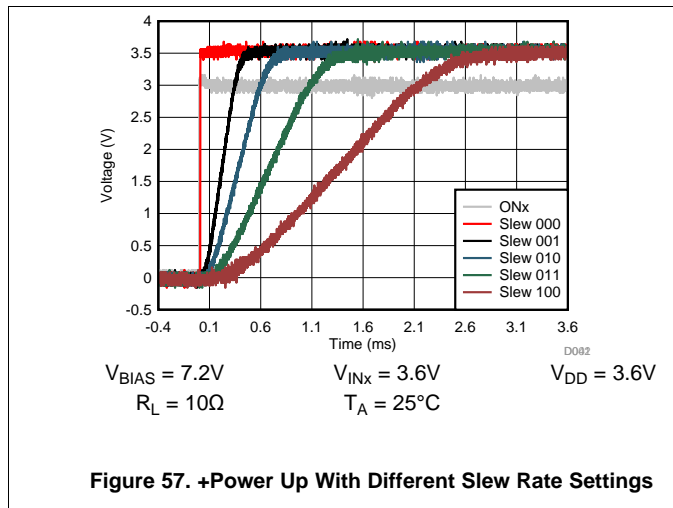
CL = capacitance on VOUTx

dt = rise time in VOUT during the ramp up of VOUTx when the device is enabled

dVOUT = change in VOUT during the ramp up of VOUTx when the device is enabled

An appropriate CL value should be placed on VOUTx such that the IMAX specifications of the device are not violated.

10.2.3.3 Application Curves



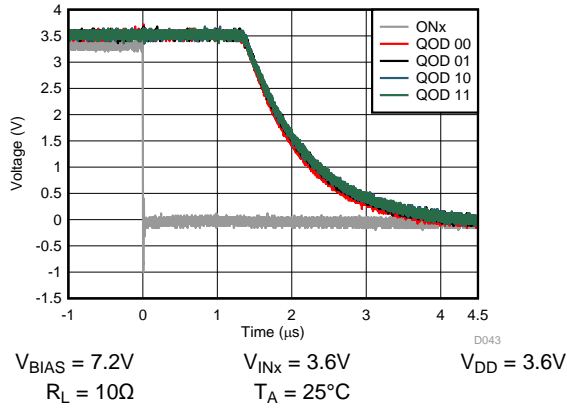


Figure 59. Power Down With Different QOD Settings With $R_L = 10 \Omega$

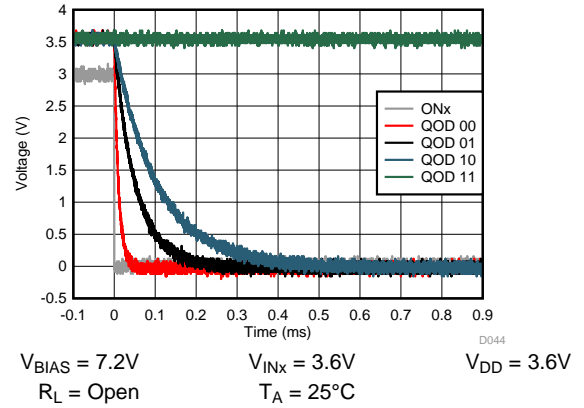


Figure 60. Power Down With Different QOD Settings With $R_L = \text{Open}$

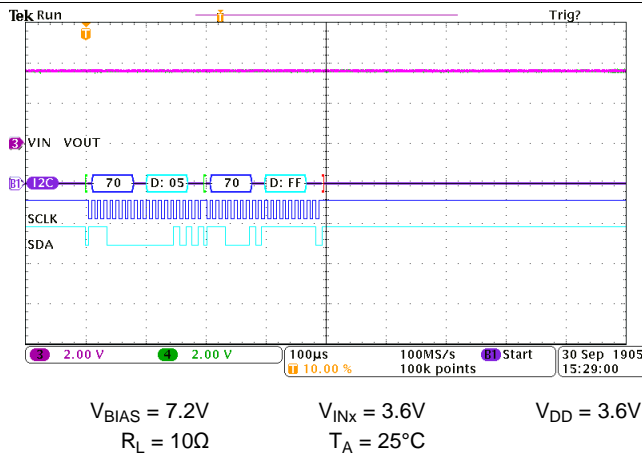
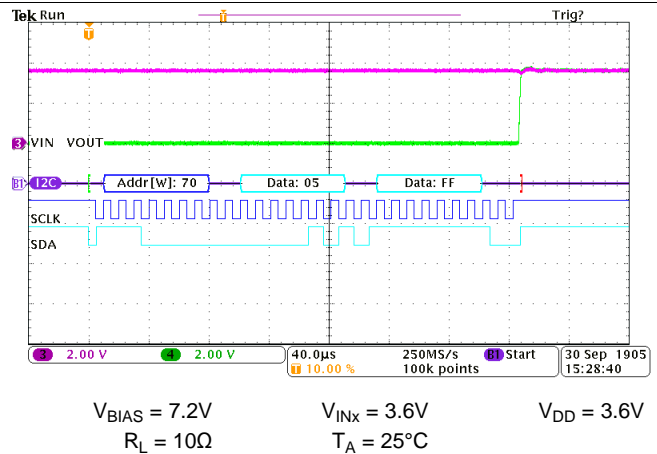


Figure 61. I2C Read Sequence



This example shows the channel of the device being turned on when a I2C "enable" command is written to the register.

Figure 62. I2C Write Sequence

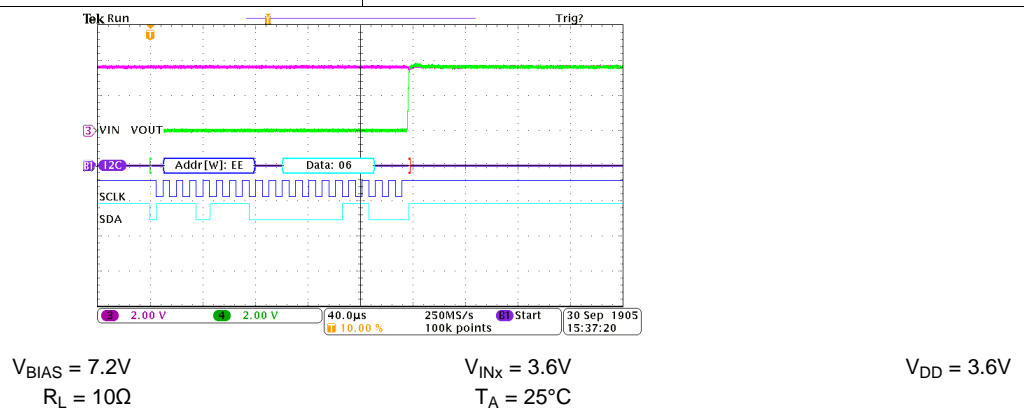


Figure 63. Enabling Channel 1 Across Two TPS22994 Devices With the SwitchALL™ Command

11 Layout

11.1 Board Layout

- VINx and VOUTx traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The VINx terminals should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- The VOUTx terminals should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device terminals as possible.
- The VBIAS terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-μF ceramic with X5R or X7R dielectric.
- The VDD terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-μF ceramic with X5R or X7R dielectric.
- ADDx pins should be tied high to VDD through a pull-up resistor or tied low to GND through a pull-down resistor.

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (4)$$

Where:

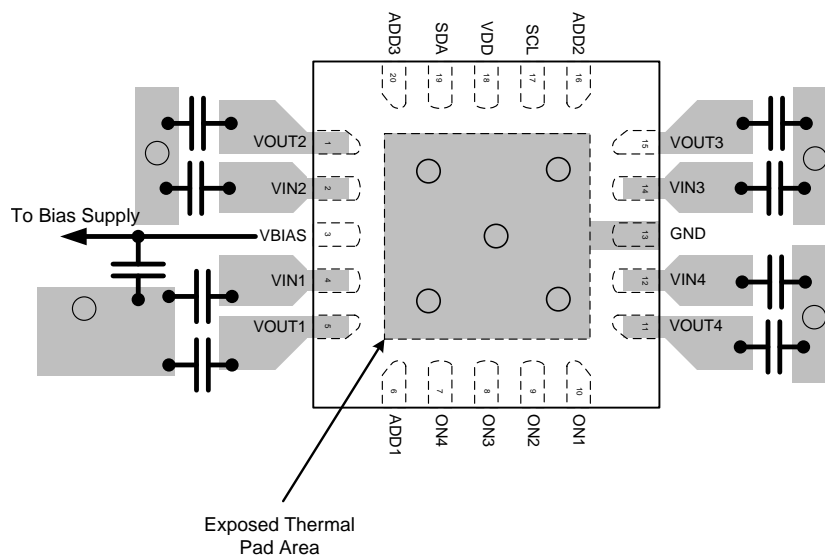
$P_{D(max)}$ = maximum allowable power dissipation

$T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22994)

T_A = ambient temperature of the device

Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout.



12 器件和文档支持

12.1 商标

SwitchALL is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22994RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	22994	Samples
TPS22994RUKT	ACTIVE	WQFN	RUK	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	22994	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22994RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS22994RUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22994RUKR	WQFN	RUK	20	3000	346.0	346.0	33.0
TPS22994RUKT	WQFN	RUK	20	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

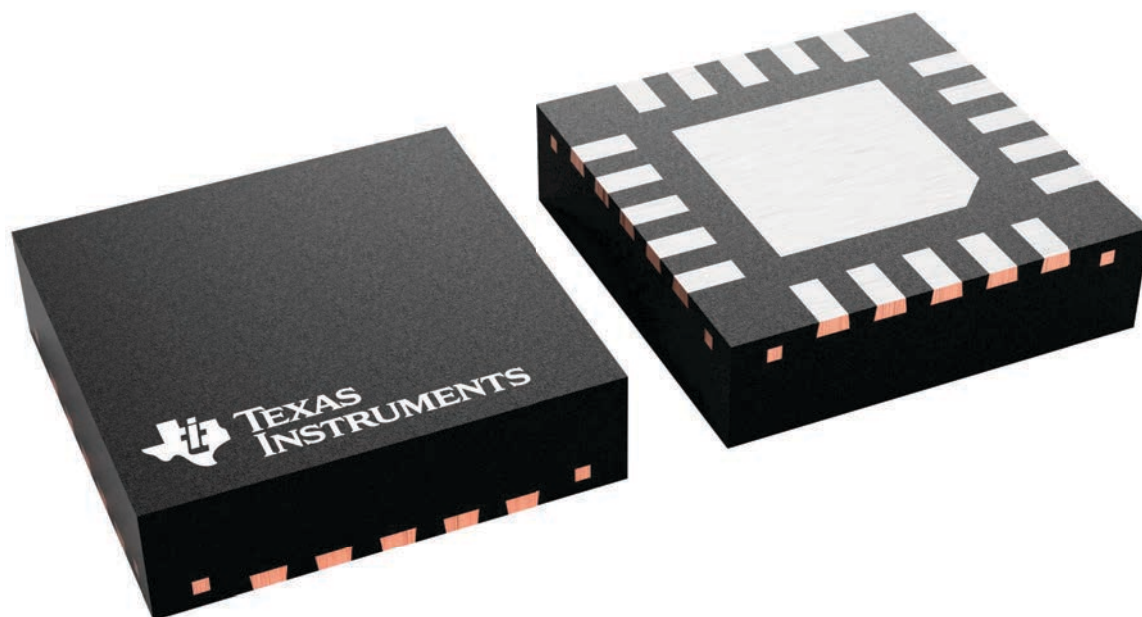
RUK 20

WQFN - 0.8 mm max height

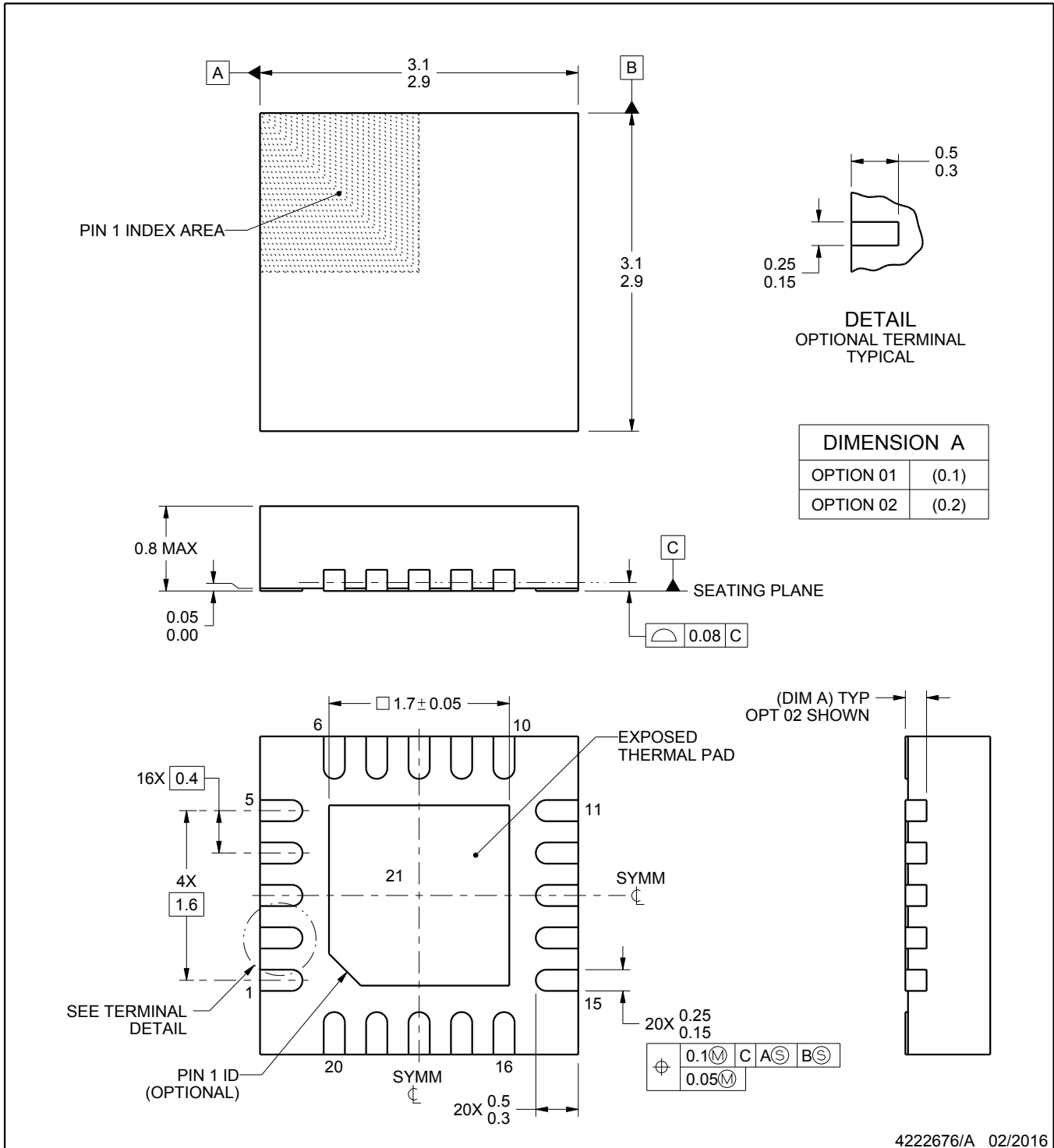
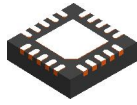
3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229651/A



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NOTES:

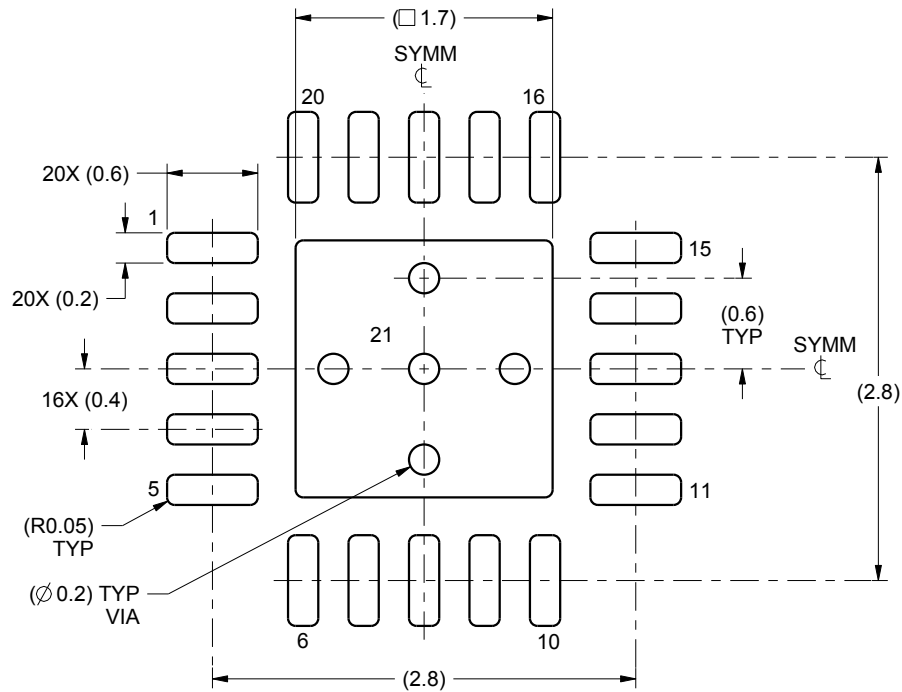
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

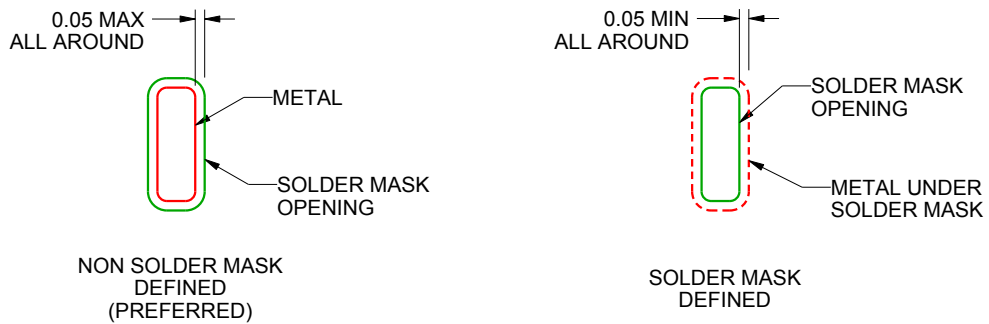
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

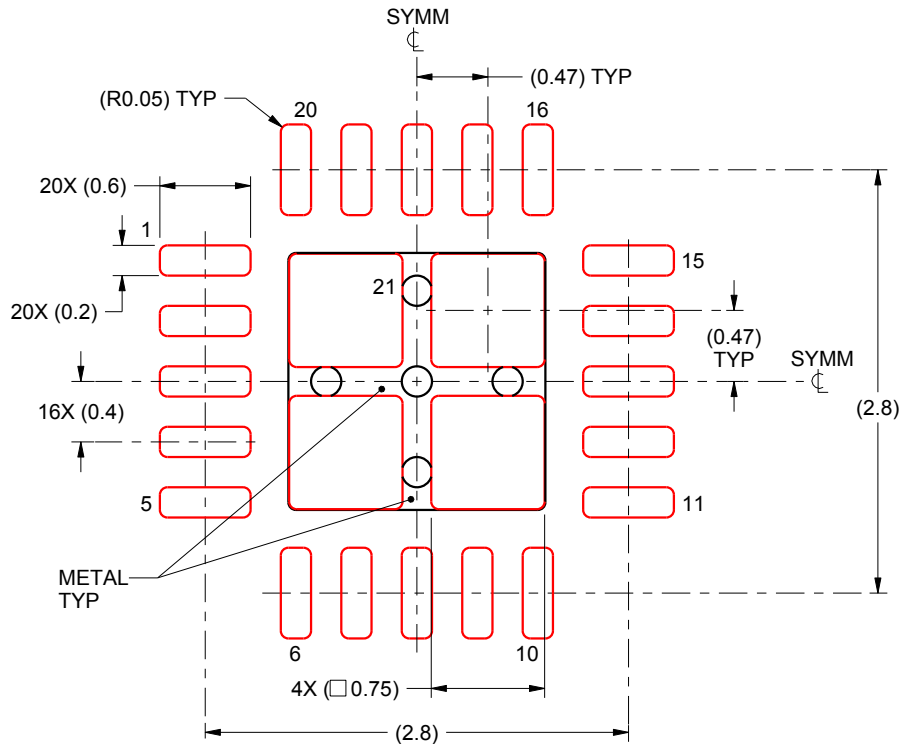
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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