带有集成场效应晶体管 (FET) 的 4A/2A 双通道同步降压转换开关

查询样片: TPS54494

特性

- **D-CAP2™** 控制模式
  - 快速瞬态响应
  - 环路补偿无需外部部件
  - 与陶瓷输出电容器兼容
- 宽输入电压范围：**4.5V** 至 **18V**
- 输出电压范围：**0.76V** 至 **7V**
- 针对低占空比应用对高效集成 **FET** 进行了优化
  - **90mΩ**（高侧）和 **60mΩ**（低侧）
- 高初始基准精度
- **4A CH1 / 2A CH2** 持续负载电流
- 低侧 $r_{DS(on)}$低损失电流感测
- 固定软启动时间：**1ms**
- 非灌入预偏置软启动
- 电源正常 **(Powergood)**
- **700kHz** 开关频率
- 逐周期过流限制控制
- 过流限制 **(OCL) /** 欠压闭锁 **(UVLO) /** 热关断 **(TSD)** 应用
- 用于过载保护的断续定时器
- 带有集成式升压 **P** 通道金属氧化物半导体 **(PMOS)** 开关的自适应栅极驱动器
- 由于热补偿 $r_{DS(on)}$的值为 **4000ppm/**℃，过流保护 **(OCP)** 恒定
- **16** 引脚散热薄型小外形尺寸封装 **(HTSSOP)**，**16** 引脚超薄型四方扁平无引线 **(VQFN)** 封装
- 自动跳跃 **Eco-mode™** 模式，以实现轻负载时的高效率

应用范围

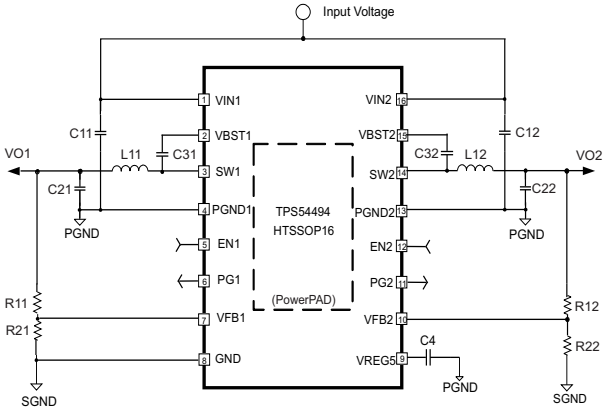
- 针对广泛应用的低功耗系统中的负载点调节
  - 数字电视电源
  - 网络互联家庭终端设备
  - 数字机顶盒 **(STB)**
  - **DVD** 播放器**/**刻录机
  - 游戏控制台和其它设备

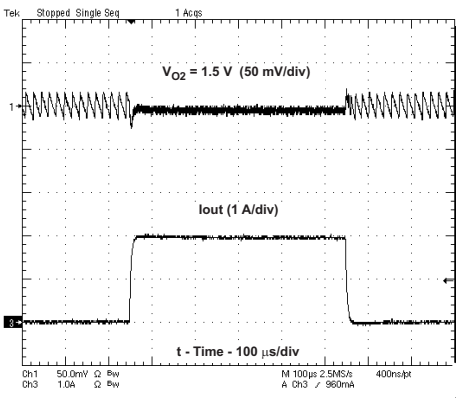
说明

TPS54494 是一款双路、自适应接通时间 D-CAP2™ 模式同步降压转换器。 TPS54494 可帮助系统设计人员通过成本有效性、低组件数量、和低待机电流解决方案来完成多种终端设备的电源总线调节器集。

TPS54494 的主控制环路采用 D-CAP2™ 模式控制，此模式控制无需外部补偿组件即可提供极快的瞬态响应。 自适应接通时间控制支持较高负载状态下的脉宽调制 (PWM) 模式与轻负载下的 Eco-mode™ 工作模式之间的无缝转换。 Eco-mode™ 使 TPS54494 能够在较轻负载条件下保持高效率。 TPS54494 也能够去适应诸如高分子有机半导体固体电容器 (POSCAP) 或者高分子聚合物电容器 (SP-CAP) 的低等效串联电阻 (ESR)，和超低 ESR 陶瓷电容器。 此器件在输入电压为 4.5V 至 18V 之间时提供便捷和有效的运行。

TPS54494 采用 4.4mm x 5mm 16 引脚 TSSOP (PWP) 封装和 4mm x 4mm 16 引脚 VQFN (RSA) 封装，额定环境运行温度范围为 -40°C 至 85°C。





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2, Eco-mode, Eco-Mode are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2) (3)	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY
–40℃ to 85℃	PWP	TPS54494PWPR	16	Tape-and-Reel
		TPS54494PWP		Tube
	RSA	TPS54494RSAR	16	Tape-and-Reel
		TPS54494RSAT		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Input voltage range	VIN1, VIN2, EN1, EN2	–0.3 to 20	V
	VBST1, VBST2	–0.3 to 26	
	VBST1, VBST2 (10ns transient)	–0.3 to 28	
	VBST1–SW1 , VBST2–SW2	–0.3 to 6.5	
	VFB1, VFB2	–0.3 to 6.5	
	SW1, SW2	–2 to 20	
	SW1, SW2 (10ns transient)	–3 to 22	
Output voltage range	VREG5, PG1, PG2	–0.3 to 6.5	V
	PGND1, PGND2	–0.3 to 0.3	
Electrostatic discharge	Human Body Model (HBM)	2	kV
	Charged Device Model (CDM)	500	V
T_A	Operating ambient temperature range	–40 to 85	°C
T_{STG}	Storage temperature range	–55 to 150	°C
T_J	Junction temperature range	–40 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to IC GND terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54494		UNITS
		PWP (16) PINS	RSA (16) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	41.4	32.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	27.8	35.4	
θ_{JB}	Junction-to-board thermal resistance	23.2	9.9	
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.4	
ψ_{JB}	Junction-to-board characterization parameter	23.0	10.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.5	1.6	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告（文献号：ZHCA543）。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			VALUES		UNIT
			MIN	MAX	
	Supply input voltage range	VIN1, VIN2	4.5	18	V
	Input voltage range	VBST1, VBST2	–0.1	24	V
		VBST1, VBST2 (10ns transient)	–0.1	27	
		VBST1–SW1, VBST2–SW2	–0.1	5.7	
		VFB1, VFB2	–0.1	5.7	
		EN1, EN2	–0.1	18	
		SW1, SW2	–1.0	18	
		SW1, SW2 (10ns transient)	–3	21	
	Output voltage range	VREG5, PG1 , PG2	–0.1	5.7	V
		PGND1, PGND2	–0.1	0.1	
		VO1, VO2	0.76	7.0	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating Junction Temperature		–40	150	°C

ELECTRICAL CHARACTERISTICS(1)

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	T_A = 25°C, EN1 = EN2 = 5 V, VFB1 = VFB2 = 0.8 V		1200	2000	µA
I_{VINSDN}	VIN shutdown current	T_A = 25°C, EN1 = EN2 = L after H,		15	20	µA
FEEDBACK VOLTAGE						
$V_{VFBTHLx}$	VFBx threshold voltage	T_A = 25°C, CH1 = 3.3 V, CH2 = 1.5 V	758	765	773	mV
TC_{VFBx}	Temperature coefficient	On the basis of 25°C(2)	–115		115	ppm/°C
I_{VFBx}	VFB Input Current	VFBx = 0.8 V, T_A = 25°C	–0.4	0.2	0.4	µA
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6 V < VIN1 < 18 V, I_{VREG} = 5 mA		5.5		V
I_{VREG5}	Output current	VIN1 = 6 V, VREG5 = 4.0 V, T_A = 25°C(2)		75		mA
MOSFETs						
$r_{DS(on)H}$	High side switch resistance	T_A = 25℃, VBSTx-SWx = 5.5 V (2)		90		mΩ
$r_{DS(on)L}$	Low side switch resistance	T_A = 25℃ (2)		60		mΩ
ON-TIME TIMER CONTROL						
T_{ON1}	SW1 On Time	SW1 = 12 V, VO1 = 1.2 V		165		ns
T_{ON2}	SW2 On Time	SW2 = 12 V, VO2 = 1.2 V		165		ns
T_{OFF1}	SW1 Min off time	T_A = 25℃, VFB1 = 0.7 V(2)		220		ns
T_{OFF2}	SW2 Min off time	T_A = 25℃, VFB2 = 0.7 V(2)		220		ns
SOFT START						
T_{SS}	Soft-start time	Internal soft-start time		1.0		ms

(1) x means either 1 or 2, that is, VFBx means VFB1 or VFB2.
(2) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS(1) (continued)

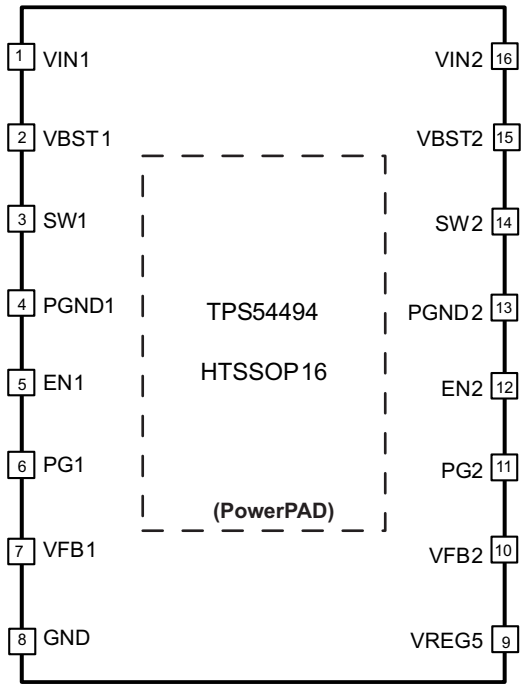
over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
V_{PGTH}	PGx threshold	PG from lower VOx (going high)		84%		
		PG from higher VOx (going low)		116%		
R_{PG}	PGx pull-down resistance	VPGx = 0.5 V	50	75	110	Ω
T_{PGDLY}	PGx delay time	Delay for PGx going high		1.5		ms
		Delay for PGx going low		2		µs
$T_{PGCOMPSS}$	PGx comparator start-up delay	PGx comparator wake-up delay		1.5		ms
UVLO						
V_{UVREG5}	VREG5 UVLO threshold	VREG5 rising		3.83		V
		Hysteresis		0.6		
LOGIC THRESHOLDs						
V_{ENH}	ENx H-level threshold voltage		2.0			V
V_{ENL}	ENx L-level threshold voltage				0.4	V
R_{ENx_IN}	ENx input resistance	ENx = 12 V	225	450	900	kΩ
CURRENT LIMITs						
I_{OCL1}	CH1 Current limit	L_{OUT1} = 2.2 µH(3)	4.5	5.7	7.0	A
I_{OCL2}	CH2 Current limit	L_{OUT2} = 1.5 µH(3)	2.8	3.9	5.0	A
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION (UVP, OVP)						
V_{UVP}	Output UVP trip threshold	measured on VFBx	63%	68%	73%	
T_{UVPDEL}	Output UVP delay time			1.5		ms
T_{UVPEN}	Output UVP enable delay			1.5		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	Shutdown temperature(3)		155		°C
		Hysteresis(3)		25		

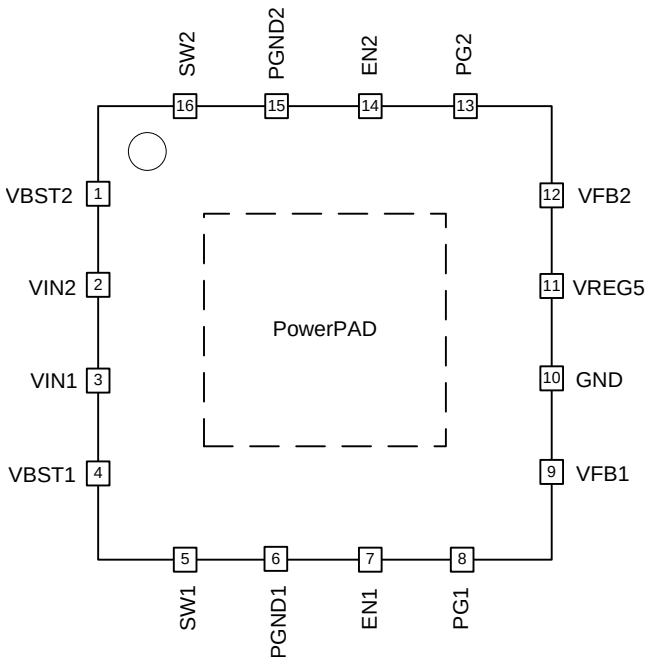
(3) Specified by design. Not production tested.

DEVICE INFORMATION

HTSSOP PACKAGE
(TOP VIEW)



RSA PACKAGE
(TOP VIEW)

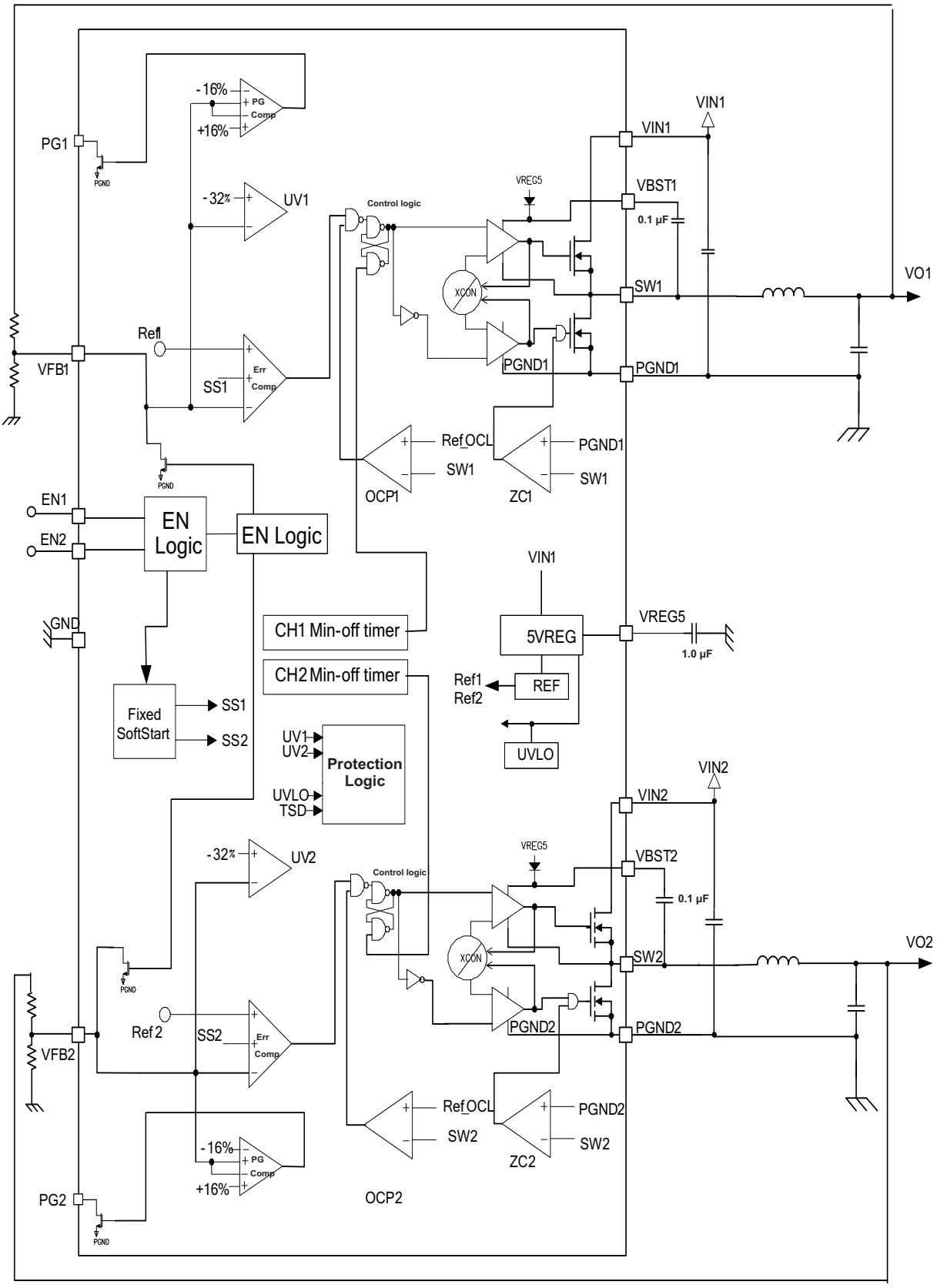


PIN FUNCTIONS(1)

PIN			I/O	DESCRIPTION
NAME	PWP	RSA		
VIN1	1	3	I	Power inputs and connects to both high side NFET drains. Supply Input for 5.5V linear regulator.
VIN2	16	2	I	
VBST1,	2	4	I	Supply input for high-side NFET gate drive circuit. Connect 0.1µF ceramic capacitor between VBSTx and SWx pins. An internal diode is connected between VREG5 and VBSTx
VBST2	15	1	I	
SW1	3	5	I/O	Switch node connections for both the high-side NFETs and low–side NFETs. Input of current comparator.
SW2	14	16	I/O	
PGND1	4	6	I/O	Ground returns for low-side MOSFETs. Input of current comparator.
PGND2	13	15	I/O	
EN1	5	7	I	Enable. Pull High to enable according converter.
EN2	12	14	I	
PG1	6	8	O	Open drain power good outputs. Low indicates the corresponding output voltage is out of regulation.
PG2	11	13	O	
VFB1	7	9	I	D-CAP2 feedback inputs. Connect to output voltage with resistor divider.
VFB2	10	12	I	
GND	8	10	I/O	Signal GND. Connect sensitive SSx and VFBx returns to GND at a single point.
VREG5	9	11	O	Output of 5.5V linear regulator. Bypass to GND with a high-quality ceramic capacitor of at least 1 µF. VREG5 is active when ENx is high.
Exposed Thermal Pad	Back side	Back side	I/O	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

(1) x means either 1 or 2, that is, VFBx means VFB1 or VFB2.

FUNCTIONAL BLOCK DIAGRAM



OVERVIEW

The TPS54494 is a 4A/2A dual synchronous step-down (buck) converter with two integrated N-channel MOSFETs for each channel. It operates using D-CAP2™ control mode. The fast transient response of D-CAP2™ control reduces the required output capacitance to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54494 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ control mode. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter's input voltage, VINx, and the output voltage, VOx, to maintain a pseudo-fixed frequency over the input voltage range hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output voltage ripple, eliminating the need for ESR induced output ripple from D-CAP™ control.

PWM Frequency and Adaptive On-Time Control

TPS54494 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54494 runs with a pseudo-fixed frequency of 700 kHz by using the input voltage and output voltage to set the on-time timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOx/VINx, the frequency is constant.

Auto-Skip Eco-Mode™ Control

The TPS54494 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current also reduces and eventually comes to the point where its ripple valley touches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode because it takes longer to discharge the output capacitor with smaller load current to the nominal output voltage. The transition point to the light load operation $I_{Ox(LL)}$ current can be estimated with Equation 1with 700-kHz used as f_{SW}.

$$I_{Ox(LL)} = \frac{1}{2 \times L1x \times f_{SW}} \times \frac{(V_{INx} - V_{Ox}) \times V_{Ox}}{V_{INx}} \quad (1)$$

Soft Start and Pre-Biased Soft Start

The TPS54494 has an internal, 1.0ms, soft-start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up.

The TPS54494 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than internal feedback voltage, VFBx), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-biased output, and ensures that the output voltage (VOx) starts and ramps up smoothly into regulation from pre-biased startup to normal mode operation.

POWERGOOD

The TPS54494 has power-good outputs that are measured on VFBx. The power-good function is activated after the soft-start has finished. If the output voltage is within 16% of the target voltage, the internal comparator detects the power good state and the power good signal becomes high after 1.5ms delay. During start-up, this internal delay starts after 1.5ms of the UVP Enable delay time to avoid a glitch of the power-good signal. If the feedback voltage goes outside of ±16% of the target value, the power-good signal becomes low after 2µs.

Current Sensing and Over-Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detection control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SWx and PGNDx pins. This voltage is proportional to the switch current and the on-resistance of the FET. To improve the measurement accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by VINx, VOx, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUTx}. If the sensed voltage on the low-side FET is above the voltage proportional to the current limit, the converter keeps the low-side switch on until the measured voltage falls below the voltage corresponding to the current limit and a new switching cycle begins. In subsequent switching cycles, the on-time is set to the value determined for CCM and the current is monitored in the same manner.

Important considerations for this type of over-current protection: The load current is one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

Undervoltage Protection and Hiccup Mode

Hiccup mode of operation protects the power supply from being damaged during an over-current fault condition. If the OCL comparator circuit detects an over-current event the output voltage falls. When the feedback voltage falls below 68% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After counting UVP delay time, the TPS54494 shuts off the power supply for a given time (7x UVP Enable Delay Time) and then tries to re-start the power supply. If the over-load condition has been removed, the power supply starts and operates normally; otherwise, the TPS54494 detects another over-current event and shuts off the power supply again, repeating the previous cycle. Excess heat due to overload lasts for only a short duration in the hiccup cycle, therefore the junction temperature of the power device is much lower.

UVLO Protection

Under-voltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than the UVLO threshold, the TPS54494 shuts down. As soon as the voltage increases above the UVLO threshold, the converter starts again.

Thermal Shutdown

TPS54494 monitors its temperature. If the temperature exceeds the threshold value (typically 155°C), the device shuts down. When the temperature falls below the threshold, the IC starts again.

When VIN1 starts up and VREG5 output voltage is below its nominal value, the thermal shutdown threshold is lower than 155°C. As long as VIN1 rises, T_J must be kept below 110°C.

TYPICAL CHARACTERISTICS

One output is enabled unless otherwise noted. $V_{IN} = V_{IN1}$ or V_{IN2}. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

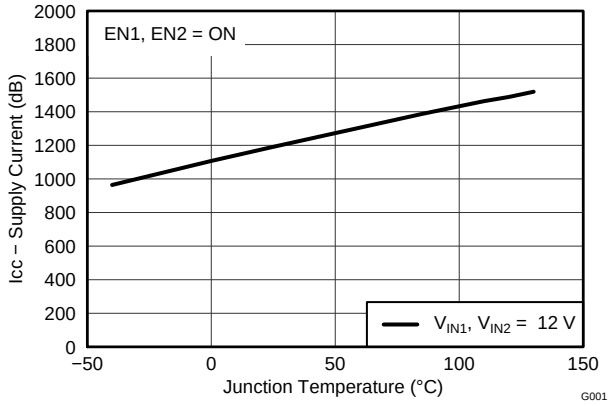


Figure 1. Input Current vs Junction Temperature

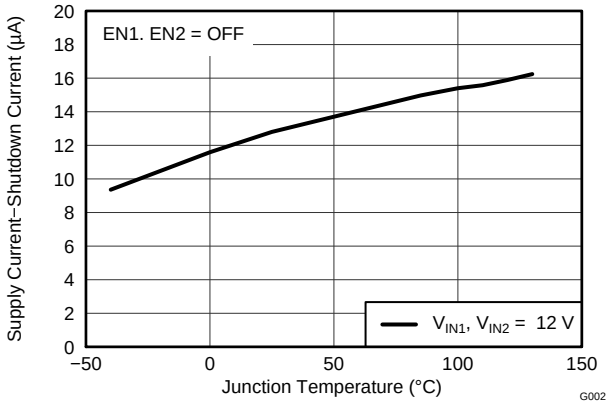


Figure 2. Input Shutdown Current vs Junction Temperature

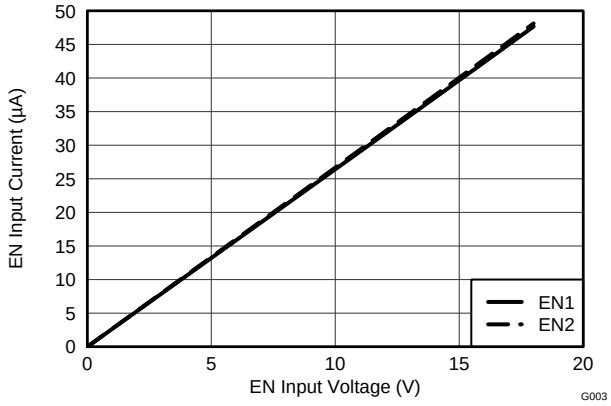


Figure 3. EN Current vs EN Voltage (VEN=12V)

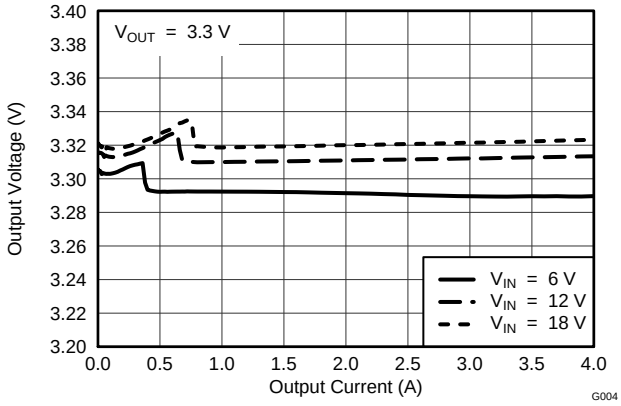


Figure 4. VO1=3.3V Output Voltage vs Output Current

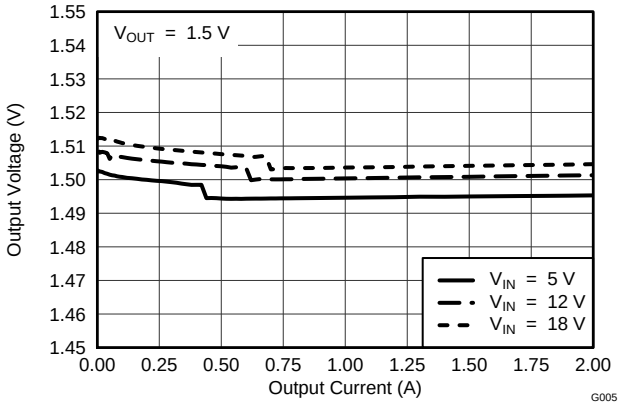


Figure 5. VO2=1.5V Output Voltage vs Output Current

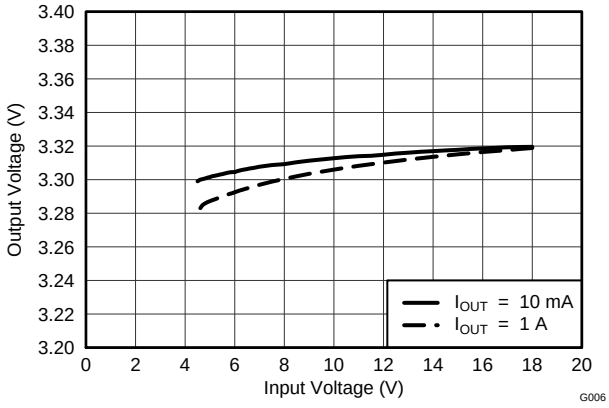


Figure 6. VO1=3.3V Output Voltage vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

One output is enabled unless otherwise noted. $V_{IN} = V_{IN1}$ or V_{IN2}. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

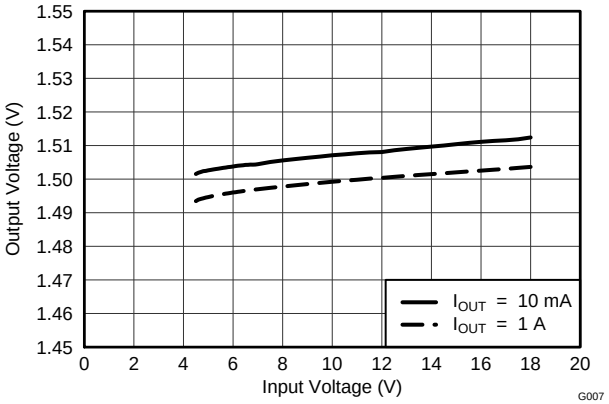


Figure 7. VO2=1.5V Output Voltage vs Input Voltage

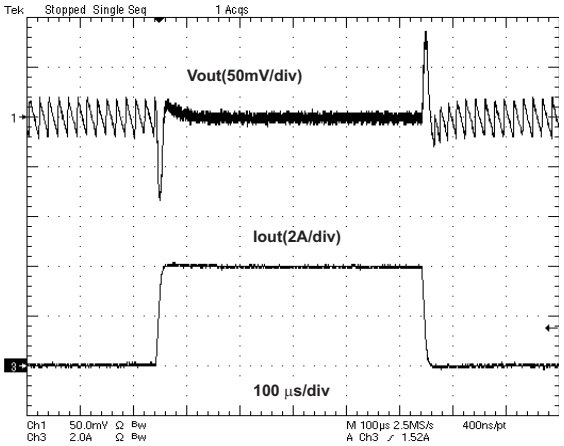


Figure 8. VO1=3.3V, 0 A to 4 A Load Transient Response

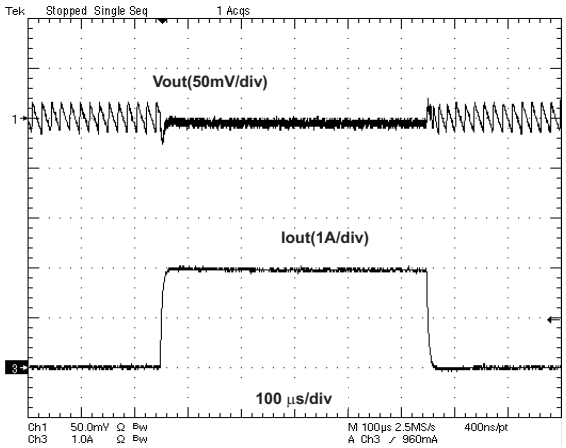


Figure 9. VO2=1.5V, 0 A to 2 A Load Transient Response

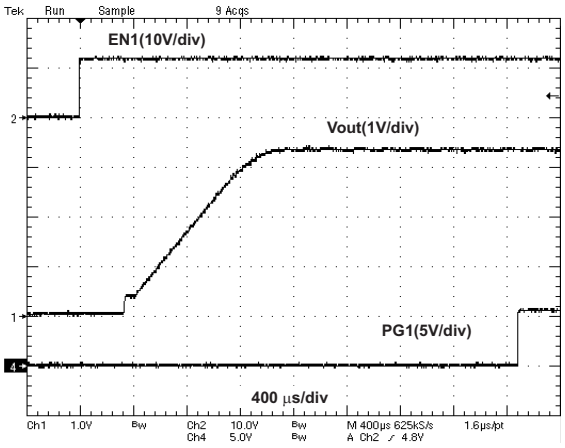


Figure 10. VO1=3.3V, PG1

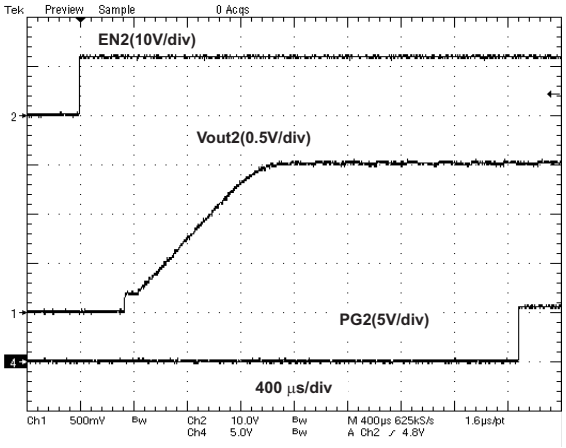


Figure 11. VO2=1.5V, PG2

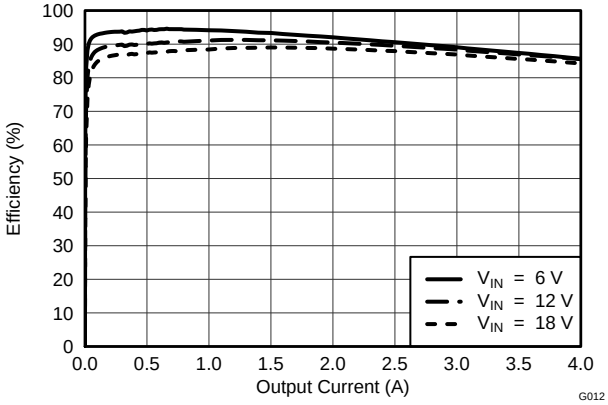


Figure 12. VO1=3.3V, Efficiency vs Output Current

TYPICAL CHARACTERISTICS (continued)

One output is enabled unless otherwise noted. $V_{IN} = V_{IN1}$ or V_{IN2}. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

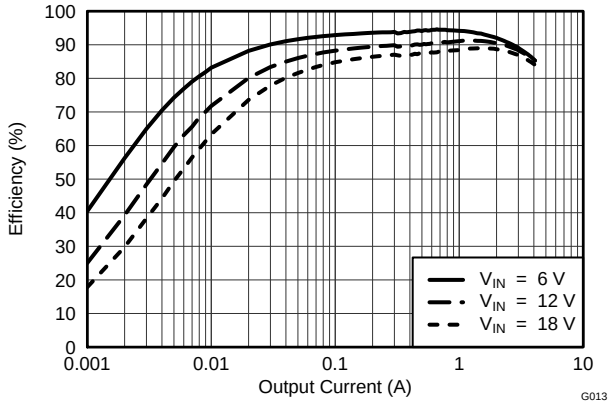


Figure 13. VO1=1.5V, Efficiency vs Output Current

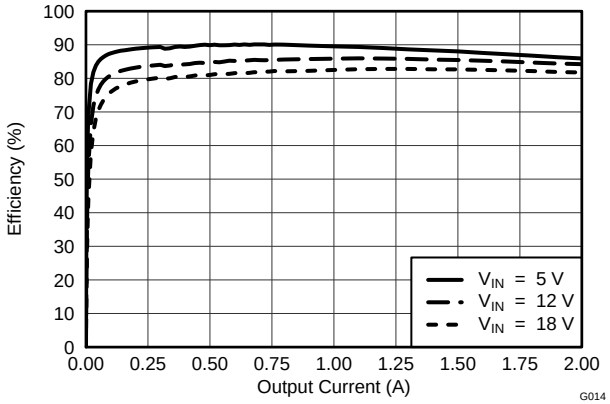


Figure 14. VO1=3.3V, Efficiency vs Output Current

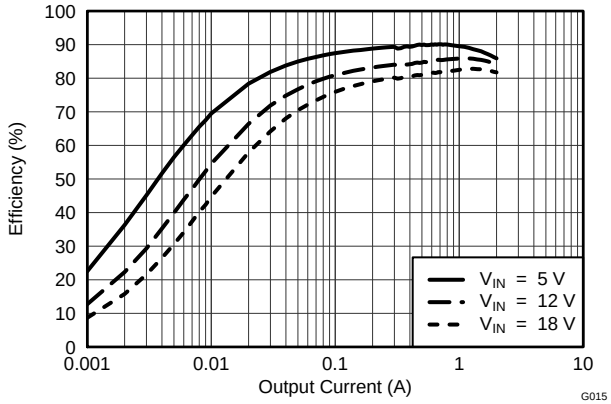


Figure 15. VO2=1.5V, Efficiency vs Output Current

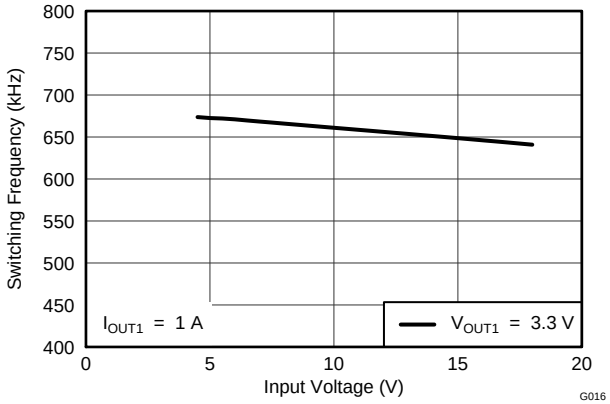


Figure 16. VO1=3.3V, SW-frequency vs Input Voltage

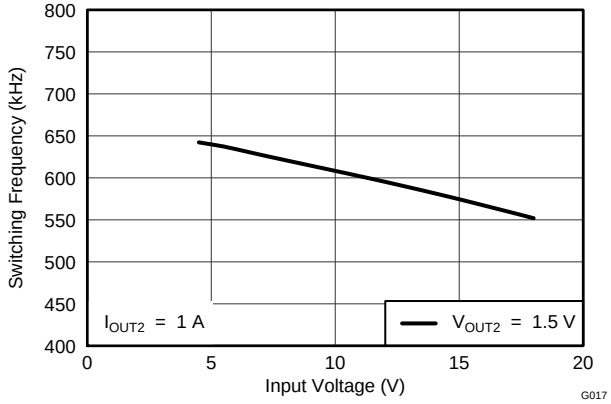


Figure 17. VO2=1.5V, SW-frequency vs Input Voltage

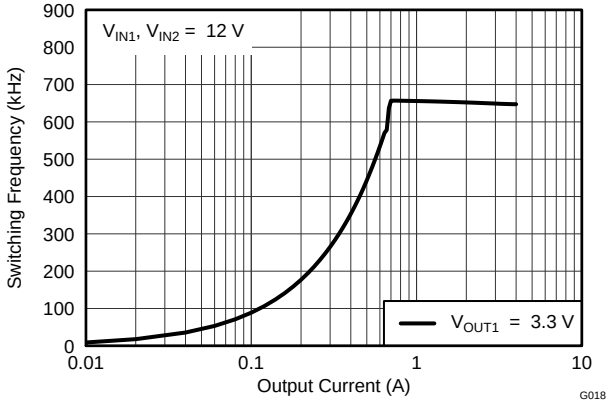


Figure 18. VO1=3.3V, SW-frequency vs Output Current

TYPICAL CHARACTERISTICS (continued)

One output is enabled unless otherwise noted. $V_{IN} = V_{IN1}$ or V_{IN2}. V_{IN} = 12 V, T_A = 25°C (unless otherwise noted).

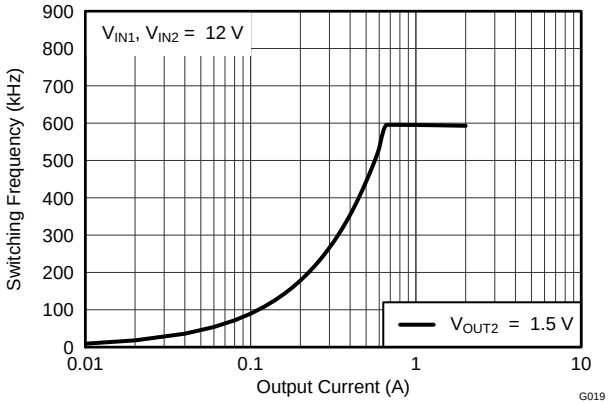


Figure 19. VO2=1.5V, SW-frequency vs Output Current

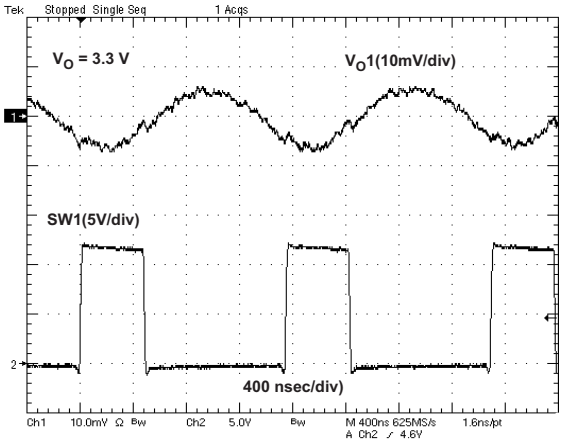


Figure 20. VO1=3.3V, VO1 Ripple Voltage (I_{O1}= 4 A)

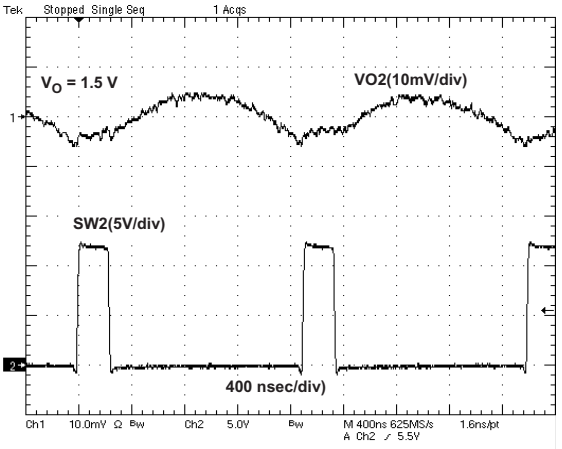


Figure 21. VO2=1.5V, Ripple Voltage (I_{O2}= 2 A)

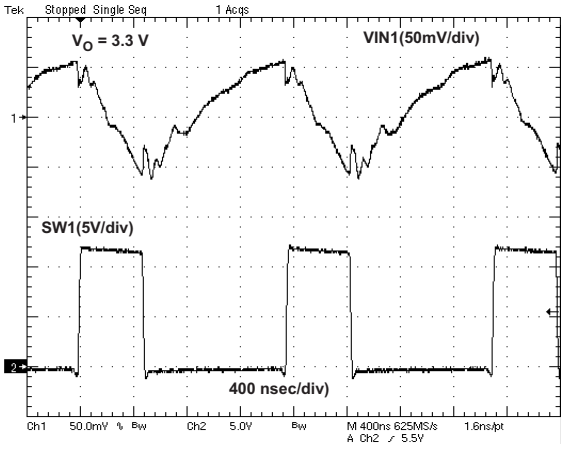


Figure 22. VIN1 Input Voltage Ripple (I_{O1}= 4 A)

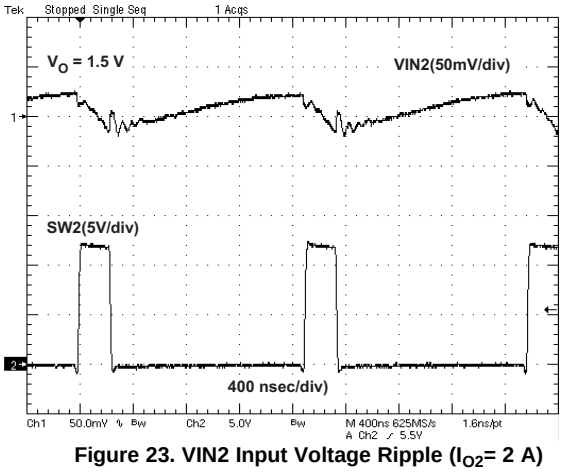


Figure 23. VIN2 Input Voltage Ripple (I_{O2}= 2 A)

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current

In all formulas x is used to indicate that they are valid for both converters. For the calculations the estimated switching frequency of 700 kHz is used.

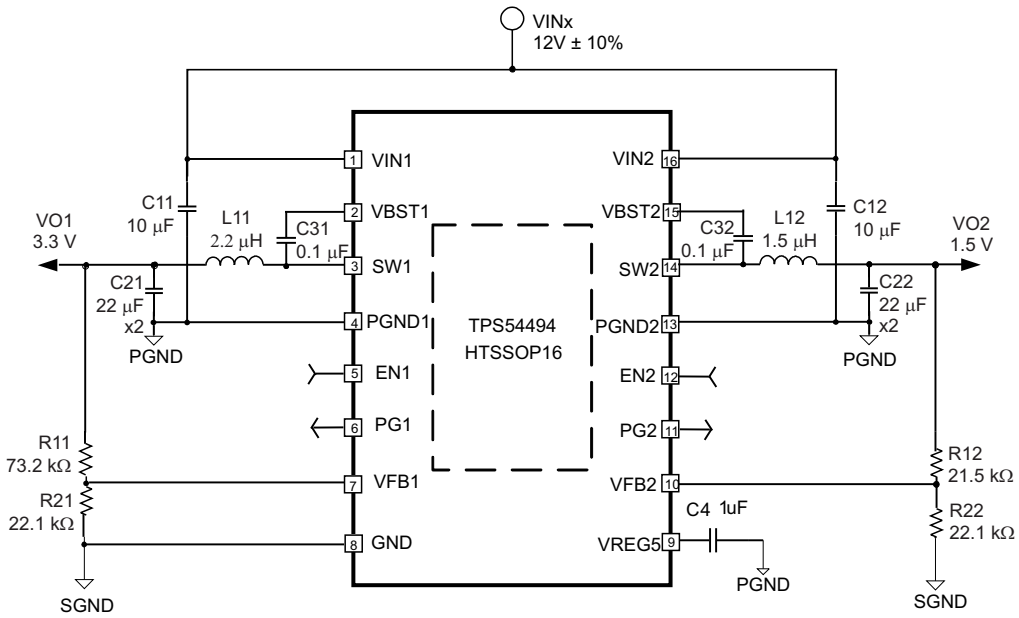


Figure 24. Schematic Diagram for the Design Example

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFBx pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate V_{Ox}.

To improve the efficiency at very light loads consider using larger value resistors, but too high resistance values will be more susceptible to noise and voltage errors due to the VFBx input current will be more noticeable.

$$V_{Ox} = 0.765\ V \times \left(1 + \frac{R1x}{R2x}\right) \quad (2)$$

Output Filter Selection

The output filter used with the TPS54494 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS545494. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

Table 1. Recommended Component Values

OUTPUT VOLTAGE (V)	R1x (kΩ)	R2x (kΩ)	Cffx (pF)(1)	L1x (µH)	C2x (µF)
1	6.81	22.1		1.5 - 2.2	20 - 68
1.05	8.25	22.1		1.5 - 2.2	20 - 68
1.2	12.7	22.1		1.5 - 2.2	20 - 68
1.5	21.5	22.1		1.5 - 2.2	20 - 68
1.8	30.1	22.1	5 - 22	2.2 - 3.3	20 - 68
2.5	49.9	22.1	5 - 22	2.2 - 3.3	20 - 68
3.3	73.2	22.1	5 - 22	2.2 - 3.3	20 - 68
5	124	22.1	5 - 22	4.7	20 - 68
6.5	165	22.1	5 - 22	4.7	20 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (Cff) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

For the calculations, use 700 kHz as the switching frequency, f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$\Delta I_{L1x} = \frac{V_{Ox}}{V_{INx(MAX)}} \times \frac{V_{INx(MAX)} - V_{Ox}}{L1x \times f_{SW}} \quad (4)$$

$$I_{Lpeakx} = I_{Ox} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_{LOx(RMS)} = \sqrt{I_{Ox}^2 + \frac{1}{12}\Delta I_L^2} \quad (6)$$

For the above design example, the calculated peak current is 4.46 A and the calculated RMS current is 4.01 A for VO1. The inductor used is a TDK CLF7045-2R2N with a rated current of 5.5 A based on the inductance change and of 4.3 A based on the temperature rise.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54494 is intended for use with ceramic or other low ESR capacitors. The recommended value range is from 20µF to 68µF. Use Equation 7 to determine the required RMS current rating for the output capacitor(s).

$$I_{COx(RMS)} = \frac{V_{Ox} \times (V_{INx} - V_{Ox})}{\sqrt{12} \times V_{INx} \times L_{Ox} \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.19A and each output capacitor is rated for 4A.

Input Capacitor Selection

The TPS54494 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor of or above 10µF is recommended for the decoupling capacitor. Additionally, 0.1 µF ceramic capacitors from pin 1 and Pin 16 to ground are recommended to improve the stability and reduce the SWx node overshoots. The capacitors voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitors must be connected between the VBSTx and SWx pins for proper operation. It is recommended to use ceramic capacitors with a dielectric of X5R or better.

VREG5 Capacitor Selection

A 1 µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. It is recommended to use a ceramic capacitor with a dielectric of X5R or better.

Thermal Information

This 16-pin PWP package incorporates an exposed thermal pad. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB is used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to the Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

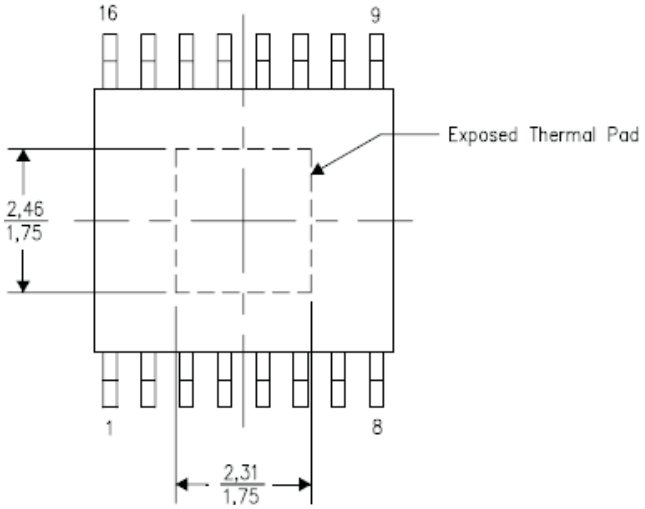
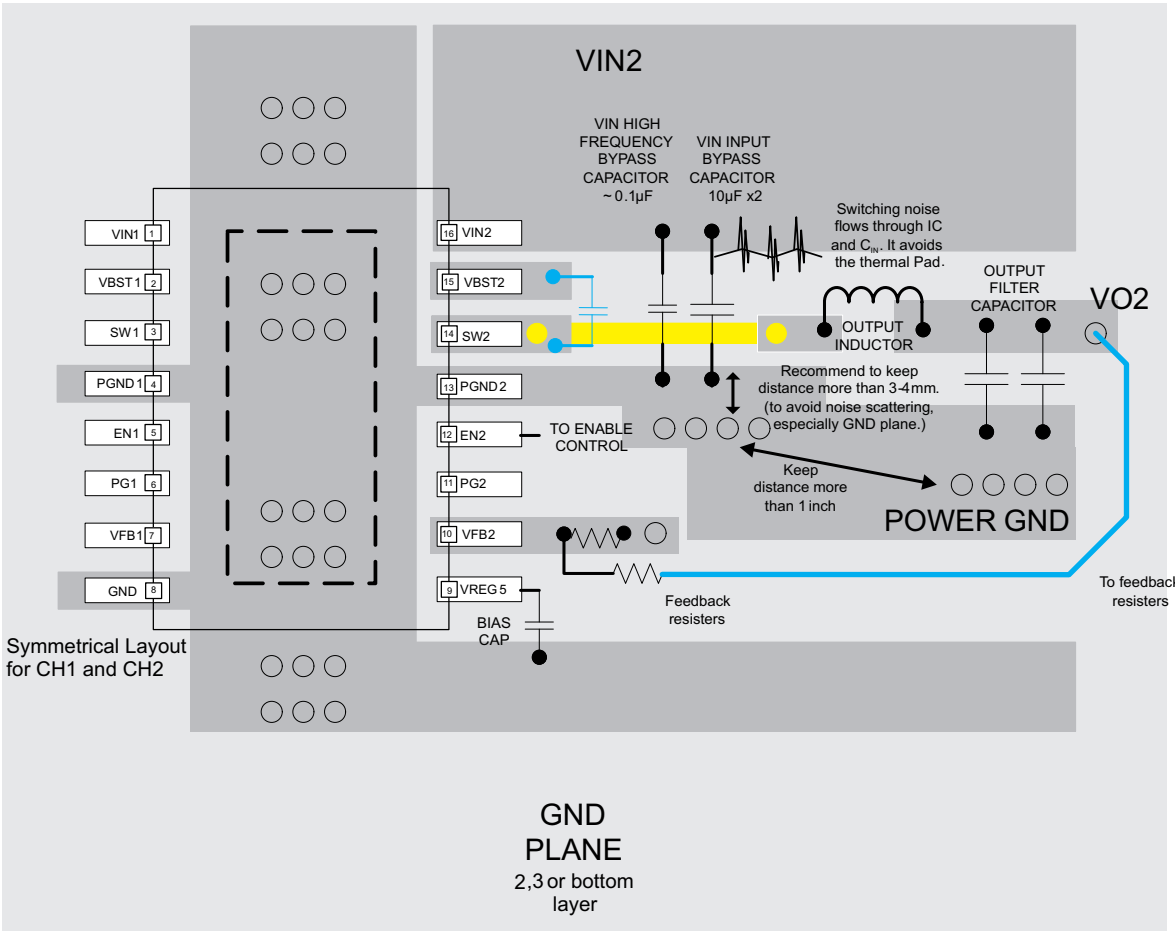


Figure 25. Thermal Pad Dimensions

Layout Considerations

1. Keep the input current loop as small as possible. And avoid the input switching current through the thermal pad.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching currents to flow under the device.
6. Keep the pattern lines for VINx and PGNDx broad.

7. Exposed pad of device must be soldered to PGND.
8. VREG5 capacitor should be placed near the device, and connected to GND.
9. Output capacitors should be connected with a broad pattern to the PGND.
10. Voltage feedback loops should be as short as possible, and preferably with ground shields.
11. Kelvin connections should be brought from the output to the feedback pin of the device.
12. Providing sufficient vias is preferable for VIN, SW and PGND connections.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. VIN Capacitor should be placed as near as possible to the device.



○ **Via to GND Plane**

- Blue parts can be placed on the bottom side

- Connect the SWx pins through another layer with the inductor (yellow line)

Figure 26. TPS54494 Layout

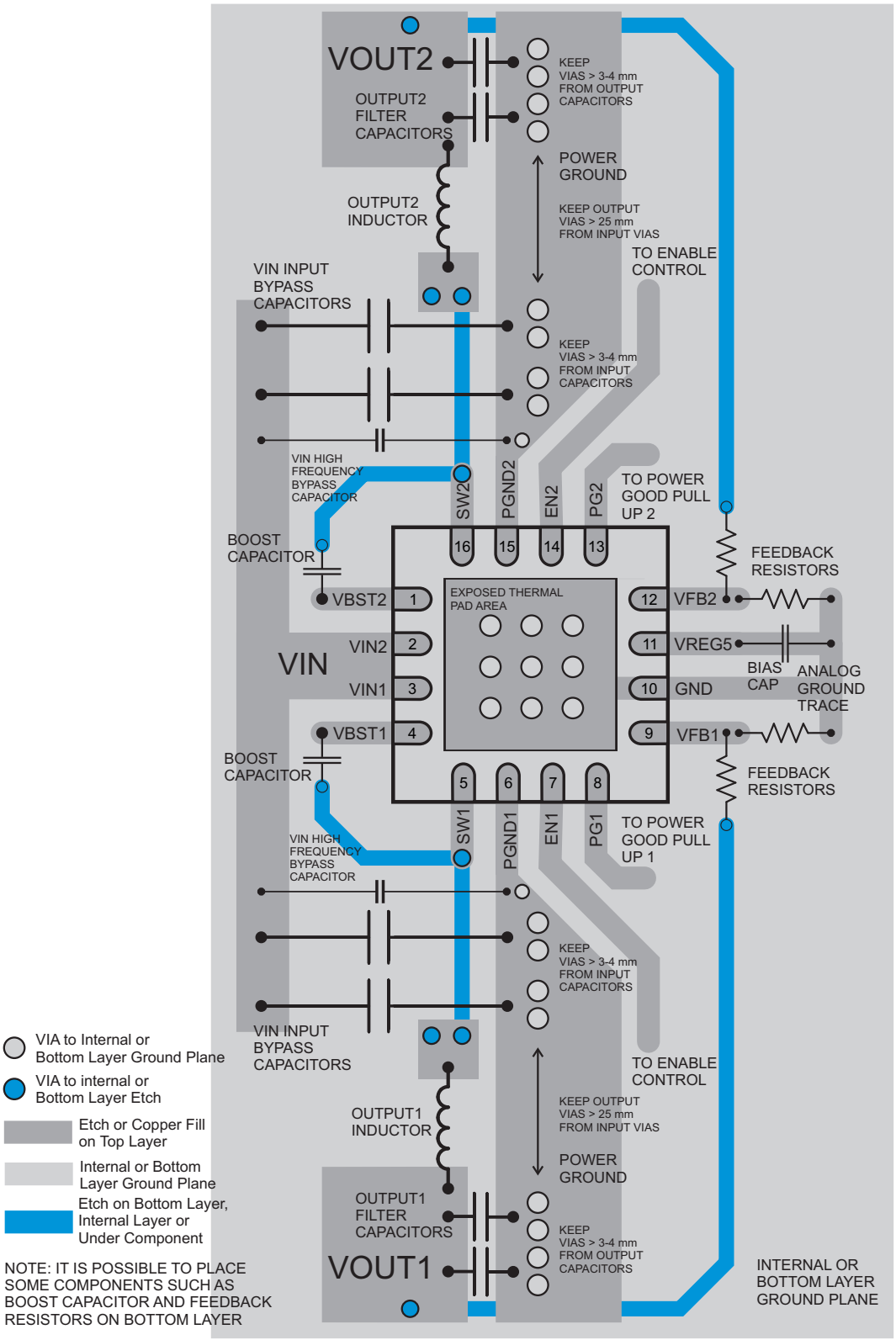


Figure 27. RSA Package Layout

REVISION HISTORY

Changes from Original (June 2012) to Revision A	Page
• 已在特性和说明中添加 16 引脚 VQFN 封装	1
• Added the RSA 16 pin package to the Ordering Information table	2
• Added the RSA package to the Thermal Information table	2
• Added the RSA 16 pin package pinout image, pin names and functions to the Device Information Section	5
• Added Figure 27	17

Changes from Revision A (May 2013) to Revision B	Page
• Change text in the Auto-Skip Eco-Mode™ Control section From: "The on-time is kept almost half as it was in the continuous..." To: "The on-time is kept almost the same as it was in the continuous..."	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54494PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54494	Samples
TPS54494PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54494	Samples
TPS54494RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54494	Samples
TPS54494RSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54494	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

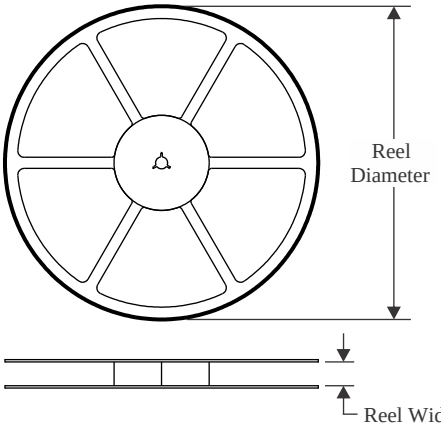
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

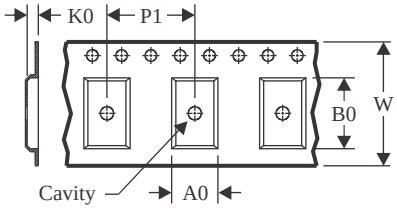
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

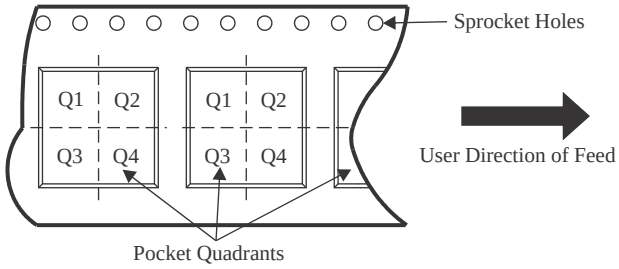


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

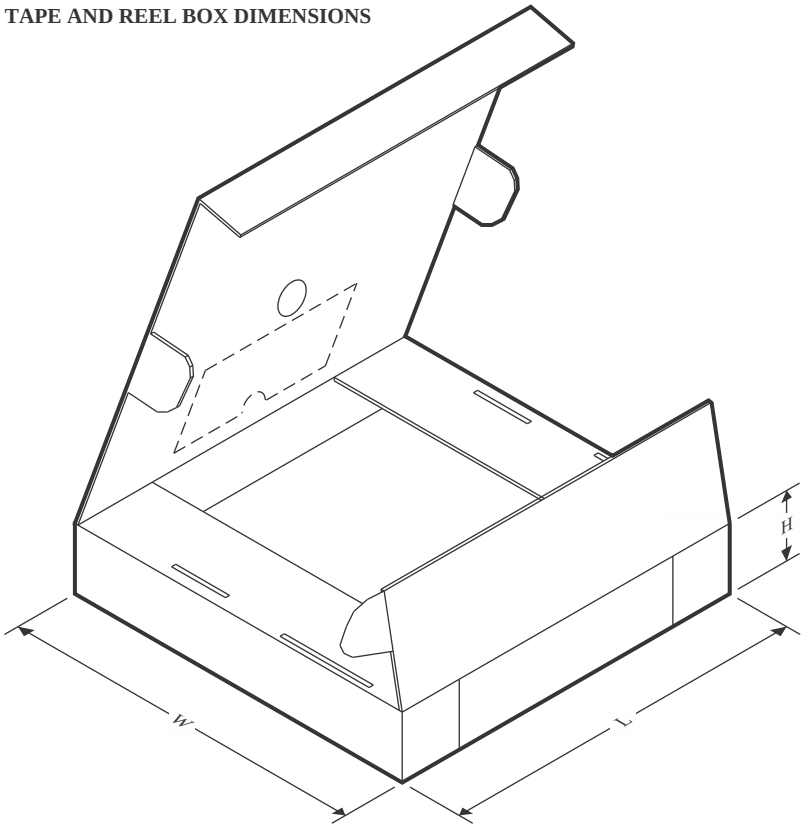
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54494PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54494RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54494RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

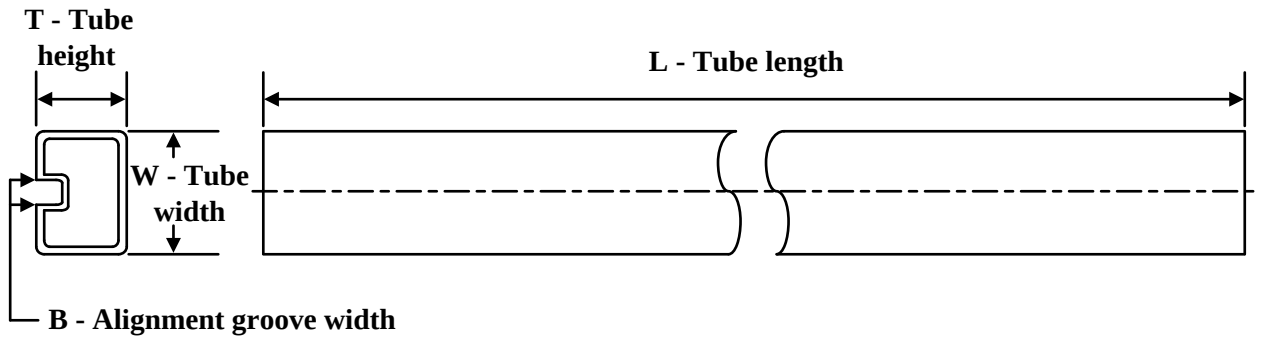
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54494PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS54494RSAR	QFN	RSA	16	3000	346.0	346.0	33.0
TPS54494RSAT	QFN	RSA	16	250	182.0	182.0	20.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54494PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

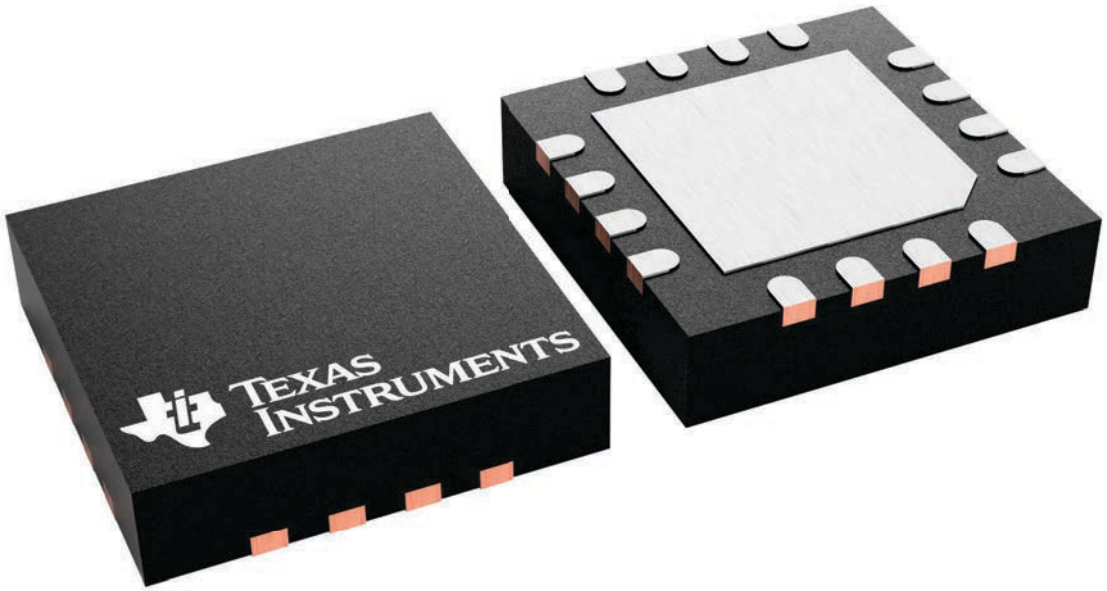
RSA 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

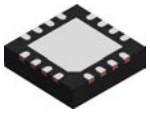
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230969/A

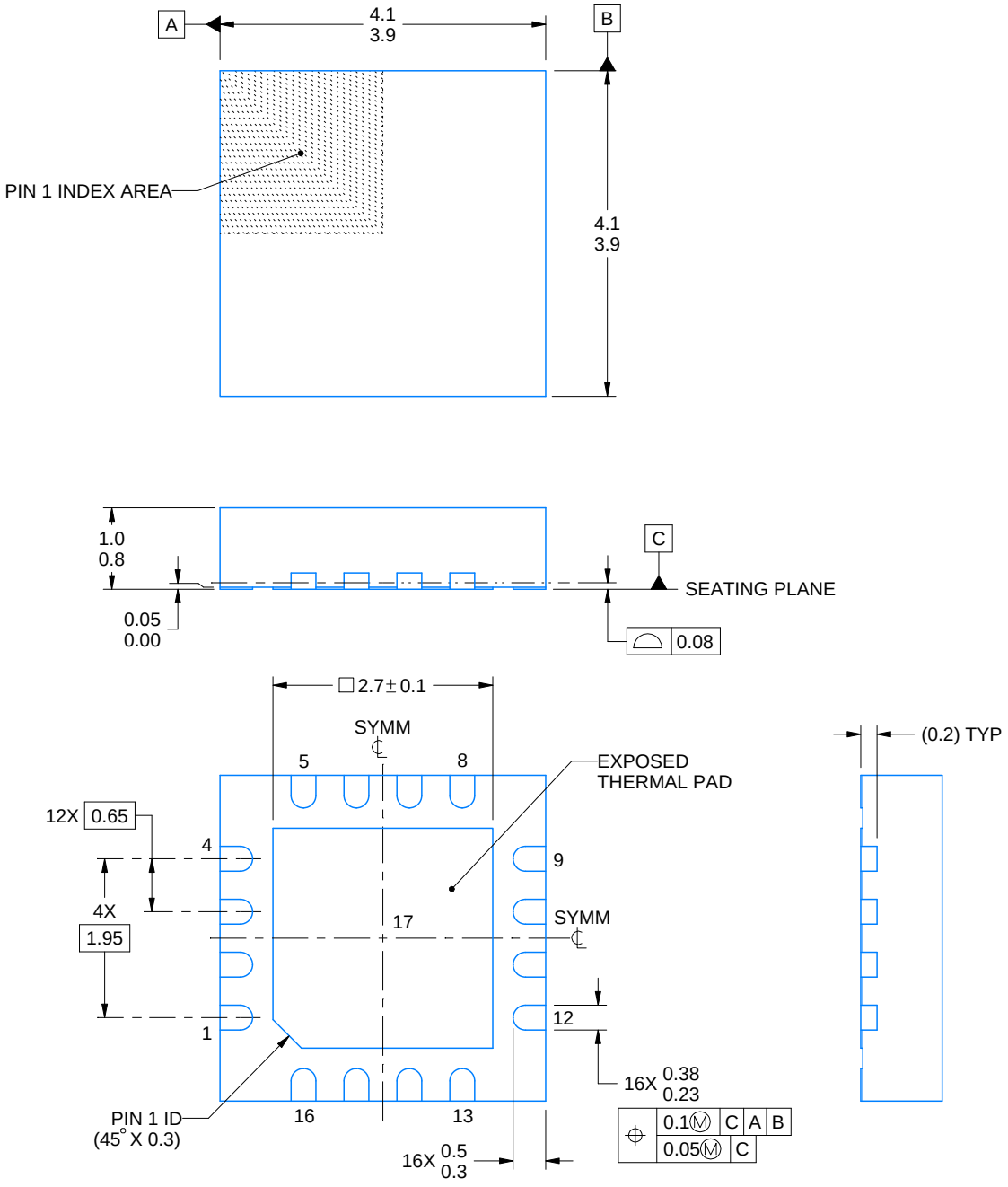
RSA0016B



PACKAGE OUTLINE

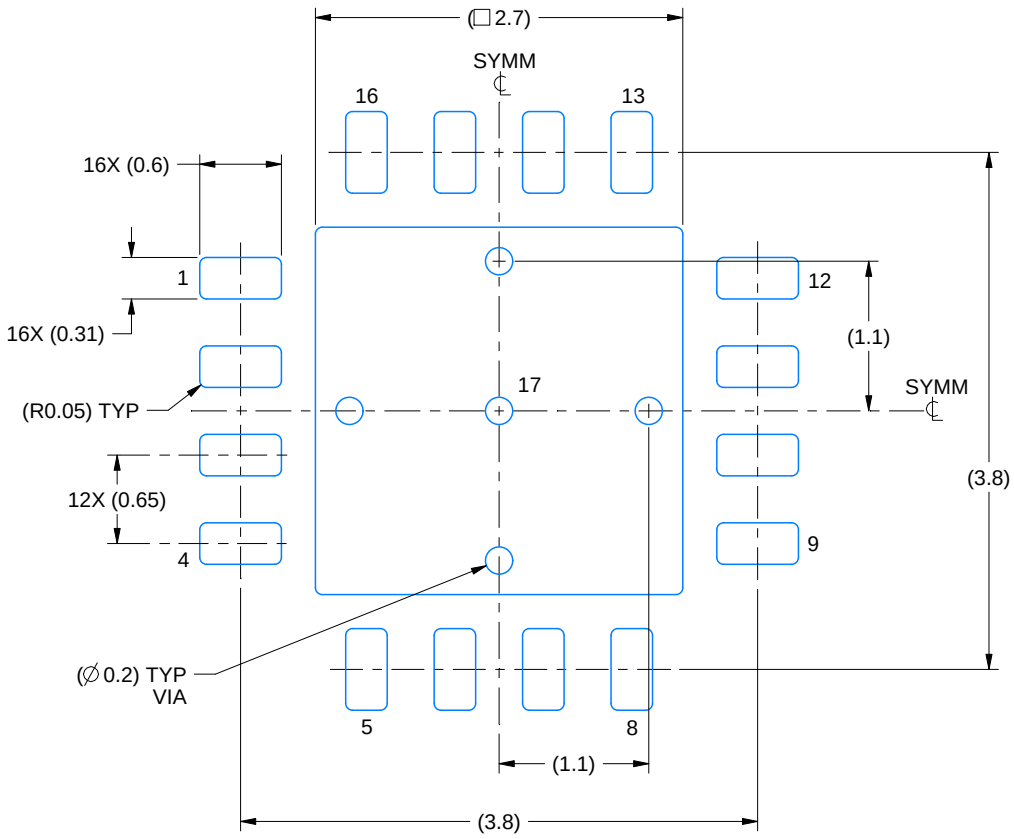
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

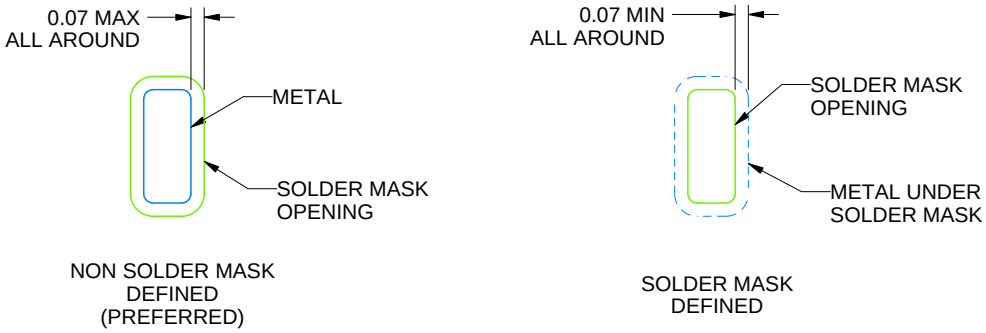


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

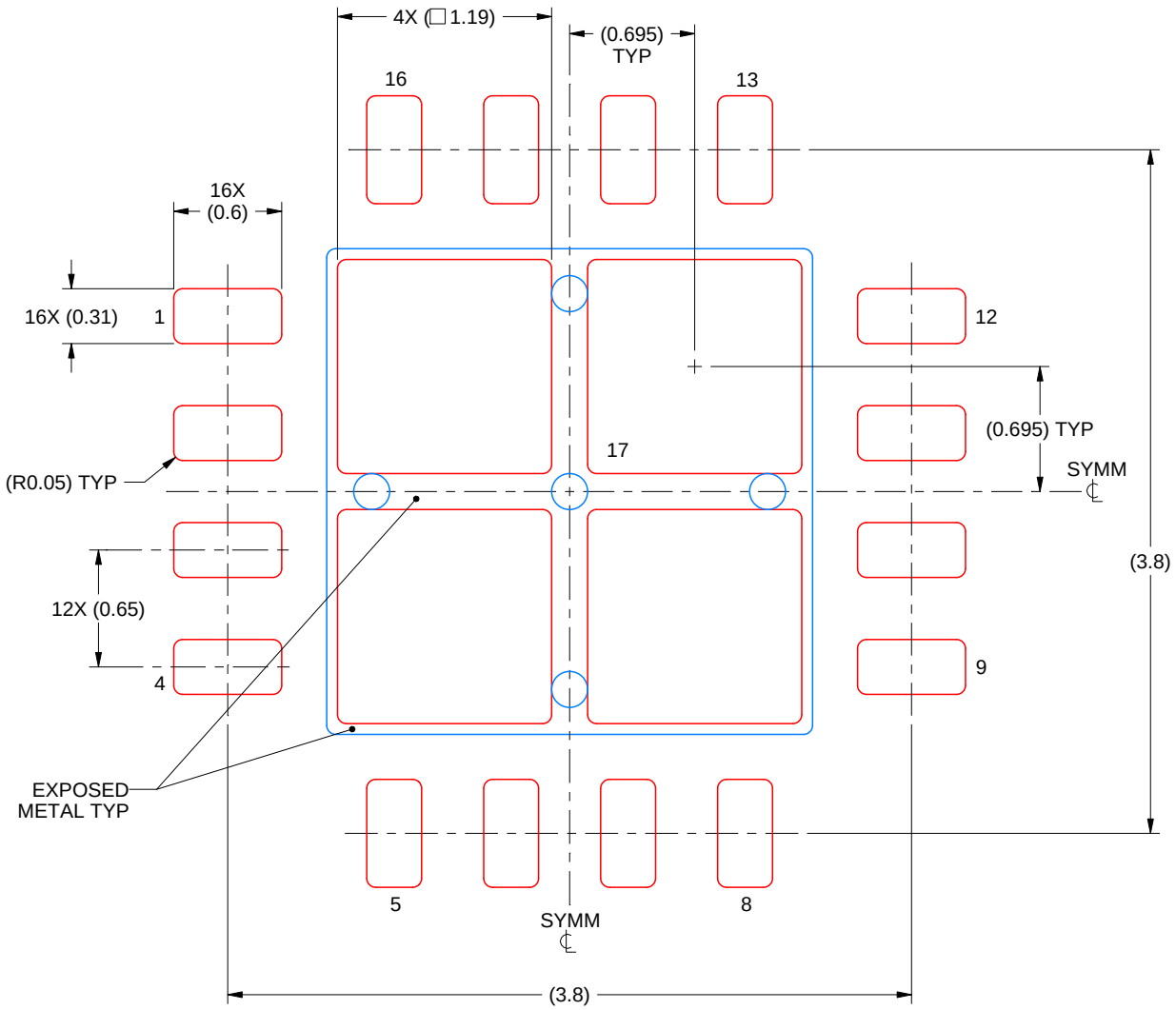


SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

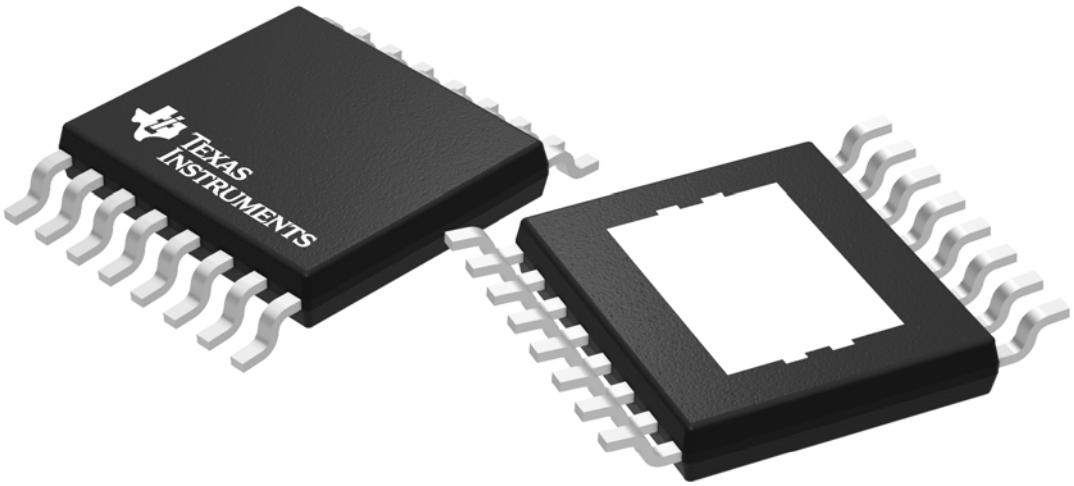
4219093/A 08/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

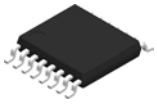
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

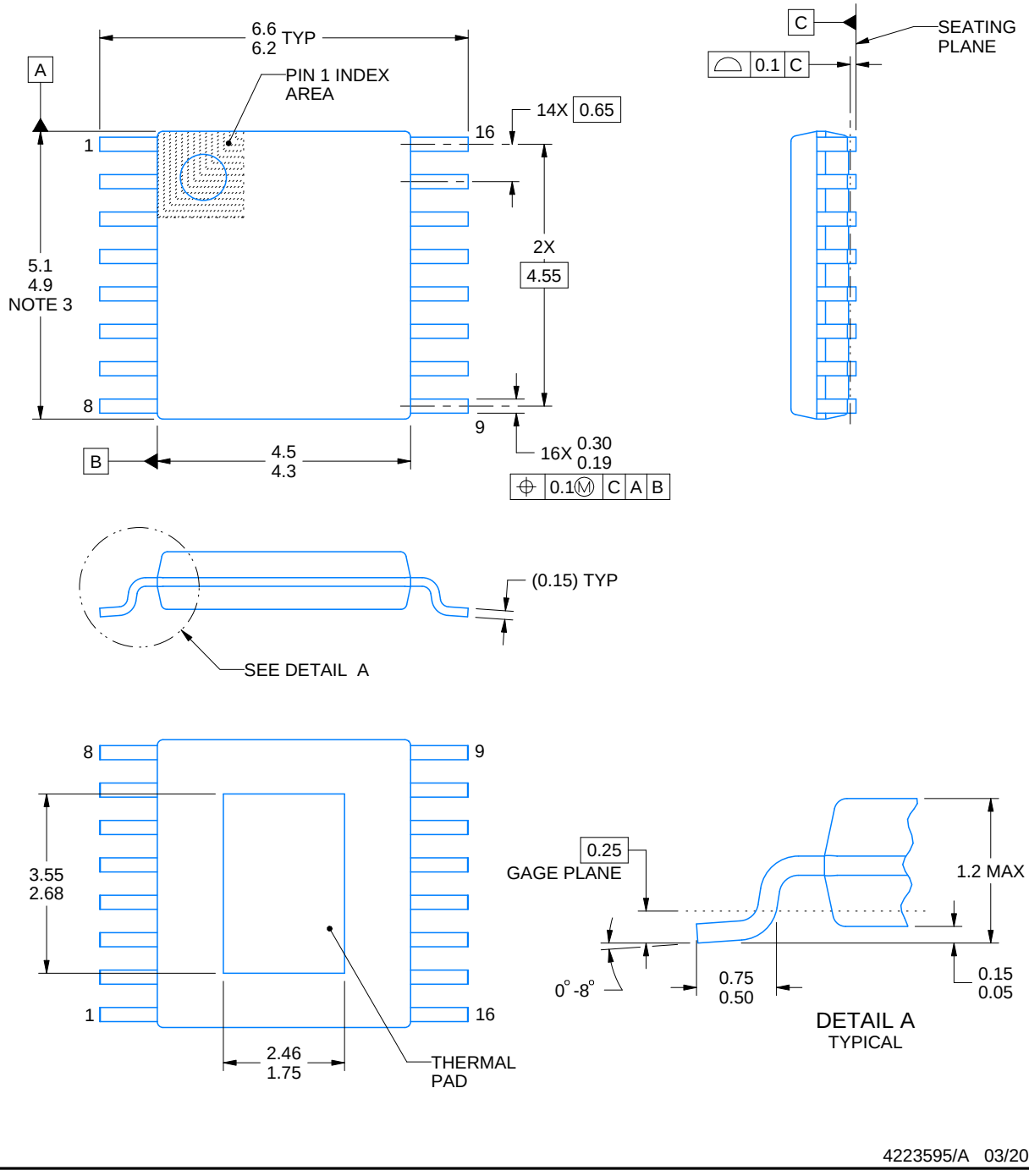
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

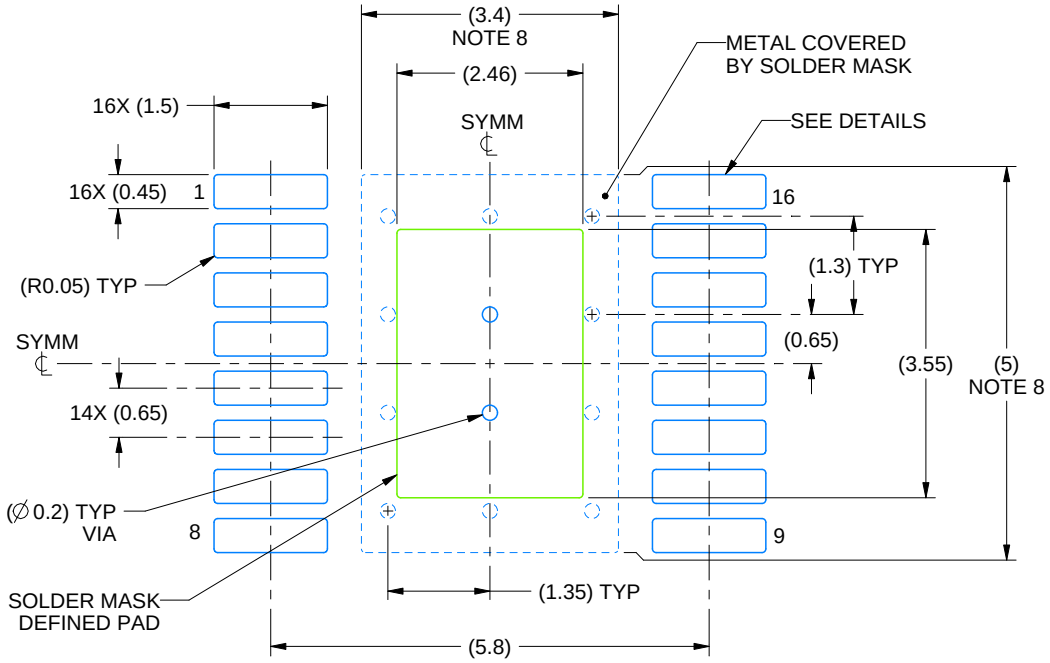
SMALL OUTLINE PACKAGE



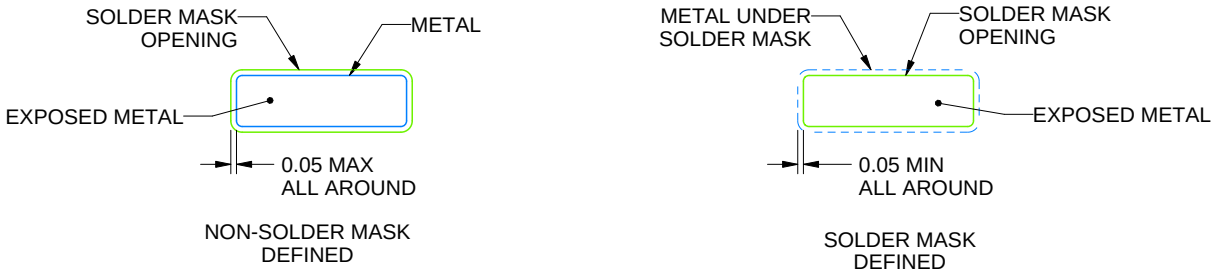
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

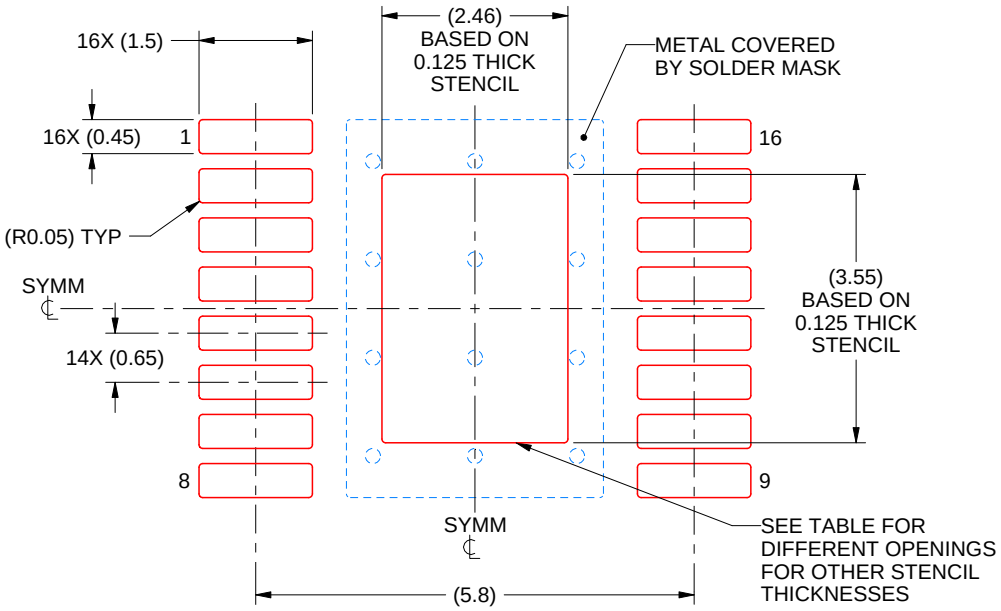


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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