TPS5450-Q1 汽车类 5.5V 至 36V、5A 降压转换器

1 特性

- 符合汽车应用 应用
- 宽输入电压范围：5.5V 至 36V
- 高达 5A 的持续（峰值为 6A）输出电流
- 通过 110mΩ 集成 MOSFET 开关实现超过 90% 的高效率
- 宽输出电压范围：可调节为低至 1.22V，初始精度为 1.5%
- 内部补偿可最大限度减少外部器件数量
- 适用于小型滤波器尺寸的固定 500kHz 开关频率
- 18μA 关断电源电流
- 通过输入电压前馈改进线路稳压和瞬态响应
- 通过过流限制、过压保护和热关断功能保护系统
- -40°C 至 125°C 的工作结温范围
- 采用小型热增强型 8 引脚 SOIC PowerPAD™封装
- 使用 TPS5450-Q1 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 高密度负载点调节器
- LCD 显示屏、等离子显示屏
- 电池充电器
- 12V/24V 分布式电源系统

3 说明

TPS5450-Q1 是一款高输出电流 PWM 转换器，集成了低电阻高侧 N 沟道 MOSFET。除了所列的特性 之外， 基板上还包含高性能电压误差放大器（可在瞬态条件下提供高稳压精度）、欠压锁定电路（用于防止在输入电压达到 5.5V 前启动）、内部设置的慢速启动电路（用于限制浪涌电流）以及电压前馈电路（用于改进瞬态响应）。通过使用 ENA 引脚，关断电源电流通常可减小至 18μA。其他 功能 包括高电平有效使能端、过流限制、过压保护和热关断。为降低设计复杂性并减少外部组件数量，TPS5450-Q1 反馈环路进行了内部补偿。

TPS5450-Q1 器件采用热增强型 8 引脚 SOIC PowerPAD™ 封装。TI 提供评估模块和软件工具，有助于实现高性能电源设计，可满足迫切的设备开发周期要求。

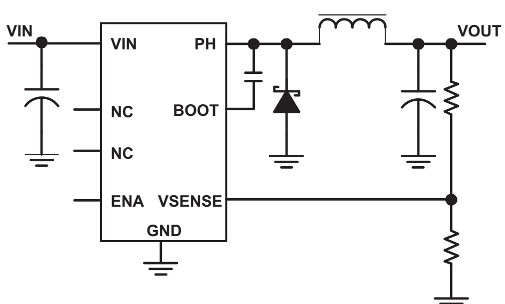
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS5450-Q1	HSOIC (8)	4.89mm × 3.90mm

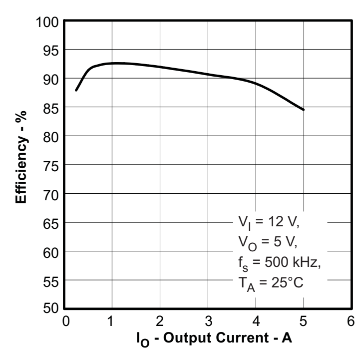
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图和效率曲线

Simplified Schematic



Efficiency vs Output Current



目录

4 修订历史记录

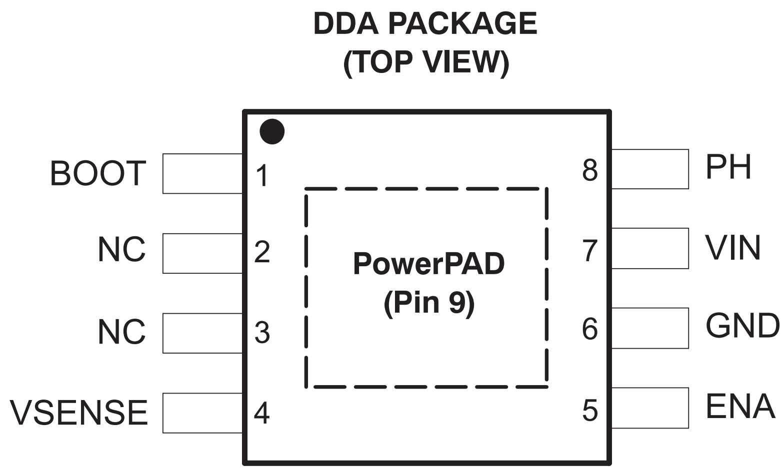
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2011) to Revision B	Page
• 仅有编辑更改；添加了 WEBENCH 链接；	1

Changes from Original (July 2008) to Revision A	Page
• Added *Thermal Table*	4

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		DESCRIPTION
NAME	**NO.**	
BOOT	1	Boost capacitor for the high-side FET gate driver. Connect 0.01-μF low-ESR capacitor from BOOT pin to PH pin.
NC	2, 3	No internal connection
VSENSE	4	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	Ground. Connect to thermal pad.
VIN	7	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality low-ESR ceramic capacitor.
PH	8	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	GND pin must be connected to the exposed pad for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1][2]

V_I	Input voltage range	VIN	–0.3 V to 40 V[3]
		BOOT	–0.3 V to 50 V
		PH (steady-state)	–0.6 V to 40 V[3]
		ENA	–0.3 V to 7 V
		BOOT-PH	10 V
		VSENSE	–0.3 V to 3 V
		PH (transient < 10 ns)	–1.2 V
I_O	Source current	PH	Internally Limited
I_{lkg}	Leakage current	PH	10 μA
T_J	Operating virtual-junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage range	5.5	36	V
T_J	Operating virtual-junction temperature	–40	125	°C

6.3 Thermal Information

THERMAL METRIC[1]		TPS5450-Q1	UNITS
		DDA	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	48.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	47.1	°C/W
θ_{JB}	Junction-to-board thermal resistance[4]	22.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter[5]	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter[6]	22.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	2.9	°C/W

(1) 有关传统和新热指标的更多信息，请参见应用报告《*半导体和 IC 封装热指标*》（文献编号：SPRA953）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部进行冷板测试仿真来获得结至外壳（顶部）热阻。JEDEC 标准中没有相关测试的描述，但 可在 ANSI SEMI 标准 G30 - 88 中找到相应的说明。
(4) 结至板热阻，可按照 JESD51-8 中的说明在使用环形冷板夹具来控制 PCB 温度的环境中进行仿真来获得。
(5) 结点至顶部特性参数 ψ_{JT} 估算器件在实际系统中的结温，可通过 JESD51-2a（第 6 节和第 7 节）介绍的步骤从获得 $R_{\theta JA}$ 的仿真数据中获取该温度。
(6) 结点至电路板特性参数 ψ_{JB} 估算器件在实际系统中的结温，可通过 JESD51-2a（第 6 节和第 7 节）介绍的步骤从获得 $R_{\theta JA}$ 的仿真数据中获取该温度。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至外壳（底部）热阻。JEDEC 标准中没有相关测试的描述，但 可在 ANSI SEMI 标准 G30 - 88 中找到相应的说明。

6.4 Dissipation Ratings[1][2]

(1) Maximum power dissipation may be limited by overcurrent protection.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.

Dissipation Ratings(1)(2) (接下页)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT
8-Pin DDA (4-layer board with solder)(3)	30°C/W

(3) Test board conditions:
(a) 2 in x 1.85 in, 4 layers, 0.062-in (1,57-mm) thickness
(b) 2-oz copper traces located on the top and bottom of the PCB
(c) 2-oz copper ground planes on the two internal layers
(d) Four thermal vias in the PowerPAD area under the device package

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 5.5 V to 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I_Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T_J = 25°C	1.202	1.221	1.239	V
		I_O = 0 A – 5 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87	89		%
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		5.4	8	10	ms
CURRENT LIMIT						
	Current limit		5.7	7.5	9.0	A
	Current limit hiccup time		13	16	21	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		°C
OUTPUT MOSFET						
$r_{DS(on)}$	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

6.6 Typical Characteristics

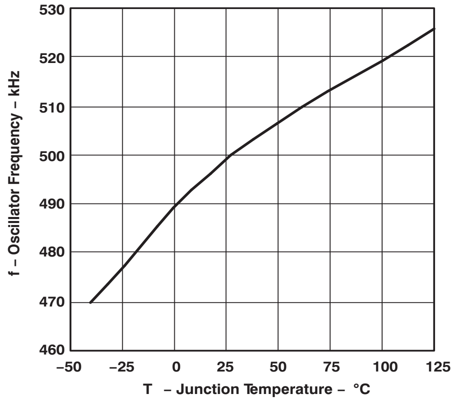


图 1. Oscillator Frequency vs Junction Temperature

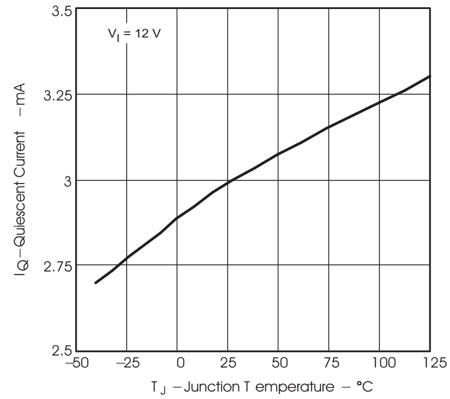


图 2. Non-Switching Quiescent Current vs Junction Temperature

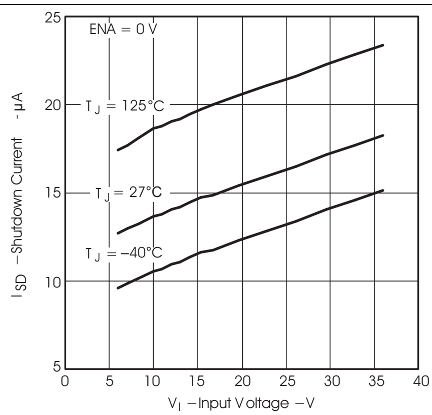


图 3. Shutdown Quiescent Currentvsinput Voltage

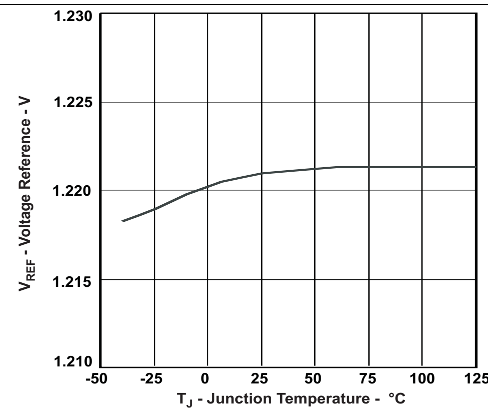


图 4. Voltage Reference vs Junction Temperature

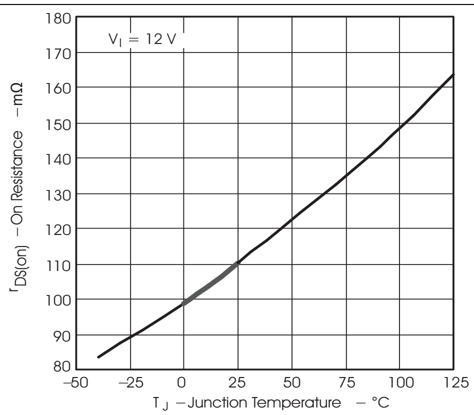


图 5. On-Resistance vs Junction Temperature

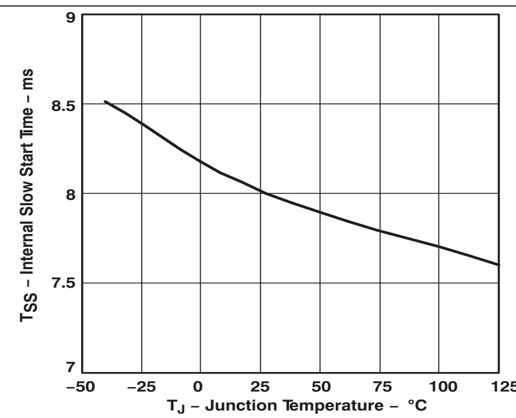


图 6. Internal Slow Start Time vs Junction Temperature

Typical Characteristics (接下页)

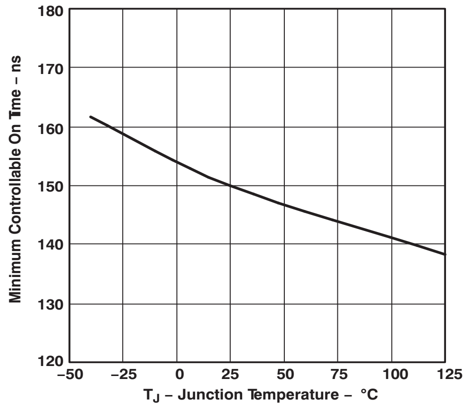


图 7. Minimum Controllable On-Time vs Junction Temperature

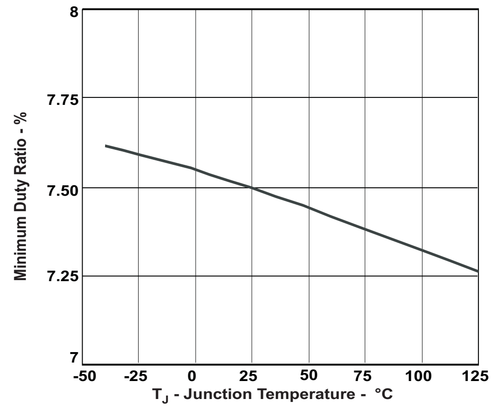


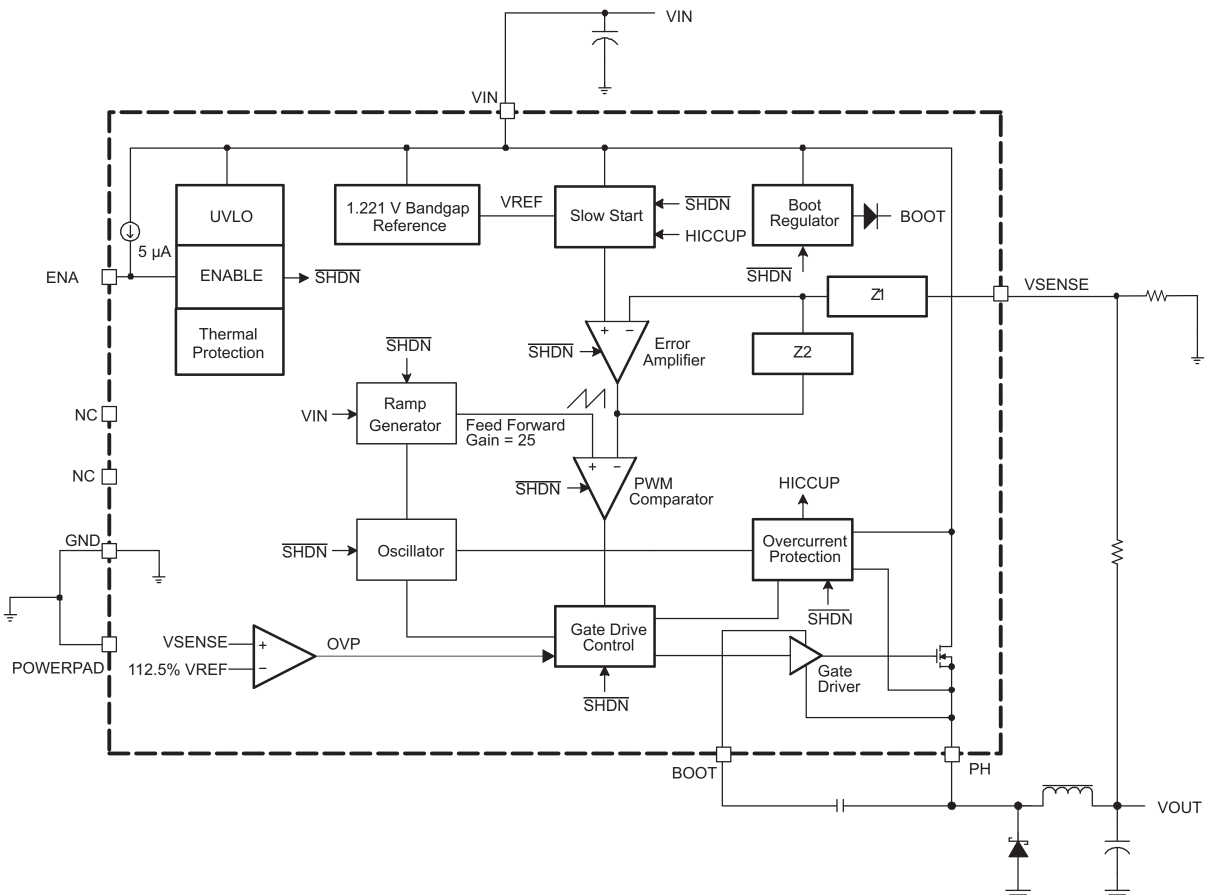
图 8. Minimum Controllable Duty Ratio vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS5450-Q1 is a high-output-current PWM converter that integrates a low-resistance high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions, an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V, an internally set slow-start circuit to limit inrush currents, and a voltage feedforward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 μA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection, and thermal shutdown. To reduce design complexity and external component count, the TPS5450-Q1 feedback loop is internally compensated.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free-running oscillator sets the PWM switching frequency at 500 kHz. The 500-kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V disables the regulator and activates the shutdown mode. The quiescent current of the TPS5450-Q1 in shutdown mode is 18 μA (typical).

The ENA pin has an internal pullup current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms (typical).

7.3.4 Undervoltage Lockout (UVLO)

The TPS5450-Q1 incorporates an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage must be equal to the voltage reference 1.221 V.

The TPS5450-Q1 implements internal compensation to simplify the regulator design. Because the TPS5450-Q1 uses voltage-mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* section for more details.

7.3.6 Voltage Feedforward

The internal voltage feedforward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feedforward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain:

$$\text{Feed Forward Gain} = \frac{\text{VIN}}{\text{Ramp}_{\text{pk}-\text{pk}}} \tag{1}$$

The typical feed forward gain of TPS5450-Q1 is 25.

Feature Description (接下页)

7.3.7 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed-frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high-gain error amplifier and compensation network to produce a error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error-voltage magnitude is converted to a pulse width, which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

7.3.8 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system ignores the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turnon noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used; in other words, hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

7.3.9 Overvoltage Protection

The TPS5450-Q1 has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of 112.5% × VREF. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET is forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET is enabled again.

7.3.10 Thermal Shutdown

The TPS5450-Q1 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

8 Application Information

8.1 Application Information

The TPS5450-Q1 can provide up to 5-A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board. The following design procedure can be used to select component values for the TPS5450-Q1.

8.2 Typical Application

图 9 shows the schematic for a typical TPS5450-Q1 application.

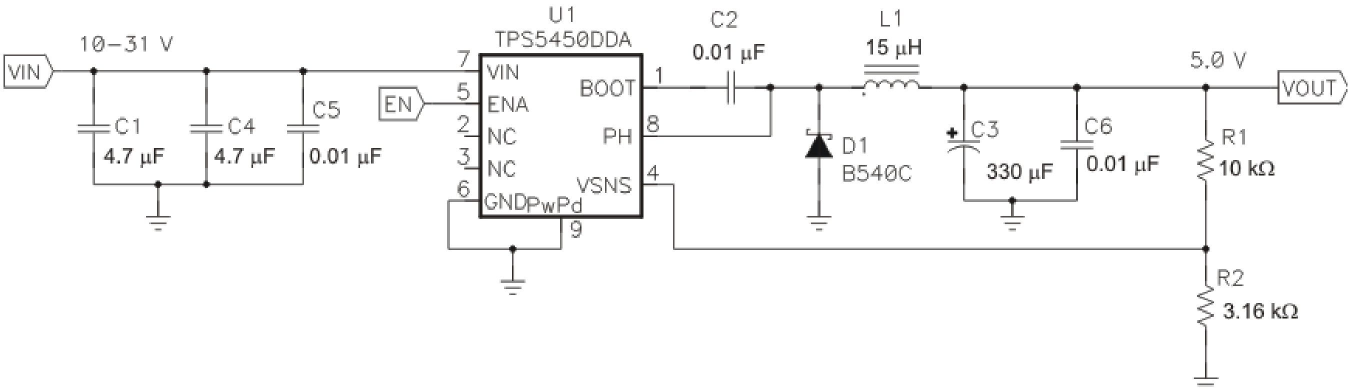


图 9. Application Circuit, 12-V to 5-V

8.2.1 Design Requirements

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

表 1. Design Parameters

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	10 V to 31 V
Output voltage	5 V
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS5450-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Boost Capacitor (BOOT)

Connect a 0.01-μF low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

8.2.2.3 Switching Frequency

The switching frequency for the TPS5450-Q1 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.2.4 Input Capacitors

The TPS5450-Q1 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum recommended decoupling capacitance is 4.7 μF. A high-quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by 公式 2 :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right)$$

where

- $I_{OUT(MAX)}$ is the maximum load current
- f_{SW} is the switching frequency
- C_{IN} is the input capacitor value
- ESR_{MAX} is the maximum series resistance of the input capacitor (2)

For this design, the input capacitance consists of two 4.7 μF capacitors, C1 and C4, in parallel. An additional high-frequency bypass capacitor, C5 is also used.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by 公式 3 :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \qquad (3)$$

In this case the input ripple voltage would be 281 mV and the RMS ripple current would be 2.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen input decoupling capacitor is rated for 50 V, and the ripple current capacity is greater than 2.5 A each, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5450-Q1 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.2.5 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Because the TPS5450-Q1 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.2.5.1 Inductor Selection

To calculate the minimum value of the output inductor, use 公式 4:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW(MIN)}} \tag{4}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak-to-peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current, and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5450-Q1, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point, and relatively low load currents can be sourced before discontinuous operation.

For this design example use K_{IND} = 0.2 and the minimum inductor value is calculated to be 10.4 μH. A higher standard value is 15 μH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from 公式 5:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}}\right)^2} \tag{5}$$

and the peak inductor current can be determined with 公式 6:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW(MIN)}} \tag{6}$$

For this design, the RMS inductor current is 5.004 A, and the peak inductor current is 5.34 A. The chosen inductor is a Sumida CDRH1127/LD-150 15 μH. It has a minimum rated current of 5.65 A for both saturation and RMS current. In general, inductor values for use with the TPS5450-Q1 are in the range of 10 μH to 100 μH.

8.2.2.5.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because, along with the inductor ripple current, it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz, as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency is between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^2}{85\ V_{OUT}} \tag{7}$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \quad (8)$$

For a desired crossover of 12 kHz and a 15-µH inductor, the calculated value for the output capacitor is 330 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \quad (9)$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP}\,(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}}$$

where

- ΔV_{PP} is the desired peak-to-peak output ripple
- N_C is the number of parallel output capacitors
- F_{SW} is the switching frequency (10)

For this design example, a single 330-µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB330M, rated at 10 V with a maximum ESR of 35 mΩ and a ripple current rating of 3 A. An additional small 0.1-µF ceramic bypass capacitor, C6 is also used in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by 公式 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right]$$

where

- N_C is the number of output capacitors in parallel
- F_{SW} is the switching frequency (11)

Other capacitor types can be used with the TPS5450-Q1, depending on the needs of the application.

8.2.2.6 Output Voltage Setpoint

The output voltage of the TPS5450-Q1 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using 公式 12:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \quad (12)$$

For any TPS5450-Q1 design, start with an R1 value of 10 kΩ. For an output voltage closest to but at least 5 V, R2 is 3.16 kΩ.

8.2.2.7 Boot Capacitor

The boot capacitor must be 0.01 µF.

8.2.2.8 Catch Diode

The TPS5450-Q1 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is V_{INMAX} + 0.5 V. Peak current must be greater than I_{OUTMAX} plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B540A is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.5 V.

8.2.2.9 Output Voltage Limitations

Due to the internal design of the TPS5450-Q1, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left(\left(V_{INMIN} - I_{OMAX} \times 0.230\right) + V_D\right) - \left(I_{OMAX} \times R_L\right) - V_D$$

where

- V_{INMIN} = minimum input voltage
- I_{OMAX} = maximum load current
- V_D = catch diode forward voltage
- R_L= output inductor series resistance (13)

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time, which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left(\left(V_{INMAX} - I_{OMIN} \times 0.110\right) + V_D\right) - \left(I_{OMIN} \times R_L\right) - V_D$$

where

- V_{INMAX} = maximum input voltage
- I_{OMIN} = minimum load current
- V_D = catch diode forward voltage
- R_L= output inductor series resistance (14)

This equation assumes nominal on resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to ensure proper functionality.

8.2.2.10 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS5450-Q1. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS5450-Q1. 公式 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times Fz1}\right) \times \left(1 + \frac{s}{2\pi \times Fz2}\right)}{\left(\frac{s}{2\pi \times Fp0}\right) \times \left(1 + \frac{s}{2\pi \times Fp1}\right) \times \left(1 + \frac{s}{2\pi \times Fp2}\right) \times \left(1 + \frac{s}{2\pi \times Fp3}\right)}$$

where

- Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz
- Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz
- Fp3 represents the non-ideal parasitics effect (15)

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.2.3 Application Curves

The performance graphs (图 10 through 图 16) are applicable to the circuit in 图 9. T_A = 25 °C. unless otherwise specified.

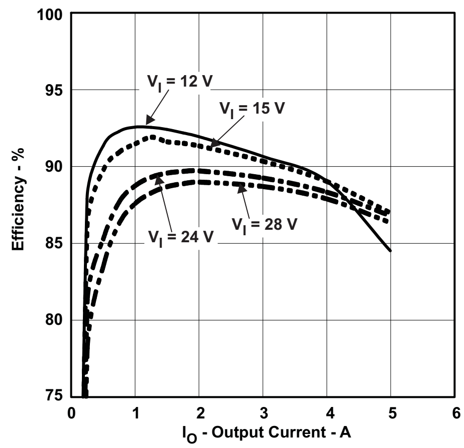


图 10. Efficiency vs Output Current

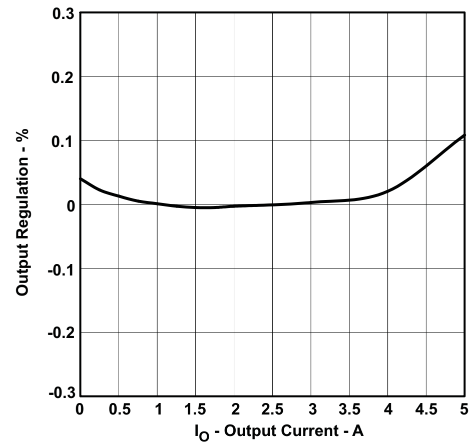


图 11. Output Regulation % vs Output Current

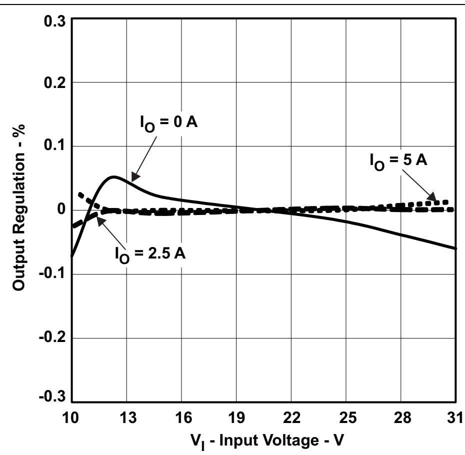
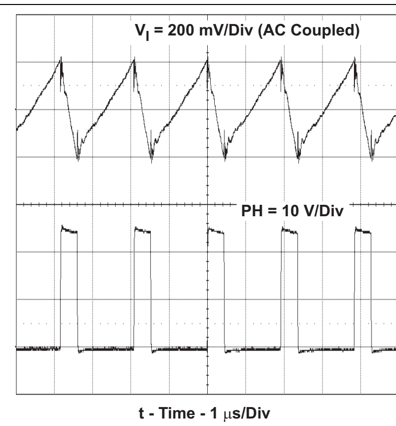
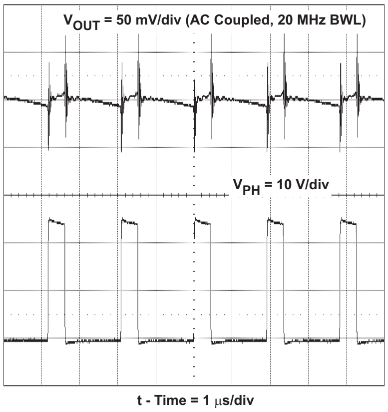


图 12. Output Regulation % vs Input Voltage



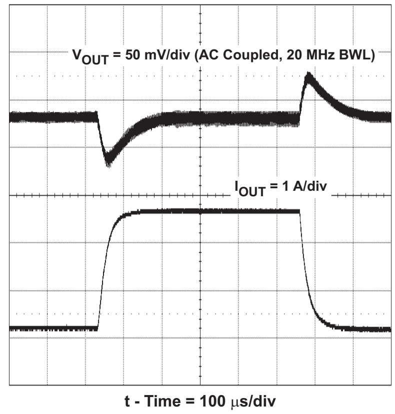
I_{OUT} = 5 A

图 13. Input Voltage Ripple and PH Node



I_{OUT} = 5 A

图 14. Output Voltage Ripple and PH Node



I_{OUT} Step 1.25 To 3.75 A

图 15. Transient Response

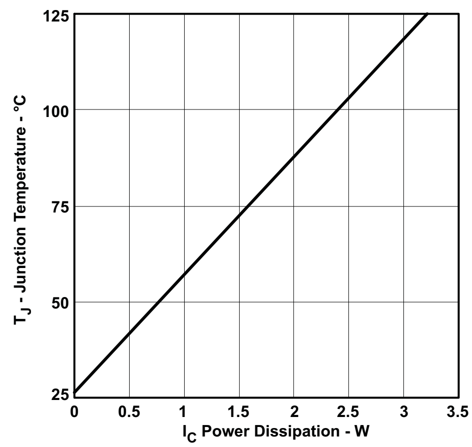


图 16. TPS5450-Q1 Power Dissipation vs Junction Temperature.

9 Layout

9.1 Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS5450-Q1 ground pin. The best way to do this is to extend the top-side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7-μF ceramic with a X5R or X7R dielectric.

There must be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. Tie the GND pin to the PCB ground by connecting it to the ground area under the device as shown below.

Route the PH pin to the output inductor, catch diode, and boot capacitor. Because the PH connection is the switching node, locate the inductor very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings also may be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, L_{OUT}, C_{OUT}, and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pinout, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in 图 17, use a via connection to a different layer to route to the ENA pin.

9.2 Layout Examples

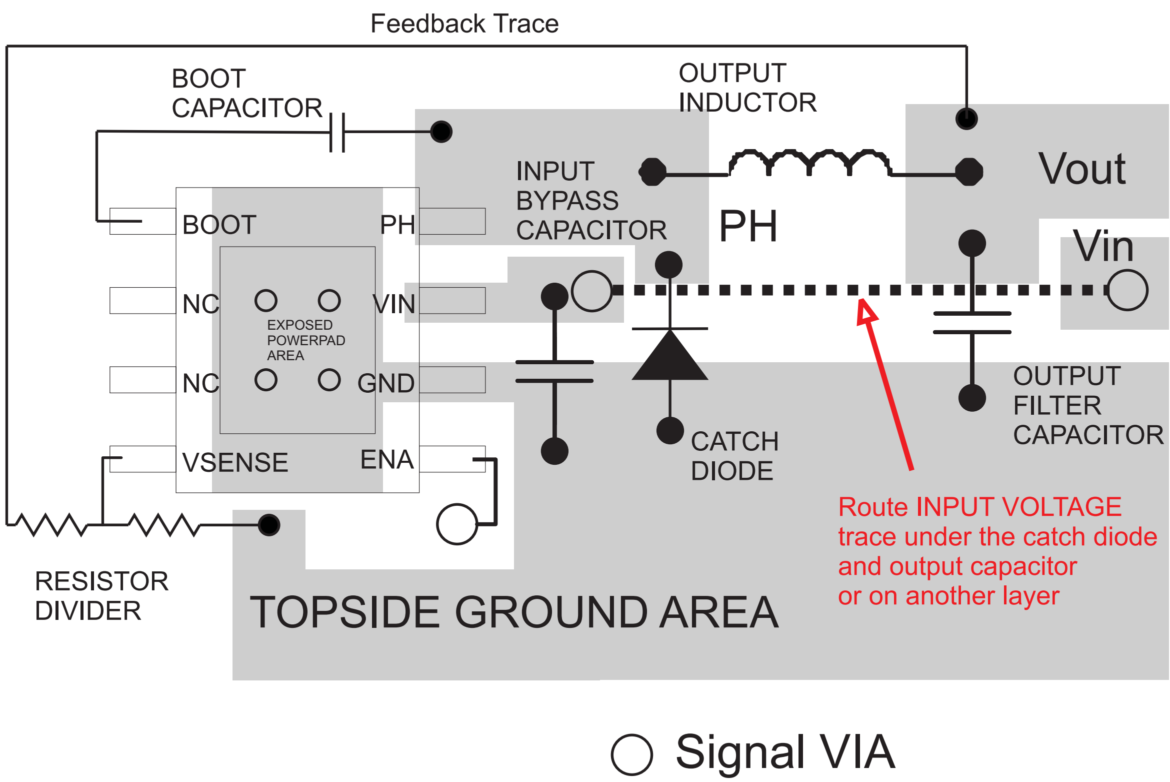


图 17. Design Layout

Layout Examples (接下页)

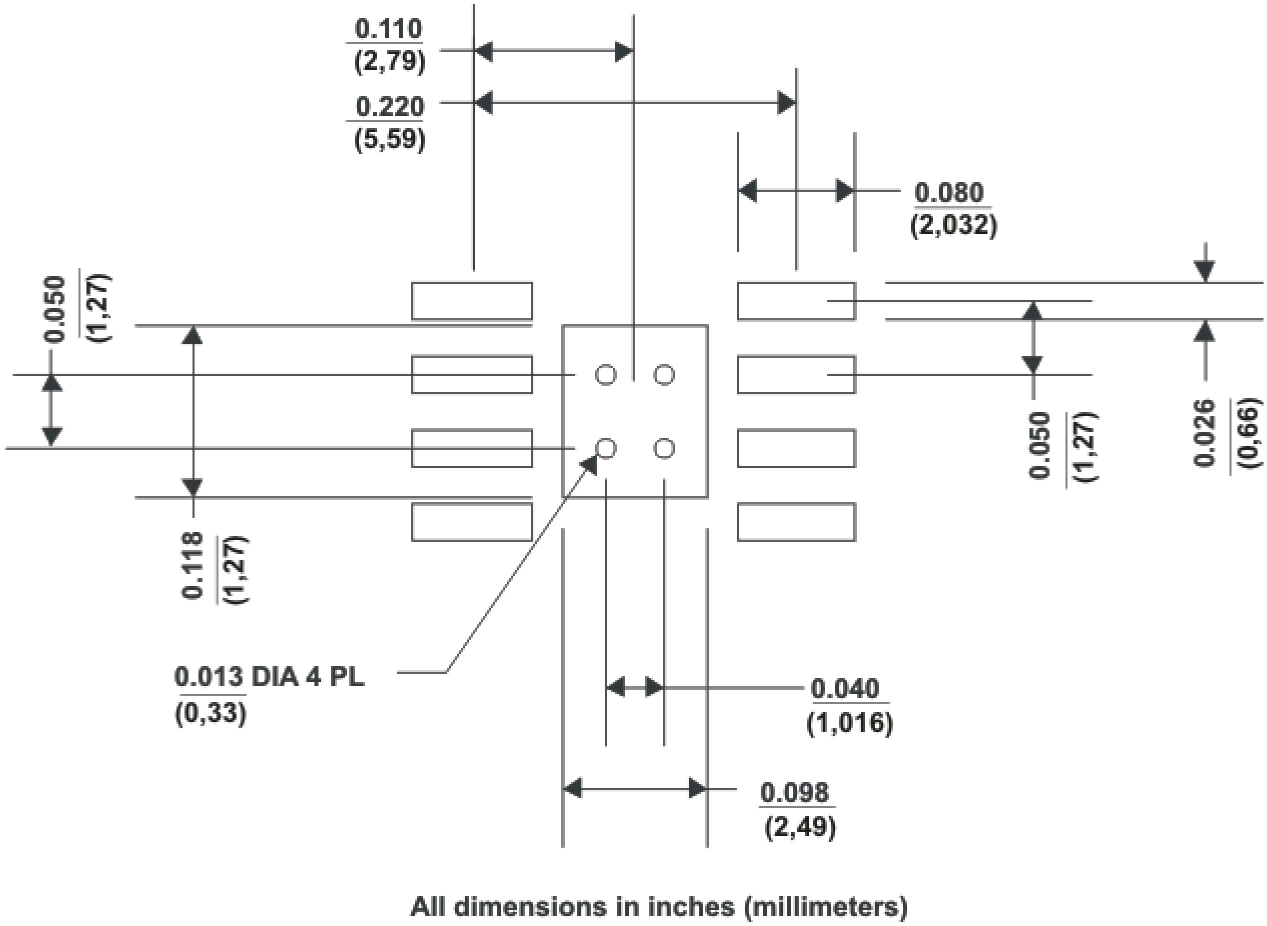


图 18. TPS5450-Q1 Land Pattern

9.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $Pcon = I_{OUT}^2 \times R_{DS(on)} \times V_{OUT}/V_{IN}$

Switching Loss: $Psw = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $Pq = V_{IN} \times 0.01$

Total Loss: Ptot = Pcon + Psw + Pq

Given T_A => Estimated Junction Temperature: $T_J = T_A + Rth \times Ptot$

Given T_{JMAX} = 125°C => Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} – Rth \times Ptot$

10 器件和文档支持

10.1 器件支持

10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

10.2 开发支持

10.2.1 使用 **WEBENCH®** 工具创建定制设计

单击此处，使用 TPS5450-Q1 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

10.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5450QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5450Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS5450-Q1 :

- Catalog : TPS5450

- Enhanced Product : TPS5450-EP

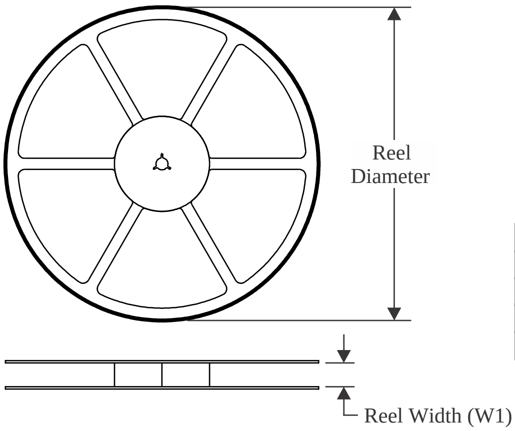
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

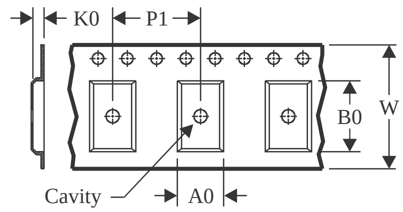
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

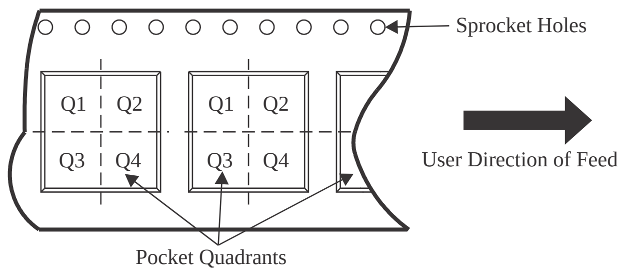


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

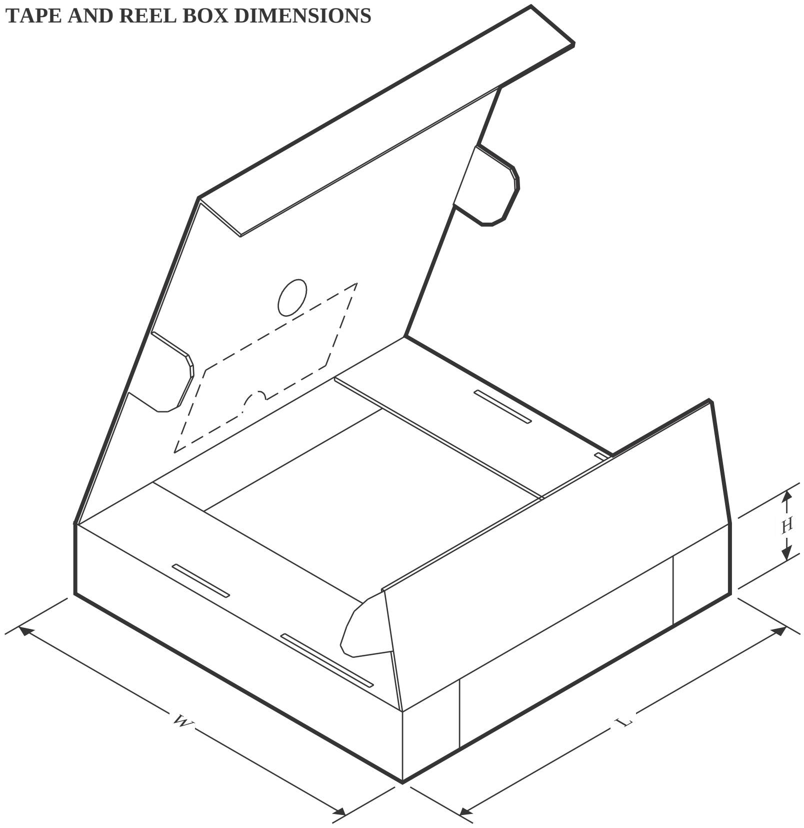
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5450QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

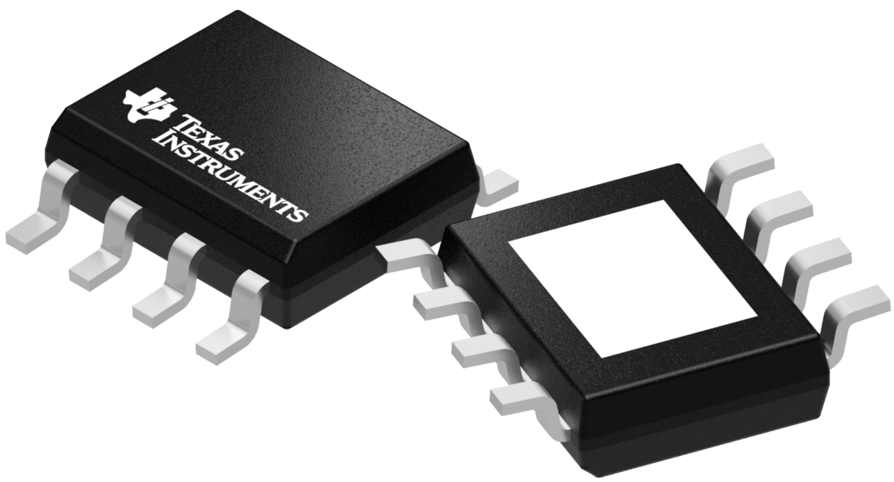


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5450QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

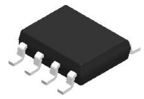
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

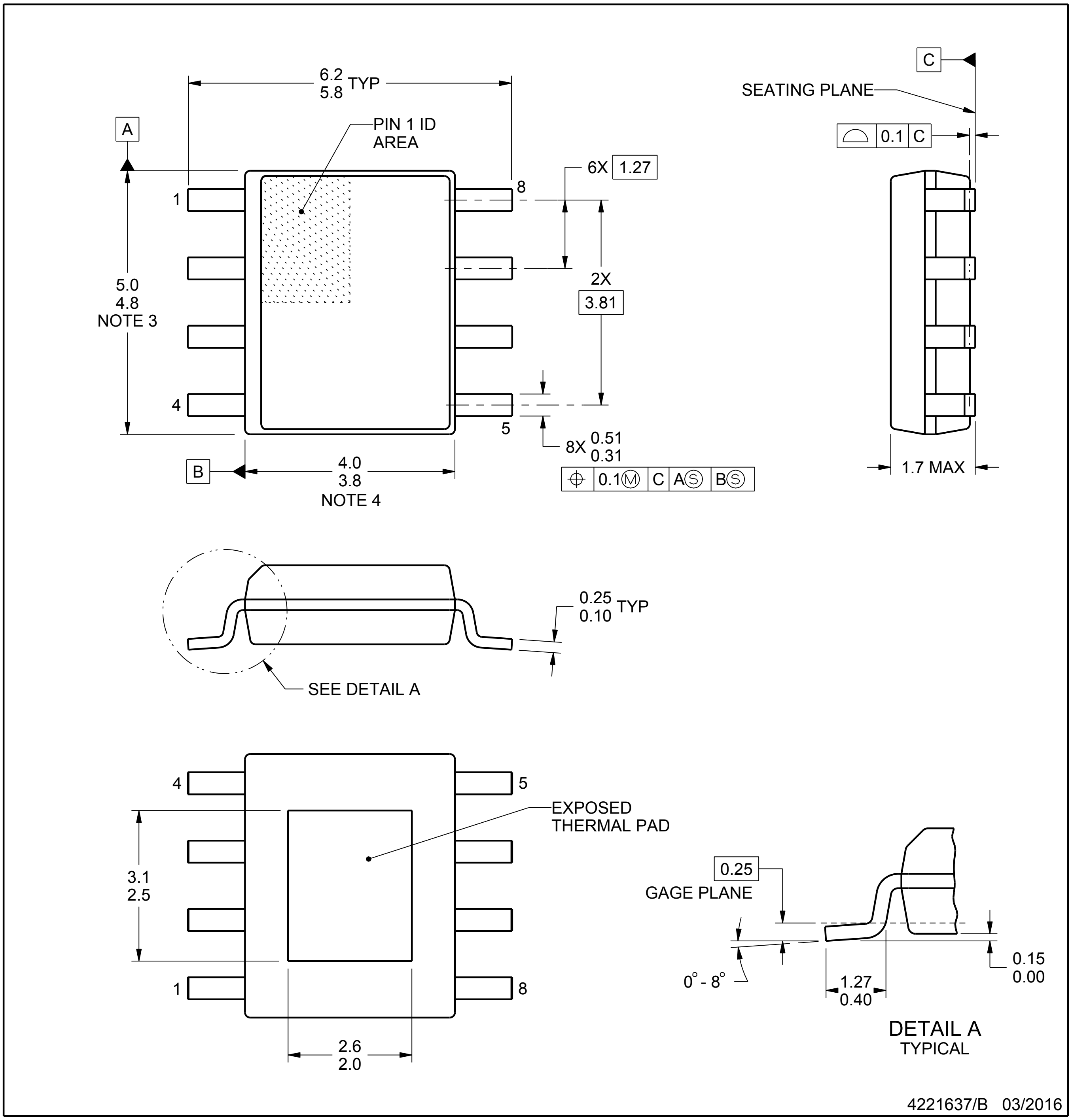
4202561/G



DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

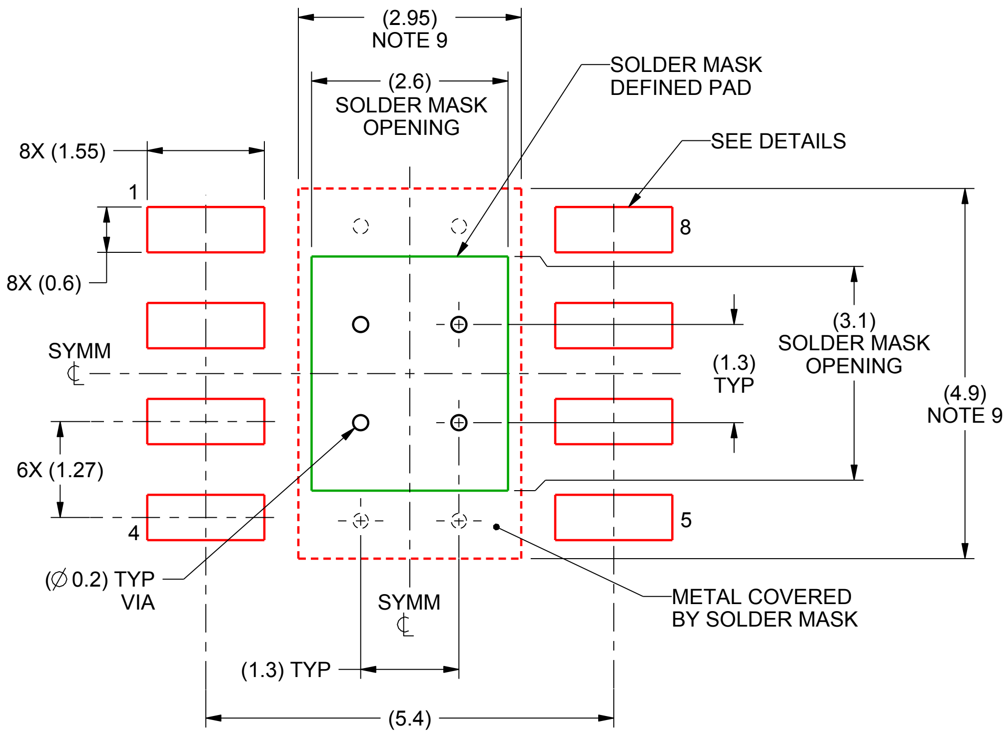
PLASTIC SMALL OUTLINE



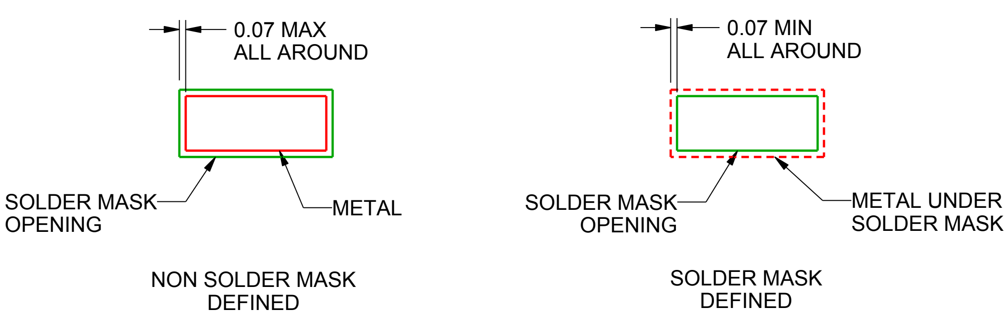
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

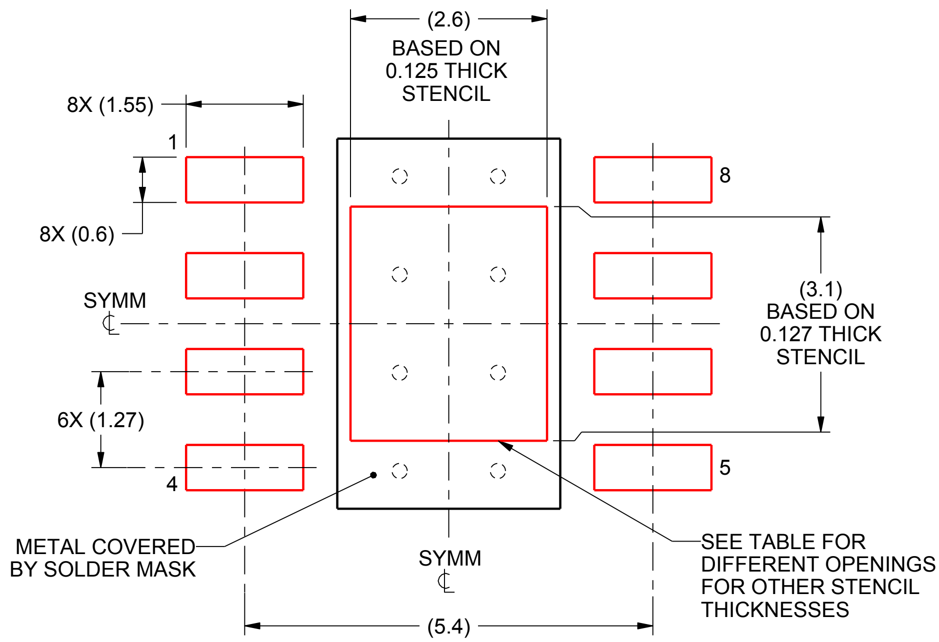


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265