TPS546D24 2.95V 至 16V、40A、高达 4× 可堆叠、 PMBus®降压转换器

1 特性

- 支持双电源：2.95V 至 16V PVIN；2.95V 至 18V AVIN（4V_{IN} VDD5 开关电压）
- 集成型 4.5mΩ/0.9mΩ MOSFET
- 具有可选内部补偿的平均电流模式控制
- 2×、3×、4× 可堆叠，电流共享高达 160A，每个输出可支持单个地址
- 通过引脚搭接的可选输出电压范围为 0.6V 至 5.5V，通过 PMBus VOUT_COMMAND 的电压范围为 0.25V 至 5.5V
- 广泛的 PMBus 命令集，可遥测 V_{OUT}、I_{OUT} 和内部裸片温度
- 通过内部反馈分压器实现差分遥感，可检测到小于 1% 的 V_{OUT} 误差，T_J 为 –40°C 至 +150°C
- 通过 PMBus 实现自适应电压调节 (AVS) 和裕量调节
- 采用 MSEL 引脚，引脚编程 PMBus 默认值
- 12 种可选开关频率，介于 225kHz 至 1.5MHz（8 个引脚搭接选项）
- 频率同步输入/同步输出
- 支持预偏置输出
- 支持强耦合电感器
- 7mm × 5mm × 1.5mm、40 引脚 QFN、间距 = 0.5mm
- 使用 TPS546D24 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 数据中心交换机、机架式服务器
- 有源天线系统、远程射频和基带单元
- 自动化测试设备、CT、PET 和 MRI
- ASIC、SoC、FPGA、DSP 内核和 I/O 电压

3 说明

TPS546D24 是一款高度集成的非隔离式直流/直流转换器，具有较高的工作频率和 40A 的电流输出，采用 7mm × 5mm 封装。可将两个、三个和四个 TPS546D24 器件互连，在单个输出上提供最高 160A 的电流。该器件可通过 VDD5 引脚，利用 5V 的外部电源对内部的 5V LDO 进行过驱动，以提高效率并降低转换器的功耗。

TPS546D24 使用专有的固定频率电流模式控制，具有输入前馈和可选的内部补偿元件，可在各种输出电容下最大限度减小尺寸和提高稳定性。

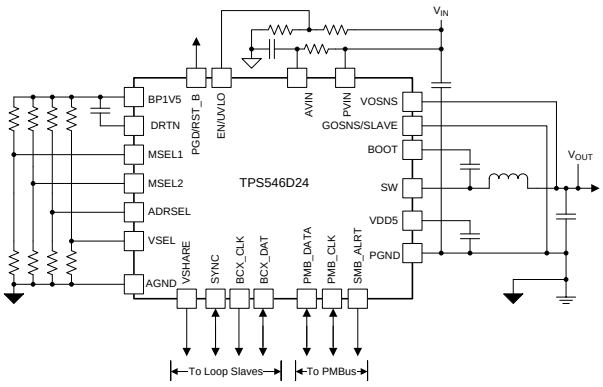
PMBus 接口具有 1MHz 时钟支持，为转换器配置提供了便捷且标准化的数字接口，并且实现了对输出电压、输出电流和内部裸片温度等关键参数的监控。对故障状况的响应可设置为重新启动、锁存或忽略，具体取决于系统要求。堆叠器件之间的反向通道通信使得所有 TPS546D24 转换器能够为单个输出轨供电，以共享一个地址，从而简化系统软件/固件设计。也可通过 BOM 选择在不进行 PMBus 通信的情况下，配置输出电压、开关频率、软启动时间和过流故障限制等关键参数，以支持无程序加电。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS546D24	LQFN-CLIP (40)	7.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化应用



目录

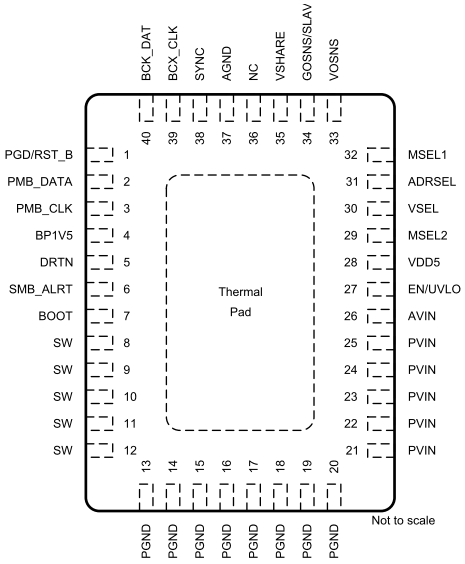
4 修订历史记录

Changes from Original (November 2018) to Revision A **Page**

- 首次发布生产数据数据表 ... 1

5 Pin Configuration and Functions

RVF Package
40-Pin LQFN-CLIP With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PGD/RST_B	I/O	Open-drain power good or reset#, As determined by user accessible bit (See in PMBUS Command detailed descriptions) . The default pin function is an open drain power-good indicator.
2	PMB_DATA	I/O	PMBus DATA pin. See PMBus specification.
3	PMB_CLK	I	PMBus CLK pin. See PMBus specification.
4	BP1V5	O	Output of the 1.5-V internal regulator. This regulator powers the digital circuitry and should be bypassed with a minimum of 1 µF to DRTN. BP1V5 is not designed to power external circuit.
5	DRTN	—	Digital bypass return for bypass capacitor for BP1V5. Internally Connected to AGND. Do not Connect to PGND or AGND.
6	SMB_ALRT	O	SMBus alert pin. See SMBus specification.
7	BOOT	I	Bootstrap pin for the internal flying high side driver. Connect a typical 100 nF from this pin to SW. To reduce the voltage spike at SW, an optional BOOT resistor of up to 8 Ω may be placed in series with the BOOT capacitor to slow down turn-on of the high-side FET.
8	SW	I/O	Switched power output of the device. Connect the output averaging filter and bootstrap to this group of pins.
9			
10			
11			
12			
13	PGND	—	Power stage ground return. These pins are internally connected to the thermal pad.
14			
15			
16			
17			
18			
19			
20			

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
21	PVIN	I	Input power to the power stage. Low-impedance bypassing of these pins to PGND is critical.
22			
23			
24			
25			
26	AVIN	I	Input power to the controller. Bypass with a minimum 1-µF ceramic capacitor to PGND. If AVIN is connected to the same input as PVIN or VDD5, a minimum 10-µs R-C filter is recommended to reduce switching noise on AVIN.
27	EN/UVLO	I	Enable switching as the PMBus CONTROL pin. EN/UVLO can also be connected to a resistor divider to program input voltage UVLO.
28	VDD5	O	Output of the 5-V internal regulator. This regulator powers the driver stage of the controller and should be bypassed with a minimum of 4.7 µF to PGND at the thermal pad. Low impedance bypassing of this pin to PGND is critical.
29	MSEL2	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of soft-start time, overcurrent fault limit, and multi-phase information. See section
30	VSEL	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of internal voltage feedback divider and default output voltage. See section.
31	ADRSEL	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of PMBus addresses and frequency sync (including determination of SYNC pin as SYNC IN or SYNC OUT function). See section.
32	MSEL1	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of switching frequency and internal compensation parameters. See section.
33	VOSNS	I	The positive input of the remote sense amplifier. For a standalone device or the loop master device in a multi-phase configuration, connect VOSNS pin to the output voltage at the load. For the loop slave device in a multi-phase configuration, the remote sense amplifier is not required for output voltage sensing or regulation, this pin can be left floating.
34	GOSNS/SLAVE	I	The negative input of the remote sense amplifier for loop master device or should be pulled up high to indicate loop slave. For standalone device or the loop master device in a multi-phase configuration, connect GOSNS pin to the ground at the load. For the loop slave device in a multi-phase configuration, the GOSNS pin must be pulled up to BP1V5 to indicate the device a loop slave.
35	VSHARE	I/O	Voltage sharing signal for multi-phase operation. For stand-alone device, the VSHARE pin must be left floating.
36	NC	-	Not internally connected. Pin can be left floating or connected to PGND at the thermal pad.
37	AGND	-	Analog ground return for controller. Connect the AGND pin directly to the thermal pad on the PCB board.
38	SYNC	I/O	For frequency synchronization, can be programmed as SYNC IN or SYNC OUT pin by ADRSEL pin or the PMBus Command. The SYNC pin can be left floating when not used.
39	BCX_CLK	I/O	Clock for back-channel communications between stacked devices.
40	BCX_DAT	I/O	Data for back-channel communications between stacked devices.
—	Thermal pad	—	Package thermal pad, internally connected to PGND. The thermal pad must have adequate solder coverage for proper operation.

6 器件和文档支持

6.1 器件支持

6.1.1 第三方产品免责声明

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6.1.2 开发支持

6.1.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 TPS546D24 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

6.1.2.2 德州仪器 (TI) Fusion Digital Power Designer

TPS546D24 器件受德州仪器 (TI) Digital Power Designer 支持。Fusion digital Power Designer 是一款图形用户界面 (GUI)，可使用德州仪器 (TI) USB-to-GPIO 适配器通过 PMBus 配置并监控器件。

单击此链接下载德州仪器 (TI) Fusion Digital Power Designer 软件包。

6.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.4 商标

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WEBENCH is a registered trademark of Texas Instruments.
PMBus is a registered trademark of System Management Interface Forum, Inc..
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6.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS546D24RVFR	ACTIVE	LQFN-CLIP	RVF	40	2500	RoHS-Exempt & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24	Samples
TPS546D24RVFT	ACTIVE	LQFN-CLIP	RVF	40	250	RoHS-Exempt & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

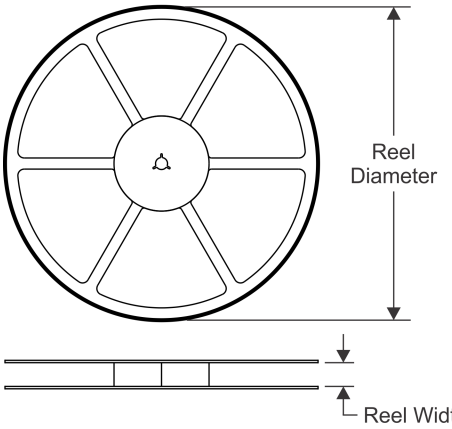
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

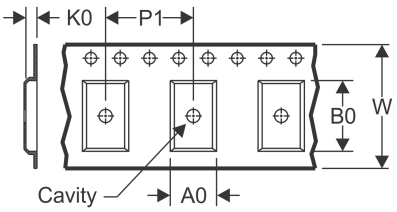
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

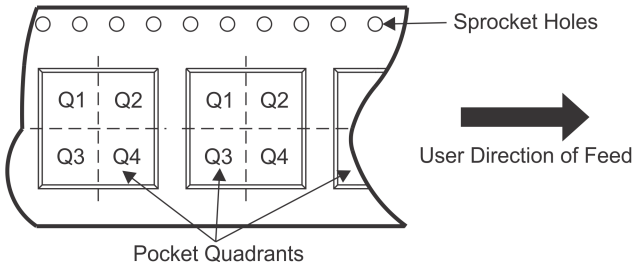


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

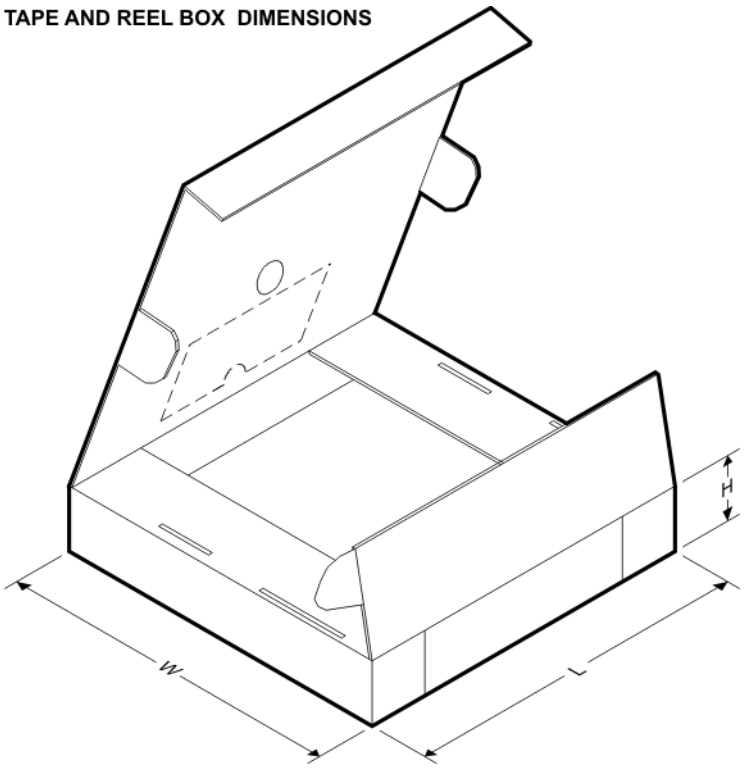
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS546D24RVFR	LQFN-CLIP	RVF	40	2500	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS546D24RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

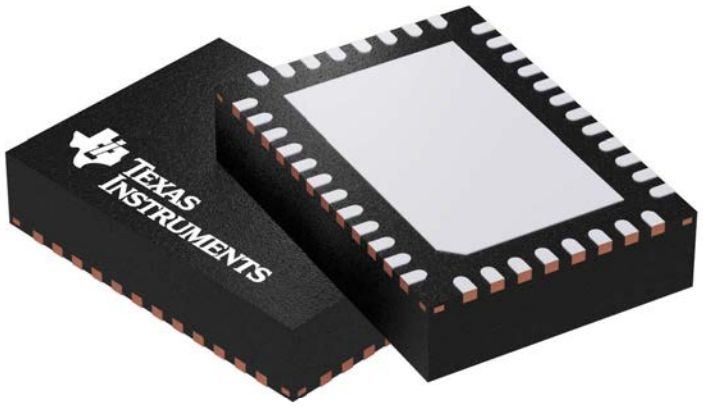


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS546D24RVFR	LQFN-CLIP	RVF	40	2500	367.0	367.0	38.0
TPS546D24RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0

RVF 40 LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



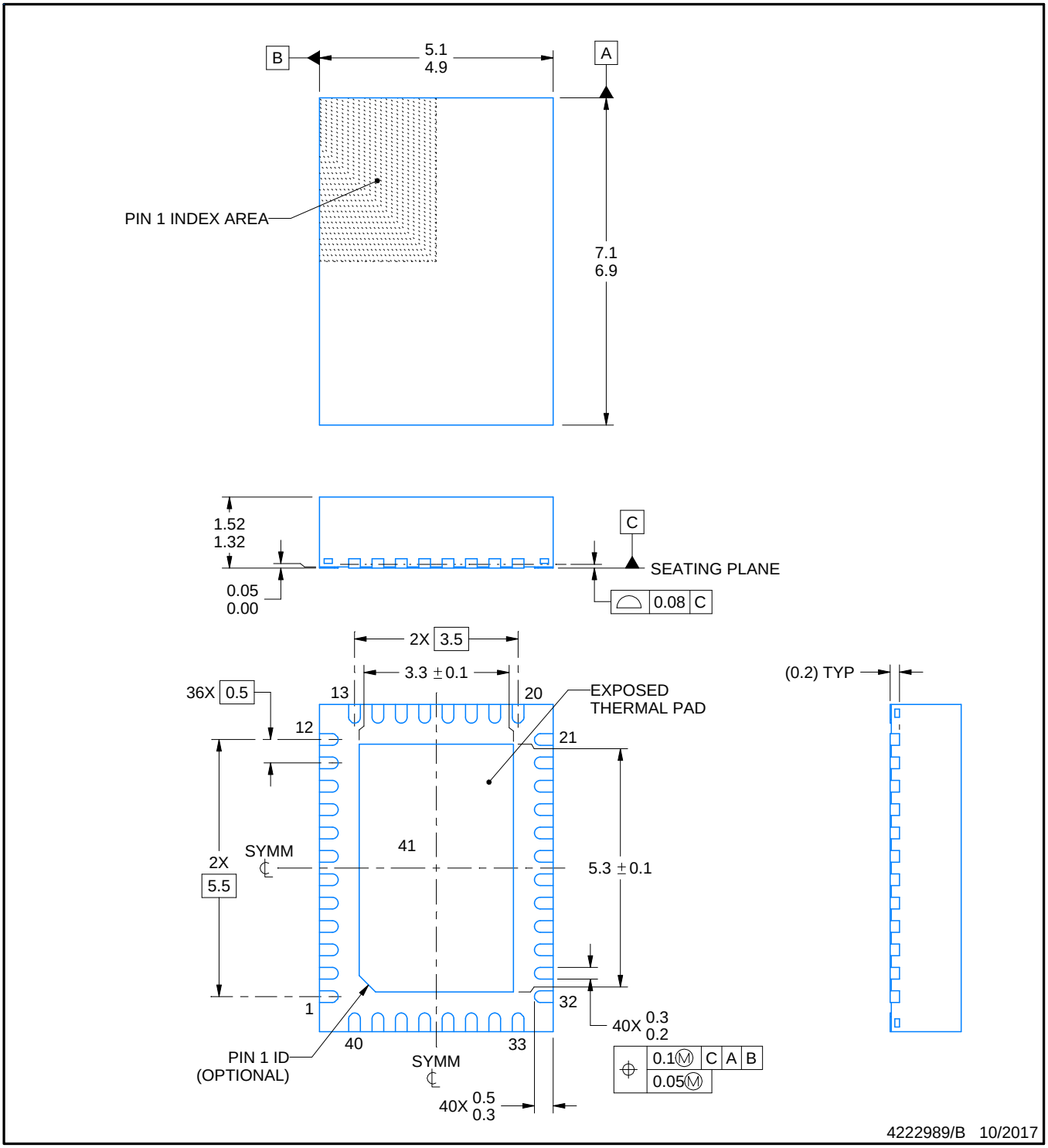
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RVF0040A

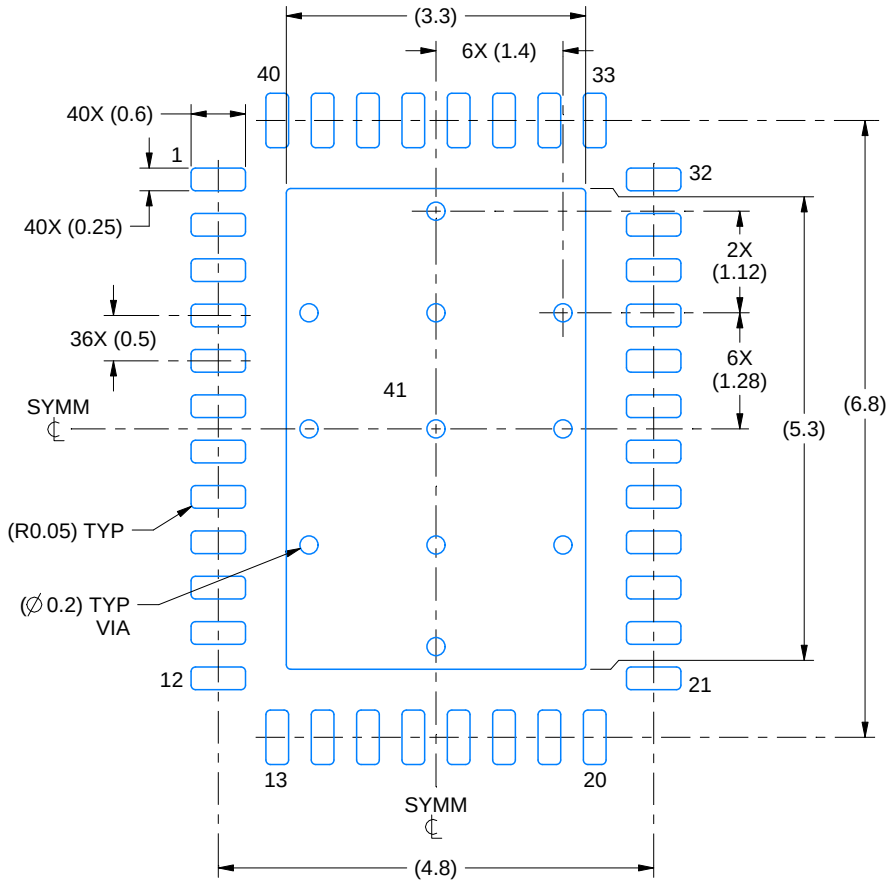
LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

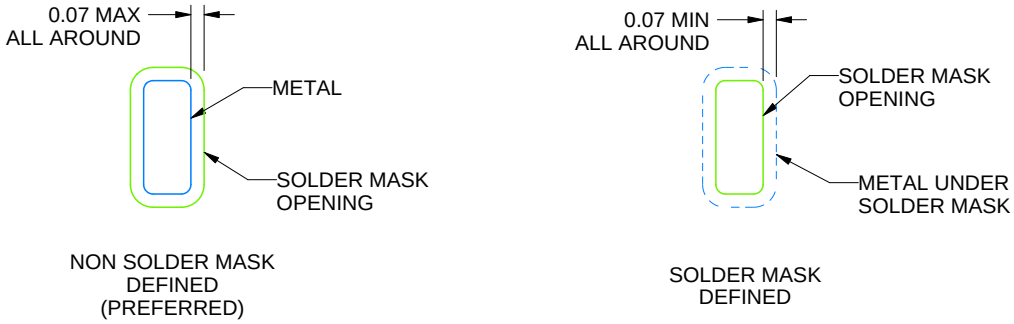


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:12X



SOLDER MASK DETAILS

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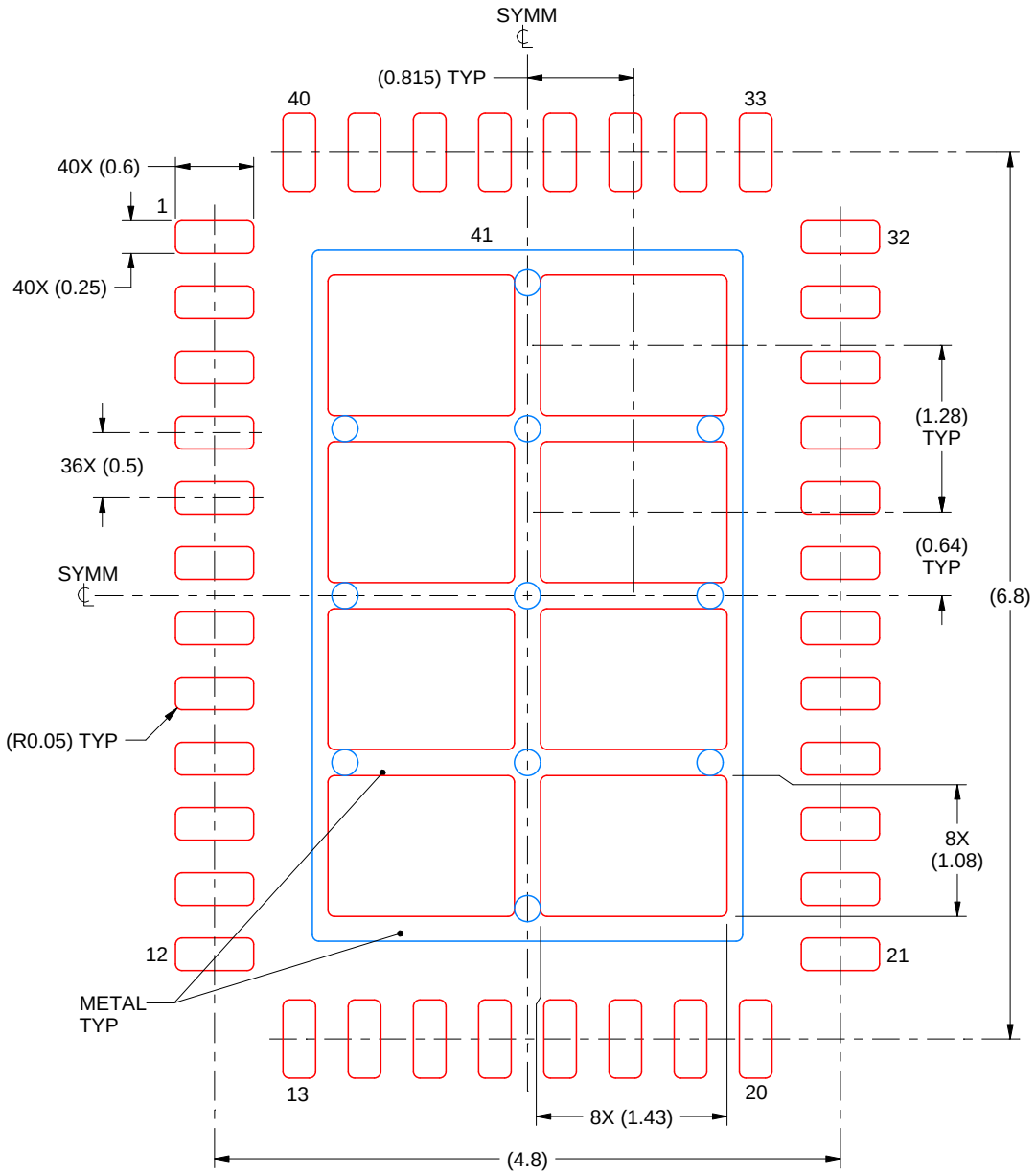
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
71% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222989/B 10/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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