TPS54A20 8V 至 14V 输入、10A、频率高达 10MHz 的 SWIFT™降压转换器

1 特性

- 双相同步串联电容降压转换器
- 自动相间电流均衡
- 2MHz 至 5MHz 的单相开关频率
- 最短导通时间为 14ns
- 输出电压范围为 0.51V 至 2V，反馈基准电压为 ±0.5%
- 输入过压锁定，实现 17V 浪涌保护
- 可调节电流限值，自动重启（断续）
- 与一个外部时钟同步
- 稳定状态下的频率固定
- 自适应导通时间控制
- 内部反馈回路补偿
- 支持外部电源选项的内部栅极驱动 LDO
- EN 引脚，支持可调节的输入欠压锁定 (UVLO)
- 可选软启动时间
- 针对预偏置输出的单调性启动
- 输出电源正常指示器（开漏）
- 输出过压/欠压保护

2 应用

- 电信、基站和通信设备
- 存储、固态硬盘 (SSD)、DDR 存储器、交换机、集线器、路由器和其他网络设备
- 薄型/背面板安装（高度低于 2mm）

3 说明

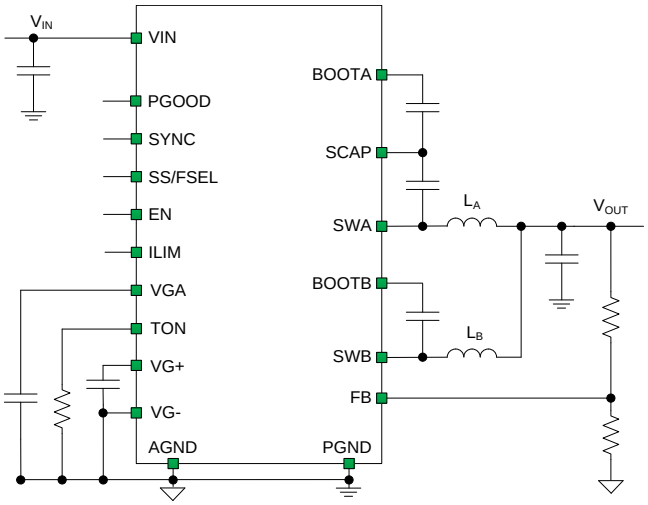
TPS54A20 是一款双相同步串联电容降压转换器，专为输入电压轨为 12V 的小尺寸、低电压 应用 而设计。该器件采用独特的拓扑结构，将开关电容电路与双相降压转换器融为一体，而且拥有诸多优势，其中包括电感间的自动电流均衡、较低的开关损耗（支持高频 (HF) 操作）以及通过串联电容实现降压。与 TPS54A20 搭配使用的低值薄型电感显著缩减了解决方案的面积和高度。该器件采用一种自适应导通时间控制架构，可在高达 10MHz 的工作频率下提供快速瞬态响应和精确稳压。通过使用锁相环 (PLL) 来锁定基准振荡器的开关信号，从而维持稳定状态下的固定频率操作。

器件信息(1)

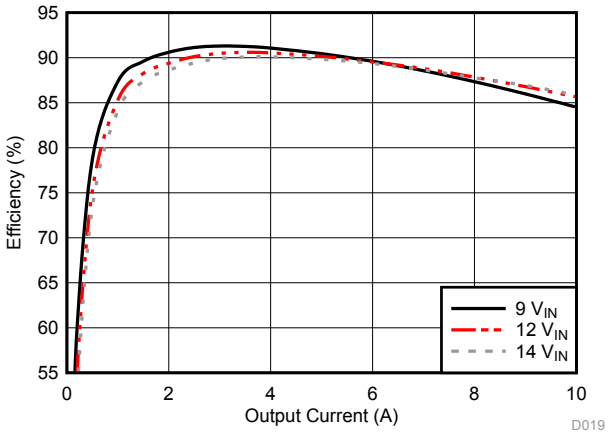
器件型号	封装	封装尺寸（标称值）
TPS54A20	VQFN（20 引脚）	3.5mm x 4mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



效率与负载电流间的关系



1.8 V_{OUT}，2MHz（每相位），外部 VG+，3.2mm x 2.5mm x 1.2mm 电感

目录

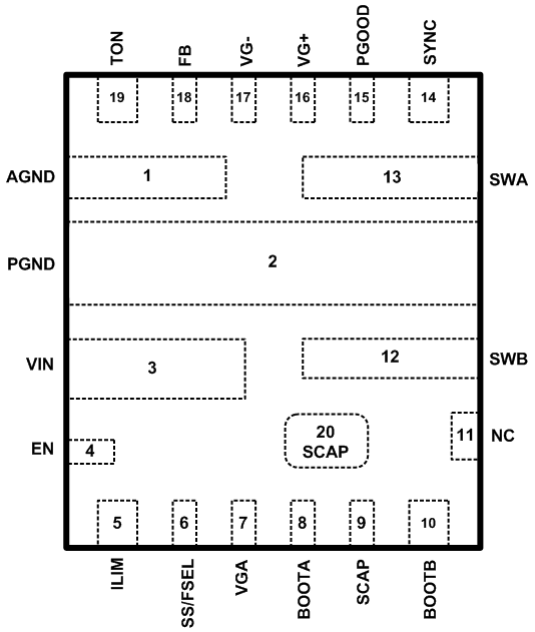
4 修订历史记录

Changes from Original (December 2015) to Revision A **Page**

- 已将器件状态改为“量产数据”。 1

5 Pin Configuration and Functions

RNJ Package
VQFN (20 Pin)
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog signal ground of the IC. AGND should be connected to PGND and VG- at a single point on PCB (e.g. underneath the IC).
BOOTA	8	S	Bootstrap capacitor node for phase A high-side MOSFET gate driver. Connect the bootstrap capacitor from this pin to the SCAP pin (pin 9).
BOOTB	10	S	Bootstrap capacitor node for phase B high-side MOSFET gate driver. Connect the bootstrap capacitor from this pin to the SWB pin.
EN	4	I	Enable pin. Floating this pin will enable the IC. Pull below 1.23V to enter shutdown mode. Can also be used to adjust the input undervoltage lockout above 8 V with two resistors.
FB	18	I	Feedback pin for voltage regulation. Connect this pin to the center tap of a resistor divider to set the output voltage.
ILIM	5	I	Current limit programming pin. A resistor between this pin and ground sets the current limit. If no resistor is included, the default load current limit is 15 A.
NC	11		No connect. This pin is not electrically connected to the IC and is included for board level reliability (BLR) purposes. Connect this pin to the SCAP trace.
PGND	2	G	Power ground of the IC. PGND should be connected to AGND and VG- at a single point on PCB (e.g. underneath the IC). Thermal vias to internal ground planes should be added beneath this pin.
PGOOD	15	O	Power good indicator. This pin is an open-drain output and will assert low if the output voltage is greater than ±5% away from the desired value or due to thermal shutdown, over-voltage/under-voltage, EN shutdown, or during soft start. A pull-up resistor can be connected between PGOOD and VG+ or an external logic supply pin.
SCAP	9,20	O	Series capacitor pin. Connect a ceramic capacitor from pin 20 to the SWA pin.
SS/FSEL	6	I	Soft start/frequency select pin. Connect a resistor from this pin to ground to set the soft-start time and the switching frequency. If no resistor is provided, the default setting of 4MHz oscillator frequency and 512µs soft start time is used.
SWA	13	O	Switching node for phase A. Connect an inductor from this pin to the output capacitors.
SWB	12	O	Switching node for phase B. Connect an inductor from this pin to the output capacitors.
SYNC	14	I	External clock synchronization pin. An external clock signal can be connected to this pin to synchronize the oscillator frequency (within ±10% of the nominal frequency set via SS/FSEL).

(1) I = Input, O = Output, S = Supply, G = Ground Return

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
TON	19	I	On-time selection. An external resistor from this pin to the AGND pin programs the nominal on-time of the high side switches.
VG+	16	S	Gate driver positive supply pin. Connect a bypass capacitor from this pin to VG-. To improve converter efficiency, the internal regulator can be overridden by connecting an external 5V supply to this pin. This supply rail also provides power to the control circuitry.
VG-	17	G	Gate driver supply return pin. VG- should be connected to PGND and AGND at a single point on PCB (e.g. underneath the IC).
VGA	7	S	High side phase A gate driver supply pin. Connect a bypass capacitor from this pin to ground.
VIN	3	I	The power input pin to the IC. Connect VIN to a supply voltage between 8 V and 14 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input Voltage	Power Conversion, VIN	DC w.r.t. PGND, switching	–0.3	15	V
		DC w.r.t. PGND, non-switching	–0.3	17	
	Bootstrap, $V_{(BOOTA)}$	DC with respect to PGND	–0.3	22	V
		DC with respect to SCAP		6	V
	Bootstrap, $V_{(BOOTB)}$	DC with respect to PGND	–0.3	14	V
		DC with respect to SWB		6	V
	Bias Supply, VG	DC with respect to PGND	–0.3	6	V
	Series Capacitor Node Voltage, $V_{(SCAP)}$	DC with respect to PGND	–0.3	16	V
	Switch Node Voltage, $V_{(SWA, SWB)}$	DC with respect to PGND	–1	9	
		Pulse < 10 ns	–4	14	
	Feedback, $V_{(FB)}$		–0.3	3	V
Output Voltage	Bias Supply, $V_{(VGA)}$	DC with respect to PGND	–0.3	15	V
Voltage	Enable Voltage, $V_{(EN)}$		–0.3	7	V
	Soft Start/Freq. Select, $V_{(SS/FSEl)}$		–0.3	3	
	Power Good Voltage, $V_{(PGOOD)}$		–0.3	6	
	External Sync Clock Voltage, $V_{(SYNC)}$		–0.3	6	
	Current Limit/Mode Select, $V_{(ILIM)}$		–0.3	3	
	On Time Pin Voltage, $V_{(TON)}$		–0.3	3	
Input Current	Power Conversion, $I_{(VIN)}$			6	A
	Bias Supply, $I_{(VG)}$			100	mA
Output Current	Switch Node A, $I_{(SWA)}$			Current Limit	A
	Switch Node B, $I_{(SWB)}$			Current Limit	A
Operating Junction Temperature, T_J			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	8		14	V
V_{OUT}	Output Voltage	0.5		V_{IN}/5	V
I_{OUT}	Output Current	0		10	A
T_J	Junction Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		RNJ	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Tested on four layer evaluation board.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	VIN Operating		8	12	14	V
	VIN Input UVLO Voltage	VIN rising	7.4	7.65	7.95	V
	VIN UVLO hysteresis			250		mV
	VIN Input OVLO Voltage	VIN rising		15.4	15.8	V
		VIN falling	14.1	14.8		V
	VIN OVLO hysteresis			600		mV
	Shutdown	EN < 0.4 V, V_{IN} = 12 V, T_A = 25°C		47		µA
I_Q	Operating into VIN	FB = 0.53 V, V_{IN} = 12 V, T_A = 25°C		6		mA
ENABLE (EN PIN)						
	Enable threshold		1.17	1.23	1.27	V
	Input current	Enable threshold + 50 mV		–4		µA
		Enable threshold – 50 mV		–1		µA
VOLTAGE REFERENCE						
	Voltage Reference	T_A = 25°C	0.5054	0.508	0.5106	V
		–40°C < T_J < 125°C	0.5029	0.508	0.5131	V
FREQUENCY						
f_{OSC}	Oscillator Frequency	$R_{(SS/FSEL)}$ = Open, 71.5 kΩ, or 48.7 kΩ	3.6	4	4.4	MHz
		$R_{(SS/FSEL)}$ = Short or 35.7 kΩ	6.3	7	7.7	MHz
		$R_{(SS/FSEL)}$ = 21.5 kΩ, 15.4 kΩ, or 8.66 kΩ	9	10	11	MHz
SYNC						
	Minimum Input Clock Pulsewidth				20	ns
	SYNC high threshold				2	V
	SYNC low threshold		0.8			V
	Frequency sync range			±10		% nominal
	Last SYNC falling/rising edge to return to resistor timing mode if SYNC is not present	10 MHz: 400 ns 7 MHz: 571 ns 4 MHz : 1 µs		4		Cycles
LOW-SIDE A MOSFET						
	On resistance	VG = 5 V, Measured at pins		6.8	10.5	mΩ
LOW-SIDE B MOSFET						
	On resistance	VG = 5 V, Measured at pins		9.3	14.8	mΩ
HIGH-SIDE MOSFETS						
	On resistance	Vgs = 5 V, Measured at pins		27	50	mΩ
	SW rise time 10% to 90%	VIN = 12 V		2		ns
	SW fall time 90% to 10%	VIN = 12 V		2		ns
CURRENT LIMIT						
	Peak Switch LSA Current Limit	~15A Load Trip, $R_{(ILIM)}$ = Open	12.7	16.3	19.9	A
		~11.25A Load Trip, $R_{(ILIM)}$ = 47 kΩ	9.9	12.7	15.5	
	Peak Switch LSB Current Limit	~15A Load Trip, $R_{(ILIM)}$ = Open	6.8	8.7	10.6	A
		~11.25A Load Trip, $R_{(ILIM)}$ = 47 kΩ	5.3	6.8	8.3	
	Overcurrent protection scheme			Hiccup		
	OCP cycle count to trip fault			3		Cycles
	Fault hiccup wait time	10 MHz: 13.1 ms 7 MHz: 18.7 ms 4 MHz: 32.8 ms		131,072		Cycles

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REGULATOR (VG LDO)					
Output Voltage	0 mA ≤ I_{VG} ≤ 100 mA	4.4	4.8	5	V
Current Limit		100	140		mA
Nominal Operating Current	Fosc = 10 MHz, I_{LOAD} = 10A		60		mA
DYNAMIC REGULATOR (VGA LDO)					
Output Voltage				15	V
	VIN = 12 V		10.5		V
SERIES CAP MONITOR					
Low Voltage Fault Trip			35	38	%VIN
Nominal Voltage			50		
High Voltage Fault Trip		62	65		
Capacitor Precharge Current		5.5	10	14.5	mA
POWER GOOD					
V_{FB} threshold	V_{FB} falling (Fault), UVP		90		%V_{REF}
	V_{FB} rising (Good)		95		
	V_{FB} rising (Fault), OVP		110		
	V_{FB} falling (Good)		105		
PGOOD sink current	$V_{(PGOOD)}$ = 0.4 V		2.7		mA
PGOOD pin leakage current	V_{FB} = V_{REF}, $V_{(PGOOD)}$= 5 V			1	µA
Minimum V_{IN} for valid PGOOD	$V_{(PGOOD)}$ ≤ 0.5 V at 100 µA		1.2	2.75	V
THERMAL SHUTDOWN					
Thermal shutdown set threshold			135		°C
Thermal shutdown hysteresis			20		°C
Thermal shutdown hiccup time	10 MHz: 13.1 ms 7 MHz: 18.7 ms 4 MHz: 32.8 ms		131,072		Cycles

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
ENABLE (EN PIN)					
Enable to Start Switching time	1 µF series cap, VIN = 12V		625		µs
SYNC					
Lock in time			30		µs
HIGH-SIDE MOSFETS					
SW minimum ON pulse width			14		ns
SW minimum OFF pulse width			10		ns
Non-Overlap Time between HS FET Off and LS FET On (deadtime)	Fsw = 5 MHz, VIN = 12 V		3		ns
Non-Overlap Time between LS FET Off and HS FET On (deadtime)			3		ns

6.7 Typical Characteristics

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.

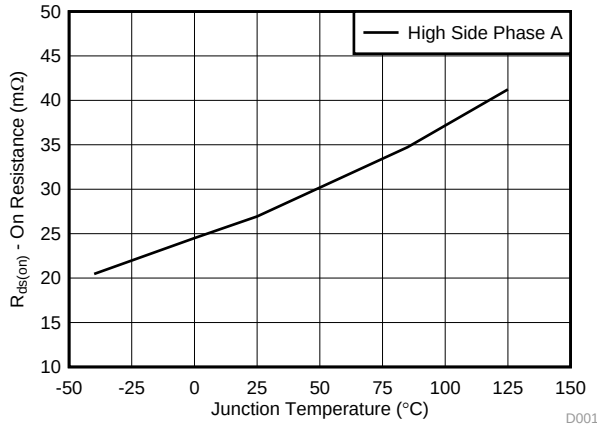


图 1. On Resistance vs Junction Temperature

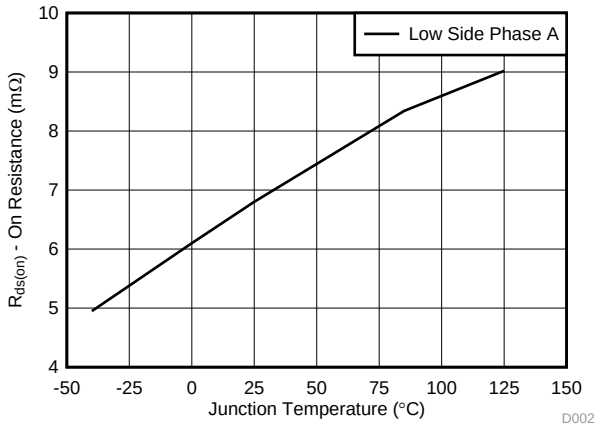


图 2. On Resistance vs Junction Temperature

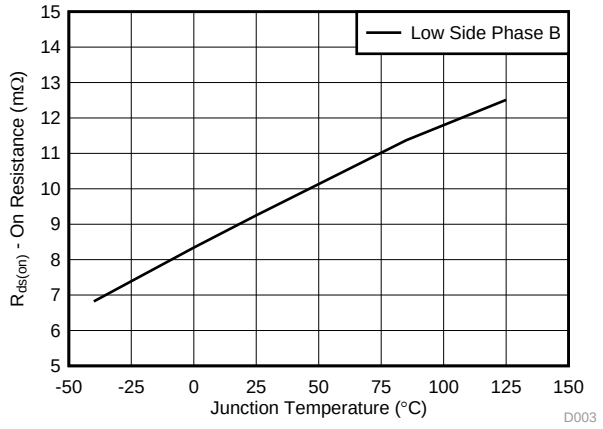


图 3. On Resistance vs Junction Temperature

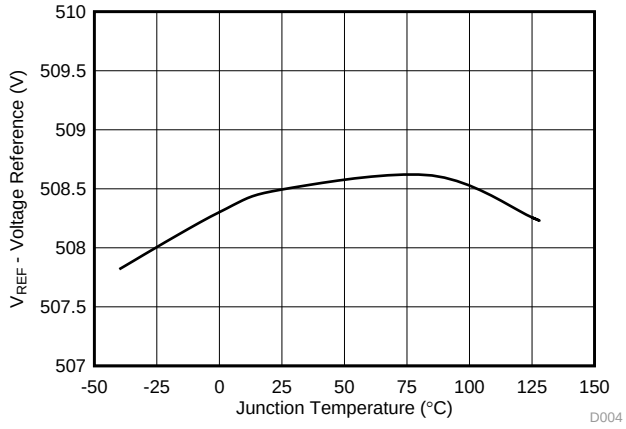


图 4. Voltage Reference vs Junction Temperature

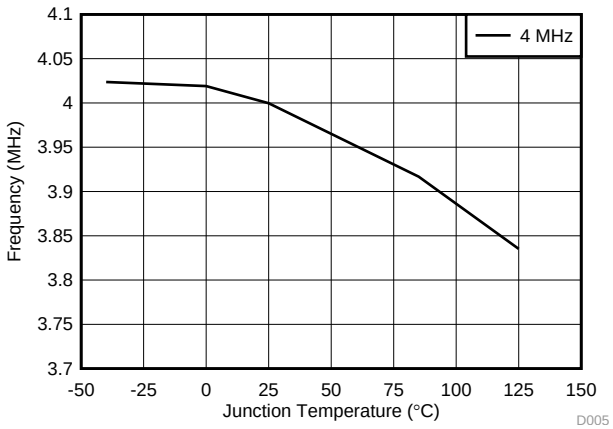


图 5. Oscillator Frequency vs Junction Temperature

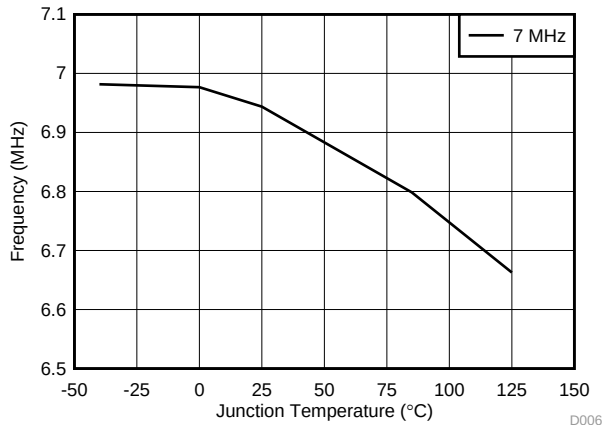


图 6. Oscillator Frequency vs Junction Temperature

Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.

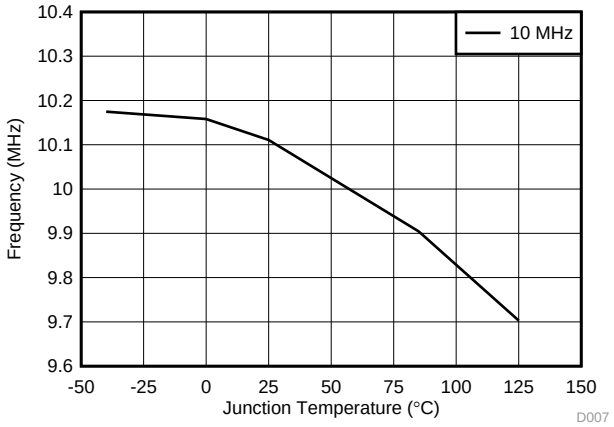
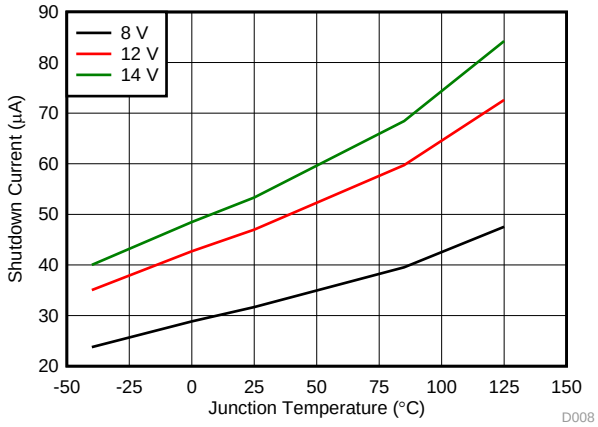
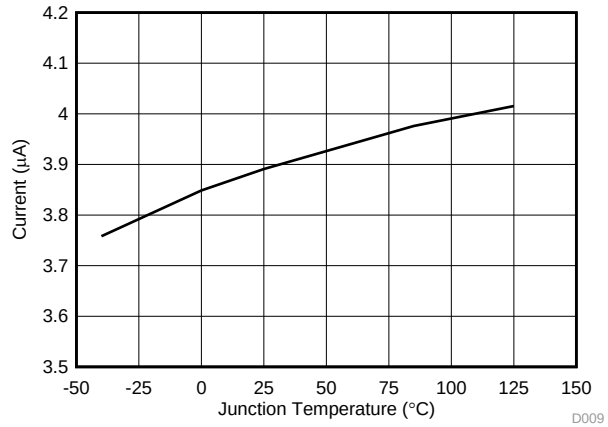


图 7. Oscillator Frequency vs Junction Temperature



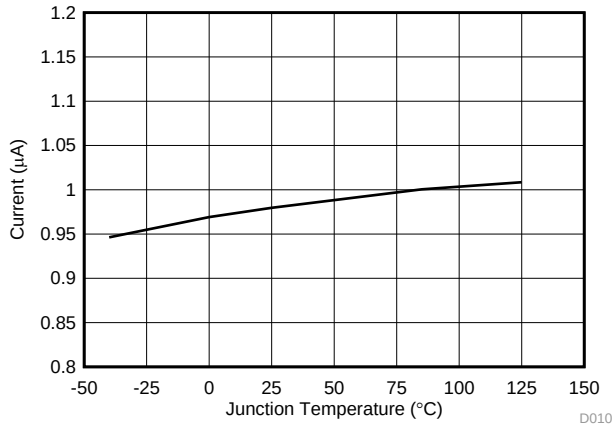
EN = 0 V

图 8. Shutdown Current vs Junction Temperature



EN = Threshold + 50 mV

图 9. EN Pin Current vs Junction Temperature



EN = Threshold - 50 mV

图 10. EN Pin Current vs Junction Temperature

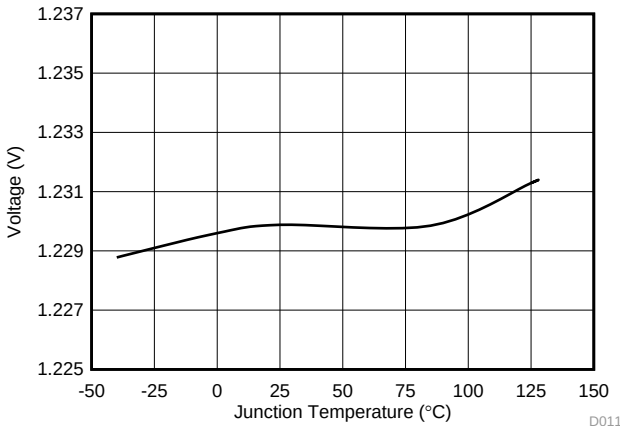
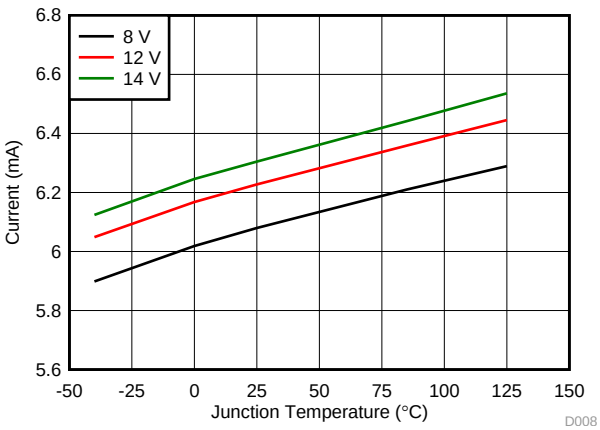


图 11. EN Pin Threshold vs Junction Temperature



FB = 0.53 V (non-switching)

图 12. Non-Switching Operating Current vs Junction Temperature

Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.

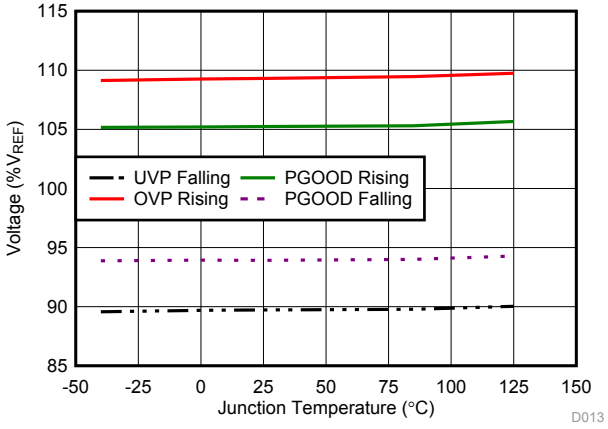


图 13. PGOOD and Under/Overvoltage Protection Threshold vs Junction Temperature

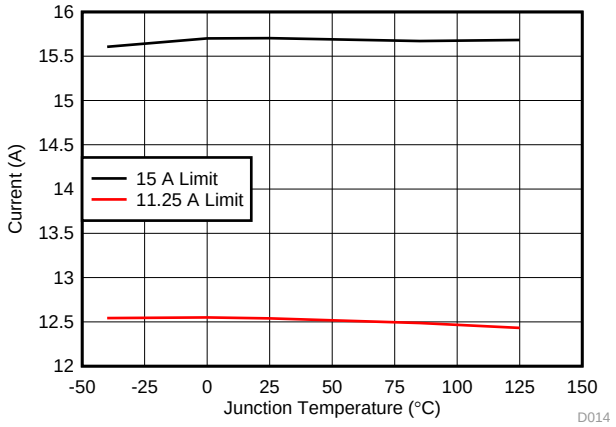


图 14. Phase A Low-Side MOSFET Current Limit vs Junction Temperature

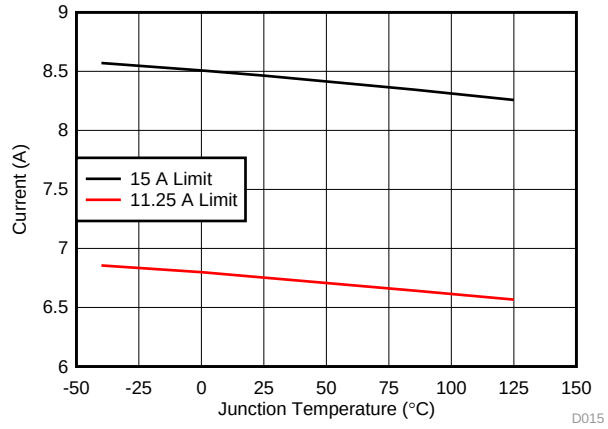


图 15. Phase B Low-Side MOSFET Current Limit vs Junction Temperature

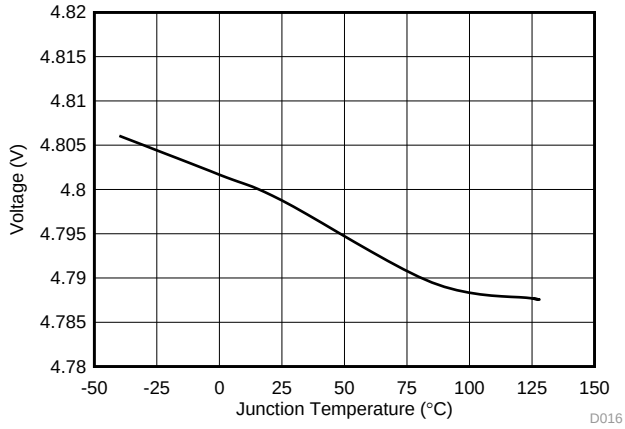


图 16. Internal Gate Drive Voltage (VG) vs Junction Temperature

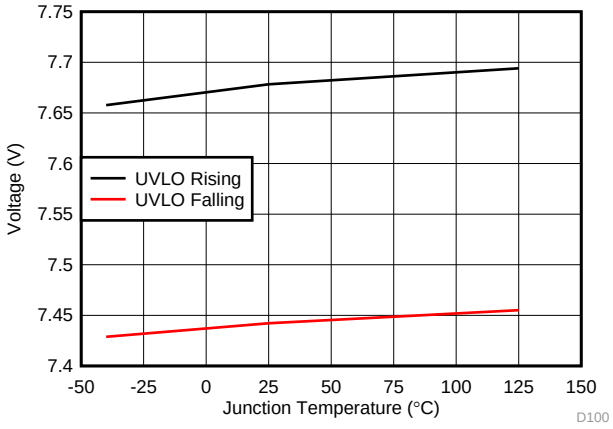


图 17. Undervoltage Lockout Threshold vs Junction Temperature

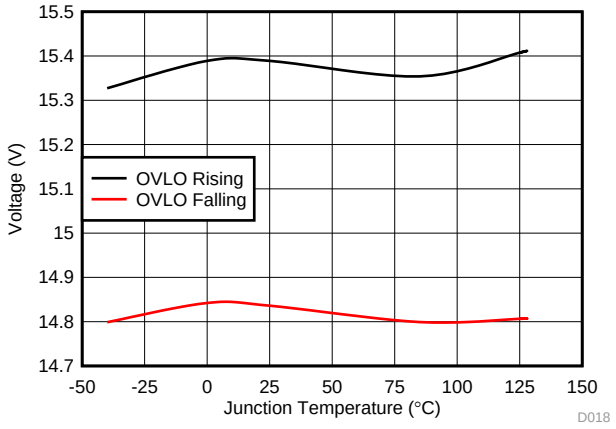
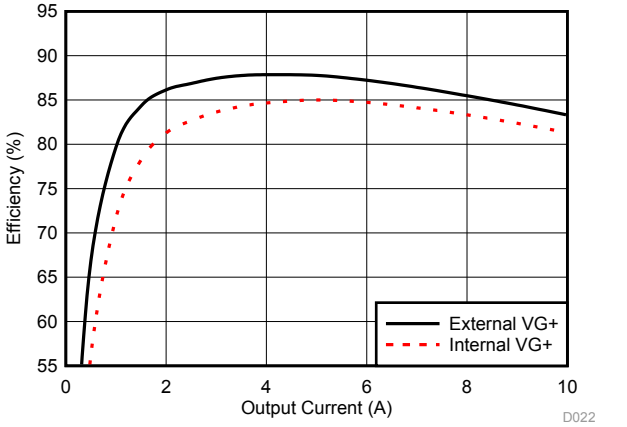


图 18. Overvoltage Lockout Threshold vs Junction Temperature

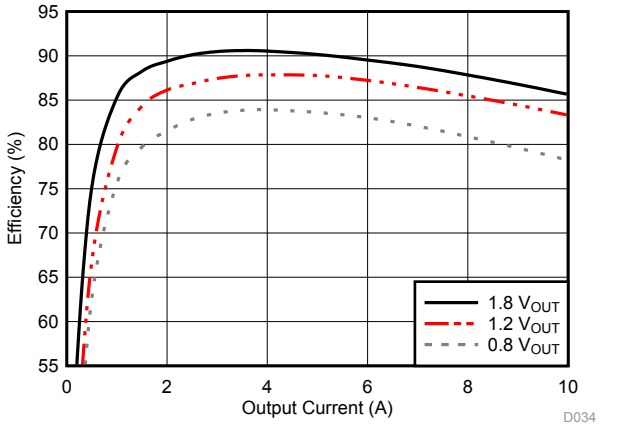
Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.



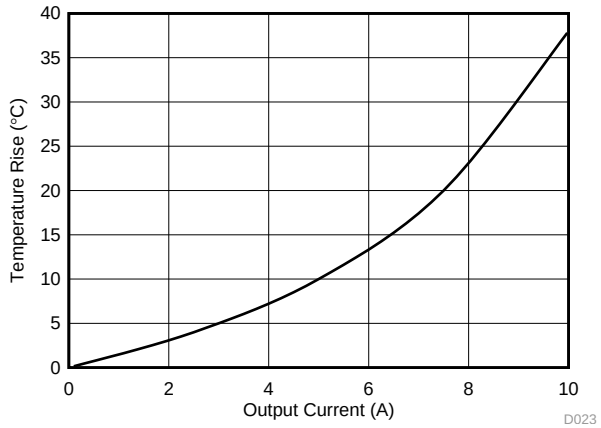
f_{sw} = 2 MHz per phase 3.2 x 2.5 x 1.2 mm inductors

图 19. Efficiency vs Output Current for Gate Drive Supply



f_{sw} = 2 MHz per phase External VG+ 3.2 x 2.5 x 1.2 mm inductors

图 20. Efficiency vs Output Current for Output Voltage



f_{sw} = 2 MHz per phase 3.2 x 2.5 x 1.2 mm inductors No air flow

图 21. Case Temperature Rise vs Output Current

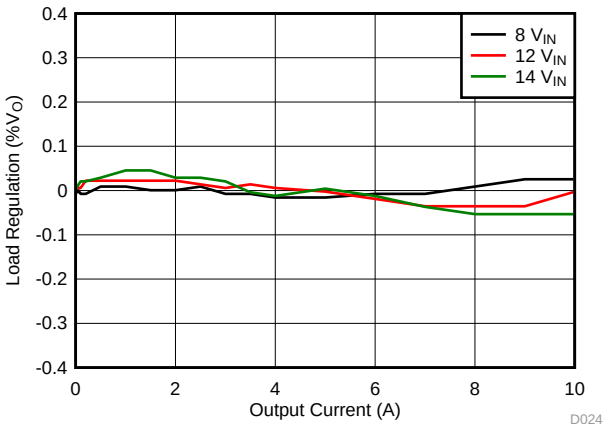


图 22. Load Regulation

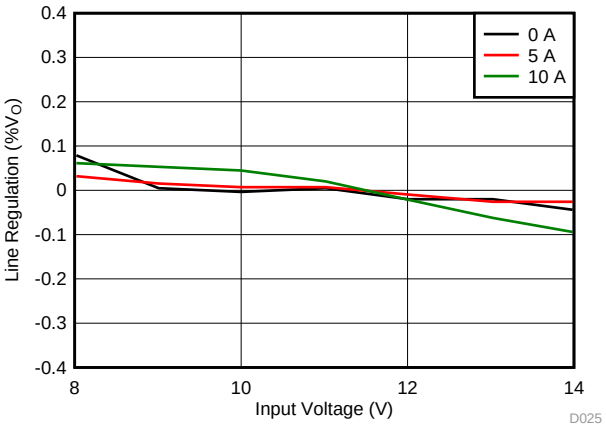


图 23. Line Regulation

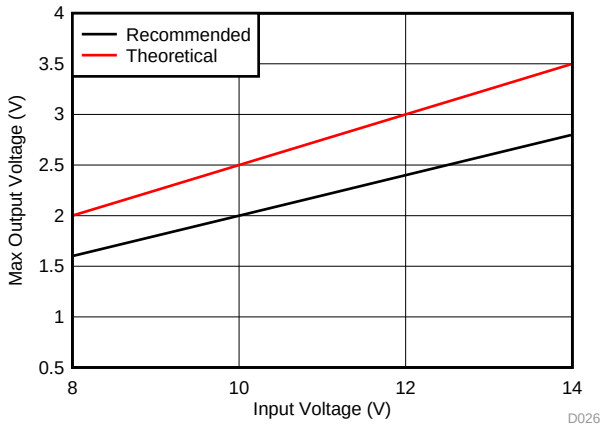


图 24. Max Output Voltage vs Input Voltage

Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.

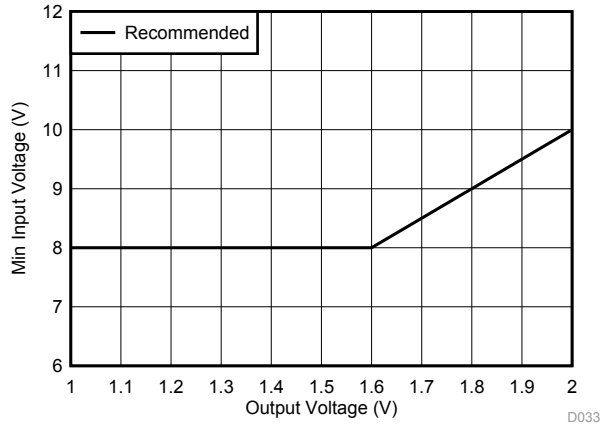


图 25. Min Input Voltage vs Output Voltage

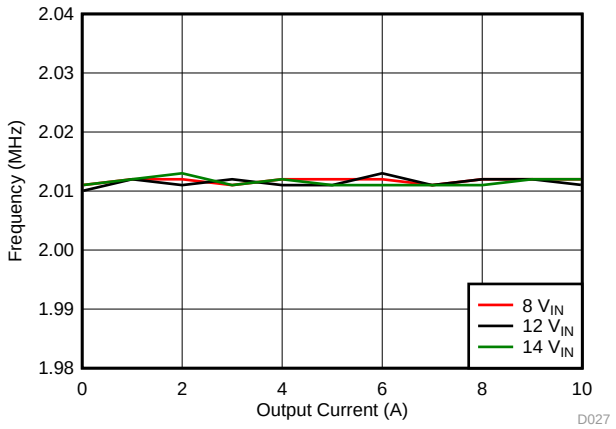
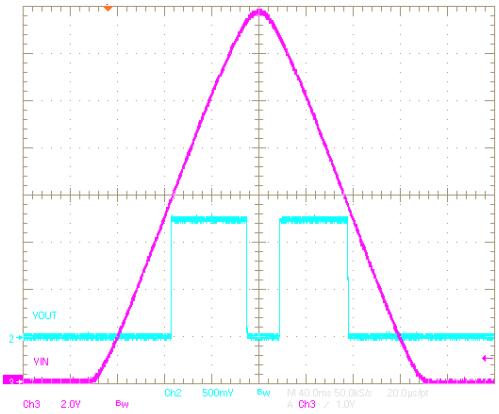
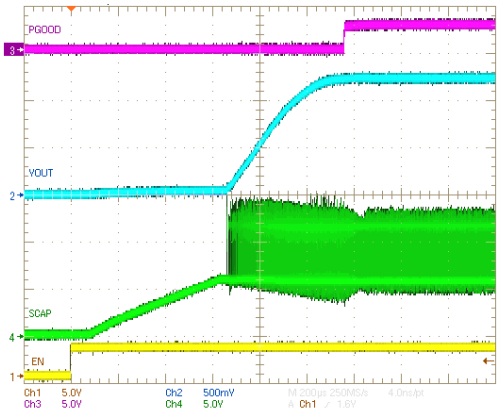


图 26. Frequency vs Output Current



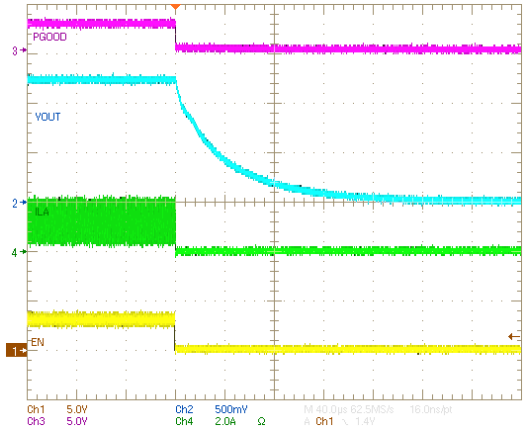
1 Ω Load f_{sw} = 2 MHz per phase
40 ms/div

图 27. Input UVLO and OVLO



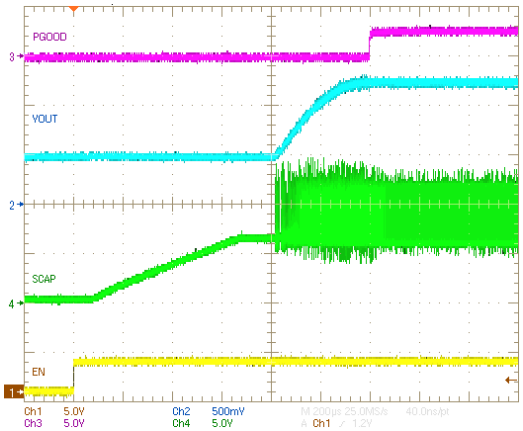
Series capacitance = 1 µF f_{sw} = 2 MHz per phase
200 µs/div

图 28. Startup Through EN



5 Ω Load f_{sw} = 2 MHz per phase 40 µs/div

图 29. Shutdown Through EN

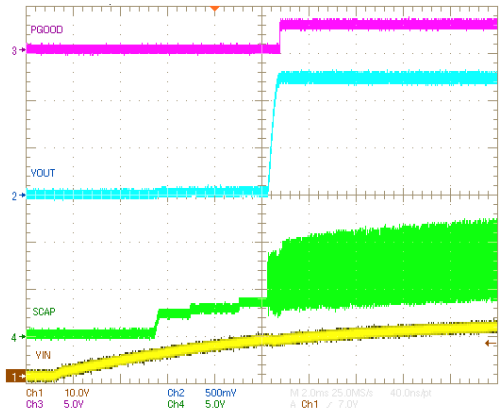


Series capacitance = 1 µF f_{sw} = 2 MHz per phase
200 µs/div

图 30. Pre-biased Startup Through EN

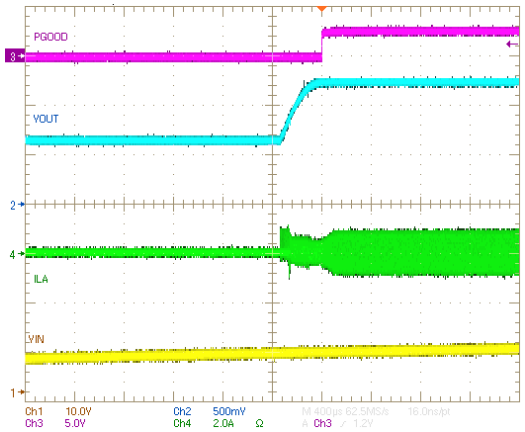
Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.



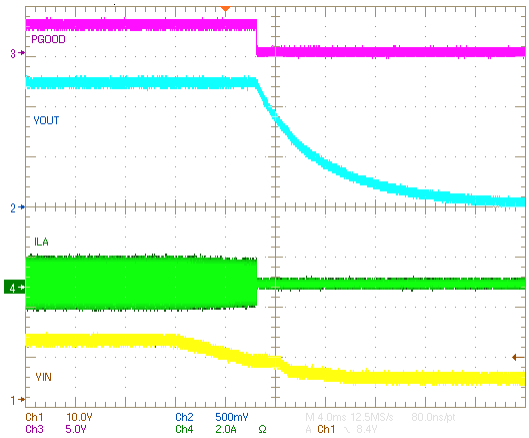
Series capacitance = 1 µF f_{sw} = 2 MHz per phase 2 ms/div

图 31. Startup Through VIN



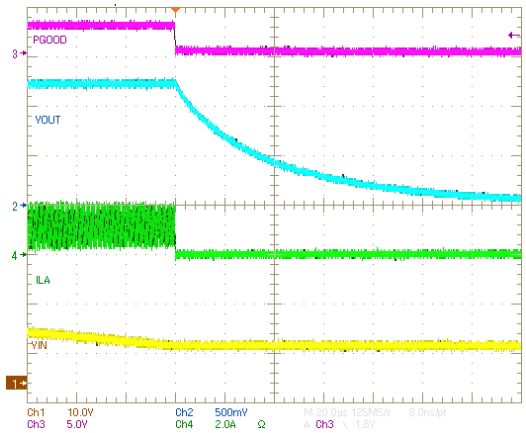
0 A Load f_{sw} = 2 MHz per phase 400 µs/div

图 32. Pre-biased Startup Through VIN



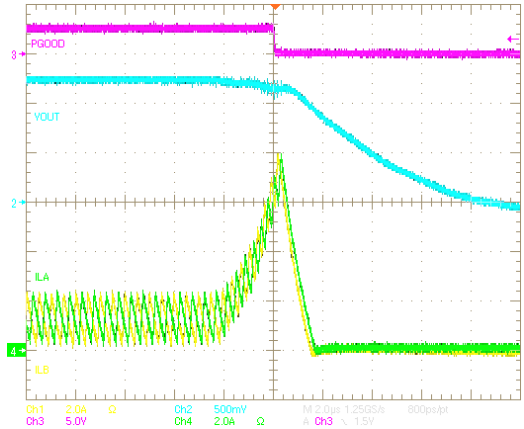
75 Ω Load 4 ms/div

图 33. Shutdown Through VIN



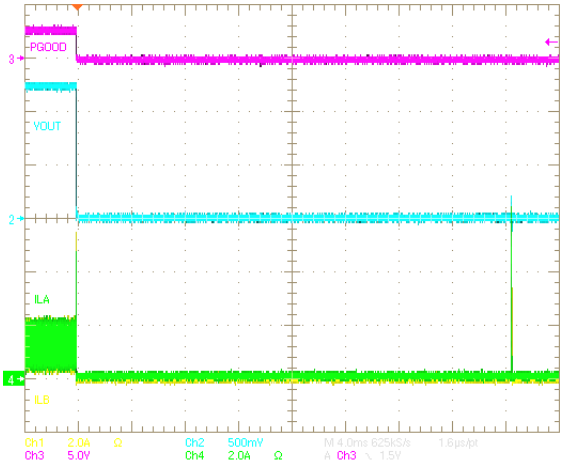
0.5 Ω Load 20 µs/div

图 34. Shutdown Through VIN



f_{sw} = 2 MHz per phase 2 µs/div

图 35. Short Circuit Protection

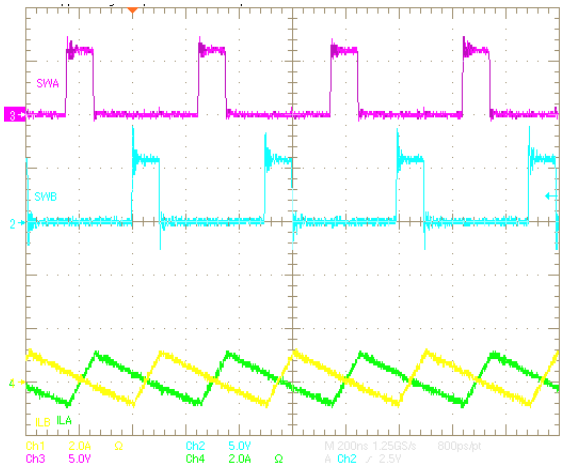


4 ms/div

图 36. Short Circuit Hiccup Restart

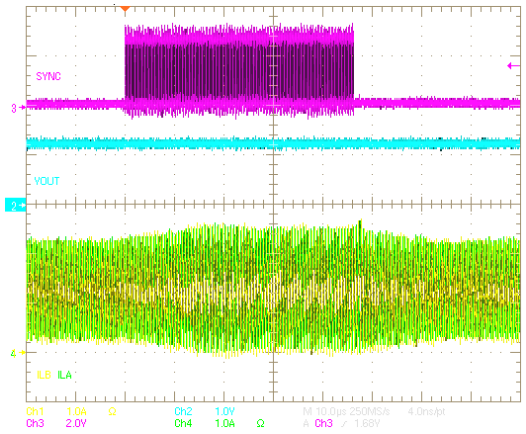
Typical Characteristics (接下页)

V_{IN} = 12 V, V_{OUT} = 1.2 V, T_A = 25 ºC, unless otherwise noted.



f_{sw} = 2 MHz per phase 0 A load 200 ns/div

图 37. Steady-State Waveforms



3.2 MHz SYNC clock

图 38. External SYNC Add/Remove

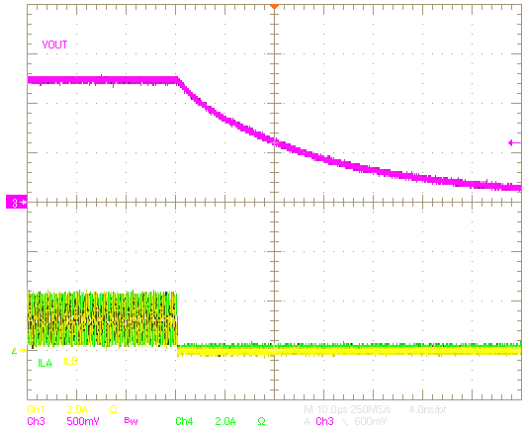


图 39. Thermal Shutdown

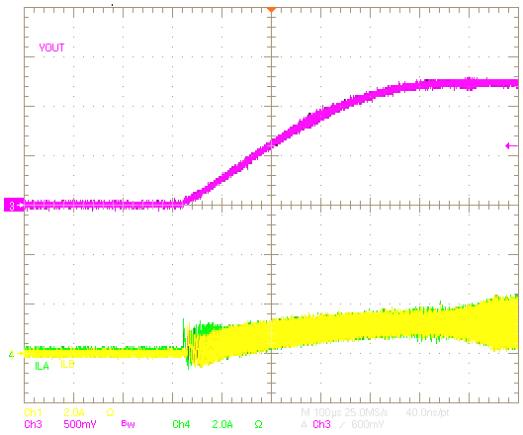
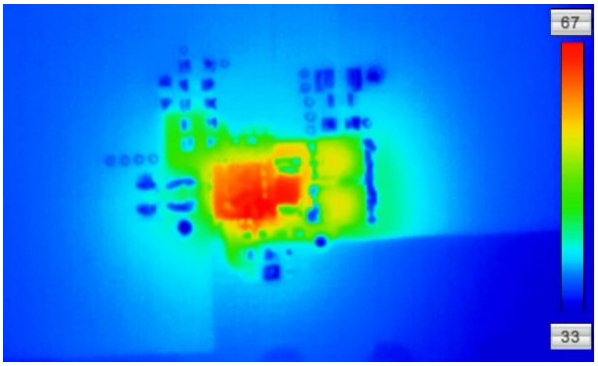


图 40. Thermal Shutdown Recovery



Room temperature 10 A load No air flow
f_{sw} = 2 MHz per phase 3.2 x 2.5 x 1.2 mm inductors Four layer board

图 41. Thermal Image

7 Detailed Description

7.1 Overview

The TPS54A20 is a 14-V, 10-A, synchronous series capacitor step-down (buck) converter with four integrated N-channel MOSFETs. To improve performance during line and load transients the TPS54A20 implements an adaptive on-time control scheme which does not require external compensation components. The selectable switching frequencies are 2 MHz, 3.5 MHz, or 5 MHz per phase which allows for efficiency and size optimization when selecting the output filter components. A resistor to ground on the TON pin sets the nominal high side switch on-time based on the desired output voltage.

The TPS54A20 contains an internal oscillator for steady-state, fixed frequency operation that is set through the SS/FSEL pin. The controller operates at twice the per phase switching frequency (that is, 4 MHz, 7 MHz, or 10 MHz) and the oscillator is set accordingly. An external synchronization clock can also be provided via the SYNC pin.

The TPS54A20 starts up safely into loads with pre-biased outputs (non-zero volts at startup). The device implements an internal under voltage lockout (UVLO) feature on the VIN pin with a nominal starting voltage of 7.65 V. The total operating current for the TPS54A20 is approximately 6 mA when not switching and under no load. When the TPS54A20 is disabled by pulling the EN pin low, the supply current is typically less than 50 µA.

The integrated MOSFETs allow for high-efficiency, high-density power supply designs with continuous output currents up to 10 A. The MOSFETs are sized to optimize efficiency for low duty cycle applications operating around 2 MHz per phase switching frequency.

The TPS54A20 reduces the external component count by integrating the bootstrap recharge circuit. Capacitors connected between the BOOTA/BOOTB and SCAP/SWB pins (respectively) supply the gate drive voltage for the integrated high-side MOSFETs. The output voltage can be stepped down to as low as the 0.5-V voltage reference (V_{REF}).

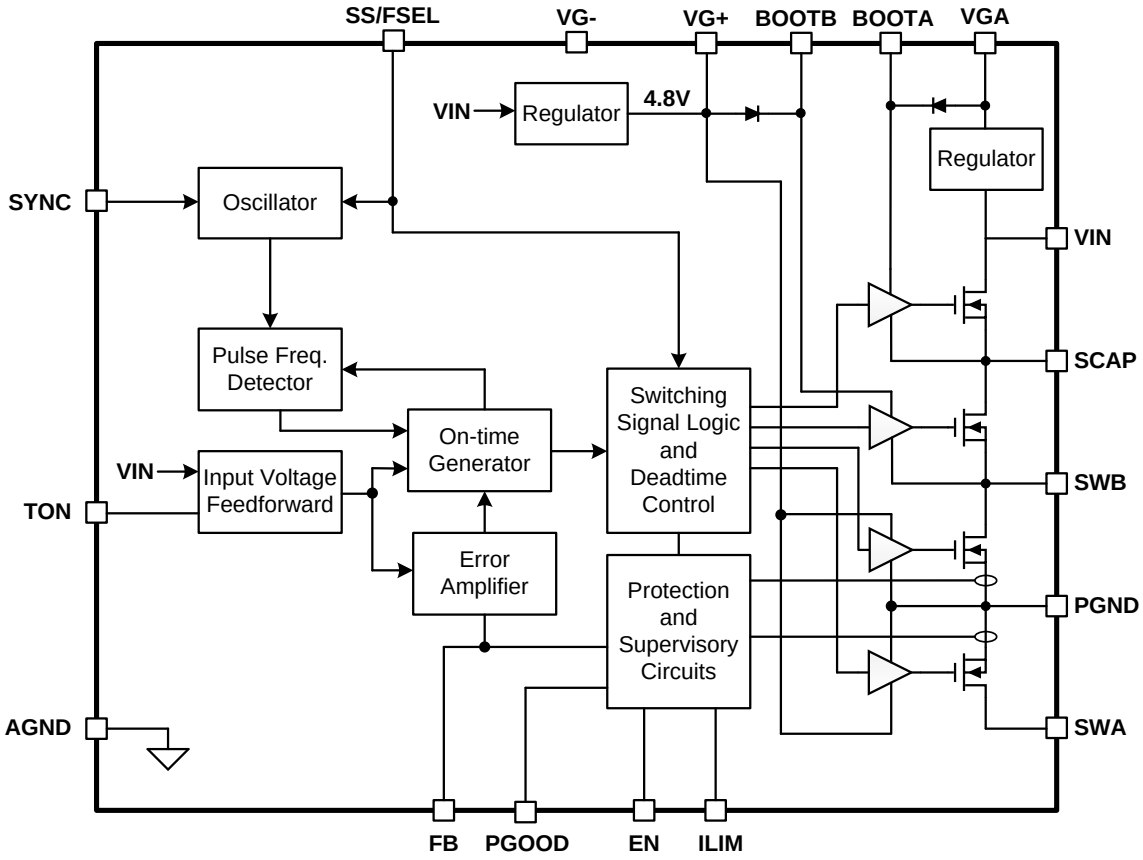
The TPS54A20 has a power good comparator (PGOOD) which monitors the output voltage through the FB pin. The PGOOD pin is an open-drain MOSFET which is pulled low when the FB pin voltage is less than 95% or greater than 105% of the reference voltage (V_{REF}). The PGOOD pin floats (de-asserted) when the FB pin voltage is between 95% to 105% of V_{REF}. The PGOOD pin is held low during startup or when a fault occurs.

The EN pin is used to provide power supply sequencing during power up. Soft start times for each frequency can be selected through the SS/FSEL pin. Soft start helps to minimize inrush currents.

The device current limit can be set via the ILIM pin. Two selectable current limits are provided.

The control scheme implemented is an adaptive on-time control. The on-time is adjusted based on input voltage and oscillator frequency. An internal phase lock loop (PLL) ensures fixed-frequency operation of the converter over the entire load range and adapts the on-time accordingly.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Frequency Selection

The oscillator frequency of this converter can be selected to be one of three options: 4, 7, or 10 MHz. The per phase switching frequency of the converter is half the oscillator frequency (that is, 2, 3.5, or 5 MHz per phase). The internal oscillator frequency is selected by programming the SS/FSEL pin. The resistor programming information is shown in 表 1. The frequency setting is latched in at power up and cannot be changed during operation. Cycling the input power or the EN pin will reset the frequency setting.

7.3.2 External Clock Syncronization

An external clock can be connected to the SYNC pin. The external clock signal overrides the internal oscillator and is used as the system clock. This feature enables the user to synchronize the switching events to a master clock on their board and reduce/manage the ripple on the input capacitors. The internal phase locked loop (PLL) has been implemented to allow synchronization at frequencies between ±10% of the nominal oscillator frequency programmed on the SS/FSEL pin. This allows the user to easily switch from the internal oscillator mode to the external clock mode. Before the external clock is present or after it is removed, the device with default to the internal oscillator setting as programmed on the SS/FSEL pin.

To implement the synchronization feature, connect a square wave clock signal to the SYNC pin with a duty cycle between 20% and 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2 V. The start of the switching cycle is synchronized to the rising edge of the SYNC pin. The device can be configured for operation in applications where both an internal oscillator mode and an external synchronization clock mode are needed. Before the external clock is present, the device functions with the internal oscillator and the switching

Feature Description (接下页)

frequency is set by the $R_{SS/FSEL}$ resistor. When the external clock is present, the SYNC mode overrides the internal oscillator. The first time the SYNC pin is pulled above the SYNC high threshold (2 V), the device switches from the internal oscillator mode to the SYNC mode and the PLL starts to lock onto the frequency of the external clock. When the external SYNC clock is removed, the converter will transition back to the internal oscillator after 4 internal clock cycles.

7.3.3 Adjusting the Output Voltage

The output voltage is set by connecting a resistor divider network from the output voltage to the FB pin of the device and to AGND. It is recommended that the lower divider resistor maintain a range between 1 kΩ and 10 kΩ. To change the output voltage of a design, it is necessary to select the value of the upper resistor. 公式 2 can be used to select the upper resistor. Selecting the value of the upper resistor can change the output voltage between 0.508 V and 2 V. The minimum output setpoint voltage cannot be less than the reference voltage of 0.508 V. The maximum output voltage can be limited by minimum input voltage as shown in 图 24. The recommended minimum input voltage should be at least five times the output voltage as shown in 图 25. This is due to the nature of the series capacitor buck converter.

7.3.4 Soft Start

Soft start is an important feature that limits current inrush into the converter and reduces the load on the bus converter that supplies this device. During soft start, the internal reference voltage is slowly ramped up to the nominal internal reference voltage (~0.5 V). This slowly increases the commanded output voltage of the converter and reduces the initial surge in current. PGOOD remains low during soft start, the PLL is not active, and output UVP/OVP faults are disabled. After the soft start interval is complete, the converter operates with normal operating conditions and PGOOD will no longer be held low when the output is within bounds.

Soft-start time is programmed with an external resistor on SS/FSEL pin (or by shorting to ground or by leaving the pin open). There are multiple soft-start time options per operating frequency available to the user through the SS/FSEL pin. The soft-start setting is latched in at power up or when the EN pin voltage is set high. Resistors used for programing the SS/FSEL pin must have ±1% or lower tolerance. The following frequencies and soft start times can be programmed on the SS/FSEL pin.

表 1. Frequency and Soft Start Resistor Selection

$R_{SS/FSEL}$ (kΩ)	F_{OSC} (MHz)	F_{SW} (MHz)	Soft Start Time (µs)	Hiccup Time (ms)
71.5	4	2	64	32.8
Open	4	2	512	32.8
48.7	4	2	4096	32.8
35.7	7	3.5	36.6	18.7
Short	7	3.5	293	18.7
21.5	10	5	25.6	13.1
15.4	10	5	205	13.1
8.66	10	5	1638	13.1

7.3.5 Startup into Pre-biased Outputs

The device prevents the low-side MOSFETs from discharging a pre-biased output. During pre-biased startup, the low-side MOSFETs do not turn on until after the phase A high-side MOSFET has started switching. The high-side MOSFETs do not start switching until the internal soft-start reference voltage exceeds the voltage at the FB pin. It is required to first apply the gate driver supply voltage (VG+) before starting up into pre-biased loads. Alternatively, 6.8 µF bypass capacitance or more can be used.

7.3.6 Power Good (PGOOD)

The Power Good (PGOOD) pin is an open drain output. After startup when the FB pin is typically between 95% and 105% of the internal voltage reference, the PGOOD pin pull-down is de-asserted and the pin floats. It is recommended to use a pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PGOOD is in a defined state once the VIN input voltage is greater than approximately 1.2 V but with reduced current sinking capability. The PGOOD achieves full current sinking capability once the VIN input voltage is above the input UVLO. The PGOOD pin is pulled low when the FB pin voltage is typically lower than 95% or greater than 105% of the nominal internal reference voltage. A resistor-capacitor (RC) filter can be connected to the PGOOD pin to filter out PGOOD being pulled low during large load transients if low output capacitance is used. The PGOOD pin is also pulled low if a fault is detected, the EN pin is pulled low, or the converter is performing its soft-start power up sequence.

7.3.7 Overcurrent Protection

The device protects itself from an overcurrent condition by a current limit detector. The device senses inductor currents using the low side MOSFETs. After three sequential overcurrent measurements are made (in phase A or B), the over current flag is triggered, the converter switches are turned off, and PGOOD is pulled low. The converter attempts to restart after a hiccup interval counter has expired (that is, 32.8 ms, 18.7 ms, or 13.1 ms when in 4 MHz, 7 MHz, or 10 MHz mode, respectively). This provides a hiccup response to an overcurrent condition.

The two overcurrent trip points are based on two full load applications of 7.5 A or 10 A. The overcurrent trip points correspond to the load demanding 1.5 times the full load current (11.25 A and 15 A, respectively). This provides enough margin for brief overshoots in inductor currents during a load transient while at the same time protecting against short circuits or other potentially catastrophic faults on the output. The table below lists the resistor values for programming the ILIM pin to select the desired overcurrent limit. Programming resistors with up to ±5% variation can be used. The current limit selection is latched in at power up and cannot be changed without cycling power input or the EN pin voltage.

表 2. Current Limit Selection

R_{ILIM} (kΩ)	Load Current Limit (A)
Open	15
47	11.25

7.3.8 Light Load Operation

The converter operates in forced continuous conduction mode (FCCM) under light load conditions. When operating in FCCM, the high side and low side MOSFETs are turned on and off in a complementary fashion and negative inductor current is allowed for part of the switching cycle. The switching frequency remains constant in FCCM.

7.3.9 Output Undervoltage/Overvoltage Protection

The device incorporates an output undervoltage/overvoltage protection (UVP/OVP) circuit to prevent damage to the load. This fault can be triggered during large, fast load transients if insufficient output capacitance is used. The UVP/OVP feature compares the FB pin voltage to internal thresholds. If the FB pin voltage is lower than 90% or greater than 110% of the nominal internal reference voltage, the converter is turned off (i.e. power MOSFETs are turned OFF), a fault is triggered, and the PGOOD pin is pulled low. When the fault hiccup interval is complete, the converter will attempt to restart.

7.3.10 Input Undervoltage/Overvoltage Lockout

The device incorporates an input undervoltage/overvoltage lockout (UVLO/OVLO) circuit. The converter will not operate if the input voltage is below the UVLO threshold. The OVLO circuit protects the converter if the input bus voltage flies higher than the input voltage rating of the device while it is switching. When the input voltage crosses the input rising OVLO trip threshold, the converter turns off all the switches (makes them high impedance) and PGOOD is pulled low. When the input voltage drops lower than the falling OVLO threshold, the converter restarts using the normal soft-start sequence. This feature increases the maximum input voltage the device can sustain without being damaged due to a fault in the system.

7.3.11 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low power state. There is no voltage hysteresis in the EN threshold. The rising and falling voltage thresholds occur at the same level.

The EN pin has an internal hysteretic current source. This allows the user to float the EN pin for self-enabling the device or to design the ON and OFF threshold input voltages with a resistor divider at the EN pin. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The EN pin can be configured as shown in 图 42. The EN pin has a 1 µA pull-up current i_P which sets the current source value before the start-up sequence. The device includes the second 3 µA current source i_H which is activated when the EN threshold voltage has been exceeded. To achieve clean transitions between the OFF and ON states, it is recommended that the turn OFF threshold is no less than 7.75 V, and the turn ON threshold is no less than 8 V on the VIN pin. It is also recommended to set the UVLO hysteresis to be greater than 500mV in order to avoid repeated chatter during start up or shut down. The value of $R_{EN(TOP)}$ and $R_{EN(BOT)}$ can be calculated using 公式 18 and 公式 19 as described in the applications section.

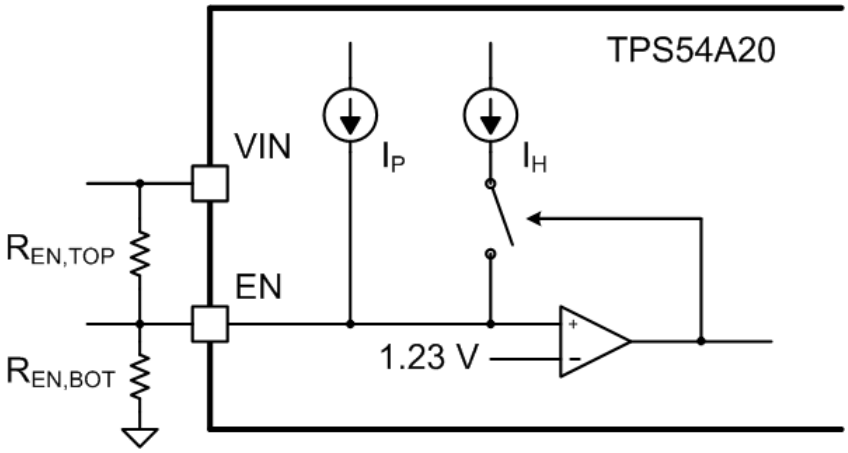


图 42. Adjustable VIN Undervoltage Lockout

7.3.12 Series Capacitor Monitoring

The series capacitor voltage is preconditioned and monitored during operation. The series capacitor is located between the source of the high-side MOSFET and the drain of the low-side MOSFET in Phase A . After the input voltage is above UVLO and the EN pin is high, the series capacitor is precharged. A 10 mA current source charges the series capacitor up to half the input voltage. When the series capacitor precharge is complete, the soft start sequence begins. The delay due series capacitor precharge can be calculated using 公式 1.

$$t_{pc} = \frac{C_t \times V_{IN}}{2 \times I_{pc}} \quad (1)$$

Here C_t is the series capacitance, I_{pc} is the precharge current, and V_{IN} is the input voltage.

The voltage monitor is continuously tracking the status of the series capacitor. Its function is to ensure the series capacitor voltage, measured differentially between the SCAP pin and the SWA pin, stays within predefined thresholds. These thresholds are relative to the VIN voltage with respect to PGND and set at 35% and 65% of VIN. If the voltage monitor indicates a voltage outside of these thresholds has occurred, a fault is triggered and following actions are taken based on which threshold has been crossed.

7.3.12.1 Dropping Below 35% Threshold

The 35% of VIN threshold detects a series capacitor undervoltage fault. Once the 35% threshold is breached, a fault is triggered, the converter shuts down, and PGOOD is pulled low. After the fault hiccup time is complete, the converter will start up in the normal manner. The start up sequence begins with pre-charging the series capacitor to half the input voltage and is followed by the soft start.

7.3.12.2 Rising Above 65% Threshold

The 65% of VIN threshold indicates a series capacitor overvoltage fault has occurred. Once the 65% threshold is breached, a fault is triggered, the converter shuts down, PGOOD is pulled low, and an internal bleed resistor is connected to the SCAP to reduce the series capacitor voltage. After the fault hiccup time is complete, the converter will start up in the normal manner.

7.3.13 Thermal Shutdown

The die temperature is continuously monitored to ensure it is within limits. The thermal shutdown (TSD) fault is triggered when the die temperature exceeds the rising temperature threshold. This interrupts switching by making the switches high impedance. The fault state persists until the die temperature cools down to below the falling temperature threshold. The converter then automatically goes through the normal soft start sequence.

7.3.14 Phase A Power Stage

Phase A implements a bootstrap driver for the high-side MOSFET, an LDO, a low-side driver and a low-side current monitor. Additional logic is included to implement deadtime control and overcurrent protection.

An LDO is implemented to manage the high-side bootstrap driver. This LDO is unique to this topology given the high-side driver is referenced to the SCAP pin and not to the conventional switch node of a buck converter. A conventional bootstrap circuit will not work because the SCAP pin is never connected to PGND during operation. The LDO is designed to produce an output voltage at the VGA pin. This allows a nominal enhancement of around 5V about the VIN rail. The bootstrap capacitor charges when the phase A low side switch is on. An external decoupling capacitor is required on the VGA pin.

The low-side MOSFET current is monitored using a sense FET configuration. This circuit enables the driver to monitor the current delivered in Phase A for overcurrent protection. In the case of overcurrent, a fault flag is set if the current detected exceeds the current limit threshold. Adjustment of this threshold is accomplished via programming the ILIM pin.

7.3.15 Phase B Power Stage

Phase B implements a bootstrap driver for the high-side MOSFET, a low-side driver and a low-side current monitor. Additional logic is included to implement deadtime control and overcurrent protection.

No additional LDO function is required for Phase B as the bootstrap capacitor is charged directly from the VG input rail. A conventional bootstrap circuit is used in phase B.

The overcurrent protection operates in the same manner as Phase A.

7.3.16 Internal Gate Drive Regulator

There is an internal linear regulator that generates a 4.8 V supply rail on the VG+ pin. The input comes from the VIN pin. The VG+ supply rail is used to power the gate drivers of phase A low side switch and phase B switches. It also is the input to another regulator that generates the internal supply rails used by the controller. To improve converter efficiency, an external 5V supply is recommended to be connected to the VG+ pin, thereby overriding the internal 4.8 V regulator. The VG+ supply requires external decoupling capacitance connected between the VG+ and VG- pins. The VG- pin must be connected to AGND and PGND. It is recommended to make this connection directly beneath the device.

7.3.17 Voltage Feed Forward

The input voltage feed forward (VFF) circuit adapts the nominal on-time of the converter in response to changes in the input voltage. The VFF provides a control signal to the on-time generator based on the value of the resistor placed on the TON pin and the input voltage.

7.3.18 Internal Oscillator

The internal oscillator provides a default system clock for the converter. The oscillator can be programmed to run at 4 MHz, 7 MHz, or 10 MHz depending on the resistor connected to the SS/FSEL pin. Synchronization to an external clock is allowed. If provided, an external synchronization clock signal is passed through to the oscillator block and bypasses internal oscillator.

7.3.19 Pulse Frequency Detector

The pulse frequency detector is an important block used to create a phase lock loop (PLL). This portion of the PLL accepts two clock signals and delivers a control signal. The PLL control is held inactive during startup and is activated once soft start is complete. The control signal is delivered to the on-time generator to make small adjustments in the on-time such that the frequency and phase of the switching signals match the reference clock (internal or external SYNC).

7.3.20 On-Time Generator

The on-time generator provides the on-time pulse for high side switches of the converter. The nominal on-time is programmed from the TON pin. The control signal generated by the VFF circuit is proportional to the on-time required by the converter and is adjusted for input voltage variation. Fine adjustment of the on-time comes from pulse frequency detector which enables fixed frequency operation in steady state.

8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54A20 is a two-phase, synchronous series capacitor buck converter optimized for small size, low voltage applications from a 12 V input rail. See (SLVA750) for a more detailed introduction to the series capacitor buck converter topology.

8.1.1 Two-Phase Series Capacitor Buck Converter Topology

The series capacitor buck converter topology uniquely merges a switched capacitor converter and a buck converter. Only one extra capacitor (the series capacitor) is needed as compared to a conventional two-phase buck converter. Advantages include automatic current balancing between the inductors (inductor current sensing and a current sharing loop are not required), lower switching losses which enable high frequency (HF) operation, and voltage step-down through the series capacitor. The on-time of both high side switches is double that of a regular buck converter. This is particularly helpful in high frequency, high conversion ratio applications. The schematic of the converter topology and the converter switch states are shown below.

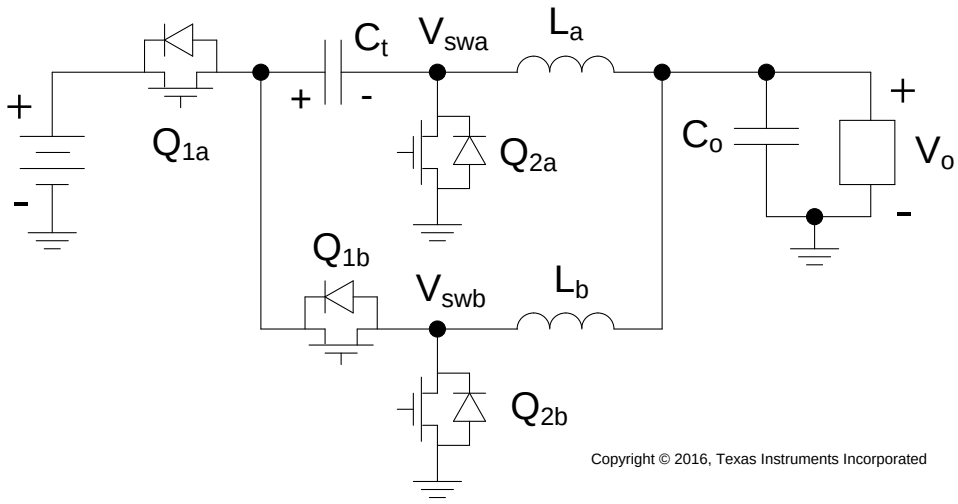


图 43. Two-Phase Series Capacitor Buck Converter Topology

8.1.2 Converter Switch Configurations

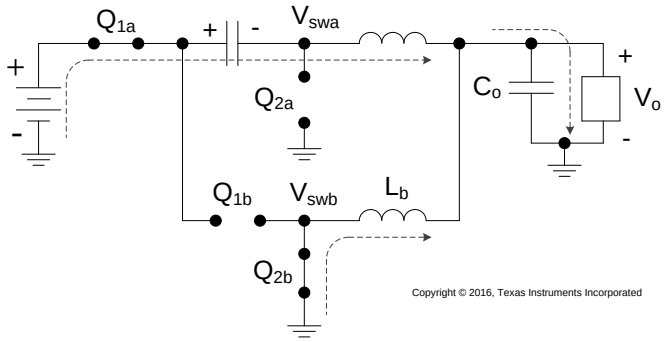


图 44. Phase A High Side MOSFET On

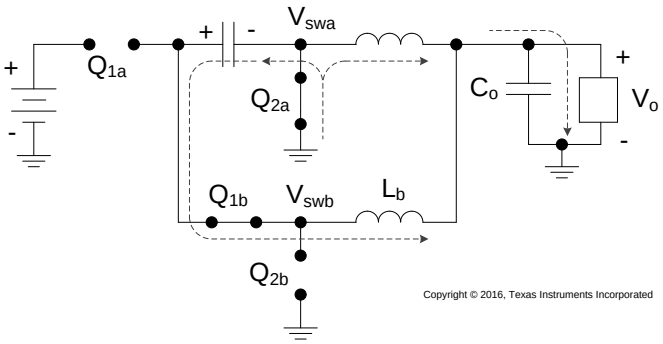


图 45. Phase B High Side MOSFET On

Application Information (接下页)

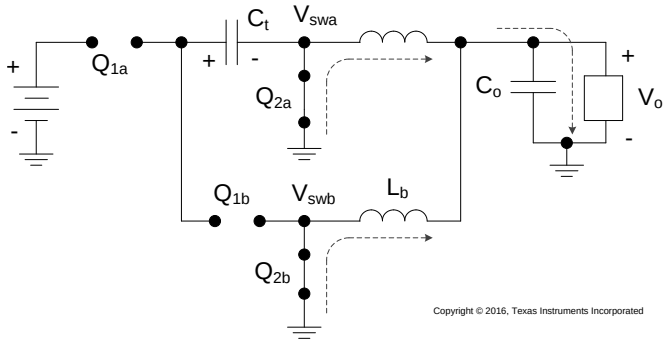


图 46. Phase A/B Low Side MOSFET On

8.2 Typical Application

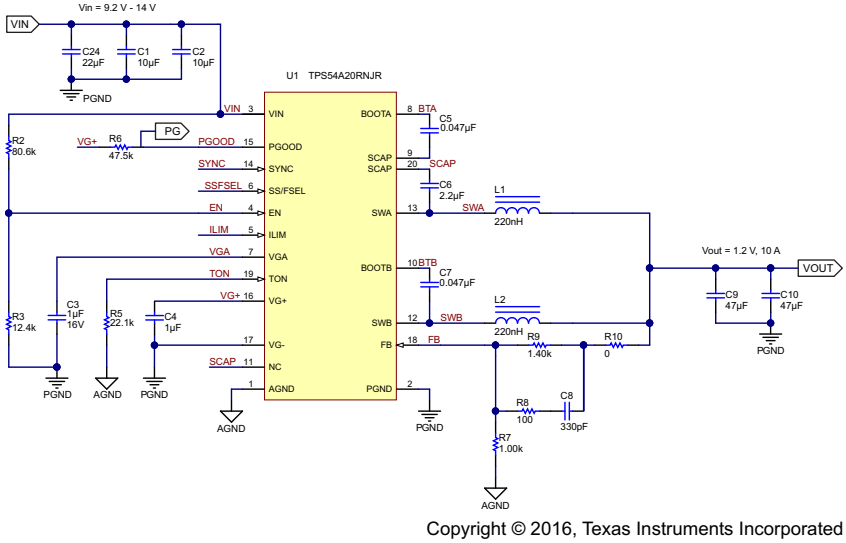


图 47. Typical Application

8.2.1 Design Requirements

表 3. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			10		A
ΔV_{OUT}	Transient response	9-A load step		60		mV
V_{IN}	Input voltage		9.2	12	14	V
$V_{OUT(ripple)}$	Output voltage ripple			20		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		9.4		V
	Stop input voltage	Input voltage falling		9.2		V
f_{SW}	Switching frequency			2		MHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage

Before beginning design, ensure that the series capacitor buck converter can be used in the application. It is recommended to use this converter when the minimum input voltage is at least five times greater than the target output voltage. If this recommendation is not followed, output voltage dropout can occur at heavy load conditions and poor transient response to load increases can result.

The output voltage is set by connecting a resistor divider network from the output voltage to the FB pin of the device and to AGND. It is recommended that the lower divider resistor maintain a range between 1 kΩ and 10 kΩ. To change the output voltage of a design, it is necessary to select the value of the upper resistor. The value of R_{TOP} for a specific output voltage can be calculated using 公式 2.

$$R_{(TOP)} = \frac{R_{(BOT)} x \left(V_{OUT} - V_{REF}\right)}{V_{REF}} \quad (2)$$

For the example design, 1 kΩ was selected for R_{BOT} (R7). Using 公式 2, R_{TOP} (R9) is calculated as 1.4 kΩ. It is recommended to use resistors with ±1% or less variation.

A capacitor can be connected in parallel with the upper resistor to provide additional phase boost near the converter's crossover frequency. See (SLVA289) for more details and design guidelines. For this design, 330 pF in series with 100 Ω is used. The values were optimized based on measured loop performance.

8.2.2.2 Switching Frequency

A key design step is to decide on a switching frequency for the regulator. There is a tradeoff between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency creates extra switching loss, which reduces the converter's efficiency and thermal performance. In this design, a moderate switching frequency of 2 MHz per phase is selected to achieve both a small solution size and a high efficiency operation. Refer to 表 1 for the SS/FSEL programming resistor selection.

8.2.2.3 On-Time

The TON pin requires a resistor to set the nominal on-time and to support the input voltage feedforward circuit. The resistance value used also influences the internal ramp in the controller. As a starting point, 公式 3 is recommended for selecting the TON resistor.

$$R_{(TON)} = 3\ k + 15\ k\ x\ V_{OUT} \quad (3)$$

The R_{TON} resistor (R5) is calculated to be 21 kΩ. The selected value for this design example is 22.1 kΩ. During startup, the converter uses the nominal on-time programmed through TON. The phase lock loop (PLL) is only activated after startup is complete. When the PLL is engaged, the on-time is adjusted. If the nominal on-time programmed through the TON pin is not close to the on-time when the PLL is engaged, the SYNC range of the device may be reduced. The TON resistor can also be adjusted to tune the controller. Lowering the R_{TON} value will increase the internal ramp height. This will reduce the converter's sensitivity to noise and jitter but it will also reduce the transient response capabilities of the converter.

8.2.2.4 Inductor Selection

To calculate the value of the output inductors, use 公式 4. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.4 for the majority of applications.

$$L = \frac{2\ x\ V_{OUT}\ x\ \left(V_{IN(MAX)} - 2\ x\ V_{OUT}\right)}{K_{(IND)}\ x\ I_{OUT}\ x\ V_{IN(MAX)}\ x\ F_{SW}} \quad (4)$$

For this design example, use K_{IND} = 0.4 and the inductor value is calculated to be 249 nH. For this design, the nearby standard value of 220 nH was chosen. For the output filter inductor, it is generally recommended that the RMS current and saturation current ratings not be exceeded. The current ripple, RMS, and peak inductor current are calculated in 公式 5, 公式 6, and 公式 7.

$$\Delta I_L = \frac{2 \times V_{OUT} \times \left(V_{IN(MAX)} - 2 \times V_{OUT}\right)}{L \times V_{IN(MAX)} \times F_{SW}} \quad (5)$$

$$I_{L(RMS)} = \sqrt{\left(\frac{I_{OUT}}{2}\right)^2 + \frac{1}{12} \times \left(\Delta I_L\right)^2} \quad (6)$$

$$I_{L(PEAK)} = \frac{I_{OUT}}{2} + \frac{\Delta I_L}{2} \quad (7)$$

For this design, the RMS inductor current is calculated to be 5.04 A and the peak inductor current is 6.13 A. The chosen inductor is 220 nH with a saturation current rating of 8.2 A and a dc current rating of 7.6 A.

The current flowing through each inductor is the inductor ripple current plus half the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than half the load current limit rather than the peak inductor current in steady state. Many inductors today have soft saturation characteristics that may be able to ride through a transient that pushes current beyond the saturation rating specified in the datasheet. An example list of inductors that have been tested to work with the TPS54A20 are shown in 表 4. Inductors not listed below can also be used with this device.

表 4. Example Inductor List

Inductance (nH)	Saturation Current Rating (A)	Dimensions [L x W x H] (mm)	DCR Typ/Max (mΩ)	Type	Vendor
220 ±20%	9.3	3.2 x 2.5 x 1.2	9 / 12	HMLW32251B-R22MS	CYNTEC
330 ±20%	7.5	3.2 x 2.5 x 1.2	13 / 16	HMLW32251B-R33MS	CYNTEC
220 ±30%	8.2	3.2 x 2.5 x 1.2	7.5 / 10.5	MLA-FY12NR22N-M3	MAGLAYERS
330 ±30%	7.5	3.2 x 2.5 x 1.2	13.5 / 16	MLA-FY12NR33N-M3	MAGLAYERS
220 ±20%	8.7	3.2 x 2.5 x 1.2	9.4 / 11.6	MCMK3225TR22MG	TAIYO YUDEN
330 ±20%	10.4	3.2 x 2.5 x 1.2	11.2 / 13.8	MCMK3225TR33MG	TAIYO YUDEN
250 ±30%	12	3.2 x 2.5 x 1.5	10 / 12.5	74479290125	WURTH ELECTRONIK
330 ±30%	12.4	4.1 x 4.1 x 2.1	6 / 7.2	744383560033	WURTH ELECTRONIK
220 ±20%	10.1	3.5 x 3.2 x 1.5	7.8 / 8.9	XEL3515-221	COILCRAFT
350 ±20%	8.2	3.5 x 3.2 x 1.5	11.6 / 13.4	XEL3515-351	COILCRAFT
330 ±20%	8.5	2.5 x 2.0 x 1.2	14 / 19	DFE252012F-R33M	TOKO

8.2.2.5 Output Capacitor Selection

For most applications, the primary consideration for selecting the value of the output capacitor is how the regulator responds to a large change in load current. The output capacitance may also be selected based on output voltage ripple or closed-loop bandwidth design objectives.

The output capacitance required to maintain an output voltage ripple ΔV_{OUT} during steady-state operation can be estimated using 公式 8.

$$C_O > \frac{\Delta I_L}{16 \times f_{SW} \times \Delta V_{OUT}} \quad (8)$$

The desired response to a large change in the load current is typically the most stringent criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast change in the load current such as a transition from no load to full load. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The minimum output capacitance required for a load increase can be estimated using 公式 9.

$$C_O > \frac{2 \times L \times (\Delta I_{OUT})^2}{(V_{IN} - 4 \times V_{OUT}) \times \Delta V_{OUT}} \quad (9)$$

In low voltage applications, the inductor slew rate during a load step decrease is sometimes slower than its slew rate during a load step increase. The minimum output capacitance required for a load decrease can be estimated using 公式 10 for a given tolerable amount of overshoot in the output voltage.

$$C_O > \frac{L \times (\Delta I_{OUT})^2}{4 \times V_{OUT} \times \Delta V_{OUT}} \quad (10)$$

Here ΔI_{OUT} is the change in output current and ΔV_{OUT} is the allowable change in the output voltage. For this design example, the transient load response is specified as a 3% change in V_{OUT} for a load step of 5A. For this example, ΔI_{OUT} = 5 A and ΔV_{OUT} = 0.03 x 1.2 = 0.036 V. Based on these design parameters, a minimum capacitance of 93 µF is calculated using 公式 9. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which also increases this minimum value. For this design example, two 47 µF, 6.3 V rated, ceramic capacitors with 3 mΩ of ESR are selected.

8.2.2.6 Input Capacitor Selection

The TPS54A20 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the VIN input voltage pin. Additional bulk capacitance may also be required for the VIN input. The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is selected to support the maximum input voltage. The input capacitance value impacts the input ripple voltage of the regulator. The minimum input capacitance can be estimated using 公式 11.

$$C_{IN(MIN)} = \frac{2 \times I_{OUT} \times V_{OUT} \left(V_{IN(MIN)} - 2 \times V_{OUT}\right)}{f_{SW} \times V^2_{IN(MIN)} \times \Delta V_{IN}} \quad (11)$$

Here ΔV_{IN} is the input voltage ripple in steady state. Using the design example values, I_{OUT} = 10 A, V_{OUT} = 1.2 V, $V_{IN(MIN)}$ = 9 V, F_{SW} = 2 MHz and ΔV_{IN} = 25 mV, 公式 11 yields an input capacitance of 39 µF. For this example, two 10µF, 25-V and a single 22-µF, 25-V ceramic capacitors in parallel have been selected for the VIN voltage rail. Because ESR is typically fairly low in ceramic capacitors, it is not included in this calculation.

The capacitor must also have a ripple current rating greater than the maximum input current ripple to the device during full load. The input ripple current can be calculated using 公式 12.

$$I_{CIN(RMS)} = \frac{I_{OUT}}{2} \times \sqrt{\frac{2 \times V_{OUT}}{V_{IN(MIN)}} \times \left(1 - \frac{2 \times V_{OUT}}{V_{IN(MIN)}}\right)} \quad (12)$$

For this example design, the RMS input ripple current is 2.21 A (RMS). The ripple current can be assumed to be shared equally between the input capacitors.

8.2.2.7 Series Capacitor Selection

A major function of the series capacitor is energy transfer. This is a different role from input and output capacitors where decoupling is the primary function. In many ways, the series capacitor is similar to the capacitor used for energy transfer in SEPIC converters and can be designed accordingly. A design objective may be to ensure the series capacitor voltage ripple does not exceed 5% to 10% of the nominal voltage under the worst case conditions. The series capacitor voltage ripple is given by 公式 13.

$$\Delta V_{(Ct)} = \frac{V_{OUT} \times I_{OUT}}{C_t \times f_{sw} \times V_{IN(MIN)}} \quad (13)$$

Here C_t is the series capacitance. 公式 13 can be rearranged to provide the design equation for series capacitor selection which is

$$C_t \geq \frac{2 \times V_{OUT} \times I_{OUT}}{k_{C_t} \times f_{sw} \times V^2_{IN(MIN)}} \quad (14)$$

where k_{Ct} represents the voltage ripple percentage. For example, if the voltage ripple target is 5%, the value for k_{Ct} is 0.05. The largest voltage ripple occurs at full load current (highest I_{OUT}), highest duty ratio (lowest input voltage/highest output voltage), and lowest frequency. For this design example, the value for k_{Ct} was selected to be 0.08. The resulting series capacitance calculated is 1.85 µF. A 10 V, X7R ceramic capacitor with 2.2 µF of capacitance is selected.

Another aspect to consider is capacitor RMS current rating. This impacts the temperature rise of the capacitor. Check the capacitor datasheet for temperature rise information. If the temperature rise is too large for a single capacitor, multiple capacitors may be placed in parallel to share the RMS current. The series capacitor has the same current profile as the high side MOSFETs. The RMS current squared can be expressed as

$$I^2_{Ct(RMS)} = 2 \times D \times I^2_{L(RMS)} \quad (15)$$

where $I_{L(RMS)}$ is the RMS inductor current of either inductor. The series capacitor RMS current can be expressed as

$$I_{Ct(RMS)} = \sqrt{4 \times \left(\frac{V_{OUT}}{V_{IN(MIN)}}\right)\left[\left(\frac{I_{OUT}}{2}\right)^2 + \left(\frac{\Delta I_L}{12}\right)^2\right]} \quad (16)$$

where ΔIL is the inductor current ripple. The largest RMS current occurs at the highest load current and highest duty ratio.

Multilayer ceramic capacitors (MLCC) are well suited for operating as the series capacitor. The equivalent series resistance (ESR) is relatively low (for example, 5 mΩ to 10 mΩ) which helps to reduce power loss and self heating. The equivalent series inductance (ESL) is fairly low which results in a high self resonant frequency (SRF). There are a few key items that should be considered when designing. First, the effective capacitance decreases with DC bias. This means that the capacitor should be selected based on its capacitance with the nominal voltage of $V_{IN}/2$ applied. Temperature variation also reduces effective capacitance. For this reason, X7R capacitors with up to 125°C operating temperature range are recommended. If capacitors are not properly selected, cracking or other failure modes may result.

8.2.2.8 Soft-Start Time Selection

The soft-start time is the amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the desired output voltage level. The large currents necessary to charge the capacitor may make the TPS54A20 reach the current limit and trigger a fault. Excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft-start time can be selected using the resistor values listed in 表 1. For the example circuit, the soft-start time is not critical since the output capacitor value is 94 µF which does not require a large amount of current to charge to 1.2 V. For this example design, the average output current is approximately 220 mA during soft start. The example circuit has the soft start time set to 512 µs which requires no resistor (open connection) on the SS/FSEL pin. The average converter output current required to charge the output capacitors to the target output voltage during soft start can be estimated using 公式 17.

$$I_{OUT,SS} = \frac{C_O \times V_{OUT}}{t_{SS}} \quad (17)$$

8.2.2.9 Bootstrap Capacitor Selection

A 0.047 µF ceramic capacitor should be connected between the BOOTA to SCAP pins and between the BOOTB and SWB pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

8.2.2.10 Gate Drive Capacitor Selection

A 1 µF ceramic capacitor should be connected between VGA and PGND and between the VG+ and VG- pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The VGA capacitor should have 16 V or higher voltage rating and the VG+ capacitor should have 10 V or higher voltage rating.

8.2.2.11 Under Voltage Lockout Set Point

The Under Voltage Lock Out (UVLO) set point can be adjusted using an external voltage divider network. The top resistor is connected between VIN and the EN pin and bottom resistor is connected between EN and GND as shown in 图 42. For the example design, the supply should turn on and start switching once the input voltage increases above 9.4 V (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 9.2 V (UVLO stop or disable). The resistor values for obtaining the desired UVLO thresholds can be calculated using 公式 18 and 公式 19. $R_{EN,TOP}$, the top UVLO divider resistor, is calculated using 公式 18. $R_{EN,BOT}$, the bottom UVLO divider resistor, is calculated in 公式 19.

$$R_{EN(TOP)} = \frac{V_{IN(RISE)} - V_{IN(FALL)}}{I_{EN(FALL)} - I_{EN(RISE)}} \tag{18}$$

$$R_{EN(BOT)} = \frac{R_{EN(TOP)} \times V_{EN}}{V_{IN(FALL)} - V_{EN} + R_{EN(TOP)} \times I_{EN(FALL)}} \tag{19}$$

For the start and stop voltages specified the resistor value selected for $R_{EN,TOP}$ (R2) is 80.6 kΩ and for $R_{EN,BOT}$ (R3) is 12.4 kΩ.

8.2.2.12 Current Limit Selection

The current limit can be selected using the ILIM pin. Refer to 表 2 for resistor selection information. It is recommended to choose a current limit that is 1.5 times or more than the full load current expected in the application. This allows for margin in the inductor currents when responding to load transients and limits nuisance trips.

8.2.3 Application Curves

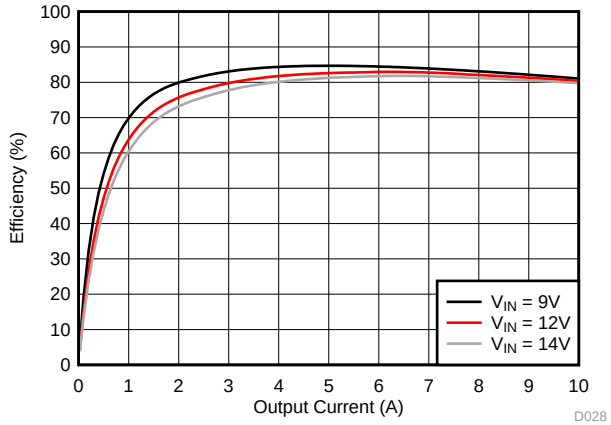


图 48. Efficiency

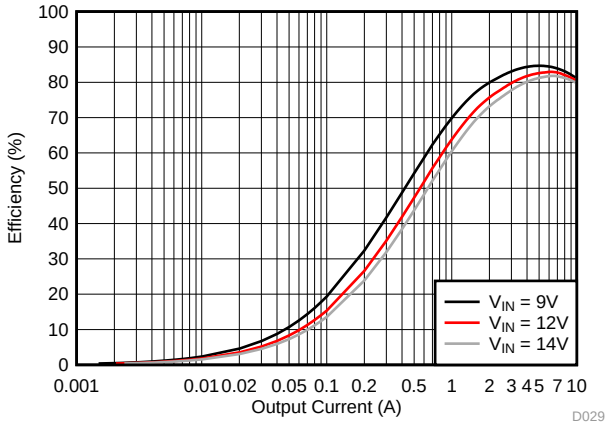


图 49. Light Load Efficiency

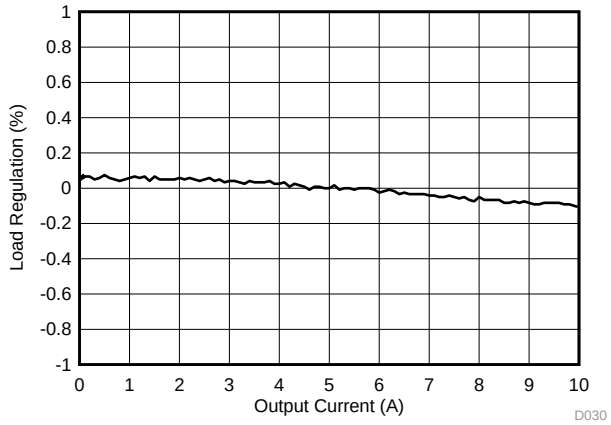


图 50. Load Regulation

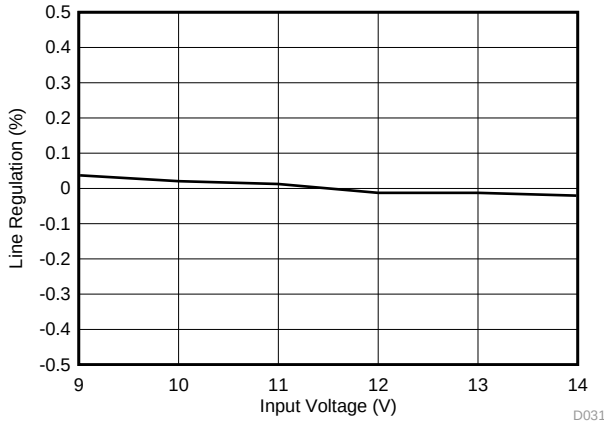


图 51. Line Regulation

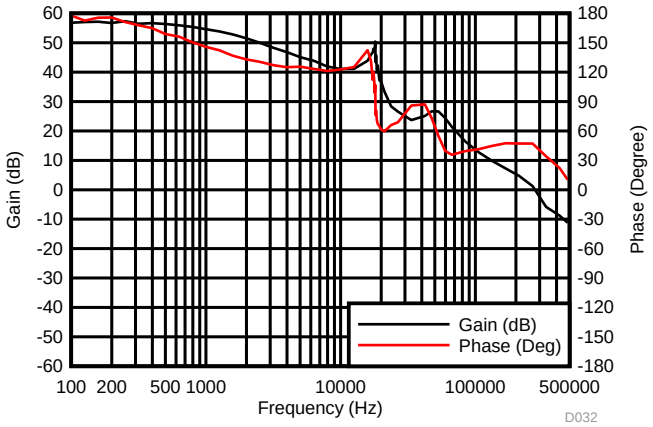


图 52. Loop Response

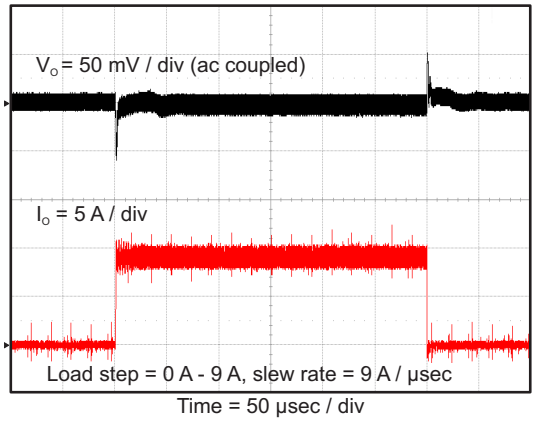


图 53. Transient Response

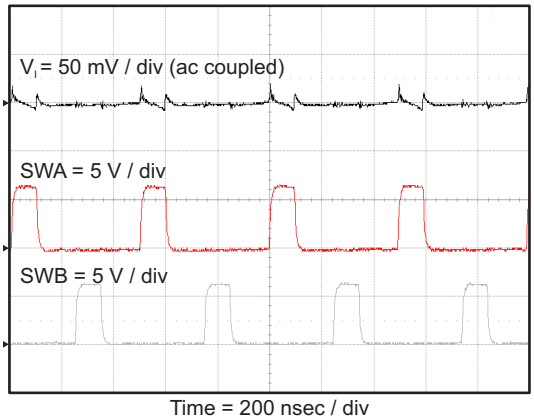


图 54. No Load Input Voltage Ripple

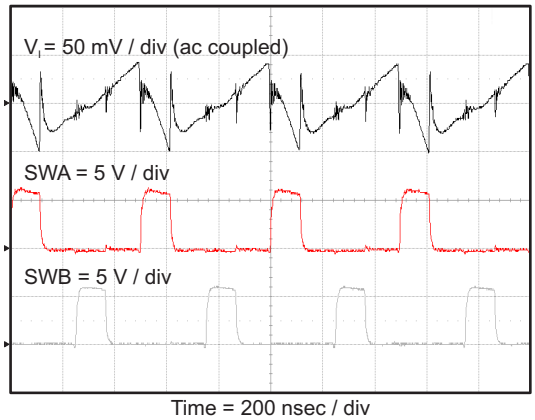


图 55. Full Load Input Voltage Ripple

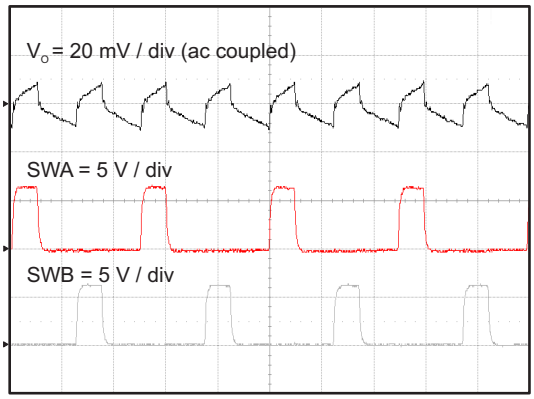


图 56. No Load Output Voltage Ripple

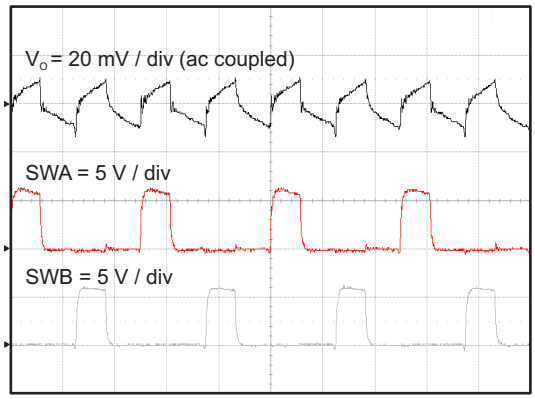


图 57. Full Load Output Voltage Ripple

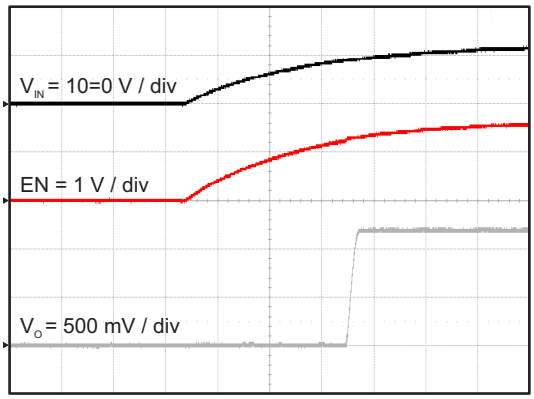


图 58. Start Up with VIN

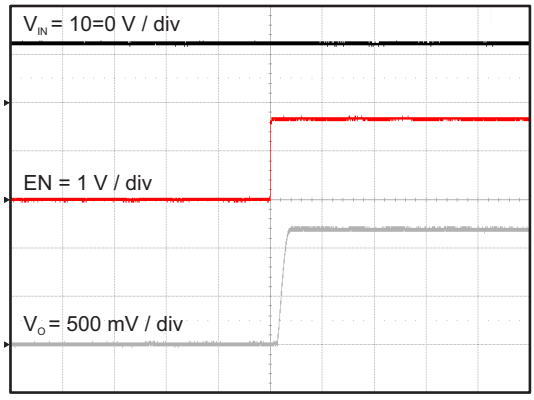


图 59. Start Up with EN

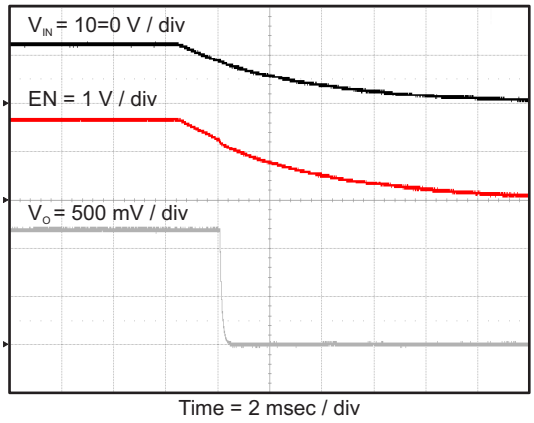


图 60. Shut Down with VIN

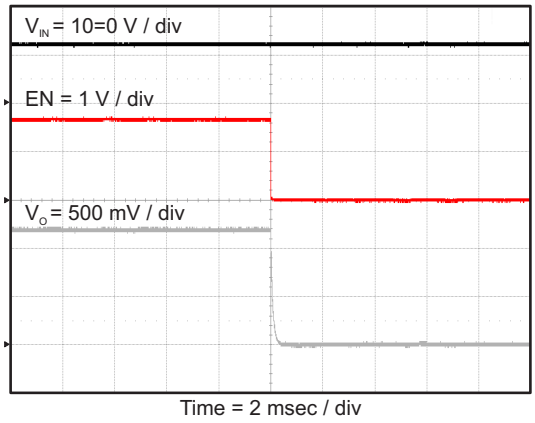


图 61. Shut Down with EN

9 Power Supply Recommendations

The TPS54A20 is designed to operate from an input voltage supply range between 8V and 14V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7µF (after de-rating) ceramic capacitor, type X5R or better, from VIN to PGND. Additional local ceramic bypass capacitance may be required in systems with small input ripple specifications, in addition to bulk capacitance, if the TPS54A20 device is located more than a few inches away from its input power supply. In systems with an auxiliary power rail available, the power stage input, VIN, and the gate driver power input, VG+, may operate from separate input supplies. See the recommendations in the Layout section for further explanation.

10 Layout

10.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See 图 62 and 图 63 for a PCB layout example. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.
- The IC package design provides several quiet pads for heat removal and enables a tight layout of the board components.
- Place the power components (including input and output capacitors, inductors, the series capacitor, and the TPS54A20 device) on the solder side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as FB, EN, TON, PGOOD, ILIM, and SS/FSEL must be placed away from high-voltage switching nodes such as SWA, SWB, SCAP, BOOTA, and BOOTB to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- Care should be taken to minimize the loop area formed by the input bypass capacitor connections, the VIN pin, and the ground connections. Place the input capacitors right next to the IC. Use low ESR ceramic capacitors with X5R or X7R dielectric.
- Care should also be taken to minimize the loop area formed by the series capacitor. Place the series capacitor directly beside the IC. If this guideline is not followed, extra voltage ringing due to parasitic inductances could occur on the switch nodes and the device could be damaged. Use low ESR ceramic capacitors with X7R or better dielectric. Ensure the capacitor operating temperature is sufficient. It is recommended to have at least 125 °C rating.
- Place the bootstrap capacitors close to the device to reduce parasitic inductance caused by switching loop area. Place the BOOTA to SCAP capacitor right next to the device.
- Thermal vias should be inserted in the PGND strip and connected to internal ground planes. This aids with heat removal and ground return current.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS54A20 device to provide a thermal path from the exposed thermal pad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground planes, must provide adequate heat dissipating area.
- Place the output inductors close to the SWA and SWB pins and keep the switch node area small. This helps to prevent excessive capacitive coupling, reduce electromagnetic interference, and reduce conduction loss.
- The output filter capacitor ground should be returned directly to the PGND strip using an inner layer.
- The FB pin is sensitive to noise. The feedback resistors should be located as close as possible to the IC and routed with minimal lengths of trace. Place the feedback resistor network near the device to minimize the FB trace distance. When operating at 7 MHz or 10 MHz, a resistor (e.g. 10 kΩ) is required in series with the FB pin to reduce noise coupling and filter out high frequency noise as shown in 图 62.
- Adding a phase boost capacitor in parallel with the top resistor of the output voltage feedback divider is recommended.
- Place the TON resistor directly next to the device. Connect the ground return to the AGND pin.
- Place the gate drive capacitor as close as possible to the VG+ and VG- pins. Make the return connection directly to the VG- pin instead of an inner ground layer. This reduces gate drive loop area.
- Place the VGA capacitor next to the VGA pin. Provide a ground via for the capacitor and ensure the loop is as small as possible.
- The no connect (NC) pin should be connected to the trace connecting the SCAP pin to the series capacitor. This will improve board level reliability.
- A snubber can be placed between the switch nodes and ground for effective ringing reduction.
- Land pattern and stencil information is provided in the data sheet addendum.
- Try to minimize conductor lengths while maintaining adequate width.
- It is recommended to experimentally validate all designs before production.

10.2 Layout Example

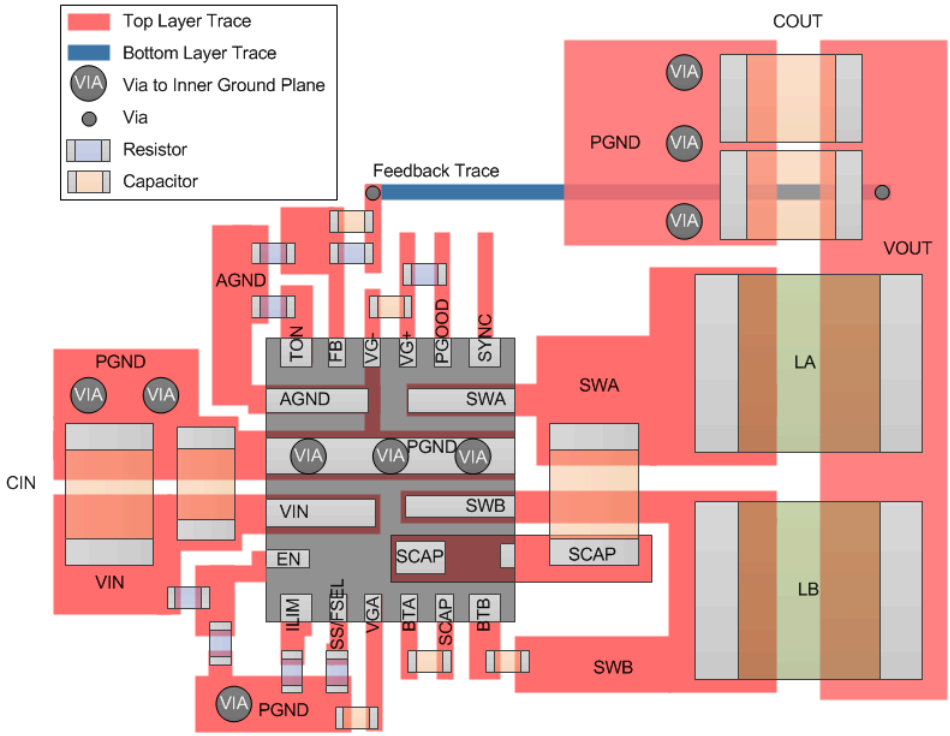


图 62. Layout Recommendation

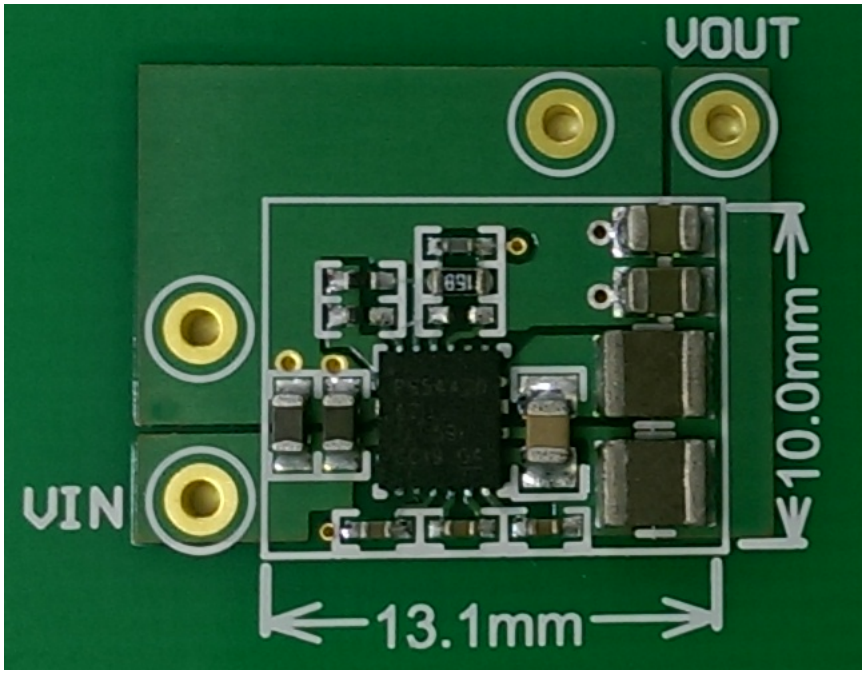


图 63. Example Converter Layout

Layout Example (接下页)

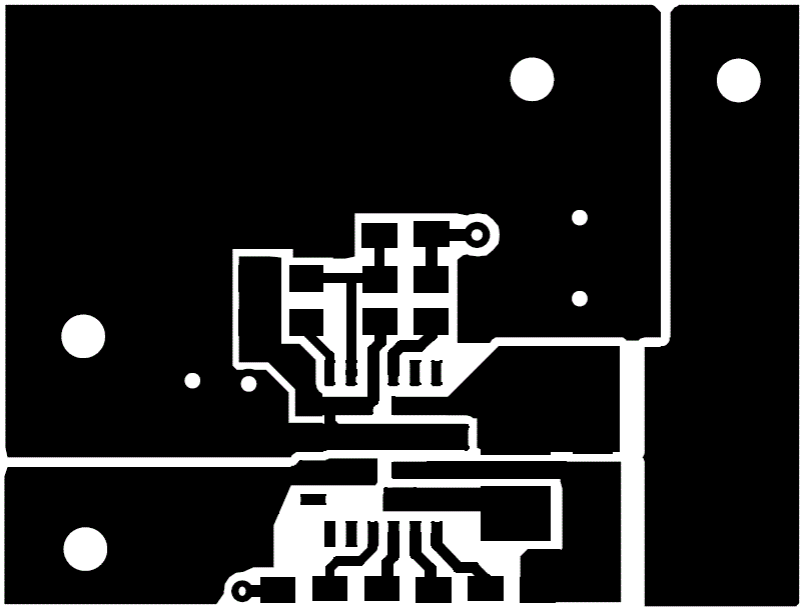


图 64. Top Layer of Example Converter Layout

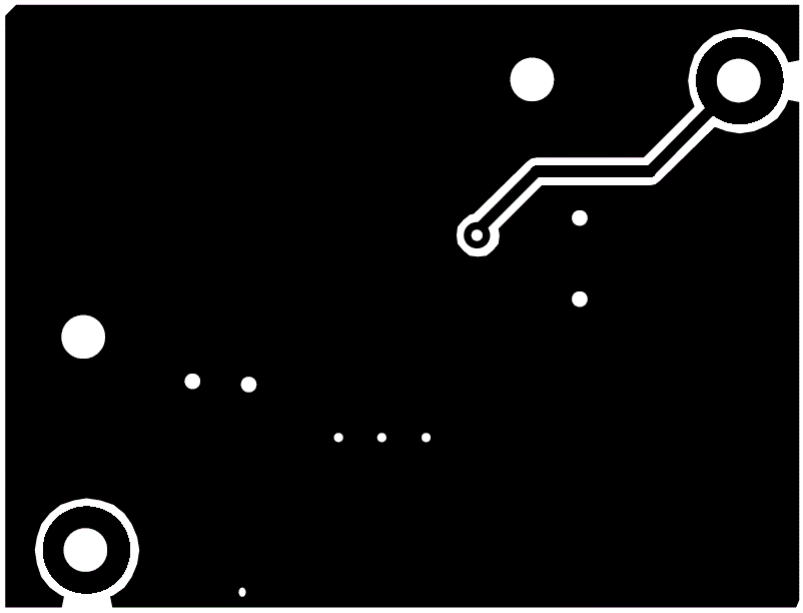


图 65. Bottom Layer of Example Converter Layout

11 器件和文档支持

11.1 文档支持

《优化内部补偿 DC-DC 转换器的瞬态响应》，SLVA289。

《串联电容降压转换器简介》，SLVA750。

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

SWIFT, E2E are trademarks of Texas Instruments.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54A20RNJR	ACTIVE	VQFN-HR	RNJ	20	3000	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54A20	Samples
TPS54A20RNJT	ACTIVE	VQFN-HR	RNJ	20	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54A20	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

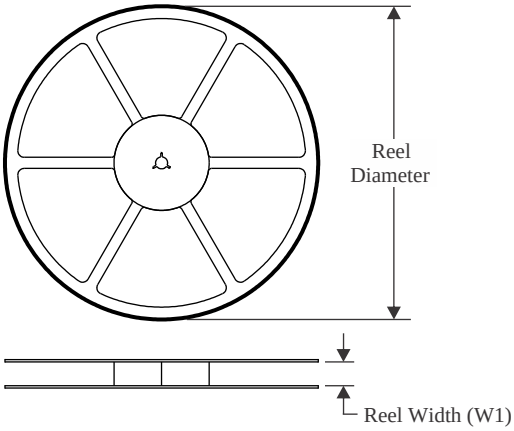
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

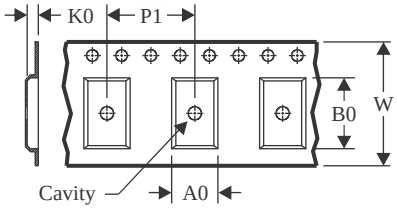
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

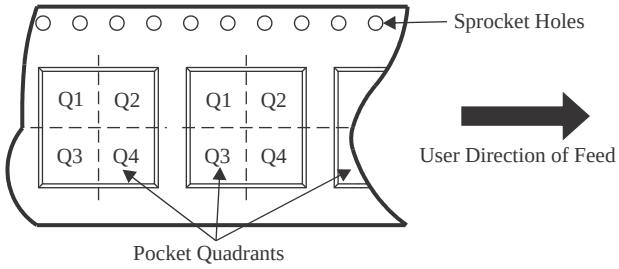


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

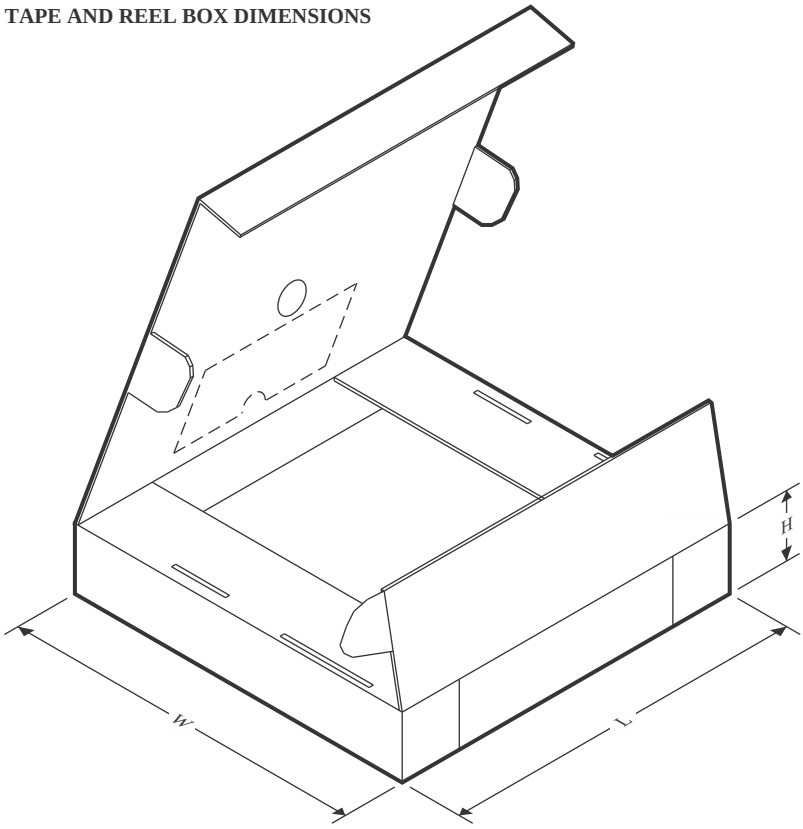
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54A20RNJR	VQFN-HR	RNJ	20	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS54A20RNJT	VQFN-HR	RNJ	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54A20RNJR	VQFN-HR	RNJ	20	3000	346.0	346.0	33.0
TPS54A20RNJT	VQFN-HR	RNJ	20	250	210.0	185.0	35.0

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