TEXAS INSTRUMENTS
TPS65218
ZHCSD17E – NOVEMBER 2014 – REVISED FEBRUARY 2021

适用于 ARM® Cortex™-A8/A9 SOC 和 FPGA 的 TPS65218 电源管理

1 特性

- 具有集成开关 FET 的 3 个可调节降压转换器（DCDC1、DCDC2 和 DCDC3）：
  - DCDC1：默认电压为 1.1V，电流高达 1.8A
  - DCDC2：默认电压为 1.1V，电流高达 1.8A
  - DCDC3：默认电压为 1.2V，电流高达 1.8A
  - 输入电压范围：2.7V 至 5.5V
  - 可调节输出电压范围：0.85V 至 1.675V（DCDC1 和 DCDC2）
  - 可调节输出电压范围：0.9V 至 3.4V (DCDC3)
  - 轻负载电流状态下进入节能模式
  - 100% 占空比，可实现最低压降
  - 禁用时支持有源输出放电
- 具有集成开关 FET 的 1 个可调节降压/升压转换器 (DCDC4)：
  - DCDC4：默认电压为 3.3V，电流高达 1.6A
  - 输入电压范围：2.7V 至 5.5V
  - 可调节输出电压范围：1.175V 至 3.4V
  - 禁用时支持有源输出放电
- 2 个适用于备用电池域的低静态电流、高效降压转换器（DCDC5、DCDC6）
  - DCDC5：1V 输出电压
  - DCDC6：1.8V 输出电压
  - 输入电压范围：2.2V 至 5.5V
  - 由系统电源或备用纽扣电池供电
- 可调节通用 LDO (LDO1)
  - LDO1：默认电压为 1.8V，电流高达 400mA
  - 输入电压范围：1.8V 至 5.5V
  - 可调节输出电压范围：0.9V 至 3.4V
  - 禁用时支持有源输出放电
- 具有 350mA 电流限制的低电压负载开关 (LS1)
  - 输入电压范围：1.2V 至 3.6V
  - 电压为 1.35V 时，开关阻抗为 110mΩ（最大值）
- 具有 100mA 或 500mA 可选电流限制的 5V 负载开关 (LS2)
  - 输入电压范围：4V 至 5.5V
  - 电压为 5V 时，开关阻抗为 500mΩ（最大值）
- 具有 100mA 或 500mA 可选电流限制的高电压负载开关 (LS3)
  - 输入电压范围：1.8V 至 10V
  - 开关阻抗：500mΩ（最大值）
- 带有内置监控功能的监控器可用于监测：
  - DCDC1、DCDC2 ±4% 容差
  - DCDC3、DCDC4 ±5% 容差
  - LDO1 ±5% 容差
- 保护、诊断和控制：
  - 欠压锁定 (UVLO)
  - 常开按钮监视器
  - 过热警告和关断
  - 备用电源和主电源采用独立的电源正常状态输出
  - I^2C 接口（地址 0x24）（请参阅 400kHz 时的 I^2C 操作*时序要求*）

2 应用

- 人机界面 (HMI)
- 工业自动化
- 电子销售点 (ePOS)
- 测试和测量
- 个人导航

3 说明

TPS65218 是一款单芯片电源管理 IC，专门用于支持便携式（锂离子电池）和非便携式（5V 适配器）应用。此器件的额定工作温度范围为 -40°C 至 +105°C，适用于各种各样的工业应用。

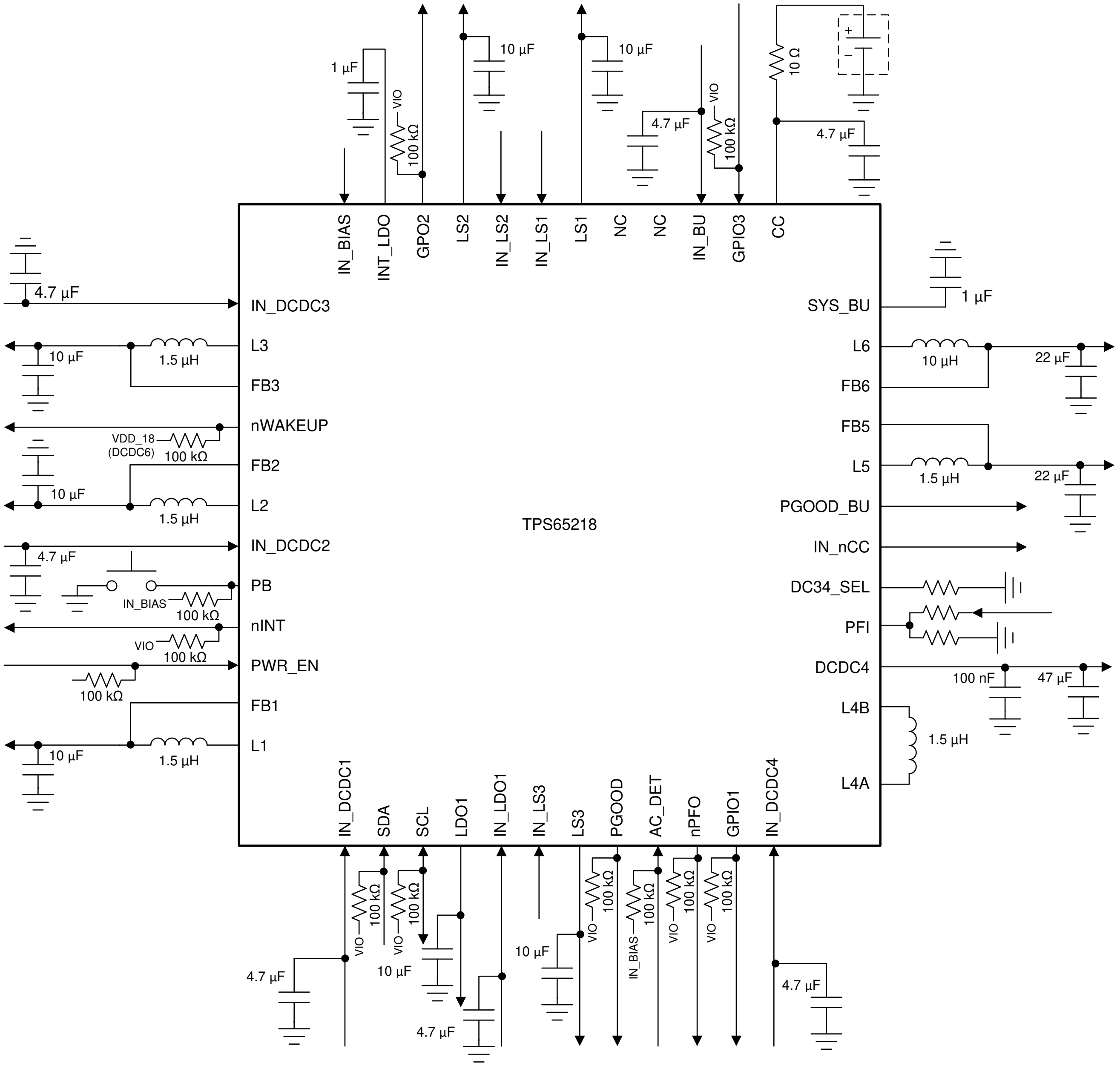
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS65218	VQFN (48)	6.00mm × 6.00mm
TPS65218	HTQFP (48)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

English Data Sheet: SLDS206

3.1 Simplified Schematic



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (January 2018) to Revision E (February 2021) **Page**

- 更新了整个文档的表、图和交叉参考的编号格式.......... 1
- 删除了 NRND 横幅。请参阅数据表末尾的*机械、封装和可订购信息*。.......... 1

Changes from Revision C (August 2017) to Revision D (January 2018) **Page**

- 向数据表添加了*不建议用于新设计* 声明.......... 1

Changes from Revision B (February 2016) to Revision C (May 2017) **Page**

- 更改了*特性* 部分中的可调节输出电压范围以分别显示 DCDC1、DCDC2 和 DCDC3 的值.......... 1
- 将*特性* 部分中的 DCDC4 默认值从 1.0A 更改为 1.6A.......... 1
- 将*特性* 部分中的 DCDC4 可调节输出电压最小值从 0.85V 更改为 1.175V.......... 1
- 将*特性* 部分中的 5V 负载开关输入电压最小值从 3.0V 更改为 4V.......... 1
- 更改了简化原理图.......... 1
- Added updates to Description column in the Pin Functions table.......... 7
- Changed input voltage for LS1 max value from 3.3 V : to 3.6 V in the *Recommended Operating Conditions* section.......... 10
- Added individual output voltage values for DCDC1, DCDC2, DCDC3, DCDC4 in the *Recommended Operating Conditions* section.......... 10
- Changed output voltage for DCDC5 from 1.0 V (MAX) and 1.1 V (MIN) : to 1 V (TYP) in the *Recommended Operating Conditions* section.......... 10
- Changed output voltage for DCDC6 from 1.8 V (MAX) and 1.8 V (MIN) : to 1.8 V (TYP) in the *Recommended Operating Conditions* section.......... 10
- Added additional voltage conditions on output current for DCDC4 in the *Recommended Operating Conditions* section.......... 10
- Changed output current for DCDC5, DCDC6 max value from 10 mA : to 25 mA in the *Recommended Operating Conditions* section.......... 10
- Changed output current max value for LS2 from 1000 mA : to 920 mA in the *Recommended Operating Conditions* section.......... 10
- Added voltage conditions to output current for LS3 in the *Recommended Operating Conditions* section.......... 10

- Deleted Note 2 in the *Electrical Characteristics* section.......... 11
- Added SYS_BU subsection in the *Electrical Characteristics* section.......... 11
- Changed first parameter of the INT_LDO subsection from V_{OUT} : to V_{INT_LDO} in the *Electrical Characteristics* section.......... 11
- Added additional test conditions to t_{HOLD} in the *Electrical Characteristics* section.......... 11
- Added typ value to INT_LDO C_{OUT} in the *Electrical Characteristics* section.......... 11
- Changed output voltage range max value for $V_{DCDC1,2}$ from 1.65 V : to 1.675 V in the *Electrical Characteristics* section.......... 11
- Changed test condition for DCDC1, DCDC2 (1.1-V BUCK) and DCDC3 (1.2-V BUCK) I_{OUT} from < 2.8 V : to < 2.7 V in the *Electrical Characteristics* section.......... 11
- Changed power-good threshold, V_{OUT} falling values for DCDC1, DCDC2 (1.1-V BUCK) V_{PG} from 96% MIN and 97% MAX : to 95.9% MIN and 97.1% MAX in the *Electrical Characteristics* section.......... 11
- Added STRICT = 1 test condition for all V_{OV} parameters in the *Electrical Characteristics* section.......... 11
- Changed overvoltage detection threshold for DCDC1, DCDC2 (1.1-V BUCK) V_{OV} from 103% MIN and 104% MAX : to 102.9% MIN and 104.1% MAX in the *Electrical Characteristics* section.......... 11
- Deleted tolerance for all C_{OUT} except INT_LDO C_{OUT} in the *Electrical Characteristics* section.......... 11
- Added min and typ values for DCDC1, DCDC2 (1.1-V BUCK) C_{OUT} in the *Electrical Characteristics* section.... 11
- Changed max value for DCDC1, DCDC2 (1.1-V BUCK) C_{OUT} from 500 µF : to 100 µF in the *Electrical Characteristics* section.......... 11
- Added additional test condition to DCDC3 (1.2-V BUCK) DC accuracy in the *Electrical Characteristics* section 11
- Added typ value for DCDC3 (1.2-V BUCK) C_{OUT} in the *Electrical Characteristics* section.......... 11
- Added additional test condition to V_{DCDC4} output voltage ripple in the *Electrical Characteristics* section.......... 11
- Changed power-good threshold, V_{OUT} falling values for DCDC4 (3.3-V BUCK-BOOST) V_{PG} from 96% MIN and 97% MAX : to 95.9% MIN and 97.1% MAX in the *Electrical Characteristics* section.......... 11
- Changed overvoltage detection threshold for DCDC4 (3.3-V BUCK-BOOST) V_{OV} from 104% MIN and 105% MAX : to 103.9% MIN and 105.1% MAX in the *Electrical Characteristics* section.......... 11
- Added typ value for DCDC4 (3.3-V BUCK-BOOST) C_{OUT} in the *Electrical Characteristics* section.......... 11
- Deleted V_{CC} voltage range test conditions from V_{IN_BU} in the *Electrical Characteristics* section.......... 11
- Added additional test condition to t_{RISE} in the *Electrical Characteristics* section.......... 11
- Added Q_{INRUSH} to the DCDC5, 6 POWER PATH in the *Electrical Characteristics* section.......... 11
- Changed DC accuracy values for V_{DCDC5} from –1.5% (MIN) and 1.5% (MAX) : to –2% (MIN) and 4% (MAX) 11
- Added and updated test conditions for V_{DCDC5} DC accuracy in the *Electrical Characteristics* section.......... 11
- Changed operators in test conditions for DCDC5 (1-V BATTERY BACKUP SUPPLY) and DCDC6 (1.8-V BATTERY BACKUP SUPPLY) I_{OUT} from < : to $\leqslant$ in the *Electrical Characteristics* section.......... 11
- Deleted I_{INRUSH} from DCDC5 (1.0-V BATTERY BACKUP SUPPLY) and DCDC6 (1.8-V BATTERY BACKUP SUPPLY) in the *Electrical Characteristics* section.......... 11
- Changed DC accuracy values for V_{DCDC6} from –1.5% and 1.5% : to –2% and 2% in the *Electrical Characteristics* section.......... 11
- Changed DC accuracy min value for V_{DCDC6} from –10% : to –5% in the *Electrical Characteristics* section.... 11
- Added test conditions for I_{OUT} when device is on IN_BU in the *Electrical Characteristics* section.......... 11
- Changed short circuit limit min value for LDO1 (1.8-V LDO) I_{LIMIT} from 490 mA : to 445 mA in the *Electrical Characteristics* section.......... 11
- Added test condition to all R_{DIS} internal discharge resistor at output parameters in the *Electrical Characteristics* section.......... 11
- Changed operator in test conditions for LOAD SWITCH 2 (LS2) I_{LIMIT} from < : to $\leqslant$ in the *Electrical Characteristics* section.......... 11
- Changed min value for I_{LIMIT}, LS2ILIM[1:0] = 00 from 100 mA : to 94 mA in the *Electrical Characteristics* section.......... 11

- Changed min value for I_{LIMIT}, LS2ILIM[1:0] = 10 from 200 mA : to 188 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, LS2ILIM[1:0] = 01 from 500 mA : to 465 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, LS2ILIM[1:0] = 11 from 1000 mA : to 922 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} > 2.3 V, LS3ILIM[1:0] = 00 from 100 mA : to 98 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} > 2.3 V, LS3ILIM[1:0] = 10 from 200 mA : to 194 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} > 2.3 V, LS3ILIM[1:0] = 01 from 500 mA : to 475 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} > 2.3 V, LS3ILIM[1:0] = 11 from 950 mA : to 900 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} $\leqslant$ 2.3 V, LS3ILIM[1:0] = 00 from 100 mA : to 98 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} $\leqslant$ 2.3 V, LS3ILIM[1:0] = 10 from 200 mA : to 194 mA in the *Electrical Characteristics* section.... 11
- Changed min value for I_{LIMIT}, V_{IN_LS3} $\leqslant$ 2.3 V, LS3ILIM[1:0] = 01 from 500 mA : to 475 mA in the *Electrical Characteristics* section.... 11
- Changed high level output voltage, PGOOD_BU min value in V_{OH} from (VDD_1 8 – 10 mV): to (V_{DCDC6} – 10 mV) in the *Electrical Characteristics* section.... 11
- Changed test condition in V_{OH} from GPO2_CNF : to GPO2_BUF in the *Electrical Characteristics* section.... 11
- Added test conditions to V_{OL} for nPFO in the *Electrical Characteristics* section.... 11
- Added new Note 2 in the *Electrical Characteristics* section.... 11
- Added updates to *Overview* section.... 23
- Changed the Functional Block Diagram.... 24
- Added updates to *Power-Up Sequencing* section.... 25
- Added updates to *Power-Down Sequencing* section.... 27
- Added updates to *Supply Voltage Supervisor and Power Good (PGOOD)* section.... 29
- Added updates and changes to *Internal LDO (INT_LDO)* section.... 30
- Added updates and changes to *Current Limited Load Switches* section.... 32
- Changed Typical Application of Load Switch 2 figure in the *Load Switch 2 (LS2)* section.... 33
- Added updates to *Load Switch 3 (LS3)* section.... 33
- Added updates and changes to *UVLO* section.... 34
- Added updates to *Battery-Backup Supply Power-Path* section.... 37
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- Added updates to *AC_DET Input (AC_DET)* section.... 43
- Changed Modes of Operation Diagram in *Device Functional Modes* section.... 47
- Changed description for Bit 5 in the STATUS Register Field Descriptions table.... 49
- Added updates to the CONFIG2 Register Field Descriptions table.... 49
- Changed description for Bits 2-0 in the SLEW Register Field Descriptions table.... 49
- Added updates to *Layout* section.... 87
- Added *Receiving Notification of Documentation Updates* section to *Device and Documentation Support* section.... 89
- Added the *Documentation Support* section.... 89
- Changed the *Electrostatic Discharge Caution* statement.... 89

Changes from Revision A (September 2015) to Revision B (February 2016) Page

- Updated description for PGOOD to clarify that the output can be configured as open drain.... 7
- Added V_{IN_LS3} conditions to I_{LIMIT} for Load Switch 3 and updated the values.... 11

Changes from Revision * (November 2014) to Revision A (September 2015) Page

- 添加了器件型号 TPS65218B101 1
- 扩大了具有 350mA 限流功能的低压负载开关的输入电压范围 1
- Moved T_{stg} to the *Absolute Maximum Ratings* table and updated *Handling Ratings* table to an *ESD Ratings* table 9
- Added device part number to *Thermal Information* table 10
- Added test conditions and values for V_{UVLO} hysteresis 11
- Changed test conditions for input voltage ranges from "V_{IN_BIAS} > 2.7 V" to "V_{IN_BIAS} > V_{UVLO}" 11
- Updated values for DCDC1-4 V_{OUT} falling and rising 11
- Added more test conditions and values for V_{IN_DCDC4} 11
- Updated V_{DCDC4} test conditions and values and added output voltage ripple specification for PFM mode 11
- Updated test conditions and added new values for V_{DCDC5}, V_{DCDC6} DC accuracy 11
- Updated V_{IN_LS1} max value and added additional test condition for $R_{DS(ON)}$ 11
- Added note for t_{HIGH} 21
- Updated 节 *7.3.1.18* and added a note 45
- Added note to *Application and Implementation* 81
- Added *Community Resources* 89

5 Pin Configuration and Functions

图 5-1 shows the 48-pin RSL Plastic Quad Flatpack No-Lead. 图 5-2 shows the 48-pin PHP PowerPAD™ Plastic Quad Flatpack.

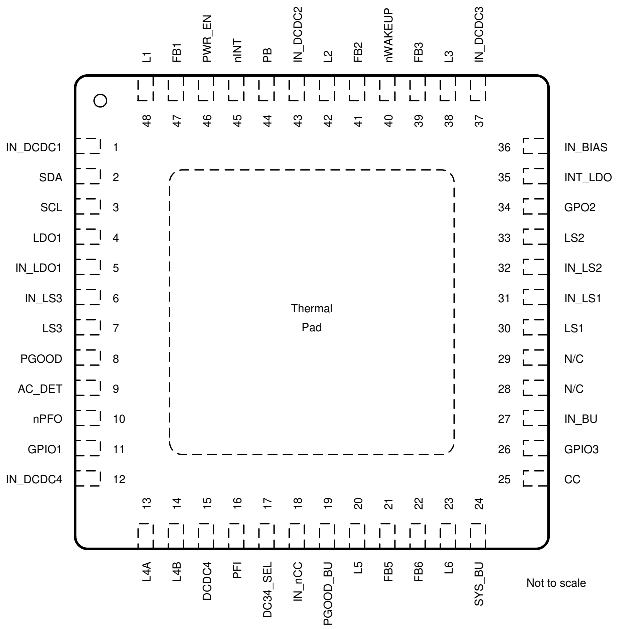


图 5-1. 48-Pin RSL VQFN With Exposed Thermal Pad (Top View, 6 mm × 6 mm × 1 mm With 0.4-mm Pitch)

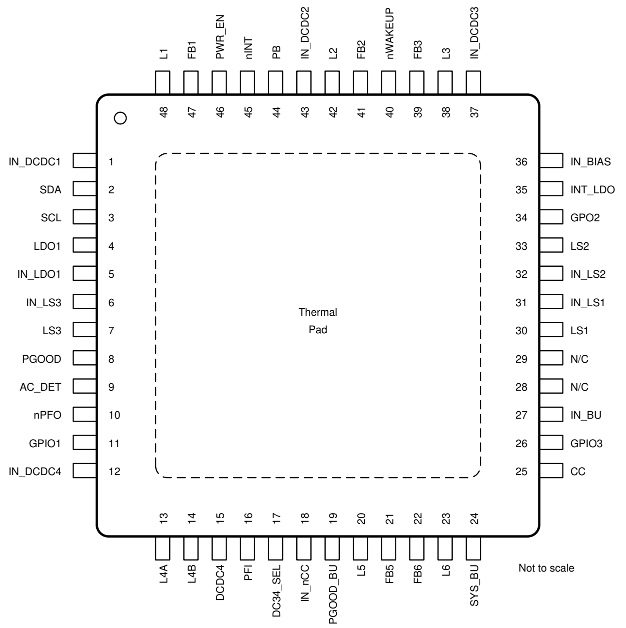


图 5-2. 48-Pin PHP PowerPAD™ HTQFP (Top View, 7 mm × 7 mm × 1 mm With 0.5-mm Pitch)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN_DCDC1	P	Input supply pin for DCDC1.
2	SDA	I/O	Data line for the I^{2}C interface. Connect to pullup resistor.
3	SCL	I	Clock input for the I^{2}C interface. Connect to pullup resistor.
4	LDO1	O	Output voltage pin for LDO1. Connect to capacitor.
5	IN_LDO1	P	Input supply pin for LDO1.
6	IN_LS3	P	Input supply pin for load switch 3.
7	LS3	O	Output voltage pin for load switch 3. Connect to capacitor.
8	PGOOD	O	Power-good output (configured as open drain). Pulled low when either DCDC1-4 or LDO1 are out of regulation. Load switches and DCDC5-6 do not affect PGOOD pin.
9	AC_DET	I	AC monitor input and enable for DCDC1-4, LDO1 and load switches. See 节 7.4.1 for details. Tie pin to IN_BIAS if not used.
10	nPFO	O	Power-fail comparator output, deglitched (open drain). Pin is pulled low when PFI input is below power-fail threshold.
11	GPIO1	I/O	Pin configured as DDR reset-input (driving GPO2) or as general-purpose, open-drain output. See 节 7.3.1.14 for more information.
12	IN_DCDC4	P	Input supply pin for DCDC4.
13	L4A	P	Switch pin for DCDC4. Connect to inductor.
14	L4B	P	Switch pin for DCDC4. Connect to inductor.
15	DCDC4	P	Output voltage pin for DCDC4. Connect to capacitor.
16	PFI	I	Power-fail comparator input. Connect to resistor divider.

表 5-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
17	DC34_SEL	I	Power-up default selection pin for DCDC3 or DCDC4. Power-up default is programmed by a resistor connected to ground. See 节 7.3.1.13 for resistor options.
18	IN_nCC	O	Output pin indicates if DCDC5 and DCDC6 are powered from main supply (IN_BU) or coin-cell battery (CC). Pin is push-pull output. Pulled low when PMIC is powered from coin cell battery. Pulled high when PMIC is powered from main supply (IN_BU).
19	PGOOD_BU	O	Power-good, push-pull output for DCDC5 and DCDC6. Pulled low when either DCDC5 or DCDC6 is out of regulation. Pulled high (to DCDC6 output voltage) when both rails are in regulation.
20	L5	P	Switch pin for DCDC5. Connect to inductor.
21	FB5	I	Feedback voltage pin for DCDC5. Connect to output capacitor.
22	FB6	I	Feedback voltage pin for DCDC6. Connect to output capacitor.
23	L6	P	Switch pin for DCDC6. Connect to inductor.
24	SYS_BU	P	System voltage pin for battery-backup supply power path. Connect to 1-µF capacitor. Connecting any external load to this pin is not recommended.
25	CC	P	Coin cell battery input. Serves as the supply to DCDC5 and DCDC6 if no voltage is applied to IN_BU. Tie this pin to ground if it is not in use.
26	GPIO3	I/O	Pin can be configured as warm reset (negative edge) for DCDC1 and DCDC2 or as a general-purpose, open-drain output. See 节 7.3.1.14 for more details.
27	IN_BU	P	Default input supply pin for battery backup supplies (DCDC5 and DCDC6).
28	N/C	—	No connect. Leave pin floating.
29	N/C		
30	LS1	O	Output voltage pin for load switch 1. Connect to capacitor.
31	IN_LS1	P	Input supply pin for load switch 1.
32	IN_LS2	P	Input supply pin for load switch 2.
33	LS2	O	Output voltage pin for load switch 2. Connect to capacitor.
34	GPO2	O	Pin configured as DDR reset signal (controlled by GPIO1) or as general-purpose output. Buffer can be configured as push-pull or open-drain.
35	INT_LDO	P	Internal bias voltage. Connecting any external load to this pin is not recommended.
36	IN_BIAS	P	Input supply pin for reference system.
37	IN_DCDC3	P	Input supply pin for DCDC3.
38	L3	P	Switch pin for DCDC3. Connect to inductor.
39	FB3	I	Feedback voltage pin for DCDC3. Connect to output capacitor.
40	nWAKEUP	O	Signal to SOC to indicate a power on event (active low, open-drain output).
41	FB2	I	Feedback voltage pin for DCDC2. Connect to output capacitor.
42	L2	P	Switch pin for DCDC2. Connect to inductor.
43	IN_DCDC2	P	Input supply pin for DCDC2.
44	PB	I	Push-button monitor input. Typically connected to a momentary switch to ground (active low). See 节 7.4.1 for details.
45	nINT	O	Interrupt output (active low, open drain). Pin is pulled low if an interrupt bit is set. The pin returns to Hi-Z state after the bit causing the interrupt has been read. Interrupts can be masked.
46	PWR_EN	I	Power enable input for DCDC1-4, LDO1 and load switches. See 节 7.4.1 for details.
47	FB1	I	Feedback voltage pin for DCDC1. Connect to output capacitor.
48	L1	P	Switch pin for DCDC1. Connect to inductor.
—	Thermal Pad	P	Power ground and thermal relief. Connect to ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

Operating under free-air temperature range (unless otherwise noted).(1)

			MIN	MAX	UNIT
	Supply voltage	IN_BIAS, IN_LDO1, IN_LS2, IN_DCDC1, IN_DCDC2, IN_DCDC3, IN_DCDC4	–0.3	7	V
		IN_LS1, CC	–0.3	3.6	
		IN_LS3	–0.3	11.2	
		IN_BU	–0.3	5.8	
	Input voltage	DC34_SEL	–0.3	3.6	V
		All pins unless specified separately	–0.3	7	
	Output voltage	DC34_SEL	–0.3	3.6	V
		All pins unless specified separately	–0.3	7	
	Source or sink current	GPO2		6	mA
		PGOOD_BU, IN_nCC		1	
	Sink current	PGOOD, nWAKEUP, nINT, nPFO, SDA, GPIO1, GPIO3		6	mA
T_A	Operating ambient temperature		–40	105	°C
T_J	Junction temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, IN_BIAS		2.7		5.5	V
Input voltage for DCDC1, DCDC2, DCDC3, and DCDC4		2.7		5.5	V
Supply voltage, IN_BU		2.2		5.5	V
Supply voltage, CC		2.2		3.3	V
Input voltage for LDO1		1.8		5.5	V
Input voltage for LS1		1.2		3.6	V
Input voltage for LS2		3		5.5	V
Input voltage for LS3		1.8		10	V
Output voltage for DCDC1		0.85		1.675	V
Output voltage for DCDC2		0.85		1.675	V
Output voltage for DCDC3		0.9		3.4	V
Output voltage for DCDC4		1.175		3.4	V
Output voltage for DCDC5			1		V
Output voltage for DCDC6			1.8		V
Output voltage for LDO1		0.9		3.4	V
Output current for DCDC1, DCDC2, and DCDC3		0		1.8	A
Output current for DCDC4	VIN_DCDC4 = 2.8 V			1	A
	VIN_DCDC4 = 3.6 V			1.3	
	VIN_DCDC4 = 5 V			1.6	
Output current for DCDC5 and DCDC6		0		25	mA
Output current for LDO1		0		400	mA
Output current for LS1		0		300	mA
Output current for LS2		0		920	mA
Output current for LS3	VIN_LS3 > 2.3 V	0		900	mA
	VIN_LS3 ≤ 2.3 V	0		475	

6.4 Thermal Information

THERMAL METRIC[1]		TPS65218		UNIT
		RSL (VQFN)	PHP (HTQFP)	
		48 PINS	48 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top)	17.2	13.3	°C/W
$R_{\theta JB}$	Junction-to-board	5.8	7.9	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient. JEDEC 4-layer, high-K board.	30.6	26.7	°C/W
Ψ_{JT}	Junction-to-package top	0.2	0.3	°C/W
Ψ_{JB}	Junction-to-board	5.6	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom)	1.5	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENTS							
V_{IN_BIAS}	Input supply voltage range	Normal operation		2.7		5.5	V
		EEPROM programming		4.5		5.5	
V_{UVLO}	Undervoltage lockout	Supply falling; measured in respect to V_{IN_BIAS}	UVLO[1:0] = 00b	2.7	2.75	2.8	V
			UVLO[1:0] = 01b	2.85	2.95	3.05	V
			UVLO[1:0] = 10b	3.15	3.25	3.35	V
			UVLO[1:0] = 11b	3.25	3.35	3.45	V
V_{UVLO}	Hysteresis	Supply rising; V_{IN_BIAS} slew rate < 30 V/s	UVLOHYS = 0b(8)		200		mV
			UVLOHYS = 1b		400		mV
		Supply rising; V_{IN_BIAS} slew rate > 30 V/s	UVLOHYS = 0b(8)		0		mV
			UVLOHYS = 1b		0		mV
	Deglitch time				5		ms
I_{OFF}	OFF state current, total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LSx, IN_BU	V_{IN} = 3.6 V; All rails disabled. T_J = 0°C to 85°C			5		µA
$I_{SUSPEND}$	SUSPEND current, total current into IN_BIAS, IN_DCDCx, IN_LDO1, IN_LSx, IN_BU	V_{IN} = 3.6 V; DCDC3 enabled, low-power mode, no load. All other rails disabled. T_J = 0°C to 105°C			220		µA
SYS_BU							
V_{SYS_BU}	SYS_BU voltage range	Powered from V_{IN_BU} or V_{CC}		2.2		5.5	V
C_{SYS_BU}	Recommended SYS_BU capacitor	Ceramic, X5R or X7R, see 表 8-2.			1		µF
	Tolerance	Ceramic, X5R or X7R, rated voltage ⩾ 6.3 V		–20%		20%	
INT_LDO							
V_{INT_LDO}	Output voltage				2.5		V
	DC accuracy	I_{OUT} < 10 mA		–2%		2%	
I_{OUT}	Output current range	Maximum allowable external load		0		10	mA
I_{LIMIT}	Short circuit current limit	Output shorted to GND			23		mA
t_{HOLD}	Hold-up time	Measured from V_{INT_LDO} = 2.5 V to V_{INT_LDO} = 1.8 V All rails enabled before power off, V_{IN_BIAS} = 2.8 V to 0 V in < 1 µs No external load on INT_LDO C_{INT_LDO} = 22 µF, see 表 8-2.		150			ms
C_{OUT}	Nominal output capacitor value	Ceramic, X5R or X7R, see 表 8-2.		0.1	1	22	µF
	Tolerance	Ceramic, X5R or X7R, rated voltage ⩾ 6.3 V		–20%		20%	
DCDC1 (1.1-V BUCK)							
V_{IN_DCDC1}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		2.7		5.5	V
V_{DCDC1}	Output voltage range	Adjustable through I^2C		0.85		1.675	V
	DC accuracy	2.7 V ⩽ V_{IN} ⩽ 5.5 V; 0 A ⩽ I_{OUT} ⩽ 1.8 A		–2%		2%	
I_{OUT}	Continuous output current	V_{IN_DCDC1} > 2.7 V				1.8	A
I_Q	Quiescent current	Total current from I_{N_DCDC1} pin; Device not switching, no load			25	50	µA
$R_{DS(ON)}$	High-side FET on resistance	V_{IN_DCDC1} = 3.6 V			230	355	mΩ
	Low-side FET on resistance	V_{IN_DCDC1} = 3.6 V			90	145	
I_{LIMIT}	High-side current limit	V_{IN_DCDC1} = 3.6 V			2.8		A
	Low-side current limit	V_{IN_DCDC1} = 3.6 V			3.1		

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	95.9%	96.5%	97.1%	
	Hysteresis	V_{OUT} rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0b		1		ms
			STRICT = 1b		50		µs
		V_{OUT} rising	STRICT = 0b		10		µs
			STRICT = 1b		10		µs
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold	V_{OUT} rising, STRICT = 1b		102.9%	103.5%	104.1%	
	Hysteresis	V_{OUT} falling, STRICT = 1b			0.25%		
	Deglitch	V_{OUT} rising, STRICT = 1b			50		µs
I_{INRUSH}	Inrush current	V_{IN_DCDC1} = 3.6 V; C_{OUT} = 10 µF to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value	See 表 8-1.		1	1.5	2.2	µH
	Tolerance			–30%		30%	
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		10	22	100[9]	µF
DCDC2 (1.1-V BUCK)							
V_{IN_DCDC2}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		2.7		5.5	V
V_{DCDC2}	Output voltage range	Adjustable through I^2C		0.85		1.675	V
	DC accuracy	$2.7 V \leq V_{IN} \leq 5.5 V$; $0 A \leq I_{OUT} \leq 1.8 A$		–2%		2%	
I_{OUT}	Continuous output current	$V_{IN\_DCDC2} > 2.7 V$				1.8	A
I_Q	Quiescent current	Total current from I_{N_DCDC2} pin; device not switching, no load			25	50	µA
$R_{DS(ON)}$	High-side FET on resistance	V_{IN_DCDC2} = 3.6 V			230	355	mΩ
	Low-side FET on resistance	V_{IN_DCDC2} = 3.6 V			90	145	
I_{LIMIT}	High-side current limit	V_{IN_DCDC2} = 3.6 V			2.8		A
	Low-side current limit	V_{IN_DCDC2} = 3.6 V			3.1		
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	95.9%	96.5%	97.1%	
	Hysteresis	V_{OUT} rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0b		1		ms
			STRICT = 1b		50		µs
		V_{OUT} rising	STRICT = 0b		10		µs
			STRICT = 1b		10		µs
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold	V_{OUT} rising, STRICT = 1b		102.9%	103.5%	104.1%	
	Hysteresis	V_{OUT} falling, STRICT = 1b			0.25%		
	Deglitch	V_{OUT} rising, STRICT = 1b			50		µs
I_{INRUSH}	Inrush current	V_{IN_DCDC2} = 3.6 V; C_{OUT} = 10 µF to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value	See 表 8-1.		1	1.5	2.2	µH
	Tolerance			–30%		30%	

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		10	22	100(9)	µF
DCDC3 (1.2-V BUCK)							
V_{IN_DCDC3}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		2.7		5.5	V
V_{DCDC3}	Output voltage range	Adjustable through I^2C		0.9		3.4	V
	DC accuracy	$2.7\ V \leqslant V_{IN} \leqslant 5.5\ V$; $0\ A \leqslant I_{OUT} \leqslant 1.8\ A$, $V_{IN\_DCDC3} \geqslant (V_{DCDC3} + 700\ mV)$		–2%		2%	
I_{OUT}	Continuous output current	$V_{IN\_DCDC3} > 2.7\ V$				1.8	A
I_Q	Quiescent current	Total current from IN_DCDC3 pin; Device not switching, no load			25	50	µA
$R_{DS(ON)}$	High-side FET on resistance	$V_{IN\_DCDC3} = 3.6\ V$			230	345	mΩ
	Low-side FET on resistance	$V_{IN\_DCDC3} = 3.6\ V$			100	150	
I_{LIMIT}	High-side current limit	$V_{IN\_DCDC3} = 3.6\ V$			2.8		A
	Low-side current limit	$V_{IN\_DCDC3} = 3.6\ V$			3		
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	95%	95.5%	96%	
	Hysteresis	V_{OUT} rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0b		1		ms
			STRICT = 1b		50		µs
		V_{OUT} rising	STRICT = 0b		10		µs
			STRICT = 1b		10		µs
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold	V_{OUT} rising, STRICT = 1b		104%	104.5%	105%	
	Hysteresis	V_{OUT} falling, STRICT = 1b			0.25%		
	Deglitch	V_{OUT} rising, STRICT = 1b			50		µs
I_{INRUSH}	Inrush current	$V_{IN\_DCDC3} = 3.6\ V$; $C_{OUT} = 10\ µF$ to $100\ µF$				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value	See 表 8-1.		1.0	1.5	2.2	µH
	Tolerance			–30%		30%	
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		10	22	100	µF
DCDC4 (3.3-V BUCK-BOOST) / ANALOG AND I/O							
V_{IN_DCDC4}	Input voltage soft-start range	$V_{IN\_BIAS} > V_{UVLO}$, –40°C to +55°C		3.4			V
		$V_{IN\_BIAS} > V_{UVLO}$, 56°C to 105°C		3.8			
	Input voltage operating range	$V_{IN\_BIAS} > V_{UVLO}$, –40°C to +105°C		2.7		5.5	V
V_{DCDC4}	Output voltage range	Adjustable through I^2C		1.175		3.4	V
	DC accuracy	$2.7\ V \leqslant V_{IN} \leqslant 5.5\ V$; $0\ A \leqslant I_{OUT} \leqslant 1\ A$		–2%		2%	
	Output voltage ripple	PFM mode enabled; $4.2\ V \leqslant V_{IN} \leqslant 5.5\ V$; $0\ A \leqslant I_{OUT} \leqslant 1\ A$ $C_{OUT} = 80\ µF$ $V_{OUT} = 3.3\ V$				200	mV_{pp}
	Minimum duty cycle in step-down mode					18%	

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Continuous output current	$V_{IN\_DCDC4} = 2.8$ V, $V_{OUT} = 3.3$ V				1	A
		$V_{IN\_DCDC4} = 3.6$ V, $V_{OUT} = 3.3$ V				1.3	
		$V_{IN\_DCDC4} = 5$ V, $V_{OUT} = 3.3$ V				1.6	
I_Q	Quiescent current	Total current from IN_DCDC4 pin; Device not switching, no load.			25	50	µA
f_{SW}	Switching frequency				2400		kHz
$R_{DS(ON)}$	High-side FET on resistance	$V_{IN\_DCDC3} = 3.6$ V	IN_DCDC4 to L4A		166		mΩ
			L4B to DCDC4		149		
	Low-side FET on resistance	$V_{IN\_DCDC3} = 3.6$ V	L4A to GND		142	190	
			L4B to GND		144	190	
I_{LIMIT}	Average switch current limit	$V_{IN\_DCDC4} = 3.6$ V			3000		mA
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0b	88.5%	90%	91.5%	
			STRICT = 1b	94.9%	95.5%	96.1%	
	Hysteresis	V_{OUT} rising	STRICT = 0b	3.8%	4.1%	4.4%	
			STRICT = 1b		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0b		1		ms
			STRICT = 1b		50		µs
		V_{OUT} rising	STRICT = 0b		10		µs
			STRICT = 1b		10		µs
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold	V_{OUT} rising, STRICT = 1b		103.9%	104.5%	105.1%	
	Hysteresis	V_{OUT} falling, STRICT = 1b			0.25%		
	Deglitch	V_{OUT} rising, STRICT = 1b			50		µs
I_{INRUSH}	Inrush current	$V_{IN\_DCDC4} = 3.6$ V; $C_{OUT} = 10$ µF to 100 µF				500	mA
R_{DIS}	Discharge resistor			150	250	350	Ω
L	Nominal inductor value	See 表 8-1.		1.2	1.5	2.2	µH
	Tolerance			−30%		30%	
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		40	80	100	µF
DCDC5 and DCDC6 POWER PATH							
V_{CC}	DCDC5 and DCDC6 input voltage range.	$V_{IN\_BU} = 0$ V		2.2		3.3	V
V_{IN_BU}	DCDC5 and DCDC6 input voltage range[1]			2.2		5.5	V
t_{RISE}	V_{CC}, V_{IN_BU} rise time	$V_{CC} = 0$ V to 3.3 V, $V_{IN\_BU} = 0$ V to 5.5 V		30			µs
$R_{DS(ON)}$	Power path switch impedance	CC to SYS_BU $V_{CC} = 2.4$ V, $V_{IN\_BU} = 0$ V			14.5		Ω
	Power path switch impedance	IN_BU to SYS_BU $V_{IN\_BU} = 3.6$ V			10.5		
I_{LEAK}	Forward leakage current	Into CC pin; $V_{CC} = 3.3$ V, $V_{IN\_BU} = 0$ V; OFF state; FSEAL = 0b; over full temperature range			50	300	nA
	Reverse leakage current	Out of CC pin; $V_{CC} = 1.5$ V; $V_{IN\_BU} = 5.5$ V; over full temperature range				500	
R_{CC}	Acceptable CC source impedance	$I_{OUT,\ DCDC5} < 10$ µA; $I_{OUT,\ DCDC6} < 10$ µA				1000	Ω

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IQ	Quiescent current	Average current into CC pin; RECOVERY or POWER_OFF state; V_{IN_BU} = 0 V; V_{CC} = 2.4 V; DCDC5 and DCDC6 enabled, no load T_J = 25°C		350		nA
Q_{INRUSH}	Inrush charge	V_{IN_BIAS} = decaying; CC = 3 V; C_{SYS_BU} = 1 µF; SYS_BU = 2.5 V to 3 V; CC_{series_resist} = 10 Ω C_{CC} = 4.7 µF		720		nC
DCDC5 (1-V BATTERY BACKUP SUPPLY)						
V_{DCDC5}	Output voltage			1		V
	DC accuracy	2.7 V ⩽ V_{IN_BU} ⩽ 5.5 V; I_{OUT} ⩾ 1 µA at −40°C ⩽ T_A ⩽ 35°C I_{OUT} ⩾ 4 µA at 35°C < T_A ⩽ 65°C I_{OUT} ⩾ 7 µA at T_A > 65°C	−2%		4%	
		2.2 V ⩽ V_{CC} ⩽ 3.3 V; I_{OUT} ⩾ 1 µA at −40°C ⩽ T_A ⩽ 35°C I_{OUT} ⩾ 4 µA at 35°C < T_A ⩽ 65°C I_{OUT} ⩾ 7 µA at T_A > 65°C V_{IN_BIAS} decay rate during CC transition > 150 V/s	−2%		4%	
		2.2 V ⩽ V_{CC} ⩽ 3.3 V; I_{OUT} ⩾ 1 µA at −40°C ⩽ T_A ⩽ 35°C I_{OUT} ⩾ 4 µA at 35°C < T_A ⩽ 65°C I_{OUT} ⩾ 7 µA at T_A > 65°C V_{IN_BIAS} decay rate during CC transition < 150 V/s	−10%		5%	
	Output voltage ripple	L = 10 µH; C_{OUT} = 22 µF; 100-µA load			32(10)	mV_{pp}
I_{OUT}	Continuous output current	2.2 V ⩽ V_{CC} ⩽ 3.3 V V_{IN_BU} = 0 V		10	100	µA
		2.7 V ⩽ V_{IN_BU} ⩽ 5.5 V			25	mA
$R_{DS(ON)}$	High-side FET on resistance	V_{IN_BU} = 2.8 V		2.5	3.5	Ω
	Low-side FET on resistance	V_{IN_BU} = 2.8 V		2	3	
I_{LIMIT}	High-side current limit	V_{IN_BU} = 2.8 V		50		mA
V_{PG}	Power-good threshold	V_{OUT} falling	79%	85%	91%	
	Hysteresis	V_{OUT} rising		6%		
L	Nominal inductor value	Chip inductor, see 表 8-2.	4.7	10	22	µH
	Tolerance		−30%		30%	
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2.	20(11)		47	µF
	Tolerance		−20%		20%	
DCDC6 (1.8-V BATTERY BACKUP SUPPLY)						
V_{DCDC6}	Output voltage			1.8		V
V_{DCDC6}	DC accuracy	2.7 V ⩽ V_{IN_BU} ⩽ 5.5 V; 1 µA ⩽ I_{OUT} ⩽ 25 mA	−2%		2%	
		2.2 V ⩽ V_{CC} ⩽ 3.3 V; 1 µA ⩽ I_{OUT} ⩽ 100 µA V_{IN_BIAS} decay rate during CC transition > 150 V/s	−2%		2%	
		2.2 V ⩽ V_{CC} ⩽ 3.3 V; 1 µA ⩽ I_{OUT} ⩽ 100 µA V_{IN_BIAS} decay rate during CC transition < 150 V/s	−5%		5%	
V_{DCDC6}	Output voltage ripple	L = 10 µH; C_{OUT} = 22 µF; 100-µA load			30(10)	mV_{pp}
I_{OUT}	Continuous output current	2.2 V ⩽ V_{CC} ⩽ 3.3 V V_{IN_BU} = 0 V		10	100	µA
		2.7 V ⩽ V_{IN_BU} ⩽ 5.5 V			25	mA

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	High-side FET on resistance	V_{IN_BU} = 3 V			2.5	3.5	Ω
	Low-side FET on resistance	V_{IN_BU} = 3 V			2	3	
I_{LIMIT}	High-side current limit	V_{IN_BU} = 3 V			50		mA
V_{PG}	Power-good threshold	V_{OUT} falling		87%	91%	95%	
	Hysteresis	V_{OUT} rising			3%		
L	Nominal inductor value	Chip inductor, see 表 8-2		4.7	10	22	µH
	Tolerance			–30%		30%	
C_{OUT}	Output capacitance value	Ceramic, X5R or X7R, see 表 8-2		20(11)		47	µF
	Tolerance			–20%		20%	
LDO1 (1.8-V LDO)							
V_{IN_LDO1}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		1.8		5.5	V
I_Q	Quiescent current	No load			35		µA
V_{OUT}	Output voltage range	Adjustable through I^2C		0.9		3.4	V
	DC accuracy	$V_{OUT} + 0.2\ V \leq V_{IN} \leq 5.5\ V$; $0\ A \leq I_{OUT} \leq 200\ mA$		–2%		2%	
I_{OUT}	Output current range	$V_{IN\_LDO1} - V_{DO} = V_{OUT}$		0		200	mA
		V_{IN_LDO1} > 2.7 V, V_{OUT} = 1.8 V		0		400	
I_{LIMIT}	Short circuit current limit	Output shorted to GND		445	550		mA
V_{DO}	Dropout voltage	I_{OUT} = 100 mA, V_{IN} = 3.6 V				200	mV
V_{PG}	Power-good threshold	V_{OUT} falling	STRICT = 0b	86%	90%	94%	
			STRICT = 1b	95%	95.5%	96%	
		Hysteresis, V_{OUT} rising	STRICT = 0b	3%	4%	5%	
			STRICT = 1b		0.25%		
	Deglitch	V_{OUT} falling	STRICT = 0b		1		ms
			STRICT = 1b		50		µs
		V_{OUT} rising	STRICT = 0b		10		µs
			STRICT = 1b		10		µs
	Time-out				5		ms
V_{OV}	Overvoltage detection threshold	V_{OUT} rising, STRICT = 1b		104%	104.5%	105%	
	Hysteresis	V_{OUT} falling, STRICT = 1b			0.25%		
	Deglitch	V_{OUT} rising, STRICT = 1b			50		µs
		V_{OUT} falling, STRICT = 1b			1		ms
R_{DIS}	Discharge resistor			150	250	350	Ω
C_{OUT}	Nominal output capacitance value	Ceramic, X5R or X7R		10		100	µF
LOAD SWITCH 1 (LS1)							
V_{IN_LS1}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		1.2		3.6	V

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Static on resistance	V_{IN_LS1} = 3.3 V, I_{OUT} = 300 mA, over full temperature range				110	m Ω
		V_{IN_LS1} = 1.8 V, I_{OUT} = 300 mA, DDR2, LPDDR, MDDR at 266 MHz over full temperature range				110	
		V_{IN_LS1} = 1.5 V, I_{OUT} = 300 mA, DDR3 at 333 MHz over full temperature range				110	
		V_{IN_LS1} = 1.35 V, I_{OUT} = 300 mA, DDR3L at 333 MHz over full temperature range				110	
		V_{IN_LS1} = 1.2 V, I_{OUT} = 200 mA, LPDDR2 at 333 MHz over full temperature range				150	
I_{LIMIT}	Short circuit current limit	Output shorted to GND		350			mA
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered.			15		ms
R_{DIS}	Internal discharge resistor at output[2]	LS1DCHRG = 1		150	250	350	Ω
T_{OTS}	Overtemperature shutdown[3]			125	132	139	°C
	Hysteresis				10		
C_{OUT}	Nominal output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		10		100	µF
LOAD SWITCH 2 (LS2)							
V_{IN_LS2}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		4		5.5	V
V_{UVLO}	Undervoltage lockout	Measured at IN_LS2. Supply falling[4]		2.48	2.6	2.7	V
	Hysteresis	Input voltage rising			170		mV
$R_{DS(ON)}$	Static on resistance	V_{IN_LS2} = 5 V, I_{OUT} = 500 mA, over full temperature range				500	m Ω
I_{LIMIT}	Short circuit current limit	Output shorted to GND; $V_{IN\_LS2} \geqslant 4$ V	LS2ILIM[1:0] = 00b	94		126	mA
			LS2ILIM[1:0] = 01b	188		251	
			LS2ILIM[1:0] = 10b	465		631	
			LS2ILIM[1:0] = 11b	922		1290	
I_{LEAK}	Reverse leakage current	$V_{LS2} > V_{IN\_LS2}$ + 1 V			12	30	µA
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered			15		ms
R_{DIS}	Internal discharge resistor at output[2]	LS2DCHRG = 1b		150	250	380	Ω
T_{OTS}	Overtemperature shutdown[4]			125	132	139	°C
	Hysteresis				10		
C_{OUT}	Nominal output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		1		100	µF
LOAD SWITCH 3 (LS3)							
V_{IN_LS3}	Input voltage range	$V_{IN\_BIAS} > V_{UVLO}$		1.8		10	V
$R_{DS(ON)}$	Static on resistance	V_{IN_LS3} = 9 V, I_{OUT}= 500 mA, over full temperature range				440	m Ω
		V_{IN_LS3} = 5 V, I_{OUT}= 500 mA, over full temperature range				526	
		V_{IN_LS3} = 2.8 V, I_{OUT}= 200 mA, over full temperature range				656	
		V_{IN_LS3} = 1.8 V, I_{OUT}= 200 mA, over full temperature range				910	

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{LIMIT}	Short circuit current limit	V_{IN_LS3} > 2.3 V, Output shorted to GND	LS3ILIM[1:0] = 00b	98		126	mA
			LS3ILIM[1:0] = 01b	194		253	
			LS3ILIM[1:0] = 10b	475		738	
			LS3ILIM[1:0] = 11b	900		1234	
		$V_{IN\_LS3} \leqslant$ 2.3 V, Output shorted to GND	LS3ILIM[1:0] = 00b	98		126	
			LS3ILIM[1:0] = 01b	194		253	
			LS3ILIM[1:0] = 10b	475		738	
t_{BLANK}	Interrupt blanking time	Output shorted to GND until interrupt is triggered.			15		ms
R_{DIS}	Internal discharge resistor at output(2)	LS3DCHRG = 1		650	1000	1500	Ω
T_{OTS}	Overtemperature shutdown(4)			125	132	139	°C
	Hysteresis				10		°C
C_{OUT}	Nominal output capacitance value	Ceramic, X5R or X7R, see 表 8-2.		1	100	220	μF
BACKUP BATTERY MONITOR							
V_{TH}	Comparator threshold	Ideal level			3		V
		Good level			2.6		V
		Low level			2.3		V
	Accuracy			–3%		3%	
R_{LOAD}	Load impedance	Applied from CC to GND during comparison.		70	100	130	kΩ
t_{DLY}	Measurement delay	R_{LOAD} is connected during delay time. Measurement is taken at the end of delay.			600		ms
I/O LEVELS AND TIMING CHARACTERISTICS							
PG_{DLY}	PGOOD delay time	PGDLY[1:0] = 00b			10		ms
		PGDLY[1:0] = 01b			20		
		PGDLY[1:0] = 10b			50		
		PGDLY[1:0] = 11b			150		
t_{DG}	Deglitch time	PB input	Rising edge		100		ms
			Falling edge		50		ms
		AC_DET input	Rising edge		100		μs
			Falling edge		10		ms
		PWR_EN input	Rising edge		10		ms
			Falling edge		100		μs
		GPIO1	Rising edge		1		ms
			Falling edge		1		ms
		GPIO3	Rising edge		5		μs
			Falling edge		5		μs
t_{RESET}	Reset time	PB input held low	TRST = 0b		8		s
			TRST = 1b		15		
V_{IH}	High level input voltage	SCL, SDA, GPIO1, and GPIO3		1.3			V
		AC_DET, PB		0.66 × IN_BIAS			
		PWR_EN		1.3			
V_{IL}	Low level input voltage	SCL, SDA, PWR_EN, AC_DET, PB, GPIO1, and GPIO3		0		0.4	V

6.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	GPO2; I_{SOURCE} = 5 mA; GPO2_BUF = 1	V_{IN_LS1} – 0.3		V_{IN_LS1}	V
		PGOOD_BU; I_{SOURCE} = 100 µA	V_{DCDC6} – 10 mV			
V_{OL}	Low level output voltage	nWAKEUP, nINT, SDA, PGOOD, GPIO1, GPO2, and GPIO3; I_{SINK} = 2 mA	0		0.3	V
		nPFO; I_{SINK} = 2 mA	0		0.35	
		PGOOD_BU; I_{SINK} = 100 µA	0		0.3	
V_{PFI}	Power-fail comparator threshold	Input falling		800		mV
	Hysteresis	Input rising		40		mV
	Accuracy		– 4%		4%	
	Deglitch	Input falling		25		µs
		Input rising		10		ms
I_{DC34_SEL}	DC34_SEL bias current	Enabled only at power-up.		10		µA
V_{DC34_SEL}	DCDC3 and DCDC4 power-up default selection thresholds	Threshold 1		100		mV
		Threshold 2		163		
		Threshold 3		275		
		Threshold 4		400		
		Threshold 5		575		
		Threshold 6		825		
		Threshold 7		1200		
R_{DC34_SEL}	DCDC3 and DCDC4 power-up default selection resistor values	Setting 0	0	0	7.7	kΩ
		Setting 1	11.3	12.1	13	
		Setting 2	18.1	20	22	
		Setting 3	30.9	31.6	32.3	
		Setting 4	44.8	45.3	46.4	
		Setting 5	64.2	64.9		
		Setting 6	92.9	95.3	96.9	
		Setting 7	135.3	150		
I_{BIAS}	Input bias current	SCL, SDA, GPIO1(5), GPIO3 (5); V_{IN} = 3.3 V		0.01	1	µA
		PB, AC_DET, PFI; V_{IN} = 3.3 V			500	nA
I_{LEAK}	Pin leakage current	nINT, nWAKEUP, nPFO, PGOOD, PWR_EN, GPIO1(6), GPO2(7), GPIO3(6) V_{OUT} = 3.3 V			500	nA
OSCILLATOR						
f_{OSC}	Oscillator frequency			2400		kHz
	Frequency accuracy	T_J = – 40°C to +105°C	– 12%		12%	
OVERTEMPERATURE SHUTDOWN						
T_{OTS}	Overtemperature shutdown	Increasing junction temperature	135	145	155	°C
	Hysteresis	Decreasing junction temperature		20		
T_{WARN}	High-temperature warning	Increasing junction temperature	90	100	110	°C
	Hysteresis	Decreasing junction temperature		15		

(1) IN_BU has priority over CC input.
(2) Discharge function disabled by default.
(3) Switch is temporarily turned OFF if temperature exceeds OTS threshold.
(4) Switch is temporarily turned OFF if input voltage drops below UVLO threshold.
(5) Configured as input.

(6) Configured as output.
(7) Configured as open-drain output.
(8) 200-mV hysteresis option is available for the TPS65218B101 device option.
(9) 500-µF of remote capacitance can be supported for DCDC1 and DCDC2.
(10) For PHP package: 160 mVpp at -40°C, and 120 mVpp from 25°C to 105°C.
(11) For PHP package: 40 µF.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
f_{SCL}	Serial clock frequency			100		kHz
				400		
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 kHz	4			µs
		SCL = 400 kHz(1)	1			
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 kHz	0		3.45	µs
		SCL = 400 kHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
t_{BUF}	Bus free time between STOP and START condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	SCL = 100 kHz	—(2)		—(2)	ns
		SCL = 400 kHz	0		50	
C_b	Capacitive load for each bus line	SCL = 100 kHz			400	pF
		SCL = 400 kHz			400	

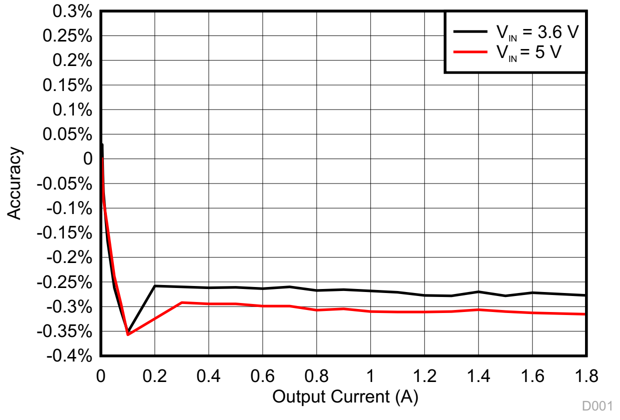
---

(1) The SCL duty cycle at 400 kHz must be > 40%.

(2) The inputs of I^2C devices in Standard-mode do not require spike suppression.

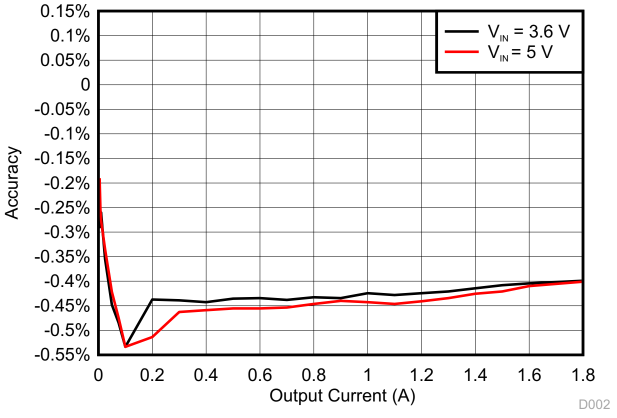
6.7 Typical Characteristics

At T_J = 25°C unless otherwise noted.



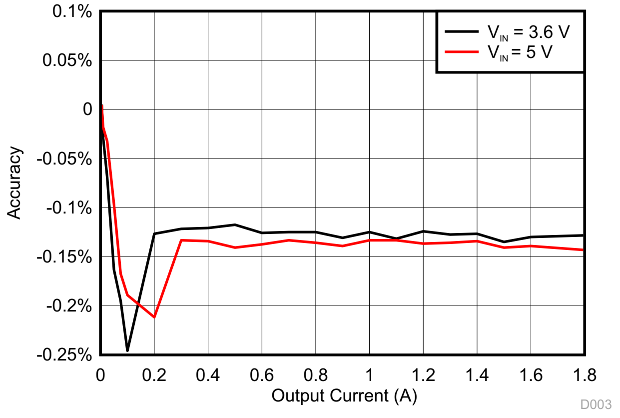
V_{OUT} = 1.1 V

图 6-1. DCDC1 Accuracy



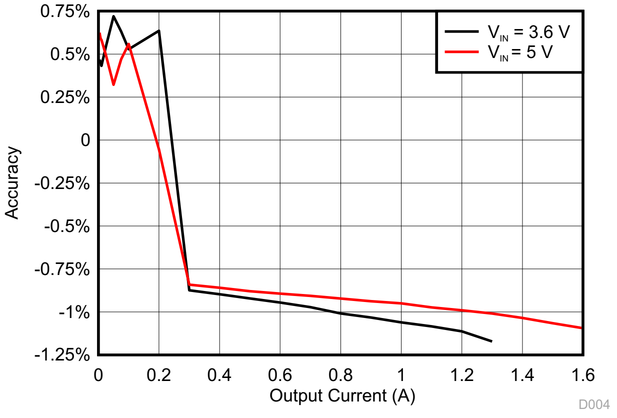
V_{OUT} = 1.1 V

图 6-2. DCDC2 Accuracy



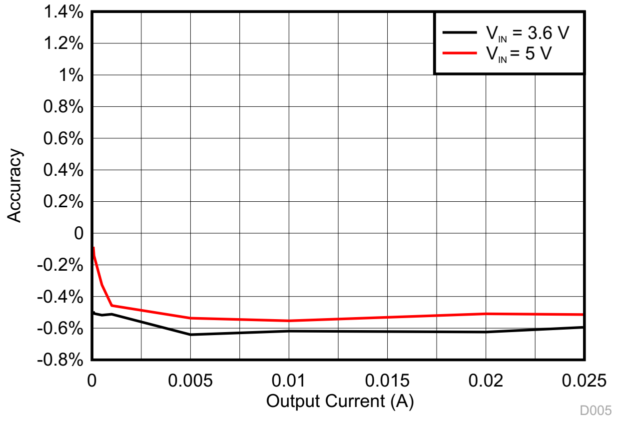
V_{OUT} = 1.2 V

图 6-3. DCDC3 Accuracy



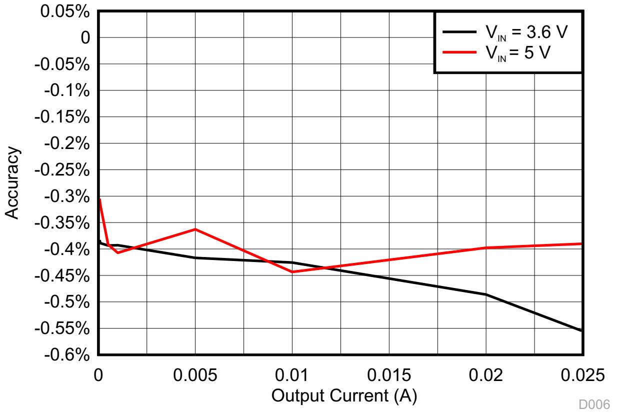
V_{OUT} = 3.3 V

图 6-4. DCDC4 Accuracy



V_{OUT} = 1 V

图 6-5. DCDC5 Accuracy



V_{OUT} = 1.8 V

图 6-6. DCDC6 Accuracy

7 Detailed Description

7.1 Overview

The TPS65218 provides three step-down converters, three load switches, three general-purpose I/Os, two battery backup supplies, one buck-boost converter, and one LDO. The system can be supplied by a single cell Li-Ion battery or regulated 5-V supply. The device is characterized across a –40°C to +105°C temperature range, which makes it suitable for various industrial applications.

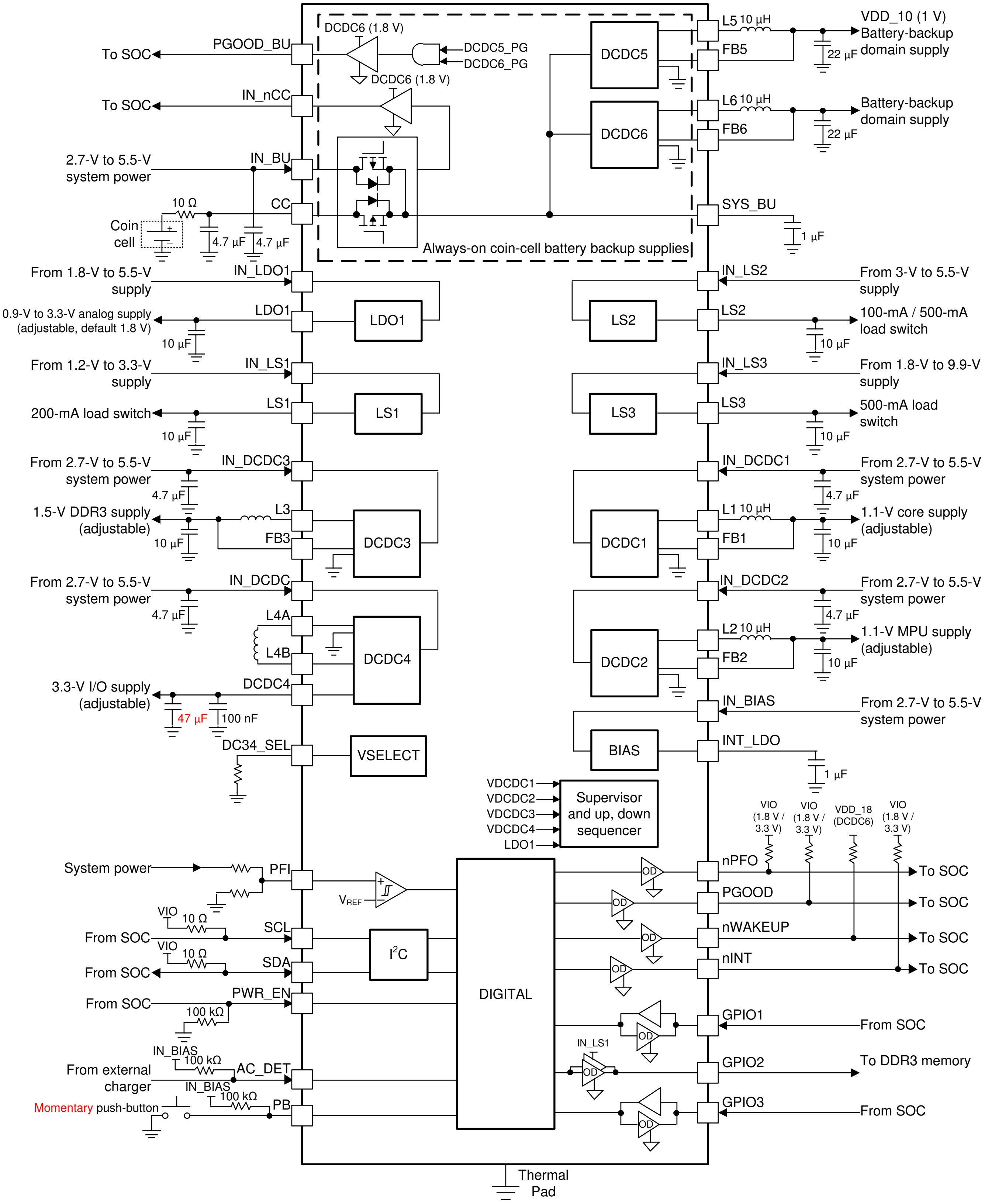
The I^2C interface provides comprehensive features for using TPS65218. All rails, load switches , and GPIOs can be enabled and disabled. Voltage thresholds for the UVLO and supervisor can be customized. Power-up and power-down sequences can also be programmed through I^2C. Interrupts for overtemperature, overcurrent, and undervoltage can be monitored for the load-switches (LSx).

The integrated voltage supervisor monitors DCDC 1-4 and LDO1. It has two settings; the standard settings only monitor for undervoltage, while the strict settings implement tight tolerances on both undervoltage and overvoltage. A power-good signal is provided to report the regulation state of the five rails.

The three hysteretic step-down converters can each supply up to 1.8 A of current. The default output voltages for each converter can be adjusted through the I^2C interface. DCDC1 and DCDC2 features dynamic voltage scaling with an adjustable slew rate. The step-down converters operate in a low power mode at light load, and can be forced into power mode (PWM) operation for noise sensitive applications.

The battery backup supplies consist of two low power step-down converters optimized for very light loads and are monitored with a separate power-good signal (PGOOD_BU). The converters can be configured to operate as always-on supplies with the addition of a coin cell battery. The state of the battery can be monitored over I^2C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Wake-Up and Power-Up and Power-Down Sequencing

The TPS65218 has a predefined power-up and power-down sequence, which does not change in a typical application. The user can define custom sequences with I^2C. The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order of enabling rails. A single rail is assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times between strobes are between 2 ms and 5 ms.

7.3.1.1 Power-Up Sequencing

When the power-up sequence initiates, STROBE 1 occurs, and any rail assigned to this strobe is enabled. After a delay time of DLY1, STROBE 2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I^2C control. The power-up sequence executes if one of the following events occurs:

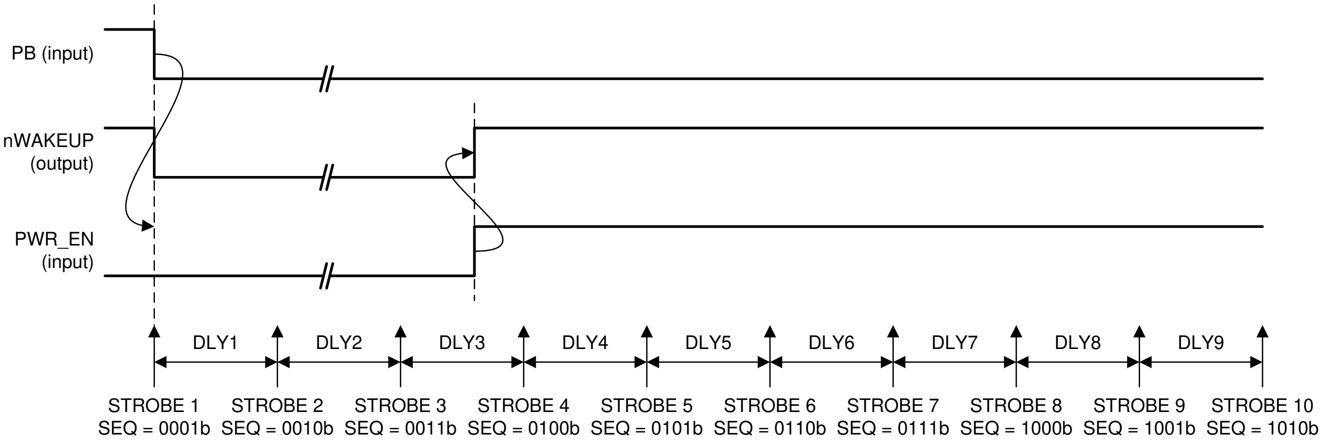
- From the OFF state:
  - The push-button (PB) is pressed (falling edge on PB) *or*
  - The AC_DET pin is pulled low (falling edge) *or*
  - The PWR_EN is asserted (driven to high-level) *or*
  - The main power is connected (IN_BIAS) and AC_DET is grounded *and*
  - The device is not in undervoltage lockout (UVLO) or overtemperature shutdown (OTS).
- From the PRE_OFF state:
  - The PB is pressed (falling edge on PB) *or*
  - The AC_DET pin is pulled low (falling edge) *or*
  - The PWR_EN is asserted (driven to high-level) *and*
  - The device is not in UVLO or OTS.
- From the SUSPEND state:
  - The PB is pressed (falling edge on PB) *or*
  - The AC_DET pin is pulled low (falling edge) *or*
  - The PWR_EN pin is pulled high (level sensitive) *and*
  - The device is not in UVLO or OTS.

When a power-up event is detected, the device enters a WAIT_PWR_EN state and triggers the power-up sequence. The device remains in WAIT_PWR_EN as long as the PWR_EN and either the PB or AC_DET pin are held low. If both, the PB and AC_DET return to logic-high state and the PWR_EN pin has not been asserted within 20 s of entering WAIT_PWR_EN state, the power-down sequence is triggered and the device returns to OFF state. Once PWR_EN is asserted, the device advances to ACTIVE state, which is functionally equivalent to WAIT_PWR_EN. However, the AC_DET pin is ignored and power-down is controlled by the PWR_EN pin only.

Rails not assigned to a strobe (SEQ = 0000b) are not affected by power-up and power-down sequencing and remain in their current ON or OFF state regardless of the sequencer. A rail can be enabled and disabled at any time by setting the corresponding enable bit in the ENABLEx register, with the exception that the ENABLEx register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail. For example, the sequencer sets and resets the enable bits for the rails under its control.

Note

The power-up sequence is defined by strobes and delay times, and can be triggered by the PB, AC_DET (not shown, same as PB), or PWR_EN pin.



Push-button deglitch time is not shown.

图 7-1. Power-Up Sequences from OFF or SUSPEND State; PB is Power-Up Event

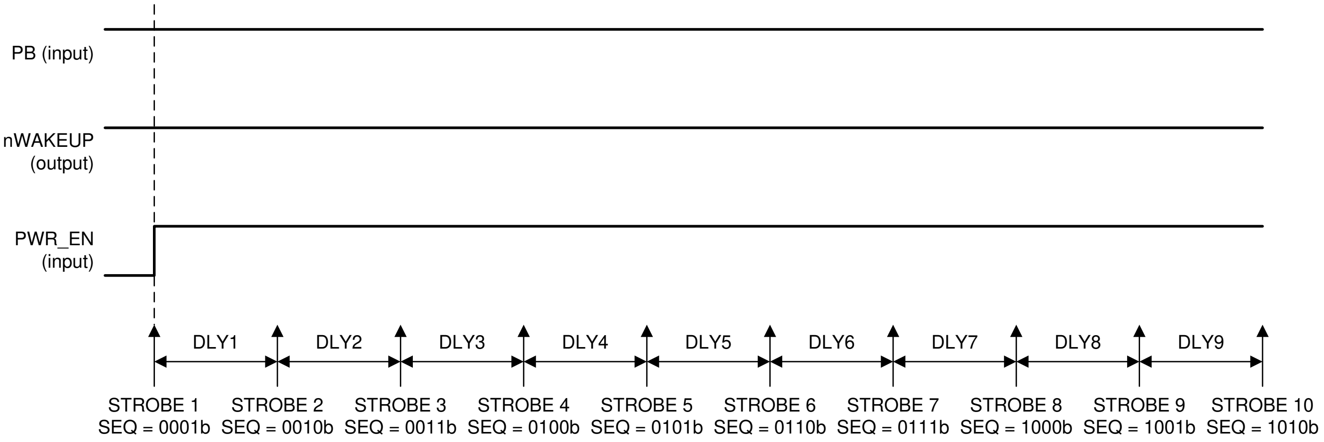


图 7-2. Power-Up Sequences from SUSPEND State; PWR_EN is Power-Up Event

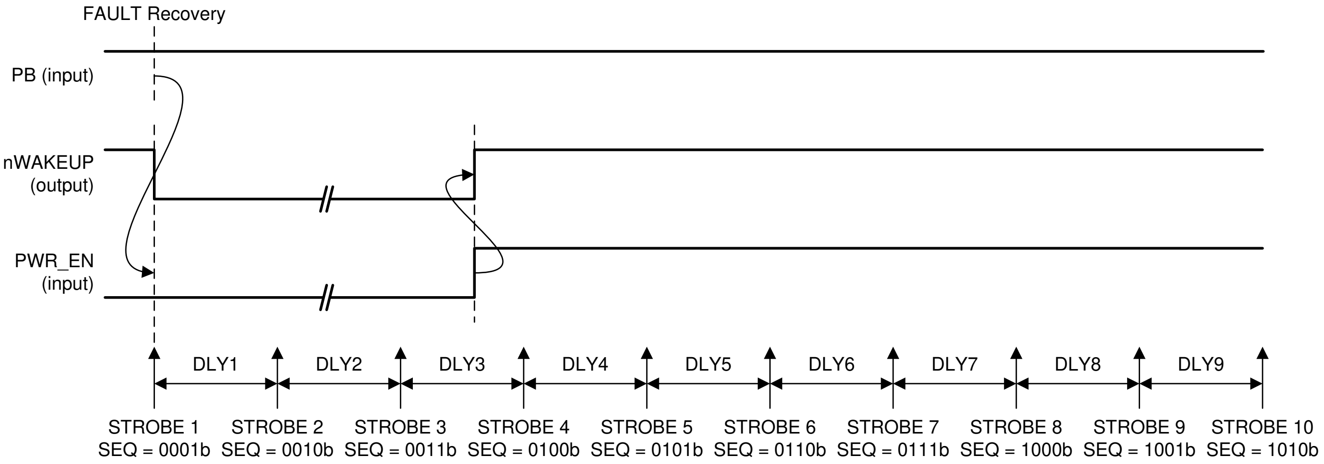


图 7-3. Power-Up Sequences from RECOVERY State

7.3.1.2 Power-Down Sequencing

By default, the power-down sequence follows the reverse of the power-up sequence. When the power-down sequence is triggered, STROBE 10 occurs and any rail assigned to STROBE 10 is shut down and its discharge circuit is enabled. After a delay time of DLY9, STROBE 9 occurs and any rail assigned to it is shut down and its discharge circuit is enabled. The sequence continues until all strobes occur and all DLYx times execute. The DLYx times are extended by a factor of 10x to provide ample time for discharge, and preventing output voltages from crossing during shut-down. The DLYFCTR bit is applied globally to all power-down delay times. Regardless of the DLYx and DLYFCTR settings, the PMIC enters OFF, SUSPEND, or RECOVERY state 500 ms after the power-down sequence initiates, to ensure that the discharge circuits remain enabled for a minimum of 150 ms before the next power-up sequence starts.

A power-down sequence executes if one of the following events occurs:

- The device is in the WAIT_PWR_EN state, the PB and AC_DET pins are high, PWR_EN is low, and the 20-s timer has expired.
- The device is in the ACTIVE state and the PWR_EN pin is pulled low.
- The device is in the WAIT_PWR_EN, ACTIVE, or SUSPEND state and the push-button is held low for > 8 s (15 s if TRST = 1b).
- A fault occurs in the device (OTS, UVLO, PGOOD failure).

When transitioning from ACTIVE to SUSPEND state, the rails not controlled by the power-down sequencer maintains the same ON/OFF state in SUSPEND state that it had in ACTIVE state. This allows for the selected power rails to remain powered up when in the SUSPEND state.

When transitioning to the OFF or RECOVERY state, rails not under sequencer control are shut-down as follows:

- DCDC1, DCDC2, DCDC3, DCDC4, LDO1, and LS1 shut down at the beginning of the power-down sequence, if not under sequencer control (SEQ = 0b).
- LS2 and LS3 shut down as the state machine enters an OFF or RECOVERY state; 500 ms after the power-down sequence is triggered.

If the supply voltage on IN_BIAS drops below 2.5 V, the digital core is reset and all power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4, and LDO1). The amount of time the discharge circuitry remains active is a function of the INT_LDO hold up time (see 节 7.3.1.6 for more details).

7.3.1.3 Strobe 1 and Strobe 2

STROBE 1 and STROBE 2 are dedicated to DCDC5 and DCDC6 which are *always-on*; powered up as soon as the device exits the OFF state, and ON in any other state. STROBE 1 and STROBE 2 options are available only for DCDC5 and DCDC6, not for any other rails.

STROBE 1 and STROBE 2 occur in every power-up sequence, regardless if the rail is already powered up. If the rail is not to be powered up, its respective strobe setting must be set to 0x00.

When a power-down sequence initiates, STROBE 1 and STROBE 2 occur only if the FSEAL bit is 0b. Otherwise, both strobes are omitted and DCDC5 and DCDC6 maintain state.

Note

The power-down sequence follows the reverse of the power-up sequence. STROBE2 and STROBE1 are executed only if FSEAL bit is 0b.

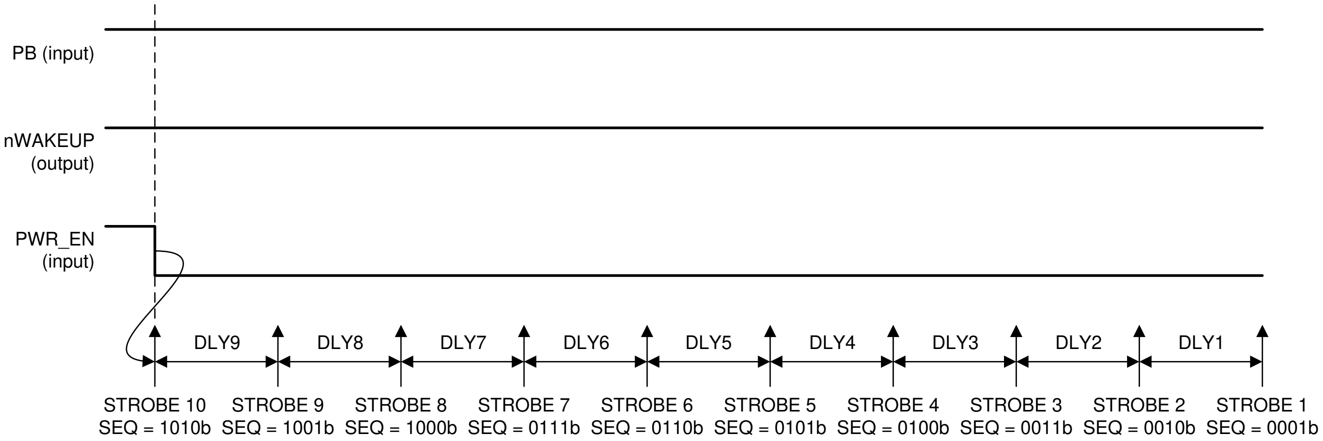
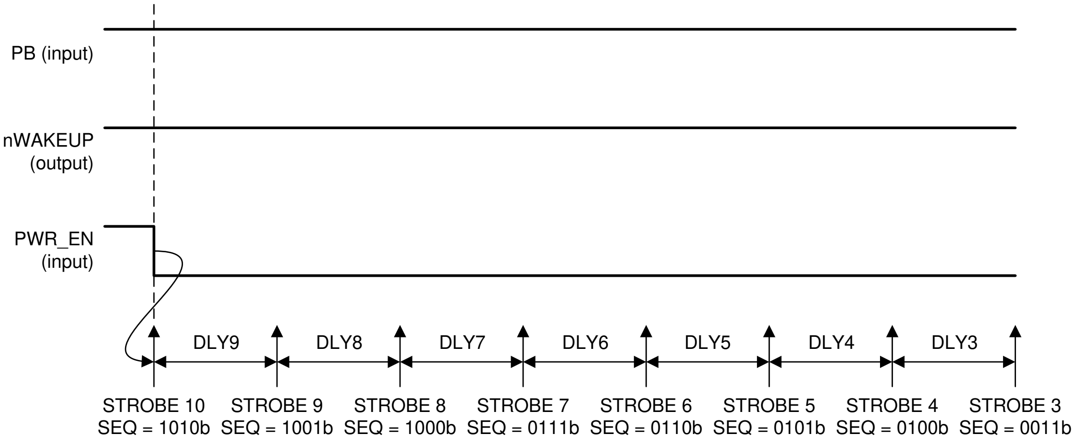
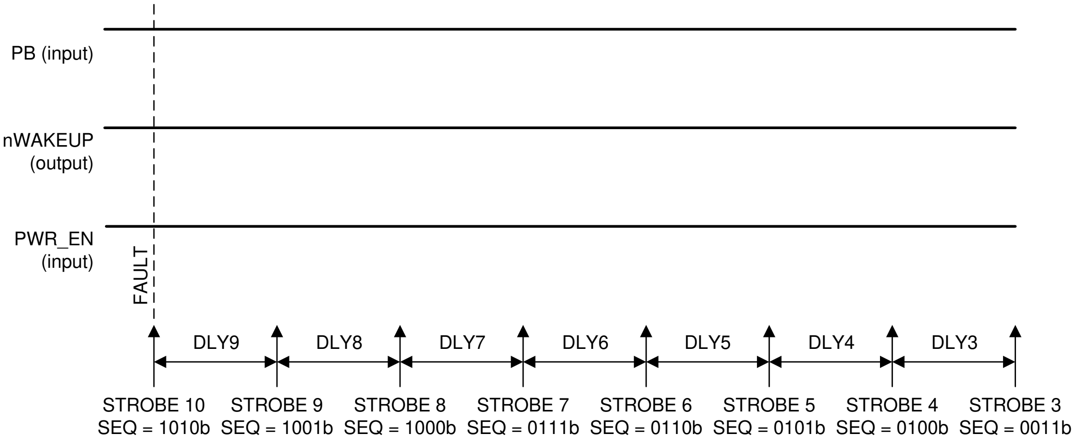


图 7-4. Power-Down Sequences to OFF State; PWR_EN is Power-Down Event; FSEAL = 0b



STROBE2 and STROBE1 are not shown.

图 7-5. Power-Down Sequences to SUSPEND State; PWR_EN is Power-Down Event; FSEAL = 1b



STROBE2 and STROBE1 are not shown.

图 7-6. Power-Down Sequences to RECOVERY State; TSD or UV is Power-Down Event; FSEAL = 1b

7.3.1.4 Supply Voltage Supervisor and Power-Good (PGOOD)

Power-good (PGOOD) is an open-drain output of the built-in voltage supervisor that monitors DCDC1, DCDC2, DCDC3, DCDC4, and LDO1. The output is Hi-Z when all enabled rails are in regulation and driven low when one or more rails encounter a fault which brings the output voltage outside the specified tolerance range. In a typical application PGOOD drives the reset signal of the SOC.

The supervisor has two modes of operation, controlled by the STRICT bit. With the STRICT bit set to 0, all enabled rails of the five regulators are monitored for undervoltage only with relaxed thresholds and deglitch times. With the STRCT bit set to 1, all enabled rails of the five regulators are monitored for undervoltage and overvoltage with tight limits and short deglitch times. 表 7-1 summarizes these details.

表 7-1. Supervisor Characteristics Controlled by the STRICT Bit

PARAMETER		STRICT = 0b (TYP)	STRICT =1b (TYP)
Undervoltage monitoring	Threshold (output falling)	90%	96.5% (DCDC1 and DCDC2) 95.5% (DCDC3, DCDC4, and LDO1)
	Deglitch (output falling)	1 ms	50 µs
	Deglitch (output rising)	10 µs	10 µs
Overvoltage monitoring	Threshold (output falling)	N/A	103.5% (DCDC1 and DCDC2) 104.5% (DCDC3, DCDC4, and LDO1)
	Deglitch (output falling)	N/A	1 ms
	Deglitch (output rising)	N/A	50 µs

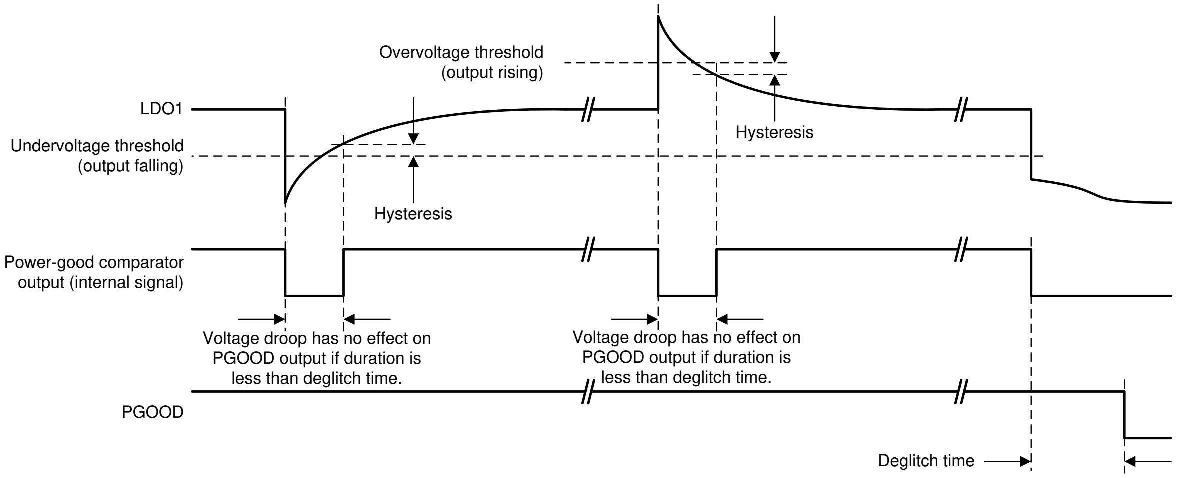


图 7-7. Definition of Undervoltage, Overvoltage Thresholds, Hysteresis, and Deglitch Times

The following rules apply to the PGOOD output:

- The power-up default state for THE PGOOD is low. When all rails are disabled, the PGOOD output is driven low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5 ms after the rail is enabled and is continuously monitored thereafter. This allows the rail to power-up.
- The PGOOD is delayed by PGDLY time after the sequencer is finished and the last rail is enabled.
- If an enabled rail is continuously outside the monitoring threshold for longer than the deglitch time, then the PGOOD is pulled low, and all rails are shut-down following the power-down sequence. PGDLY does not apply.
- Disabling a rail manually by resetting the DCx_EN or LDO1_EN bit has no effect on the PGOOD pin. If all rails are disabled, the PGOOD is driven low as the last rail is disabled.
- If the power-down sequencer is triggered, PGOOD is driven low.
- The PGOOD is driven low in the SUSPEND state, regardless of the number of rails that are enabled.

图 7-8 shows a typical power-up sequence and PGOOD timing.

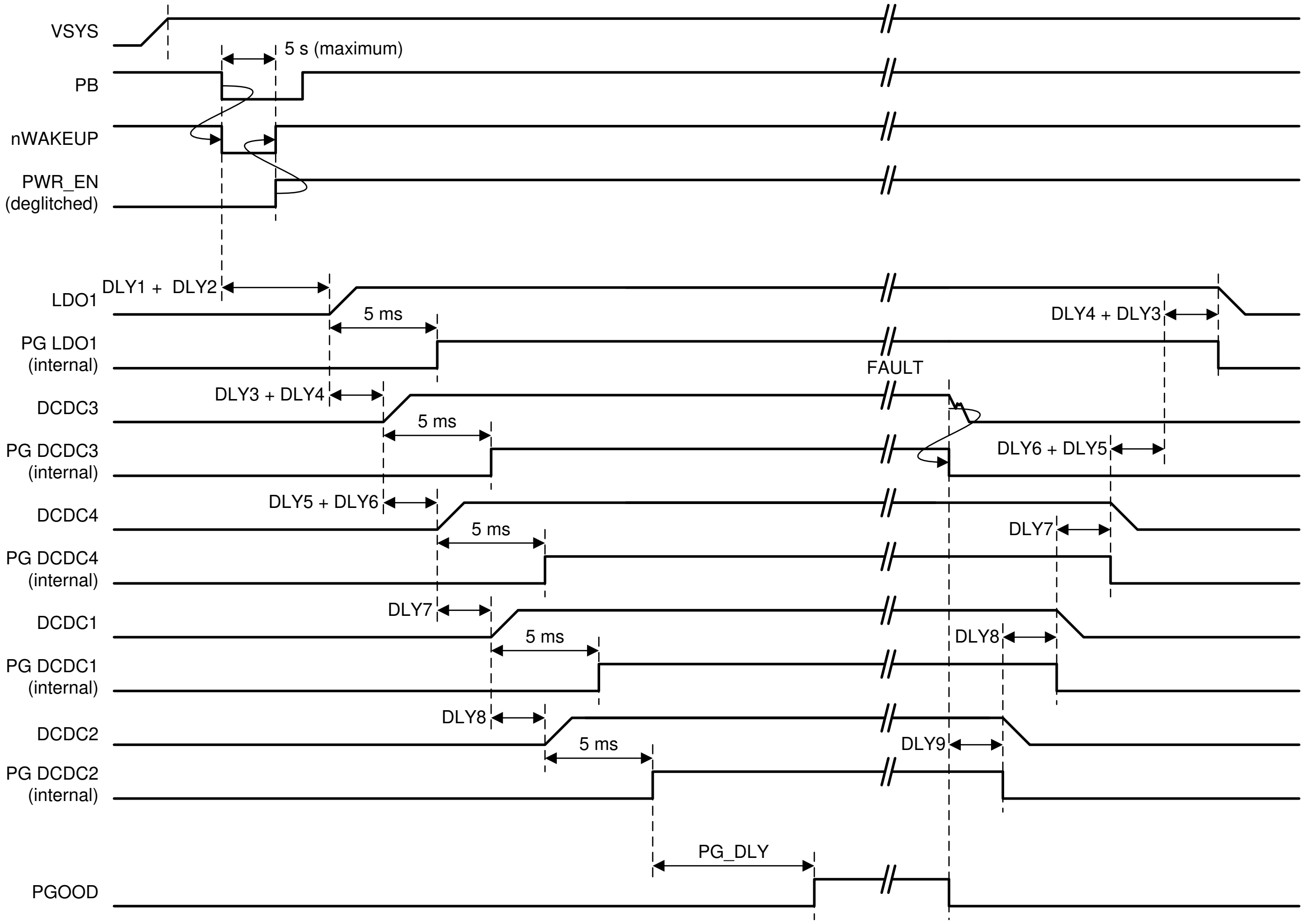


图 7-8. Typical Power-Up Sequence of the Main Output Rails

7.3.1.5 Backup Supply Power-Good (PGOOD_BU)

PGOOD_BU is a push-pull output indicating if DCDC5 and DCDC6 are in regulation. The output is driven to high when both rails are in regulation, and driven low if at least one of the rails is below the power-good threshold. The output-high level is equal to the output voltage of DCDC6.

PGOOD_BU is the logical *and* between PGOOD (DCDC5) and PGOOD (DCDC6), and has no delay time built-in. Unlike the main power-good, a fault on DCDC5 or DCDC6 does not trigger the power-down sequencer, does not disable any of the rails in the system, and has no effect on the PGOOD pin. DCDC5 and DCDC6 recover automatically once the fault is removed.

Note

In this example, the power-down is triggered by a fault on DCDC3.

7.3.1.6 Internal LDO (INT_LDO)

The internal LDO provides a regulated voltage to the internal digital core and analog circuitry. The internal LDO has a nominal output voltage of 2.5 V and can support up to 10 mA of external load.

When system power fails, the UVLO comparator triggers the power-down sequence. If system power drops below 2.5 V, the digital core is reset and all remaining power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4 and LDO1).

The internal LDO reverse blocks to prevent the discharging of the output capacitor (C_{INT_LDO}) on the INT_LDO pin. The remaining charge on the INT_LDO output capacitor provides a supply for the power rail discharge circuitry to ensure the outputs are discharged to ground even if the system supply has failed. The amount of hold-up time specified in 节 6.5 is a function of the output capacitor value (C_{INT_LDO}) and the amount of external load on the INT_LDO pin, if any. The design allows for enough hold-up time to sufficiently discharge DCDC1-4, and LDO1 to ensure proper processor power-down sequencing. The amount of hold-up time is a function of the output capacitor value, which should not exceed 22 µF and the amount of external load, if any.

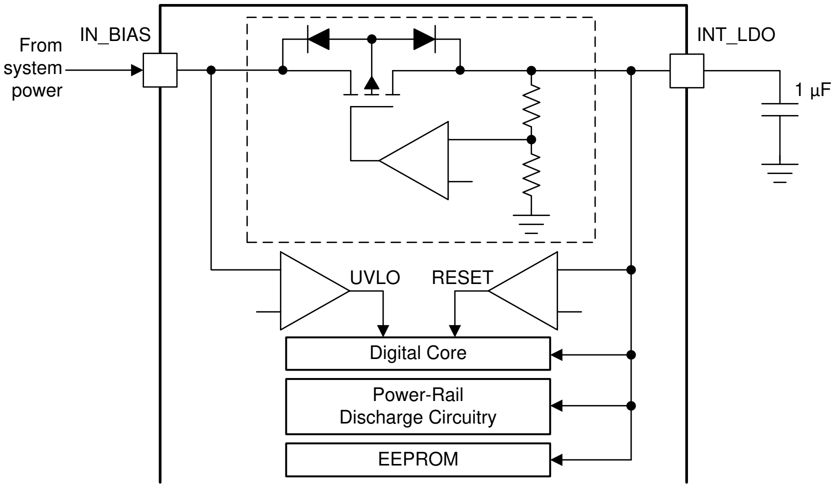


图 7-9. Internal LDO and UVLO Sensing

7.3.1.7 Current Limited Load Switches

The TPS65218 provides three current limited load switches with individual inputs, outputs, and enable control. Each switch provides the following control and diagnostic features:

- The ON or OFF state of the switch is controlled by the corresponding LSx_EN bit in the ENABLE register.
- LS1 can be controlled by the sequencer or through I^{2}C communication.
- LS2 and LS3 can *only* be controlled through I^{2}C communication. The sequencer has no control over LS2 and LS3.
- Each switch has an active discharge function, disabled by default, and enabled through the LSxDCHRG bit. When enabled, the switch output is discharged to ground whenever the switch is disabled.
- When the PFI input drops below the power-fail threshold (the power-fail comparator trips), the load switches are automatically disabled to shed system load. This function must be individually enabled for each switch through the corresponding LSxnPFO bit. The switches do not turn back on automatically as the system voltage recovers, and must be manually re-enabled.
- An interrupt (LSx_I) issues whenever a load switch actively limits the output current, such as when the output load exceeds the current limit value. The switch remains ON and provides current to the load according to the current-limit setting.
- All three load switches have local overtemperature sensors which disable the corresponding switch if the power dissipation and junction temperature exceeds the safe operating value. The switch automatically recovers once the temperature drops below the OTS threshold value minus hysteresis. The LSx_F (fault) interrupt bit is set while the switch is held OFF by the OTS function.

7.3.1.7.1 Load Switch 1 (LS1)

LS1 is a non-reverse blocking, low-voltage (< 3.6 V), low-impedance switch intended to support DDRx self-refresh mode by cutting off the DDRx supply to the SOC DDRx interface during SUSPEND mode. In a typical application, the input of LS1 is tied to the output of DCDC3 while the output of LS1 is connected to the memory-interface supply pin of the SOC. LS1 can be controlled by the internal sequencer, just as any power rail.

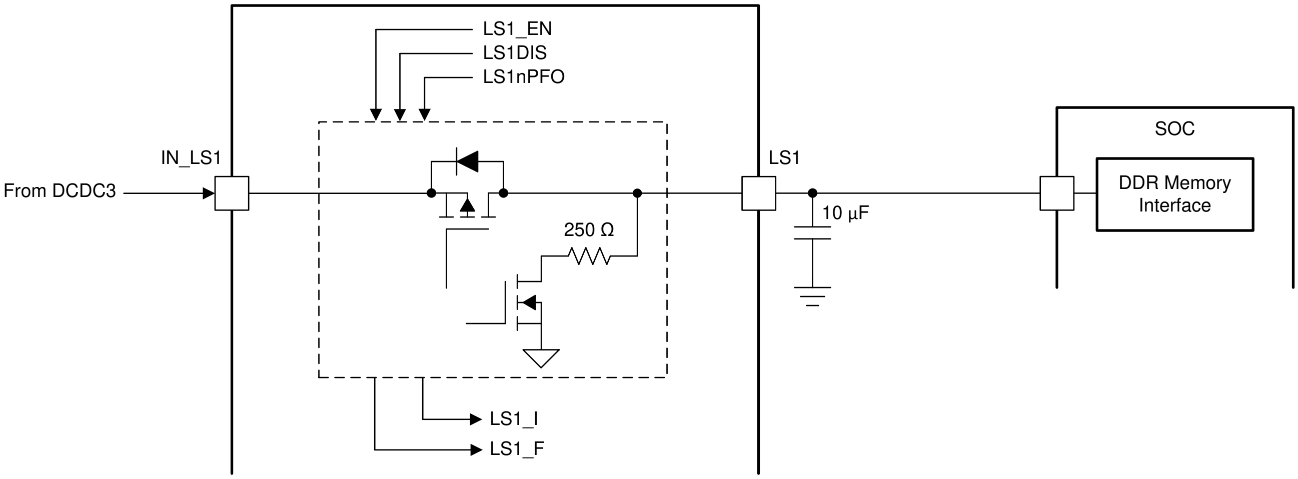


图 7-10. Typical Application of Load Switch 1

7.3.1.7.2 Load Switch 2 (LS2)

LS2 is a reverse-blocking, 5 V, low-impedance switch. Load switch 2 provides four different current limit values (100/200/500/1000 mA) that are selectable through LS2ILIM[1:0] bits. Overcurrent is reported through the LS2_I interrupt.

LS2 has its own input-undervoltage protection which forces the switch OFF if the switch input voltage (V_{IN_LS2}) is <2.7 V. Similar to OTS, the LS2_F interrupt is set when the switch is held OFF by the local UVLO function, and the switch recovers automatically when the input voltage rises above the UVLO threshold.

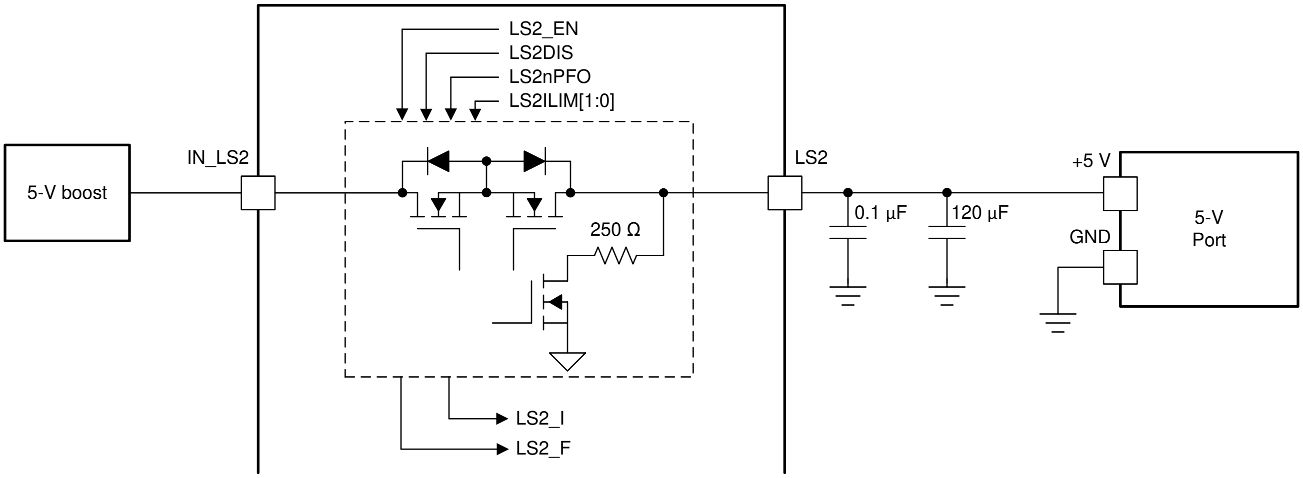


图 7-11. Typical Application of Load Switch 2

7.3.1.7.3 Load Switch 3 (LS3)

LS3 is a non-reverse blocking, medium-voltage (< 10 V), low-impedance switch that can be used to provide 1.8-V to 10-V power to an auxiliary port. LS3 has four selectable current limit values that are selectable through LS3ILIM[1:0].

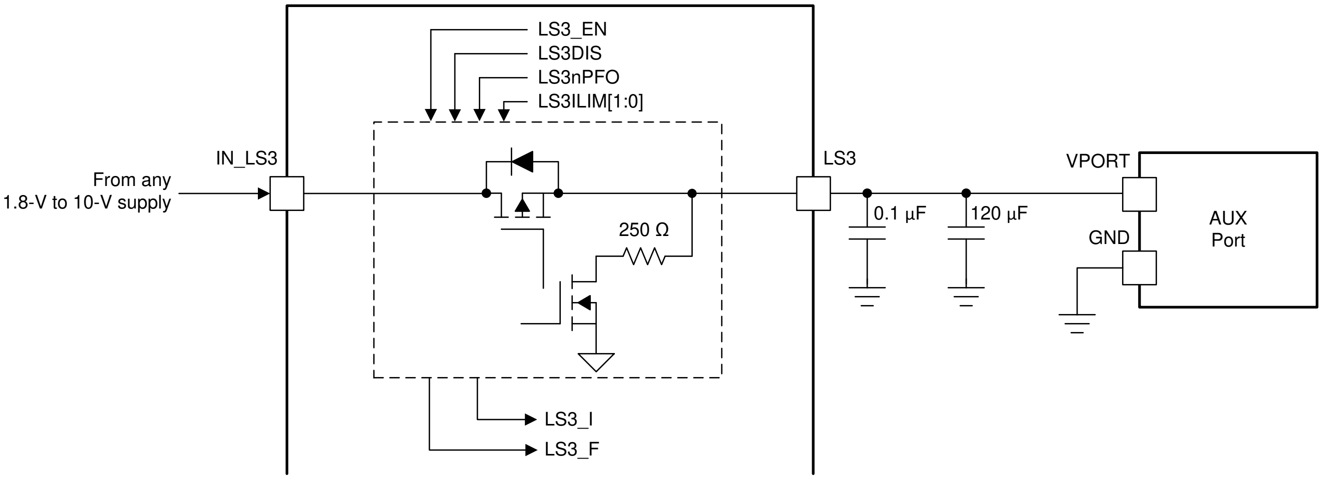
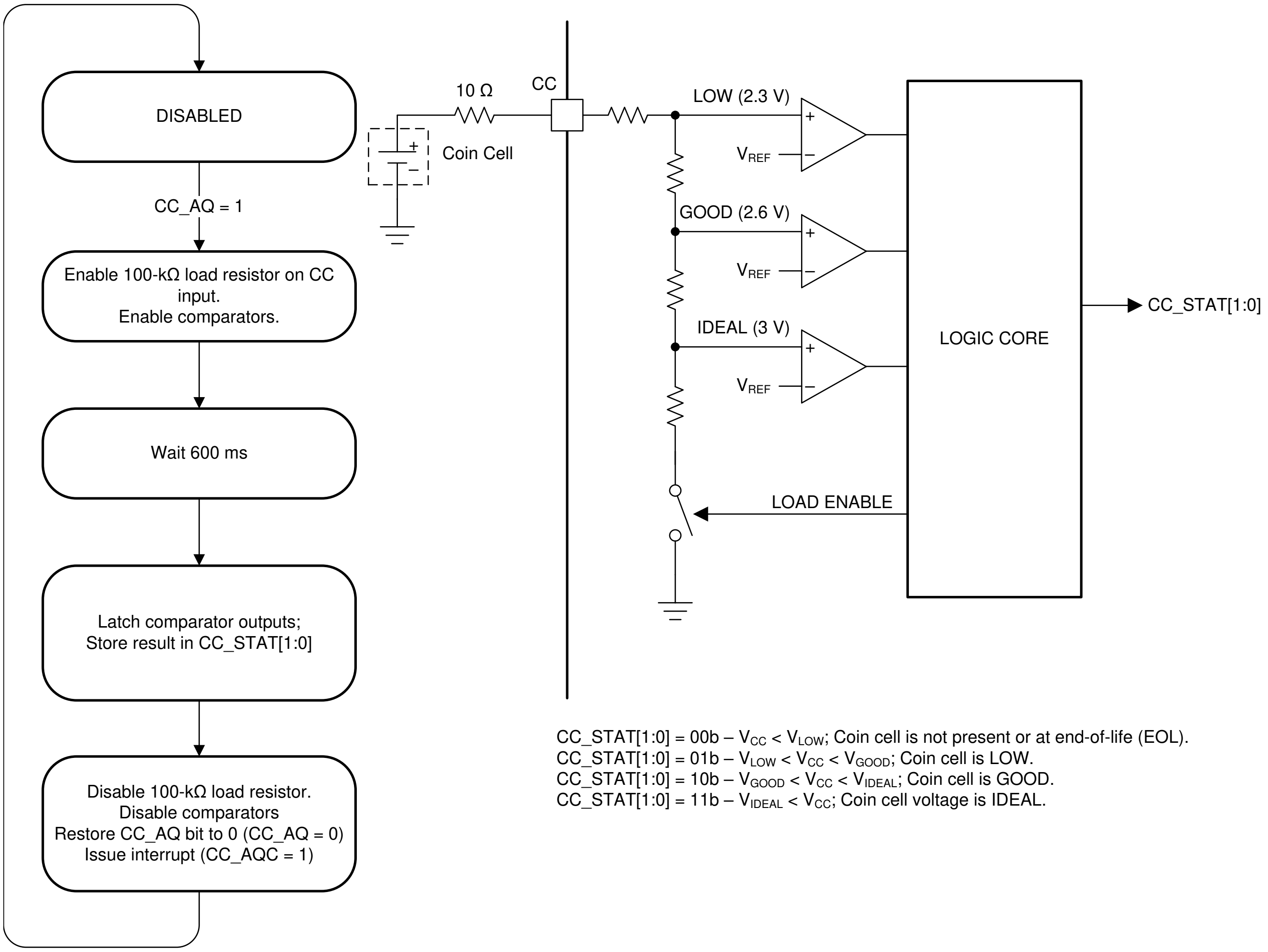


图 7-12. Typical Application of Load Switch 3

7.3.1.8 LDO1

LDO1 is a general-purpose LDO intended to provide power to analog circuitry on the SOC. LDO1 has an input voltage range from 1.8 V to 5.5 V, and can be connected either directly to the system power or the output of a DCDC converter. The output voltage is programmable in the range of 0.9 V to 3.4 V with a default of 1.8 V. LDO1 supports up to 200 mA at the minimum specified headroom voltage, and up to 400 mA at the typical operating condition of V_{OUT} = 1.8 V, V_{IN_LDO1} > 2.7 V.

7.3.1.9 Coin Cell Battery Voltage Acquisition



CC_STAT[1:0] = 00b – $V_{CC} < V_{LOW}$; Coin cell is not present or at end-of-life (EOL).
CC_STAT[1:0] = 01b – $V_{LOW} < V_{CC} < V_{GOOD}$; Coin cell is LOW.
CC_STAT[1:0] = 10b – $V_{GOOD} < V_{CC} < V_{IDEAL}$; Coin cell is GOOD.
CC_STAT[1:0] = 11b – $V_{IDEAL} < V_{CC}$; Coin cell voltage is IDEAL.

图 7-13. Left: Flow Chart for Acquiring Coin Cell Battery Voltage Right: Comparator Circuit

7.3.1.10 UVLO

Depending on the slew rate of the input voltage into the IN_BIAS pin, the power rails of TPS65218 will be enabled at either V_{ULVO} or $V_{ULVO} + V_{HYS}$.

If the slew rate of the IN_BIAS voltage is greater than 30 V/s, then TPS65218 will power up at V_{ULVO}. Once the input voltage rises above this level, the input voltage may drop to the V_{UVLO} level before the PMIC shuts down. In this scenario, if the input voltage were to fall below V_{UVLO} but above 2.55 V, the input voltage would have to recover above V_{UVLO} in less than 5 ms for the device to remain active.

If the slew rate of the IN_BIAS voltage is less than 30 V/s, then TPS65218 will power up at $V_{ULVO} + V_{HYS}$. Once the input voltage rises above this level, the input voltage may drop to the V_{UVLO} level before the PMIC shuts down. In this scenario, if the input voltage were to fall below V_{UVLO} but above 2.5 V, the input voltage would have to recover above $V_{UVLO} + V_{HYS}$ in less than 5 ms for the device to remain active.

In either slew rate scenario, if the input voltage were to fall below 2.5 V, the digital core is reset and all remaining power rails are shut down instantaneously and are pulled low to ground by their internal discharge circuitry (DCDC1-4 and LDO1).

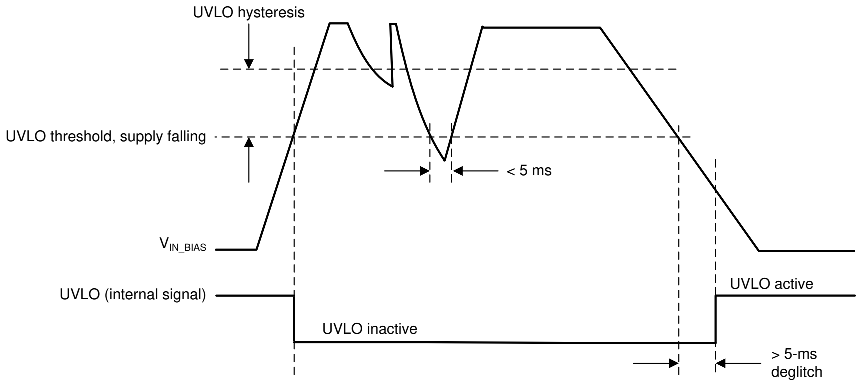


图 7-14. Definition of UVLO and Hysteresis, IN_BIAS Slew Rate > 30 V/s

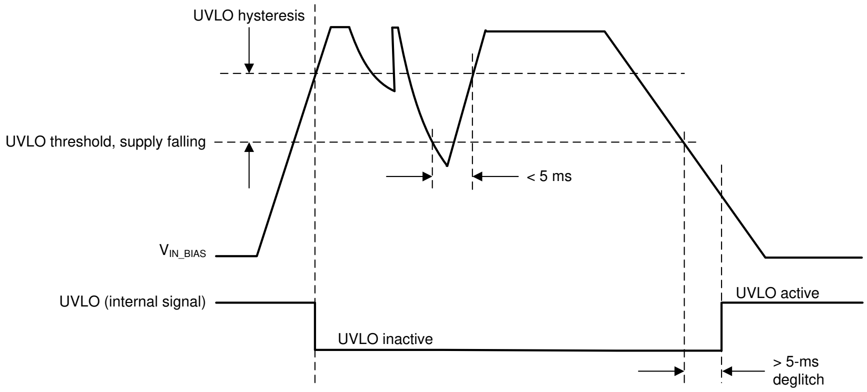


图 7-15. Definition of UVLO and Hysteresis, IN_BIAS Slew Rate < 30 V/s

After the UVLO triggers, the internal LDO blocks current flow from its output capacitor back to the IN_BIAS pin, allowing the digital core and the discharge circuits to remain powered for a limited amount of time to properly shut-down and discharge the output rails. The hold-up time is determined by the value of the capacitor connected to INT_LDO. See 节 7.3.1.6 for more details.

7.3.1.11 Power-Fail Comparator

The power-fail comparator notifies the system host if the system supply voltage drops and the system is at risk of shutting down. The comparator has an internal 800-mV threshold and the trip-point is adjusted by an external resistor divider.

By default, the power-fail comparator has no impact on any of the power rails or load switches. Load switches are configured individually, to be disabled when the PFI comparator trips to shed system load and extend hold-up time as described in 节 7.3.1.7. The power-fail comparator also triggers the power-down sequencer, such that all or selective rails power-down when the system voltage fails. To tie the power-fail comparator into the power-down sequence, the OFFnPFO bit in the CONTROL register must be set to 1.

The power-fail comparator cannot be monitored by software, such that no interrupt or status bit is associated to this function.

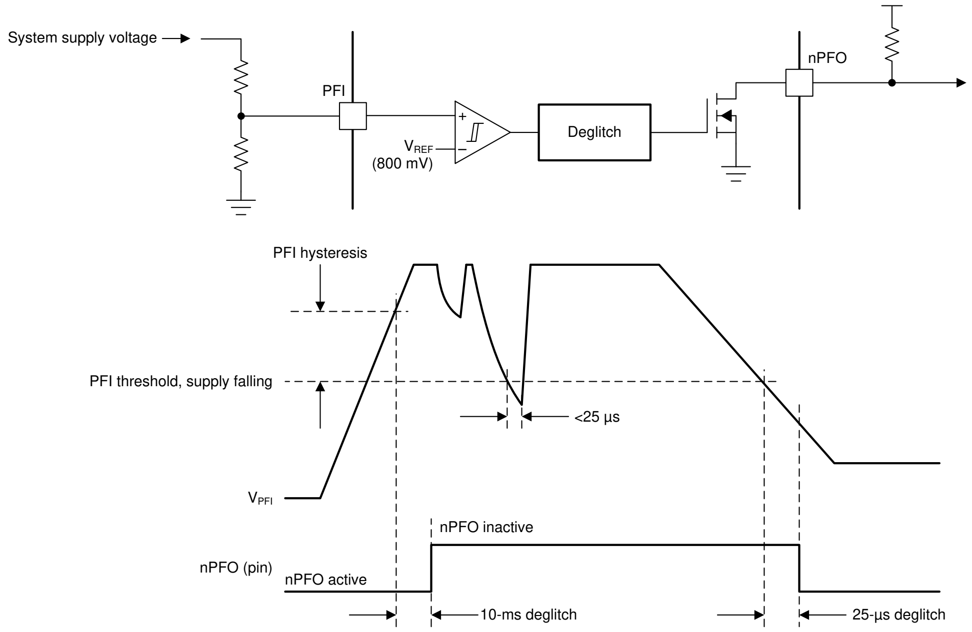


图 7-16. Power-Fail Comparator Simplified Circuit and Timing Diagram

7.3.1.12 Battery-Backup Supply Power-Path

DCDC5 and DCDC6 are supplied from either the CC (coin-cell battery) input or IN_BU (main system supply). The power-path is designed to prioritize IN_BU to maximize coin-cell battery life. Whenever the PMIC is powered-up (WAIT_PWR_EN, ACTIVE, SUSPEND, and RECOVERY state), the power-path is forced to select the IN_BU input. In OFF mode the power-path selects the higher of the two inputs with a built-in hysteresis of 150 mV as shown in 图 7-17.

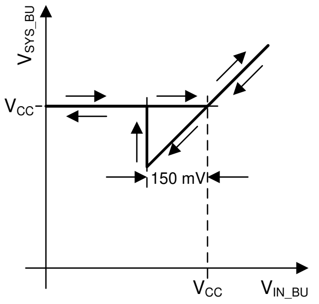
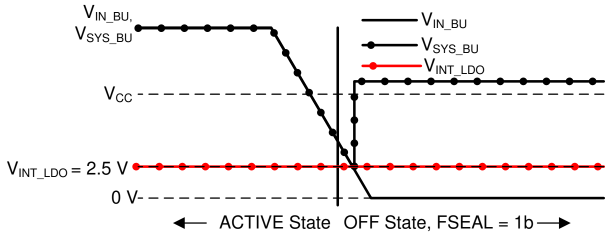
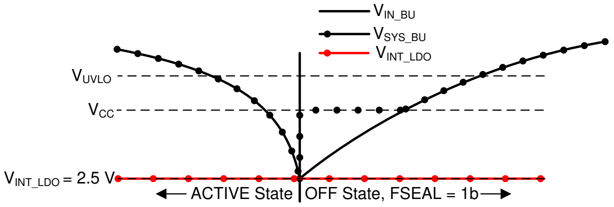


图 7-17. Switching Behavior of the Battery-Backup-Supply Power-Path; Power-Path Hysteresis



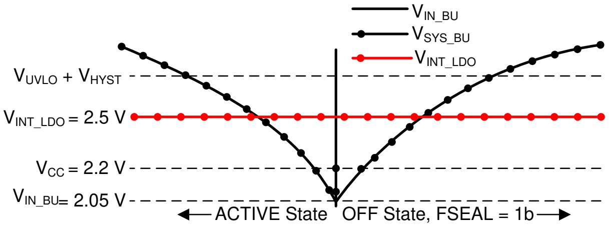
A. Main Supply is disconnected or decays rapidly.
B. Rapid decay of VIN_BIAS (preregulator)

图 7-18. Switching Behavior of the Battery-Backup-Supply Power-Path; Main Power Supply Removal



A. System is supplied by Li-Ion battery with a fresh coin-cell backup battery.
B. (VIN_BIAS slow decay)

图 7-19. Switching Behavior of the Battery-Backup-Supply Power-Path; Weakening Main Battery, Strong Coin-Cell



A. System is supplied by Li-Ion battery with a weak coin-cell backup battery.
B. VIN_BIAS slow decay

图 7-20. Switching Behavior of the Battery-Backup-Supply Power-Path; Weakening Main Battery, Weak Coin-Cell

When V_{IN_BIAS} drops below the UVLO threshold, the PMIC shuts down all rails and enters OFF mode. At this point the power-path selects the higher of the two input supplies. If the coin-cell battery is less than 150 mV above the UVLO threshold, SYS_BU remains connected to IN_BU (see 图 7-19). If the coin-cell is >150 mV above the UVLO threshold, the power-path switches to the CC input as shown in 图 7-20. With no load on the main supply, the input voltage may recover over time to a value greater than the coin-cell voltage and the power-path switches back to IN_BU. This is a typical behavior in a Li-Ion battery powered system.

Depending on the system load, V_{IN_BIAS} may drop below V_{INT_LDO} before the power-down sequence is completed. In that case, INT_LDO is turned OFF and the digital core is reset forcing the unit into OFF mode and the power-path switches to IN_BU as shown in 图 7-18.

7.3.1.13 DCDC3 and DCDC4 Power-Up Default Selection

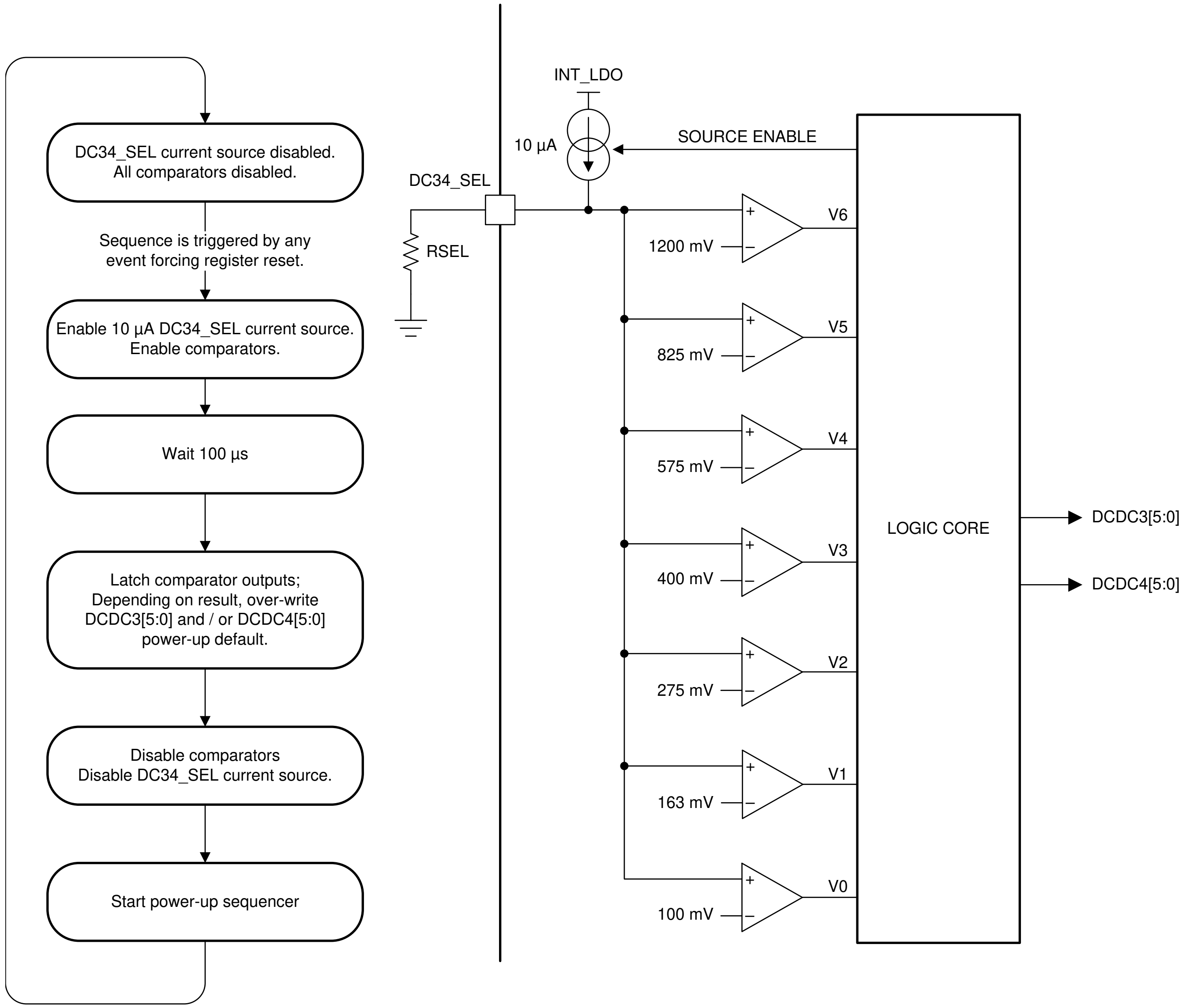


图 7-21. Left: Flow Chart for Selecting DCDC Power-Up Default Voltage Right: Comparator Circuit

表 7-2. Power-Up Default Values of DCDC3 and DCDC4

RSEL [KΩ]			POWER-UP DEFAULT	
MIN	TYP	MAX	DCDC3[5:0]	DCDC4[5:0]
0	0	7.7	Programmed default (1.2 V)	Programmed default (3.3 V)
11.3	12.1	13	0x12 (1.35 V)	Programmed default (3.3 V)
18.1	20	22	0x18 (1.5 V)	Programmed default (3.3 V)
30.9	31.6	32.3	0x1F (1.8 V)	Programmed default (3.3 V)
44.8	45.3	46.4	0x3D (3.3 V)	0x01 (1.2 V)
64.2	64.9		Programmed default (1.2 V)	0x07 (1.35 V)
92.9	95.3	96.9	Programmed default (1.2 V)	0x0D (1.5 V)
135.3	150	Tied to INT_LDO	Programmed default (1.2 V)	0x14 (1.8 V)

7.3.1.14 I/O Configuration

The device has two GPIOs and one GPO pin, which are configured as follows:

- GPIO1:
  - General-purpose, open-drain output is controlled by the GPO1 user bit or sequencer.
  - DDR3 reset input signal from SOC. The signal is either latched or passed-through to the GPO2 pin. See 表 7-3 for details.
- GPO2:
  - General-purpose output is controlled by the GPO2 user bit.
  - DDR3 reset output signal. Signal is controlled by GPIO1 and PGOOD. See 表 7-4 for details.
  - Output buffer is configured as open-drain or push-pull.
- GPIO3:
  - General-purpose, open-drain output id controlled by the GPO3 user bit or sequencer.
  - Reset input-signal for DCDC1 and DCDC2.

表 7-3. GPIO1 Configuration

IO1_SEL (EEPROM)	GPO1 (USER BIT)	PGOOD (PMIC SIGNAL)	GPIO1 (I/O PIN)	COMMENTS
0	0	X	0	Open-drain output, driving low
0	1	X	HiZ	Open-drain output, HiZ
1	X	0	X	Pin is configured as input and intended as DDR RESET signal. Coming out of POR, GPO2 is driven low. Otherwise, GPO2 status is latched at falling edge of PGOOD. See 图 7-24.
1	X	1	0	Pin is configured as input and intended as DDR RESET signal. GPO2 is driven low.
1	X	1	1	Pin is configured as input and intended as DDR RESET signal. GPO2 is driven high.

表 7-4. GPO2 Configuration

IO1_SEL (EEPROM)	GPO2_BUF (EEPROM)	GPO2 (USER BIT)	COMMENTS
0	0	0	GPO2 is open drain output controlled by GPO2 user bit (driving low).
0	0	1	GPO2 is open drain output controlled by GPO2 user bit (HiZ).
0	1	0	GPO2 is push-pull output controlled by GPO2 user bit (driving low).
0	1	1	GPO2 is push-pull output controlled by GPO2 user bit (driving high).
1	0	X	GPO2 is open drain output controlled by GPIO1 and PGOOD.
1	1	X	GPO2 is push-pull output controlled by GPIO1 and PGOOD.

表 7-5. GPIO3 Configuration

DC12_RST (EEPROM)	GPO3 (USER BIT)	GPIO3 (I/O PIN)	COMMENTS
0	0	0	Open-drain output, driving low
0	1	HiZ	Open-drain output, HiZ
1	X	Active low	GPIO3 is DCDC1 and DCDC2 reset input signal to PMIC (active low). See *节 7.3.1.14.2* for details.

7.3.1.14.1 Configuring GPO2 as Open-Drain Output

GPO2 may be configured as open-drain or push-pull output. The supply for the push-pull driver is internally connected to the IN_LS1 input pin, whereas an external pull-up resistor and supply are required in the open-drain configuration. Because of the internal connection to IN_LS1, the external pull-up supply must not exceed the voltage on the IN_LS1 pin, otherwise leakage current may be observed from GPO2 to IN_LS1 as shown in 图 7-22.

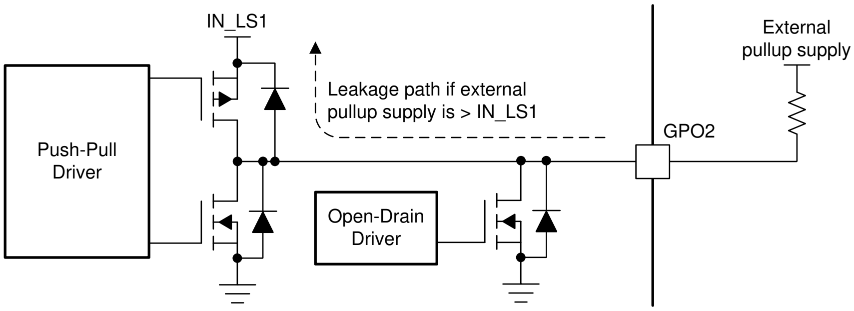


图 7-22. GPO2 as Open-Drain Output

Note

When configured as open-drain output, the external pull-up supply must not exceed the voltage level on IN_LS1 pin.

7.3.1.14.2 Using GPIO3 as Reset Signal to DCDC1 and DCDC2

The GPIO3 is an edge-sensitive reset input to the PMIC, when the DC12_RST bit set to 1. The reset signal affects DCDC1 and DCDC2 only, so that only those two registers are reset to the power-up default whenever GPIO3 input transitions from high to low, while all other registers maintain their current values. DCDC1 and DCDC2 transition back to the default value following the SLEW settings, and are not power cycled. This function recovers the processor from reset events while in low-power mode.

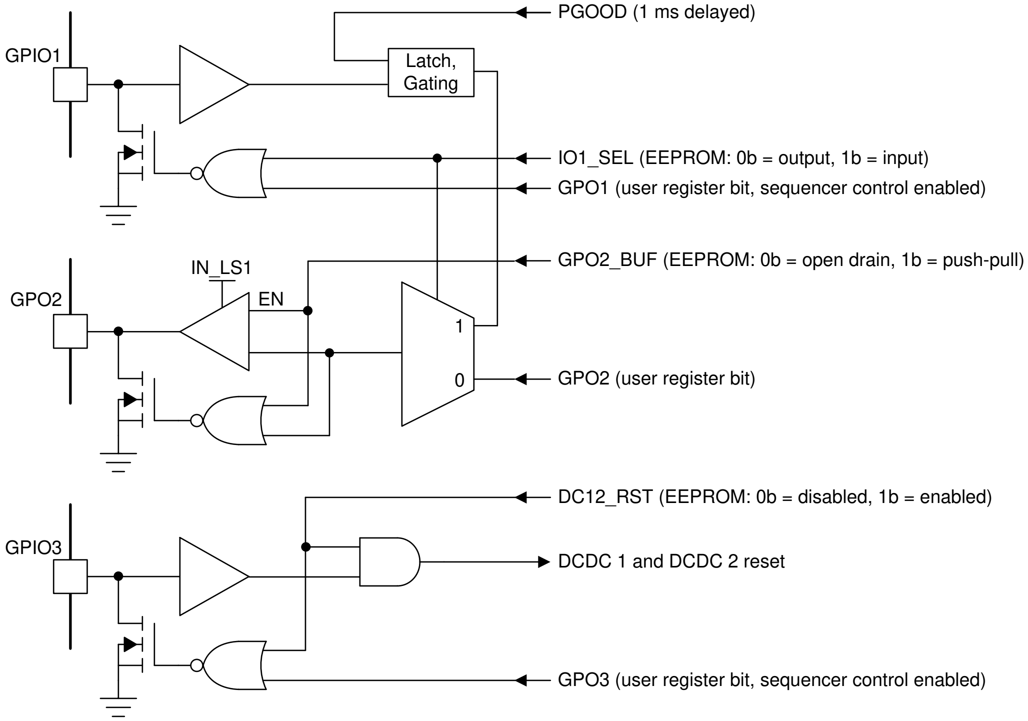


图 7-23. I/O Pin Logic

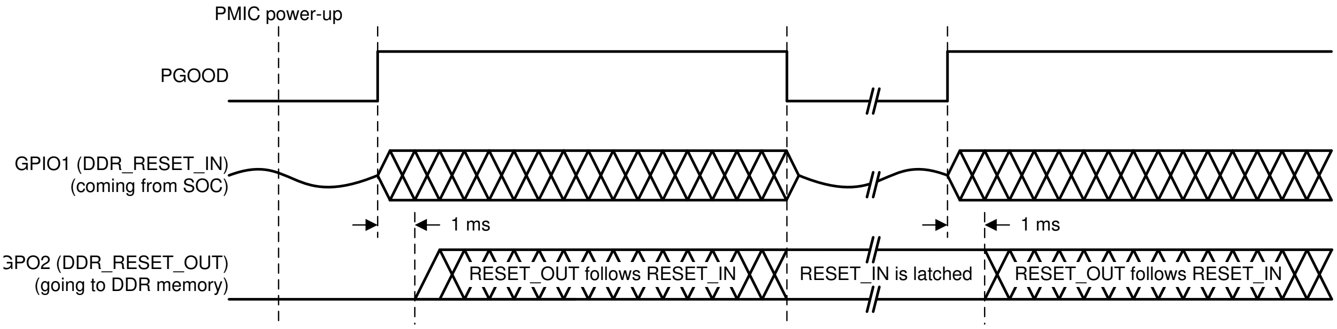


图 7-24. DDR3 Reset Timing Diagram

Note

GPIO must be configured as input (IO1_SEL = 1b). GPO2 is automatically configured as output.

7.3.1.15 Push Button Input (PB)

The PB pin is a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor. The power-up sequence is triggered if the PB input is held low for 600 ms.

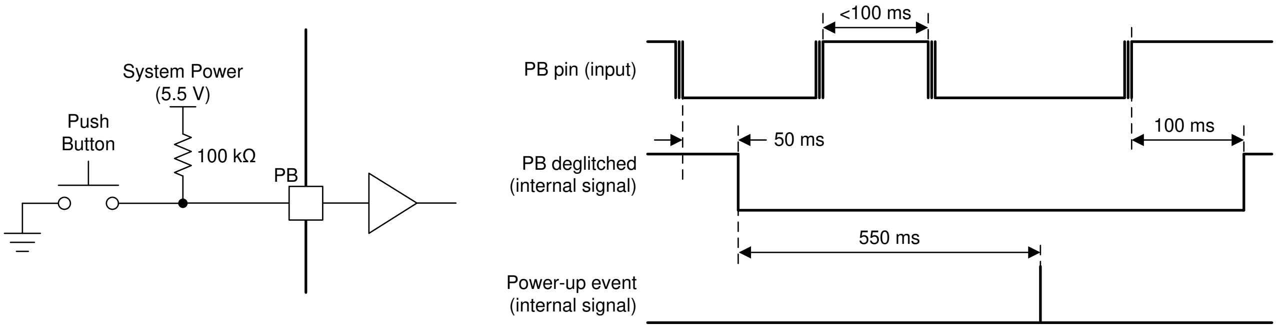
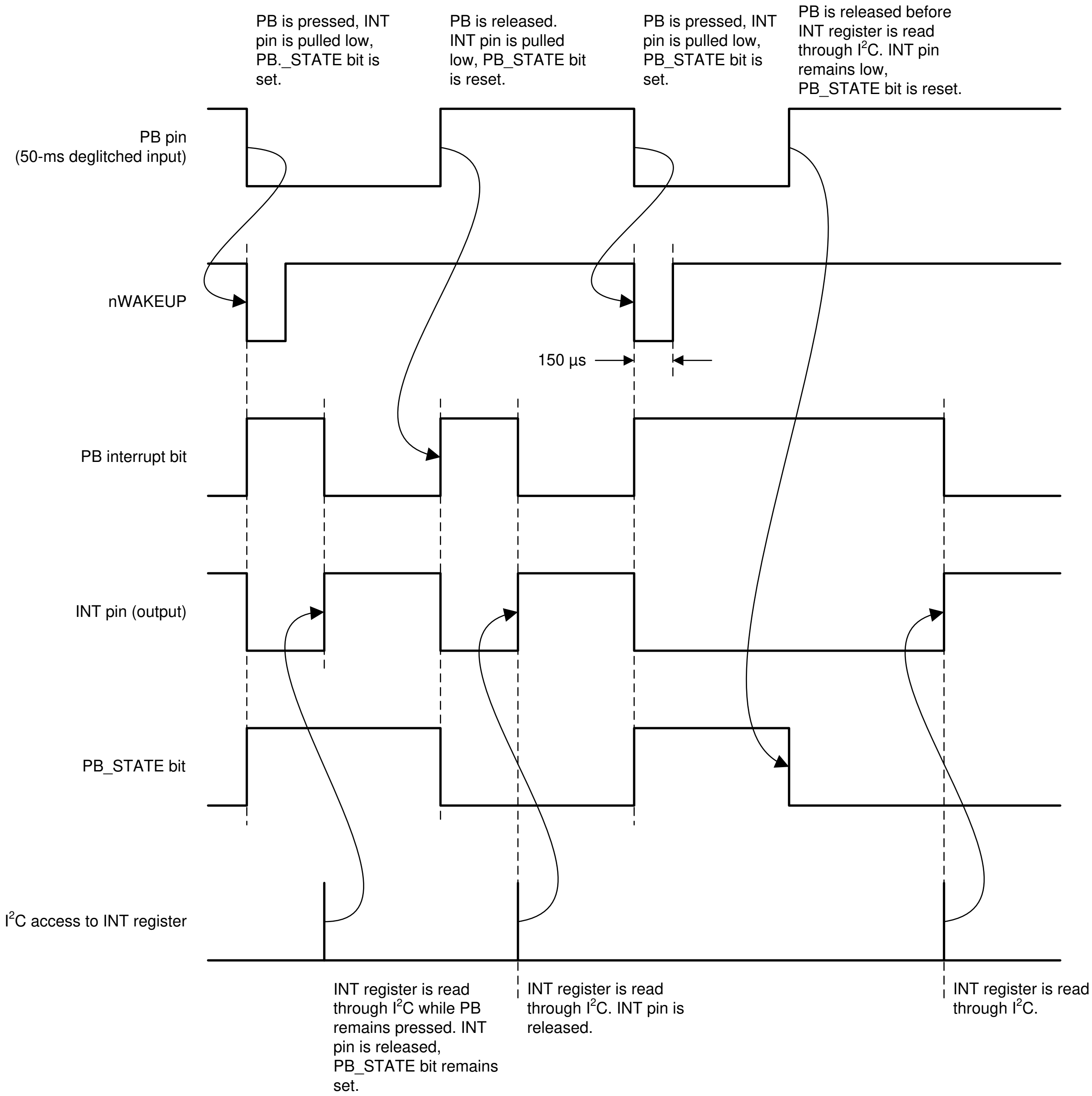


图 7-25. Left: Typical PB Input Circuit Right: Push-Button Input (PB) Deglitch and Power-Up Timing

In ACTIVE mode, the TPS65218 monitors the PB input and issues an interrupt when the pin status changes, such as when it drops below or rises above the PB input-low or input-high thresholds. The interrupt is masked by the PBM bit in the INT_MASK1 register.



PB is pressed, INT pin is pulled low, PB._STATE bit is set.

PB is released. INT pin is pulled low, PB_STATE bit is reset.

PB is pressed, INT pin is pulled low, PB_STATE bit is set.

PB is released before INT register is read through I^2C. INT pin remains low, PB_STATE bit is reset.

INT register is read through I^2C while PB remains pressed. INT pin is released, PB_STATE bit remains set.

INT register is read through I^2C. INT pin is released.

INT register is read through I^2C.

图 7-26. PB Input-Low or Input-High Thresholds

Note

Interrupts are issued whenever the PB pin status changes. The PB_STATE bit reflects the current status of the PB input. nWAKEUP is pulled low for 150 µs on every falling edge of PB.

7.3.1.15.1 Signaling PB-Low Event on the nWAKEUP Pin

In ACTIVE state, the nWAKEUP pin is pulled low for five 32-kHz clock cycles (approximately 150 μs) whenever a falling edge on the PB input is detected. This allows the host processor to wakeup from DEEP SLEEP mode of operation. It is recommended to pull-up the nWAKEUP pin to DCDC6 output through a 1-MΩ resistor .

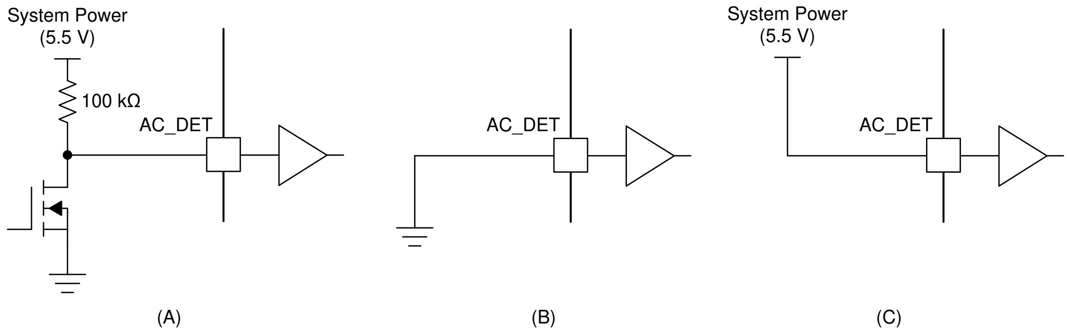
7.3.1.15.2 Push Button Reset

If the PB input is pulled low for 8 s (15 s if TRST = 1b) or longer, then all rails except for DCDC5 and DCDC6 are disabled, and the device enters the RECOVERY state. The device powers up automatically after the 500 ms power-down sequence is complete, regardless of the state of the PB input. Holding the PB pin low for 8 s (15 s if TRST = 1b), only turns off the device temporarily and forces a system restart, and is not a power-down function. If the PB is held low continuously, the device power-cycles in 8-s and 15-s intervals.

7.3.1.16 AC_DET Input (AC_DET)

The AC_DET pin is a CMOS-type input used in three different ways to control the power-up of the PMIC:

- In a battery operated system, AC_DET is typically connected to an external battery charger with an open-drain power-good output pulled low when a valid charger supply is connected to the system. A falling edge on the AC_DET pin causes the PMIC to power up.
- In a non-portable system, the AC_DET pin may be shorted to ground and the device powers up whenever system power is applied to the chip.
- If none of the above behaviors are desired, AC_DET may be tied to system power (IN_BIAS). Power-up is then controlled through the push-button input or PWR_EN input.



A. Portable Systems
B. Non-portable Systems
C. Disabled

图 7-27. AC_DET Pin Configurations

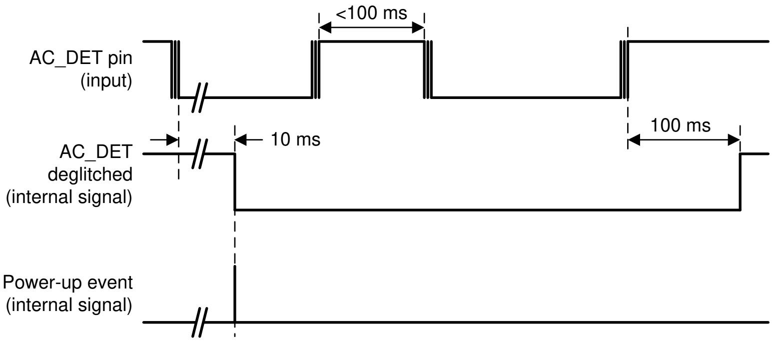


图 7-28. AC_DET Input Deglitch and Power-Up Timing (Portable Systems)

In ACTIVE state, the TPS65218 monitors the AC_DET input and issues an interrupt when the pin status changes, such as when it drops below or rises above the AC_DET input-low or input-high thresholds. The interrupt is masked by the ACM bit in the INT_MASK1 register.

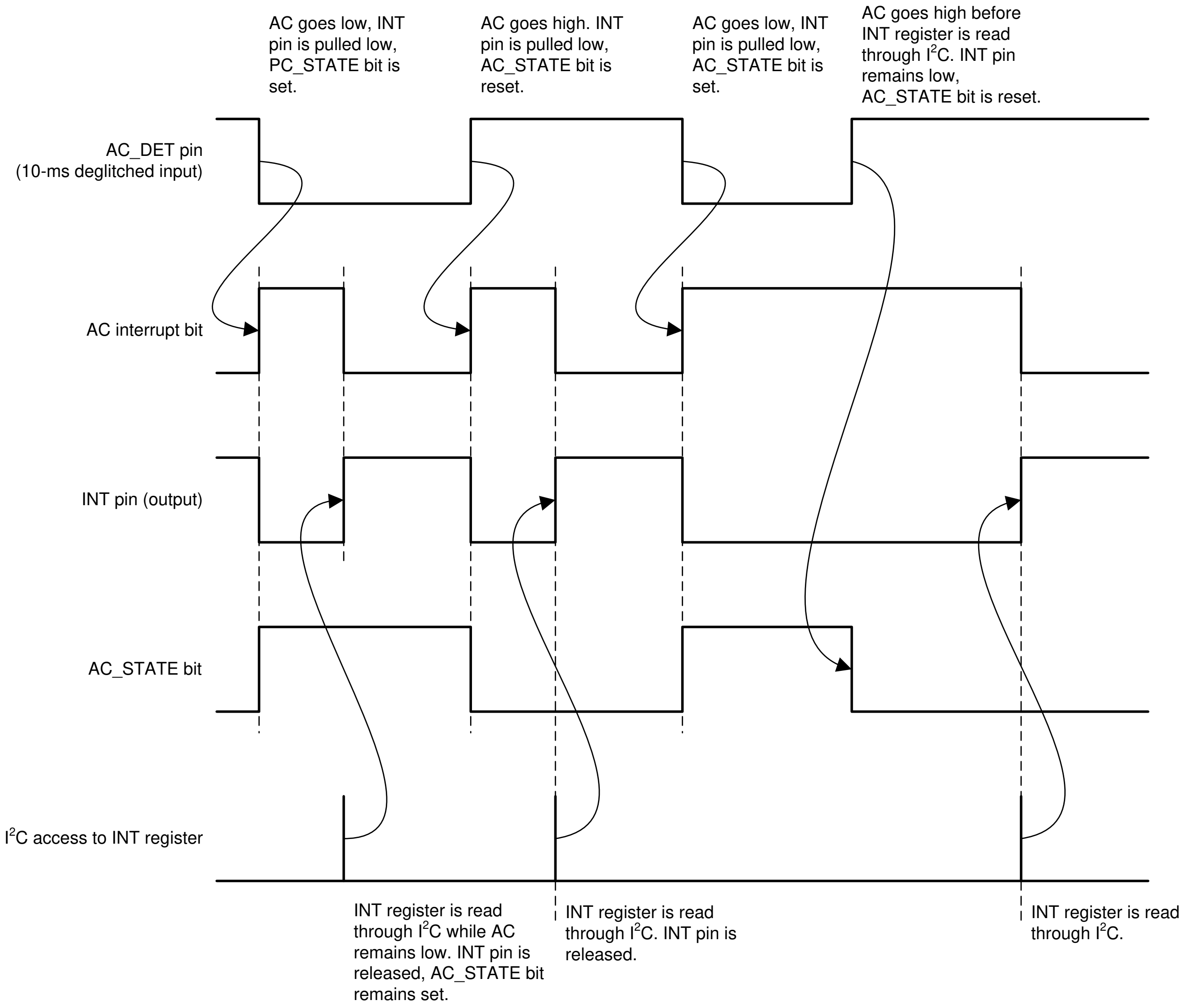


图 7-29. AC_STATE Pin

Note

Interrupts are issued whenever the AC_DET pin status changes. The AC_STATE bit reflects the current status of the AC_DET input.

7.3.1.17 Interrupt Pin (INT)

The interrupt pin signals any event or fault condition to the host processor. Whenever a fault or event occurs in the device, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INT pin is released (returns to Hi-Z state) and fault bits are cleared when the host reads the INT register. If a failure persists, the corresponding INT bit remains set and the INT pin is pulled low again after a maximum of 32 µs.

The MASK register masks events from generating interrupts. The MASK settings affect the INT pin only, and have no impact on the protection and monitor circuits.

7.3.1.18 I²C Bus Operation

The TPS65218 hosts a slave I²C interface (address 0x24) that supports data rates up to 400 kbps, auto-increment addressing. [1]

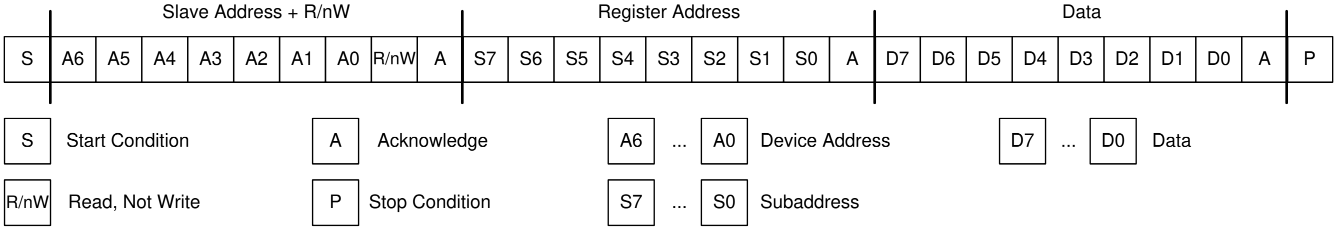
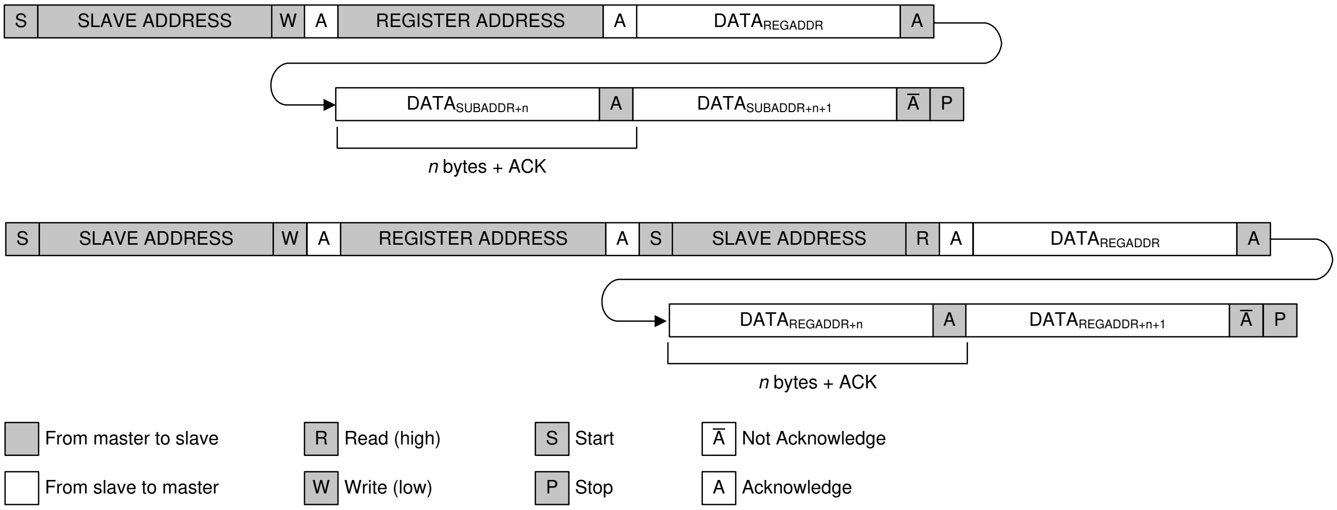


图 7-30. Subaddress in I²C Transmission

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission initiates with a start bit from the controller as shown in 图 7-32. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and checks for valid address and control information. If the appropriate slave address is set for the device, the device issues an acknowledge pulse and prepares to receive register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge issues after the reception of valid slave address, register-address, and data words. The I²C interfaces an auto-sequence through the register addresses, so that multiple data words can be sent for a given I²C transmission. Reference I²C Data Protocol and 图 7-32 for details.



Top: Master Writes Data to Slave
Bottom: Master Reads Data from Slave

图 7-31. I²C Data Protocol

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[1] Note: The SCL duty cycle at 400 kHz must be >40%.

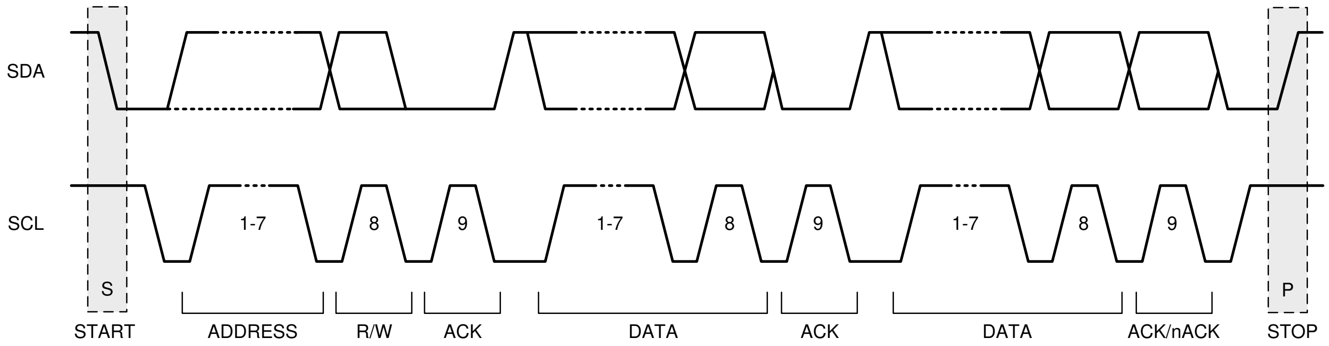


图 7-32. I^{2}C Protocol and Transmission Timing I^{2}C Start Stop and Acknowledge Protocol

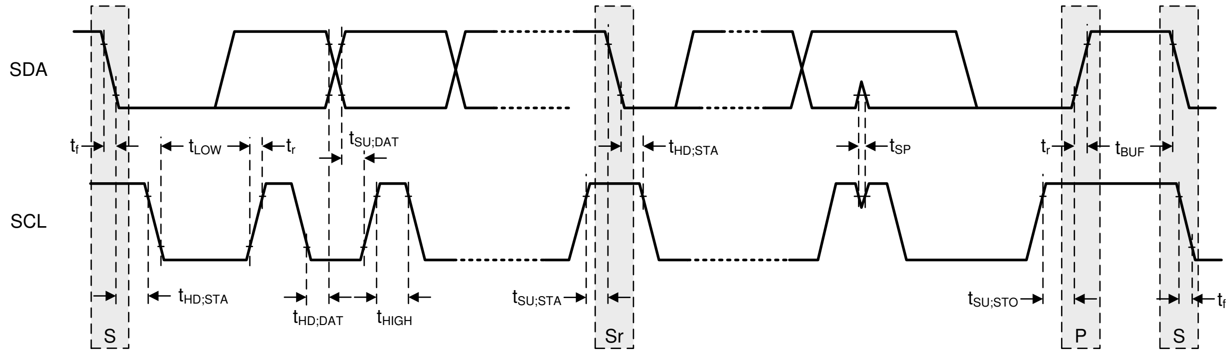
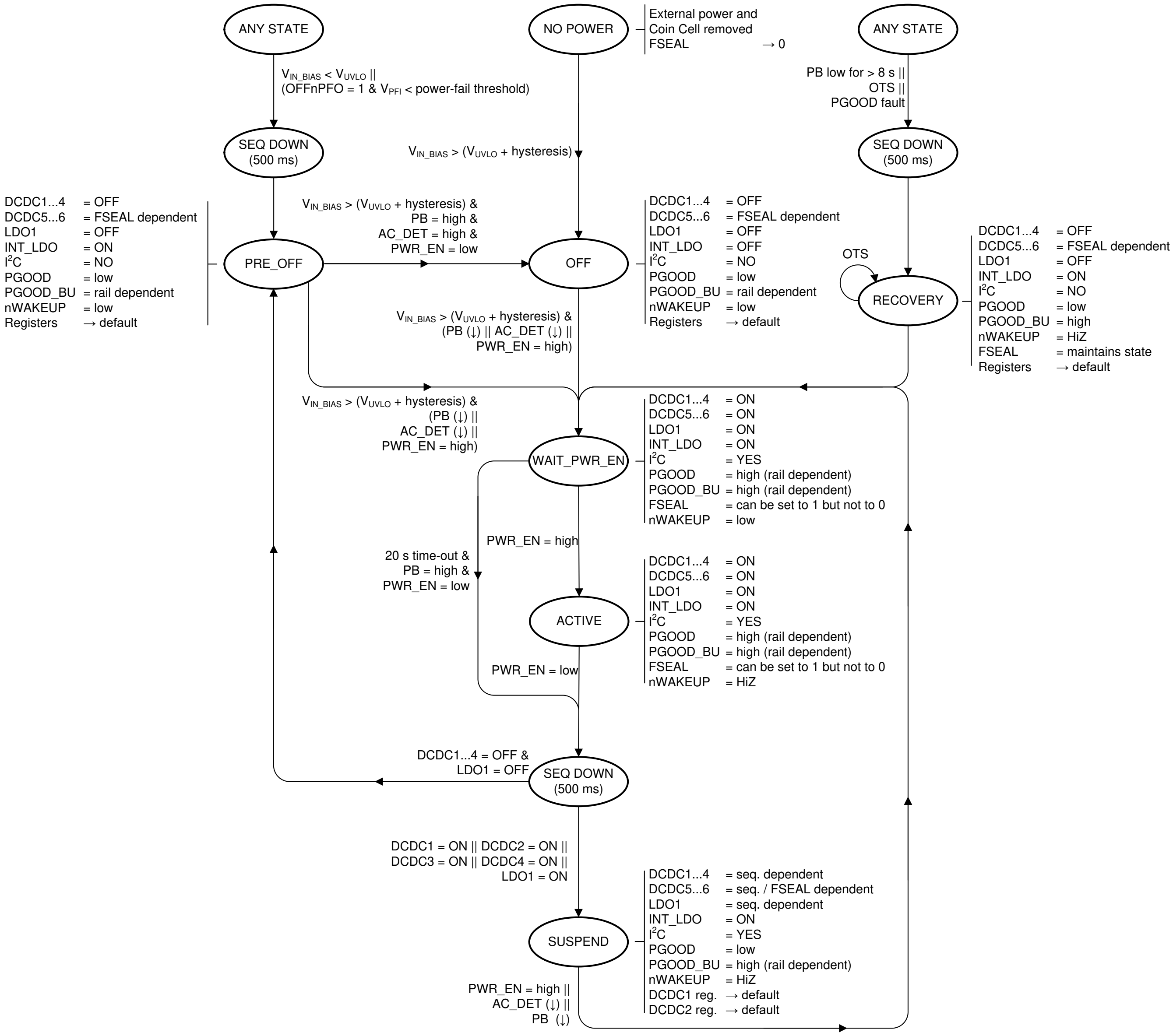


图 7-33. I^{2}C Protocol and Transmission Timing I^{2}C Data Transmission Timing

7.4 Device Functional Modes

7.4.1 Modes of Operation



PB (↓) has 50 ms debounce.

AC_DET (↓) has 10 ms debounce.

(↓) = denotes falling edge of signal.

图 7-34. Modes of Operation Diagram

7.4.2 OFF

In OFF mode, the PMIC is completely shut down with the exception of a few circuits to monitor the AC_DET, PWR_EN, and PB input. All power rails are turned off and the registers are reset to their default values. The I^2C communication interface is turned off. This is the lowest-power mode of operation. To exit OFF mode V_{IN_BIAS} must exceed the UVLO threshold and one of the following wake-up events must occur:

- The PB input is pulled low.
- THE AC_DET input is pulled low.
- The PWR_EN input is pulled high.

To enter the OFF state, ensure that all power rails are assigned to the sequencer, then pull the PWR_EN pin low. Additionally, if the OFFnPFO bit is set to 1b and the PFI input falls below the power fail threshold the device transitions to the OFF state. If the freshness seal is broken, DCDC5 and DCDC6 remains on in the OFF state. If a PGOOD or OTS fault occurs while in the ACTIVE state, TPS65218 will transition to the RESET state.

7.4.3 ACTIVE

This is the typical mode of operation when the system is up and running. All DCDC converters, LDOs, and load switches are operational and can be controlled through the I^2C interface. After a wake-up event, the PMIC enables all rails controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device only enters the ACTIVE state if the host asserts the PWR_EN pin within 20 s after the wake-up event. Otherwise it will enter the OFF state. The nWAKEUP pin returns to HiZ mode after the PWR_EN pin is asserted. The ACTIVE state can also be directly entered from the SUSPEND state by pulling the PWR_EN pin high. See the SUSPEND state description for details. To exit the ACTIVE mode, the PWR_EN pin must be pulled low.

7.4.4 SUSPEND

The SUSPEND state is a low-power mode of operation intended to support system standby. Typically all power rails are turned off with the exception of any rail with an SEQ register set to 0h. DCDC5 and DCDC6 also remain enabled if the freshness seal is broken. To enter the SUSPEND state, pull the PWR_EN pin low. All power rails controlled by the power-down sequencer are shut down, and after 500 ms the device enters the SUSPEND state. All rails not controlled by the power-down sequencer will maintain its state. Note: all register values are reset as the device enters the SUSPEND state. The device enters the ACTIVE state after it detects a wake-up event as described in the previous sections.

7.4.5 RESET

The TPS65218 can be reset by holding the PB pin low for more than 8 or 15 s, depending on the value of the TRST bit. All rails are shut down by the sequencer and all register values reset to their default values. Rails not controlled by the sequencer are shut down additionally. Note: the RESET function power-cycles the device and only temporarily shuts down the output rails. Resetting the device does not lead to an OFF state. If the PB_IN pin is kept low for an extended amount of time, the device continues to cycle between the ACTIVE and RESET state, entering the RESET every 8 or 15 s.

The device is also reset if a PGOOD or OTS fault occurs. The TPS65218 remains in the RECOVERY state until the fault is removed, at which time it transitions back to the ACTIVE state.

7.5 Register Maps

7.5.1 Password Protection

Registers 0x11 through 0x26 are protected against accidental write by a 8-bit password. The password must be written prior to writing to a protected register and automatically resets to 0x00 after the next I^2C transaction, regardless of the register accessed or transaction type (read or write). The password is required for write access only and is not required for read access.

To write to a protected register:

1. Write the address of the destination register, XORed with the protection password (0x7D), to the PASSWORD register (0x10).
2. Write the data to the password protected register.
3. If the content of the PASSWORD register is XORed, with an address send that matches 0x7D, then the data transfers to the protected register. Otherwise, the transaction is ignored. In either case the PASSWORD register resets to 0x00 after the transaction.

The cycle must be repeated for any other register that is Level1 write protected.

7.5.2 Freshness Seal (FSEAL) Bit

The FSEAL (freshness seal) bit prevents accidental shut-down of the always-on supplies, DCDC5 and DCDC6. The FSEAL bit exists in a default state of 0b, and can be set to 1b and reset to 0b once for factory testing. The second time the bit is set to 1b, it remains 1b and cannot reset again under software control. Coin-cell battery and main supply must be disconnected from the device to reset the FSEAL bit again. With the FSEAL bit set to 1b, DCDC5 and DCDC6 are forced ON regardless of the state of the DC5_EN and DC6_EN bit, and the rails do not turn off when the device enters the OFF state.

A consecutive write of [0xB1, 0xFE, and 0xA3] to the password register sets the FSEAL bit to 1b. The three bytes must be written consecutively for the sequence to be valid. No other read or write transactions are allowed between the three bytes, or the sequence is invalid. After a valid sequence, the FSEAL bit in the STATUS register reflects the new setting.

After setting the FSEAL bit, the device can enter the OFF state or any other mode of operation without affecting the state of the FSEAL bit, provided the coin-cell supply remains connected to the chip.

A second write of [0xB1, 0xFE, and 0xA3] to the password register resets the FSEAL bit to 0b. The three bytes must be written consecutively for the sequence to be valid.

A third write of [0xB1, 0xFE, and 0xA3] to the password register sets the FSEAL bit to 1b and locks it into this state for as long as the coin-cell supply (CC) remains connected to the device.

7.5.3 FLAG Register

The FLAG register contains a bit for each power rail and GPO to keep track of the enable state of the rails while the system is suspended. The following rules apply to the FLAG register:

- The power-up default value for any flag bit is 0.
- Flag bits are read-only and cannot be written to.
- Upon entering a SUSPEND state, the flag bits are set to same value as their corresponding ENABLE bits. Rails and GPOs enabled in a SUSPEND state have flag bits set to 1, while all other flag bits are set to 0. Flag bits are not updated while in the SUSPEND state or when exiting the SUSPEND state.
- The FLAG register is static in WAIT_PWR_EN and ACTIVE state. The FLAG register reflects the enable state of DCDC1, DCDC2, DCDC3, DCDC4, and LDO1; and, reflects the enable state of GPO1, GPO2, and GPO3 during the last SUSPEND state.

The host processor reads the FLAG register to determine if the system powered up from the OFF or SUSPEND state. In the SUSPEND state, typically the DDR memory is kept in self refresh mode and therefore the DC3_FLG or DC4_FLG bits are set.

7.5.4 TPS65218 Registers

表 7-6 lists the memory-mapped registers for the TPS65218. All register offset addresses not listed in 表 7-6 should be considered as reserved locations and the register contents should not be modified.

表 7-6. TPS65218 Registers

SUBADDRESS	ACRONYM	REGISTER NAME	R/W	PASSWORD PROTECTED	SECTION
0x00	CHIPID	CHIP ID	R	No	节 7.5.5
0x01	INT1	INTERRUPT 1	R	No	节 7.5.6
0x02	INT2	INTERRUPT 2	R	No	节 7.5.7
0x03	INT_MASK1	INTERRUPT MASK 1	R/W	No	节 7.5.8
0x04	INT_MASK2	INTERRUPT MASK 2	R/W	No	节 7.5.9
0x05	STATUS	STATUS	R	No	节 7.5.10
0x06	CONTROL	CONTROL	R/W	No	节 7.5.11
0x07	FLAG	FLAG	R	No	节 7.5.12
0x10	PASSWORD	PASSWORD	R/W	No	节 7.5.13
0x11	ENABLE1	ENABLE 1	R/W	Yes	节 7.5.14
0x12	ENABLE2	ENABLE 2	R/W	Yes	节 7.5.15
0x13	CONFIG1	CONFIGURATION 1	R/W	Yes	节 7.5.16
0x14	CONFIG2	CONFIGURATION 2	R/W	Yes	节 7.5.17
0x15	CONFIG3	CONFIGURATION 3	R/W	Yes	节 7.5.18
0x16	DCDC1	DCDC1 CONTROL	R/W	Yes	节 7.5.19
0x17	DCDC2	DCDC2 CONTROL	R/W	Yes	节 7.5.20
0x18	DCDC3	DCDC3 CONTROL	R/W	Yes	节 7.5.21
0x19	DCDC4	DCDC4 CONTROL	R/W	Yes	节 7.5.22
0x1A	SLEW	SLEW RATE CONTROL	R/W	Yes	节 7.5.23
0x1B	LDO1	LDO1 CONTROL	R/W	Yes	节 7.5.24
0x20	SEQ1	SEQUENCER 1	R/W	Yes	节 7.5.25
0x21	SEQ2	SEQUENCER 2	R/W	Yes	节 7.5.26
0x22	SEQ3	SEQUENCER 3	R/W	Yes	节 7.5.27
0x23	SEQ4	SEQUENCER 4	R/W	Yes	节 7.5.28
0x24	SEQ5	SEQUENCER 5	R/W	Yes	节 7.5.29
0x25	SEQ6	SEQUENCER 6	R/W	Yes	节 7.5.30
0x26	SEQ7	SEQUENCER 7	R/W	Yes	节 7.5.31

表 7-7 explains the common abbreviations used in this section.

表 7-7. Common Abbreviations

Abbreviation	Description
R	Read
W	Write
R/W	Read and write capable
h	Hexadecimal notation of a group of bits
b	Hexadecimal notation of a bit or group of bits
X	Do not care reset value

7.5.5 CHIPID Register (subaddress = 0x00) [reset = 0x03]

CHIPID is shown in 图 7-30 and described in 表 7-8.

Return to 表 7-6.

图 7-30. CHIPID Register

7	6	5	4	3	2	1	0
CHIP					REV		
R-0h					R-3h		

表 7-8. CHIPID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	CHIP	R	0h	Chip ID: 0h = TPS65218 1h = Future use 2h = TPS6521815 3h = Future use 4h = TPS6521825 5h = Future use 6h = TPS6521835 7h = Future use 8h = TPS6521845 ... 1Fh = Future use
2-0	REV	R	3h	Revision code: 0h = Revision 1.0 1h = Revision 1.1 2h = Revision 2.0 3h = Revision 2.1 4h = Revision 3.0 5h = Revision 4.0 (D0) 6h = Future use 7h = Future use

7.5.6 INT1 Register (subaddress = 0x01) [reset = 0x00]

INT1 is shown in 图 7-31 and described in 表 7-9.

Return to 表 7-6.

图 7-31. INT1 Register

7	6	5	4	3	2	1	0
RESERVED		VPRG	AC	PB	HOT	CC_AQC	PRGC
R-00b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-9. INT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	VPRG	R	0b	Programming voltage interrupt: 0b = No significance. 1b = Input voltage is too low for programming power-up default values.

表 7-9. INT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	AC	R	0b	AC_DET pin status change interrupt. Note: Status information is available in STATUS register. 0b = No change in status. 1b = AC_DET status change (AC_DET pin changed high to low or low to high).
3	PB	R	0b	Push-button status change interrupt. Note: Status information is available in STATUS register 0b = No change in status. 1b = Push-button status change (PB changed high to low or low to high).
2	HOT	R	0b	Thermal shutdown early warning: 0b = Chip temperature is below HOT threshold. 1b = Chip temperature exceeds HOT threshold.
1	CC_AQC	R	0b	Coin cell battery voltage acquisition complete interrupt: 0b = No significance. 1b = Backup battery status comparators have settled and results are available in STATUS register.
0	PRGC	R	0b	EEPROM programming complete interrupt: 0b = No significance. 1b = Programming of power-up default settings has completed successfully.

7.5.7 INT2 Register (subaddress = 0x02) [reset = 0x00]

INT2 is shown in 图 7-32 and described in 表 7-10.

Return to 表 7-6.

图 7-32. INT2 Register

7	6	5	4	3	2	1	0
RESERVED		LS3_F	LS2_F	LS1_F	LS3_I	LS2_I	LS1_I
R-00b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-10. INT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LS3_F	R	0b	Load switch 3 fault interrupt: 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit and is temporarily disabled.
4	LS2_F	R	0b	Load switch 2 fault interrupt: 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit or input voltage dropped below minimum value. Switch is temporarily disabled.
3	LS1_F	R	0b	Load switch 1 fault interrupt: 0b = No fault. Switch is working normally. 1b = Load switch exceeded operating temperature limit and is temporarily disabled.

表 7-10. INT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LS3_I	R	0b	Load switch 3 current-limit interrupt: 0b = Load switch is disabled or not in current limit. 1b = Load switch is actively limiting the output current (output load is exceeding current limit value).
1	LS2_I	R	0b	Load switch 2 current-limit interrupt: 0b = Load switch is disabled or not in current limit. 1b = Load switch is actively limiting the output current (output load is exceeding current limit value).
0	LS1_I	R	0b	Load switch 1 current-limit interrupt: 0b = Load switch is disabled or not in current limit. 1b = Load switch is actively limiting the output current (output load is exceeding current limit value).

7.5.8 INT_MASK1 Register (subaddress = 0x03) [reset = 0x00]

INT_MASK1 is shown in 图 7-33 and described in 表 7-11.

Return to 表 7-6.

图 7-33. INT_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED		VPRGM	ACM	PBM	HOTM	CC_AQCM	PRGCM
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-11. INT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	VPRGM	R/W	0b	Programming voltage interrupt mask bit. Note: mask bit has no effect on monitoring function: 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
4	ACM	R/W	0b	AC_DET interrupt masking bit: 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin). Note: mask bit has no effect on monitoring function.
3	PBM	R/W	0b	PB interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
2	HOTM	R/W	0b	HOT interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
1	CC_AQCM	R/W	0b	C_AQC interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).

表 7-11. INT_MASK1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PRGCM	R/W	0b	PRGC interrupt masking bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).

7.5.9 INT_MASK2 Register (subaddress = 0x04) [reset = 0x00]

INT_MASK2 is shown in 图 7-34 and described in 表 7-12.

Return to 表 7-6.

图 7-34. INT_MASK2 Register

7	6	5	4	3	2	1	0
RESERVED		LS3_FM	LS2_FM	LS1_FM	LS3_IM	LS2_IM	LS1_IM
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-12. INT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LS3_FM	R/W	0b	LS3 fault interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
4	LS2_FM	R/W	0b	LS2 fault interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
3	LS1_FM	R/W	0b	LS1 fault interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
2	LS3_IM	R/W	0b	LS3 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
1	LS2_IM	R/W	0b	LS2 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).
0	LS1_IM	R/W	0b	LS1 current-limit interrupt mask bit. Note: mask bit has no effect on monitoring function. 0b = Interrupt is unmasked (interrupt event pulls nINT pin low). 1b = Interrupt is masked (interrupt has no effect on nINT pin).

7.5.10 STATUS Register (subaddress = 0x05) [reset = 00XXXXXXb]

Register mask: C0h

STATUS is shown in 图 7-35 and is described in 表 7-13.

Return to 表 7-6.

图 7-35. STATUS Register

7	6	5	4	3	2	1	0
FSEAL	EE	AC_STATE	PB_STATE	STATE		CC_STAT	
R-0b	R-0b	R-X	R-X	R-X		R-X	

表 7-13. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FSEAL	R	0b	Freshness seal (FSEAL) status. Note: See 节 7.5.2 for details. 0b = FSEAL is in native state (fresh). 1b = FSEAL is broken.
6	EE	R	0b	EEPROM status: 0b = EEPROM values have not been changed from factory default setting. 1b = EEPROM values have been changed from factory default settings.
5	AC_STATE	R	X	AC_DET input status bit: 0b = AC_DET input is inactive (AC_DET input pin is high). 1b = AC_DET input is active (AC_DET input is low).
4	PB_STATE	R	X	PB input status bit: 0b = Push Button input is inactive (PB input pin is high). 1b = Push Button input is active (PB input pin is low).
3-2	STATE	R	X	State machine STATE indication: 0h = PMIC is in transitional state. 1h = PMIC is in WAIT_PWR_EN state. 2h = PMIC is in ACTIVE state. 3h = PMIC is in SUSPEND state.
1-0	CC_STAT	R	X	Coin cell state of charge. Note: Coin-cell voltage acquisition must be triggered first before status bits are valid. See CC_AQ bit in 节 7.5.11 . 0h = $V_{CC} < V_{LOW\_LEVEL}$; Coin cell is not present or approaching end-of-life (EOL). 1h = $V_{LOW\_LEVEL} < V_{CC} < V_{GOOD\_LEVEL}$; Coin cell voltage is LOW. 2h = $V_{GOOD\_LEVEL} < V_{CC} < V_{IDEAL\_LEVEL}$; Coin cell voltage is GOOD. 3h = $V_{IDEAL} < V_{CC}$; Coin cell voltage is IDEAL.

7.5.11 CONTROL Register (subaddress = 0x06) [reset = 0x00]

CONTROL is shown in 图 7-36 and described in 表 7-14.

Return to 表 7-6.

图 7-36. CONTROL Register

7	6	5	4	3	2	1	0
RESERVED						OFFnPFO	CC_AQ
R-0000 00b						R/W-0b	R/W-0b

表 7-14. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0000 00b	

表 7-14. CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OFFnPFO	R/W	0b	Power-fail shutdown bit: 0b = nPFO has no effect on PMIC state. 1b = All rails are shut down and PMIC enters OFF state when PFI comparator trips (nPFO is low).
0	CC_AQ	R/W	0b	Coin Cell battery voltage acquisition start bit: 0b = No significance 1b = Triggers voltage acquisition. Bit is automatically reset to 0.

7.5.12 FLAG Register (subaddress = 0x07) [reset = 0x00]

FLAG is shown in 图 7-37 and described in 表 7-15.

Return to 表 7-6.

图 7-37. FLAG Register

7	6	5	4	3	2	1	0
GPO3_FLG	GPO2_FLG	GPO1_FLG	LDO1_FLG	DC4_FLG	DC3_FLG	DC2_FLG	DC1_FLG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-15. FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO3_FLG	R	0b	GPO3 Flag bit: 0b = Device powered up from OFF or SUSPEND state and GPO3 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO3 was enabled while in SUSPEND.
6	GPO2_FLG	R	0b	GPO2 Flag bit 0b = Device powered up from OFF or SUSPEND state and GPO2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO2 was enabled while in SUSPEND.
5	GPO1_FLG	R	0b	GPO1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and GPO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GPO1 was enabled while in SUSPEND.
4	LDO1_FLG	R	0b	LDO1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and LDO1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and LDO1 was enabled while in SUSPEND.
3	DC4_FLG	R	0b	DCDC4 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC4 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC4 was enabled while in SUSPEND.

表 7-15. FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DC3_FLG	R	0b	DCDC3 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC3 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC3 was enabled while in SUSPEND.
1	DC2_FLG	R	0b	DCDC2 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC2 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and DCDC2 was enabled while in SUSPEND.
0	DC1_FLG	R	0b	DCDC1 Flag bit: 0b = Device powered up from OFF or SUSPEND state and DCDC1 was disabled while in SUSPEND. 1b = Device powered up from SUSPEND state and GDCDC1PO3 was enabled while in SUSPEND.

7.5.13 PASSWORD Register (subaddress = 0x10) [reset = 0x00]

PASSWORD is shown in 图 7-38 and described in 表 7-16.

Return to 表 7-6.

图 7-38. PASSWORD Register

7	6	5	4	3	2	1	0
PWRD							
R/W-00h							

表 7-16. PASSWORD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWRD	R/W	00h	Register is used for accessing password protected registers (see 节 7.5.1 for details). Breaking the freshness seal (see 节 7.5.2 for details). Programming power-up default values . Read-back always yields 0x00.

7.5.14 ENABLE1 Register (subaddress = 0x11) [reset = 0x00]

ENABLE1 is shown in 图 7-39 and described in 表 7-17.

Return to 表 7-6.

Password protected.

图 7-39. ENABLE1 Register

7	6	5	4	3	2	1	0
RESERVED		DC6_EN	DC5_EN	DC4_EN	DC3_EN	DC2_EN	DC1_EN
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-17. ENABLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	DC6_EN	R/W	0b	DCDC6 enable bit. DCDC6 can only be disabled if FSEAL = 0. See 节 7.5.2 for details. 0b = Disabled 1b = Enabled
4	DC5_EN	R/W	0b	DCDC5 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. DCDC5 can only be disabled if FSEAL = 0. See 节 7.5.2 for details. 0b = Disabled 1b = Enabled
3	DC4_EN	R/W	0b	DCDC4 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
2	DC3_EN	R/W	0b	DCDC3 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
1	DC2_EN	R/W	0b	DCDC2 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled
0	DC1_EN	R/W	0b	DCDC1 enable bit. Note: At power-up and down this bit is automatically updated by the internal power sequencer. 0b = Disabled 1b = Enabled

7.5.15 ENABLE2 Register (subaddress = 0x12) [reset = 0x00]

ENABLE2 is shown in 图 7-40 and described in 表 7-18.

Return to 表 7-6.

Password protected.

图 7-40. ENABLE2 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO3	GPIO2	GPIO1	LS3_EN	LS2_EN	LS1_EN	LDO1_EN

图 7-40. ENABLE2 Register (continued)

R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-18. ENABLE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	
6	GPIO3	R/W	0b	General purpose output 3 / reset polarity. Note: If DC12_RST bit (register 0x14) is set to 1 this bit has no function. 0b = GPIO3 output is driven low. 1b = GPIO3 output is HiZ.
5	GPIO2	R/W	0b	General purpose output 2. Note: If IO_SEL bit (register 0x13) is set to 1 this bit has no function. 0b = GPO2 output is driven low. 1b = GPO2 output is HiZ.
4	GPIO1	R/W	0b	General purpose output 1. Note: If IO_SEL bit (register 0x13) is set to 1 this bit has no function. 0b = GPO1 output is driven low. 1b = GPO1 output is HiZ.
3	LS3_EN	R/W	0b	Load switch 3 (LS3) enable bit. 0b = Disabled 1b = Enabled
2	LS2_EN	R/W	0b	Load switch 2 (LS2) enable bit. 0b = Disabled 1b = Enabled
1	LS1_EN	R/W	0b	Load switch 1 (LS1) enable bit. 0b = Disabled 1b = Enabled Note: At power-up and down this bit is automatically updated by the internal power sequencer.
0	LDO1_EN	R/W	0b	LDO1 enable bit. 0b = Disabled 1b = Enabled Note: At power-up and down this bit is automatically updated by the internal power sequencer.

7.5.16 CONFIG1 Register (subaddress = 0x13) [reset = 0x048]

CONFIG1 is shown in 图 7-41 and described in 表 7-19.

Return to 表 7-6.

Password protected.

图 7-41. CONFIG1 Register

7	6	5	4	3	2	1	0
TRST	GPO2_BUF	IO1_SEL	PGDLY		STRICT	UVLO	
R/W-0b	R/W-1b	R/W-0b	R/W-01b		R/W-0b	R/W-00b	

表 7-19. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRST	R/W	0b	Push-button reset time constant: 0b = 8 s 1b = 15 s
6	GPO2_BUF	R/W	1b	GPO2 output buffer configuration: 0b = GPO2 buffer is configured as open-drain. 1b = GPO2 buffer is configured as push-pull (high-level is driven to IN_LS1).
5	IO1_SEL	R/W	0b	GPIO1 / GPO2 configuration bit. See 节 7.3.1.14 for details. 0b = GPIO1 is configured as general-purpose, open-drain output. GPO2 is independent output. 1b = GPIO1 is configured as input, controlling GPO2. Intended for DDR3 reset signal control.
4-3	PGDLY	R/W	01b	Power-Good delay. Note: Power-good delay applies to rising-edge only (power-up), not falling edge (power-down or fault). 00b = 10 ms 01b = 20 ms 10b = 50 ms 11b = 150 ms
2	STRICT	R/W	0b	Supply Voltage Supervisor Sensitivity selection. See 节 6.5 for details. 0b = Power-good threshold (VOUT falling) has wider limits. Over-voltage is not monitored. 1b = Power-good threshold (VOUT falling) has tight limits. Over-voltage is monitored.
1-0	UVLO	R/W	00b	UVLO setting 00b = 2.75 V 01b = 2.95 V 10b = 3.25 V 11b = 3.35 V

7.5.17 CONFIG2 Register (subaddress = 0x14) [TPS65218 reset = 0xC0; TPS65218B101 reset = 0x80]

CONFIG2 is shown in 图 7-42 and described in 表 7-20.

Return to 表 7-6.

Password protected.

图 7-42. CONFIG2 Register

7	6	5	4	3	2	1	0
DC12_RST	UVLOHYS	RESERVED		LS3ILIM		LS2ILIM	
R/W-1b	R/W-1b	R-00b		R/W-00b		R/W-00b	

表 7-20. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DC12_RST	R/W	1b	DCDC1 and DCDC2 reset-pin enable: 0b = GPIO3 is configured as general-purpose output. 1b = GPIO3 is configured as warm-reset input to DCDC1 and DCDC2.

表 7-20. CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	UVLOHYS	R/W	TPS65218: 1b TPS65218B101: 0b	UVLO hysteresis: 0b = 200 mV(1) 1b = 400 mV
5-4	RESERVED	R	00b	
3-2	LS3ILIM	R/W	00b	Load switch 3 (LS3) current limit selection: 00b = 100 mA, (MIN = 98 mA) 01b = 200 mA, (MIN = 194 mA) 10b = 500 mA, (MIN = 475 mA) 11b = 1000 mA, (MIN = 900 mA) See the LS3 current limit specification in 节 6.5 for more details.
1-0	LS2ILIM	R/W	00b	Load switch 2 (LS2) current limit selection: 00b = 100 mA, (MIN = 94 mA) 01b = 200 mA, (MIN = 188 mA) 10b = 500 mA, (MIN = 465 mA) 11b = 1000 mA, (MIN = 922 mA) See the LS2 current limit specification in 节 6.5 for more details.

(1) 200-mV hysteresis option is available for TPS65218B101

7.5.18 CONFIG3 Register (subaddress = 0x15) [reset = 0x0]

CONFIG3 is shown in 图 7-43 and described in 表 7-21.

Return to 表 7-6.

Password protected.

图 7-43. CONFIG3 Register

7	6	5	4	3	2	1	0
RESERVED		LS3nPFO	LS2nPFO	LS1nPFO	LS3DCHRG	LS2DCHRG	LS1DCHRG
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-21. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	
5	LS3nPFO	R/W	0b	Load switch 3 power-fail disable bit: 0b = Load switch status is not affected by power-fail comparator. 1b = Load switch is disabled if power-fail comparator trips (nPFO is low).
4	LS2nPFO	R/W	0b	Load switch 2 power-fail disable bit: 0b = Load switch status is not affected by power-fail comparator. 1b = Load switch is disabled if power-fail comparator trips (nPFO is low).
3	LS1nPFO	R/W	0b	Load switch 1 power-fail disable bit: 0b = Load switch status is not affected by power-fail comparator. 1b = Load switch is disabled if power-fail comparator trips (nPFO is low).
2	LS3DCHRG	R/W	0b	Load switch 3 discharge enable bit: 0b = Active discharge is disabled. 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF).
1	LS2DCHRG	R/W	0b	Load switch 2 discharge enable bit: 0b = Active discharge is disabled. 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF).
0	LS1DCHRG	R/W	0b	Load switch 1 discharge enable bit: 0b = Active discharge is disabled. 1b = Active discharge is enabled (load switch output is actively discharged when switch is OFF).

7.5.19 DCDC1 Register (offset = 0x16) [reset = 0x99]

DCDC1 is shown in 图 7-44 and described in 表 7-22.

Return to 表 7-6.

Note 1: This register is password protected. For more information, see 节 7.5.1 .
Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC1 register.
Note 3: To change the output voltage of DCDC1, the GO bit or the GODSBL bit must be set to 1b in register 0x1A.

图 7-44. DCDC1 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC1					
R/W-1b	R-0b	R/W-19h					

表 7-22. DCDC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	

表 7-22. DCDC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	DCDC1	R/W	19h	DCDC1 output voltage setting: 0h = 0.850 1h = 0.860 2h = 0.870 3h = 0.880 4h = 0.890 5h = 0.900 6h = 0.910 7h = 0.920 8h = 0.930 9h = 0.940 Ah = 0.950 Bh = 0.960 Ch = 0.970 Dh = 0.980 Eh = 0.990 Fh = 1.000 10h = 1.010 11h = 1.020 12h = 1.030 13h = 1.040 14h = 1.050 15h = 1.060 16h = 1.070 17h = 1.080 18h = 1.090 19h = 1.100 1Ah = 1.110 1Bh = 1.120 1Ch = 1.130 1Dh = 1.140 1Eh = 1.150 1Fh = 1.160 20h = 1.170 21h = 1.180 22h = 1.190 23h = 1.200

表 7-22. DCDC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				24h = 1.210 25h = 1.220 26h = 1.230 27h = 1.240 28h = 1.250 29h = 1.260 2Ah = 1.270 2Bh = 1.280 2Ch = 1.290 2Dh = 1.300 2Eh = 1.310 2Fh = 1.320 30h = 1.330 31h = 1.340 32h = 1.350 33h = 1.375 34h = 1.400 35h = 1.425 36h = 1.450 37h = 1.475 38h = 1.500 39h = 1.525 3Ah = 1.550 3Bh = 1.575 3Ch = 1.600 3Dh = 1.625 3Eh = 1.650 3Fh = 1.675

7.5.20 DCDC2 Register (subaddress = 0x17) [reset = 0x99]

DCDC2 is shown in 图 7-45 and described in 表 7-23.

Return to 表 7-6.

Note 1: This register is password protected. For more information, see 节 7.5.1 .
Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC2 register.
Note 3: To change the output voltage of DCDC2, the GO bit or the GODSBL bit must be set to 1b in register 0x1A.

图 7-45. DCDC2 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC2					
R/W-1b	R-0b	R/W-19h					

表 7-23. DCDC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse frequency modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	
5-0	DCDC2	R/W	19h	DCDC2 output voltage setting: 0h = 0.850 1h = 0.860 2h = 0.870 3h = 0.880 4h = 0.890 5h = 0.900 6h = 0.910 7h = 0.920 8h = 0.930 9h = 0.940 Ah = 0.950 Bh = 0.960 Ch = 0.970 Dh = 0.980 Eh = 0.990 Fh = 1.000 10h = 1.010 11h = 1.020 12h = 1.030 13h = 1.040 14h = 1.050 15h = 1.060 16h = 1.070 17h = 1.080 18h = 1.090 19h = 1.100 1Ah = 1.110 1Bh = 1.120 1Ch = 1.130 1Dh = 1.140 1Eh = 1.150 1Fh = 1.160 20h = 1.170 21h = 1.180 22h = 1.190 23h = 1.200

表 7-23. DCDC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				24h = 1.210 25h = 1.220 26h = 1.230 27h = 1.240 28h = 1.250 29h = 1.260 2Ah = 1.270 2Bh = 1.280 2Ch = 1.290 2Dh = 1.300 2Eh = 1.310 2Fh = 1.320 30h = 1.330 31h = 1.340 32h = 1.350 33h = 1.375 34h = 1.400 35h = 1.425 36h = 1.450 37h = 1.475 38h = 1.500 39h = 1.525 3Ah = 1.550 3Bh = 1.575 3Ch = 1.600 3Dh = 1.625 3Eh = 1.650 3Fh = 1.675

7.5.21 DCDC3 Register (subaddress = 0x18) [reset = 0x8C]

DCDC3 is shown in 图 7-46 and described in 表 7-24.

Return to 表 7-6.

Note 1: This register is password protected. For more information, see 节 7.5.1 .
Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC3 register.

Note

Power-up default may differ depending on RSEL value. See 节 7.3.1.13 for details.

图 7-46. DCDC3 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC3					
R/W-1b	R-0b	R/W-Ch					

表 7-24. DCDC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	
5-0	DCDC3	R/W	Ch	DCDC3 output voltage setting: 0h = 0.900 1h = 0.925 2h = 0.950 3h = 0.975 4h = 1.000 5h = 1.025 6h = 1.050 7h = 1.075 8h = 1.100 9h = 1.125 Ah = 1.150 Bh = 1.175 Ch = 1.200 Dh = 1.225 Eh = 1.250 Fh = 1.275 10h = 1.300 11h = 1.325 12h = 1.350 13h = 1.375 14h = 1.400 15h = 1.425 16h = 1.450 17h = 1.475 18h = 1.500 19h = 1.525 1Ah = 1.550 1Bh = 1.600 1Ch = 1.650 1Dh = 1.700 1Eh = 1.750 1Fh = 1.800 20h = 1.850 21h = 1.900 22h = 1.950 23h = 2.000

表 7-24. DCDC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				24h = 2.050 25h = 2.100 26h = 2.150 27h = 2.200 28h = 2.250 29h = 2.300 2Ah = 2.350 2Bh = 2.400 2Ch = 2.450 2Dh = 2.500 2Eh = 2.550 2Fh = 2.600 30h = 2.650 31h = 2.700 32h = 2.750 33h = 2.800 34h = 2.850 35h = 2.900 36h = 2.950 37h = 3.000 38h = 3.050 39h = 3.100 3Ah = 3.150 3Bh = 3.200 3Ch = 3.250 3Dh = 3.300 3Eh = 3.350 3Fh = 3.400

7.5.22 DCDC4 Register (subaddress = 0x19) [reset = 0xB2]

DCDC4 is shown in 图 7-47 and described in 表 7-25.

Return to 表 7-6.

Note 1: This register is password protected. For more information, see 节 7.5.1 .
Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the DCDC4 register.

Note

Power-up default may differ depending on RSEL value. See 节 7.3.1.13 for details. The Reserved setting should not be selected and the output voltage settings should not be modified while the converter is operating.

图 7-47. DCDC4 Register

7	6	5	4	3	2	1	0
PFM	RESERVED	DCDC4					
R/W-1b	R-0b	R/W-32h					

表 7-25. DCDC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PFM	R/W	1b	Pulse Frequency Modulation (PFM, also known as pulse-skip-mode) enable. PFM mode improves light-load efficiency. Actual PFM mode operation depends on load condition. 0b = Disabled (forced PWM) 1b = Enabled
6	RESERVED	R	0b	
5-0	DCDC4	R/W	32h	DCDC4 output voltage setting: 0h = 1.175 1h = 1.200 2h = 1.225 3h = 1.250 4h = 1.275 5h = 1.300 6h = 1.325 7h = 1.350 8h = 1.375 9h = 1.400 Ah = 1.425 Bh = 1.450 Ch = 1.475 Dh = 1.500 Eh = 1.525 Fh = 1.550 10h = 1.600 11h = 1.650 12h = 1.700 13h = 1.750 14h = 1.800 15h = 1.850 16h = 1.900 17h = 1.950 18h = 2.000 19h = 2.050 1Ah = 2.100 1Bh = 2.150 1Ch = 2.200 1Dh = 2.250 1Eh = 2.300 1Fh = 2.3500 20h = 2.400 21h = 2.450 22h = 2.500 23h = 2.550

表 7-25. DCDC4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				24h = 2.600 25h = 2.650 26h = 2.700 27h = 2.750 28h = 2.800 29h = 2.850 2Ah = 2.900 2Bh = 2.950 2Ch = 3.000 2Dh = 3.050 2Eh = 3.100 2Fh = 3.150 30h = 3.200 31h = 3.250 32h = 3.300 33h = 3.350 34h = 3.400 35h = reserved 36h = reserved 37h = reserved 38h = reserved 39h = reserved 3Ah = reserved 3Bh = reserved 3Ch = reserved 3Dh = reserved 3Eh = reserved 3Fh = reserved

7.5.23 SLEW Register (subaddress = 0x1A) [reset = 0x06]

SLEW is shown in 图 7-48 and described in 表 7-26.

Return to 表 7-6.

Note

Slew-rate control applies to DCDC1 and DCDC2 only. If changing from a higher voltage to lower voltage while STRICT = 1 and converters are in a no load state, PFM bit for DCDC1 and DCDC2 must be set to 0.

图 7-48. SLEW Register

7	6	5	4	3	2	1	0
GO	GODSBL	RESERVED			SLEW		
R/W-0b	R/W-0b	R-000b			R/W-6h		

表 7-26. SLEW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GO	R/W	0b	Go bit. Note: Bit is automatically reset at the end of the voltage transition. 0b = No change 1b = Initiates the transition from present state to the output voltage setting currently stored in DCDC1 and DCDC2 register. SLEW setting does apply.
6	GODSBL	R/W	0b	Go disable bit 0b = Enabled 1b = Disabled; DCDC1 and DCDC2 output voltage changes whenever set-point is updated in DCDC1 and DCDC2 register without having to write to the GO bit. SLEW setting does apply.
5-3	RESERVED	R	000b	
2-0	SLEW	R/W	6h	Output slew rate setting: 0h = 160 µs/step (0.0625 mV/µs at 10 mV per step) 1h = 80 µs/step (0.125 mV/µs at 10 mV per step) 2h = 40 µs/step (0.250 mV/µs at 10 mV per step) 3h = 20 µs/step (0.500 mV/µs at 10 mV per step) 4h = 10 µs/step (1.0 mV/µs at 10 mV per step) 5h = 5 µs/step (2.0 mV/µs at 10 mV per step) 6h = 2.5 µs/step (4.0 mV/µs at 10 mV per step) 7h = Immediate; slew rate is only limited by control loop response time. Note: The actual slew rate depends on the voltage step per code. Refer to DCDCx registers for details.

7.5.24 LDO1 Register (subaddress = 0x1B) [reset = 0x1F]

LDO1 is shown in 图 7-49 and described in 表 7-27.

Return to 表 7-6.

Note 1: This register is password protected. For more information, see 节 7.5.1 .
Note 2: A 5-ms blanking time of the over-voltage and under-voltage monitoring occurs when a write is performed on the LDO1 register.

图 7-49. LDO1 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">LDO1</td></tr>
<tr><td colspan="2">R-00b</td><td colspan="6">R/W-1Fh</td></tr>
</table>

表 7-27. LDO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	

表 7-27. LDO1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	LDO1	R/W	1Fh	LDO1 output voltage setting: 0h = 0.900 1h = 0.925 2h = 0.950 3h = 0.975 4h = 1.000 5h = 1.025 6h = 1.050 7h = 1.075 8h = 1.100 9h = 1.125 Ah = 1.150 Bh = 1.175 Ch = 1.200 Dh = 1.225 Eh = 1.250 Fh = 1.275 10h = 1.300 11h = 1.325 12h = 1.350 13h = 1.375 14h = 1.400 15h = 1.425 16h = 1.450 17h = 1.475 18h = 1.500 19h = 1.525

表 7-27. LDO1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				1Ah = 1.550 1Bh = 1.600 1Ch = 1.650 1Dh = 1.700 1Eh = 1.750 1Fh = 1.800 20h = 1.850 21h = 1.900 22h = 1.950 23h = 2.000 24h = 2.050 25h = 2.100 26h = 2.150 27h = 2.200 28h = 2.250 29h = 2.300 2Ah = 2.350 2Bh = 2.400 2Ch = 2.450 2Dh = 2.500 2Eh = 2.550 2Fh = 2.600 30h = 2.650 31h = 2.700 32h = 2.750 33h = 2.800 34h = 2.850 35h = 2.900 36h = 2.950 37h = 3.000 38h = 3.050 39h = 3.100 3Ah = 3.150 3Bh = 3.200 3Ch = 3.250 3Dh = 3.300 3Eh = 3.350 3Fh = 3.400

7.5.25 SEQ1 Register (subaddress = 0x20) [reset = 0x00]

SEQ1 is shown in 图 7-50 and described in 表 7-28.

Return to 表 7-6.

Password protected.

图 7-50. SEQ1 Register

7	6	5	4	3	2	1	0
DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-28. SEQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DLY8	R/W	0b	Delay8 (occurs after Strobe 8 and before Strobe 9.) 0b = 2 ms 1b = 5 ms
6	DLY7	R/W	0b	Delay7 (occurs after Strobe 7 and before Strobe 8.) 0b = 2 ms 1b = 5 ms
5	DLY6	R/W	0b	Delay6 (occurs after Strobe 6 and before Strobe 7.) 0b = 2 ms 1b = 5 ms
4	DLY5	R/W	0b	Delay5 (occurs after Strobe 5 and before Strobe 6.) 0b = 2 ms 1b = 5 ms
3	DLY4	R/W	0b	Delay4 (occurs after Strobe 4 and before Strobe 5.) 0b = 2 ms 1b = 5 ms
2	DLY3	R/W	0b	Delay3 (occurs after Strobe 3 and before Strobe 4.) 0b = 2 ms 1b = 5 ms
1	DLY2	R/W	0b	Delay2 (occurs after Strobe 2 and before Strobe 3.) 0b = 2 ms 1b = 5 ms
0	DLY1	R/W	0b	Delay1 (occurs after Strobe 1 and before Strobe 2.) 0b = 2 ms 1b = 5 ms

7.5.26 SEQ2 Register (subaddress = 0x21) [reset = 0x00]

SEQ2 is shown in 图 7-51 and described in 表 7-29.

Return to 表 7-6.

Password protected.

图 7-51. SEQ2 Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>DLYFCTR</td><td colspan="6">RESERVED</td><td>DLY9</td></tr>
<tr><td>R/W -0b</td><td colspan="6">R-000 000b</td><td>R/W -0b</td></tr>
</table>

表 7-29. SEQ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DLYFCTR	R/W	0b	Power-down delay factor: 0b = 1x 1b = 10x (delay times are multiplied by 10x during power-down.) Note: DLYFCTR has no effect on power-up timing.
6-1	RESERVED	R	000 000b	
0	DLY9	R/W	0b	Delay9 (occurs after Strobe 9 and before Strobe 10.) 0b = 2 ms 1b = 5 ms

7.5.27 SEQ3 Register (subaddress = 0x22)[reset = 0x98]

SEQ3 is shown in 图 7-52 and described in 表 7-30.

Return to 表 7-6.

Password protected.

图 7-52. SEQ3 Register

7	6	5	4	3	2	1	0
DC2_SEQ				DC1_SEQ			
R/W-9h				R/W-8h			

表 7-30. SEQ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DC2_SEQ	R/W	9h	DCDC2 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.
3-0	DC1_SEQ	R/W	8h	DCDC1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

7.5.28 SEQ4 Register (subaddress = 0x23) [reset = 0x75]

SEQ4 is shown in 图 7-53 and described in 表 7-31.

Return to 表 7-6.

Password protected.

图 7-53. SEQ4 Register

7	6	5	4	3	2	1	0
DC4_SEQ				DC3_SEQ			
R/W-7h				R/W-5h			

表 7-31. SEQ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DC4_SEQ	R/W	7h	DCDC4 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.
3-0	DC3_SEQ	R/W	5h	DCDC3 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

7.5.29 SEQ5 Register (subaddress = 0x24) [reset = 0x12]

SEQ5 is shown in 图 7-54 and described in 表 7-32.

Return to 表 7-6.

Password protected.

图 7-54. SEQ5 Register

7	6	5	4	3	2	1	0
RESERVED		DC6_SEQ		RESERVED		DC5_SEQ	

图 7-54. SEQ5 Register (continued)

R-0h	R/W-1h	R-0h	R/W-2h

表 7-32. SEQ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-4	DC6_SEQ	R/W	1h	DCDC6 enable STROBE. Note: STROBE 1 and STROBE 2 are executed only if FSEAL = 0. DCDC5 and 6 cannot be disabled by sequencer once freshness seal is broken. 0h = Rail is not controlled by sequencer. 1h = Enable at STROBE 1. 2h = Enable at STROBE 2. 3h = Rail is not controlled by sequencer.
3-2	RESERVED	R	0h	
1-0	DC5_SEQ	R/W	2h	DCDC5 enable STROBE. Note: STROBE 1 and STROBE 2 are executed only if FSEAL = 0. DCDC5 and 6 cannot be disabled by sequencer once freshness seal is broken. 0h = Rail is not controlled by sequencer. 1h = Enable at STROBE 1. 2h = Enable at STROBE 2. 3h = Rail is not controlled by sequencer.

7.5.30 SEQ6 Register (subaddress = 0x25) [reset = 0x63]

SEQ6 is shown in 图 7-55 and described in 表 7-33.

Return to 表 7-6.

Password protected.

图 7-55. SEQ6 Register

7	6	5	4	3	2	1	0
LS1_SEQ				LDO1_SEQ			
R/W-6h				R/W-3h			

表 7-33. SEQ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LS1_SEQ	R/W	6h	LS1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

表 7-33. SEQ6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	LDO1_SEQ	R/W	3h	LDO1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

7.5.31 SEQ7 Register (subaddress = 0x26) [reset = 0x03]

SEQ7 is shown in 图 7-56 and described in 表 7-34.

Return to 表 7-6.

Password protected.

图 7-56. SEQ7 Register

7	6	5	4	3	2	1	0
GPO3_SEQ				GPO1_SEQ			
R/W-0h				R/W-3h			

表 7-34. SEQ7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO3_SEQ	R/W	0h	GPO3 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

表 7-34. SEQ7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	GPO1_SEQ	R/W	3h	GPO1 enable STROBE: 0h = Rail is not controlled by sequencer. 1h = Rail is not controlled by sequencer. 2h = Rail is not controlled by sequencer. 3h = Enable at STROBE 3. 4h = Enable at STROBE 4. 5h = Enable at STROBE 5. 6h = Enable at STROBE 6. 7h = Enable at STROBE 7. 8h = Enable at STROBE 8. 9h = Enable at STROBE 9. Ah = Enable at STROBE 10. Bh = Rail is not controlled by sequencer. Ch = Rail is not controlled by sequencer. Dh = Rail is not controlled by sequencer. Eh = Rail is not controlled by sequencer. Fh = Rail is not controlled by sequencer.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS65218 is designed to pair with various applications. For detailed information on using TPS65218 with Sitara™ AM335x or AM437x processors, refer to *Powering the AM335x/AM437x with TPS65218*. The typical application in 节 8.2 is based on and uses terminology consistent with the Sitara™ family of processors.

8.1.1 Applications Without Backup Battery

In applications that require always-on supplies but no battery backup, the CC input to the power path must be connected to ground.

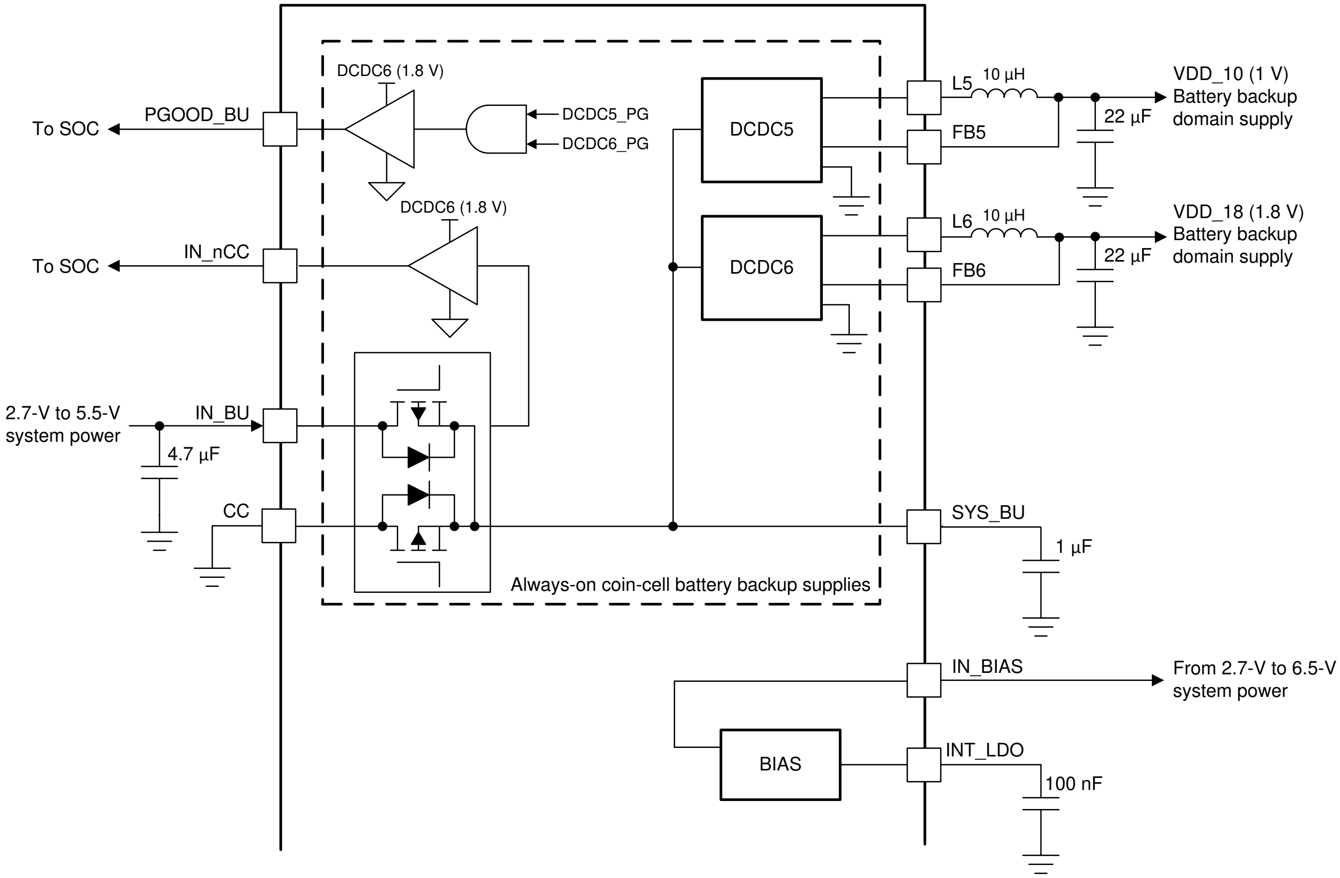


图 8-1. CC Input to Power Path

Note

In applications without backup battery, CC input must be tied to ground.

8.1.2 Applications Without Battery Backup Supplies

In applications that do not require always-on supplies, both inputs and the output of the power-path can simply be grounded. All pins related to DCDC5 and DCDC6 are also tied to ground, and PGOOD_BU and IN_nCC are kept floating. With the backup supplies completely disabled, the FSEAL bit in the STATUS register is undefined and should be ignored.

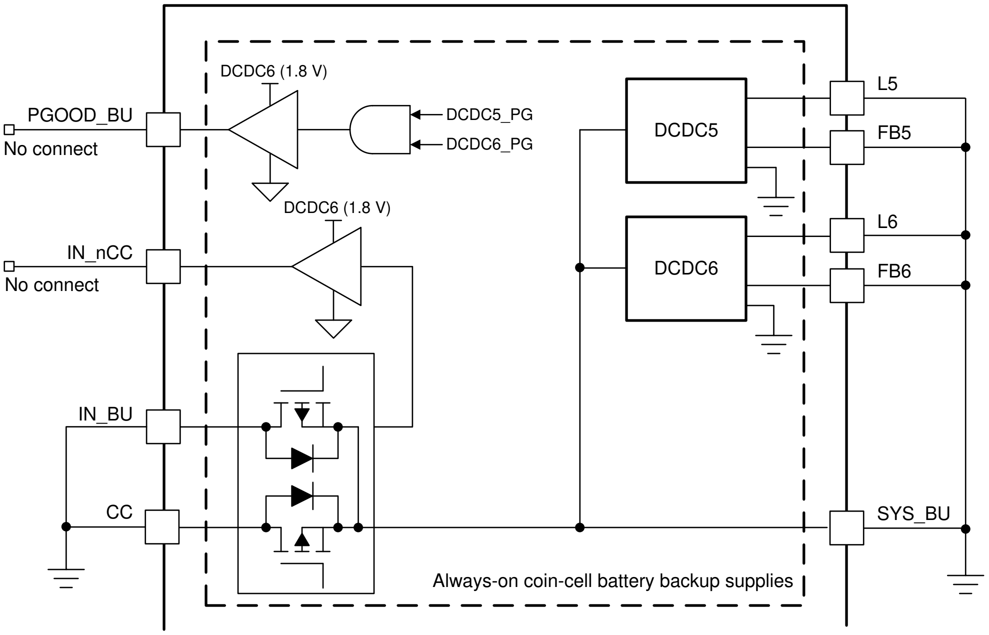


图 8-2. DCDC5 and DCDC6 Pins

Note

In applications that do not require always-on supplies, PGOOD_BU and IN_nCC can be kept floating. All other pins are tied to ground.

8.2 Typical Application

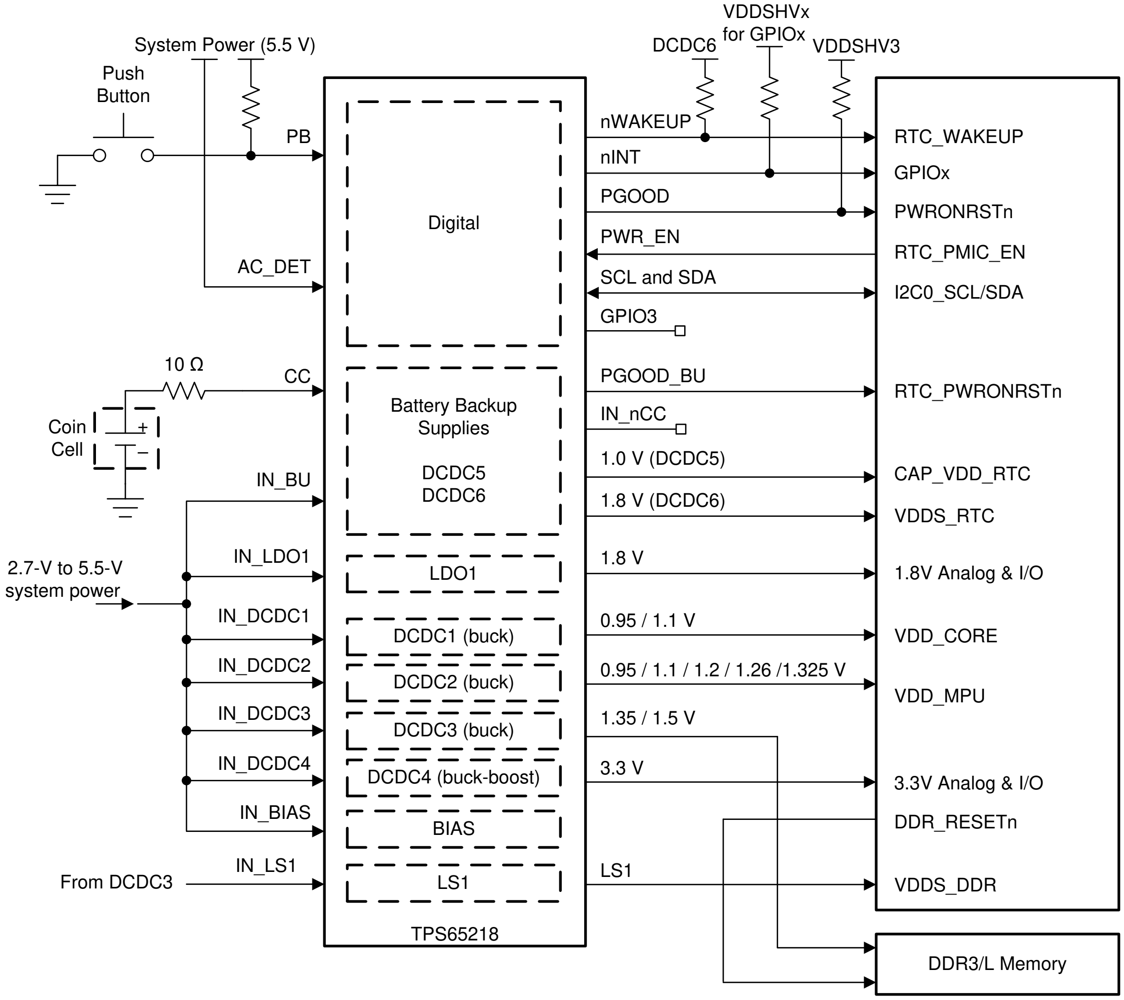


图 8-3. Typical Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Output Filter Design

The step down converters (DCDC1, DCDC2, and DCDC3) on TPS65218 are designed to operate with effective inductance values in the range of 1 to 2.2 µH and with effective output capacitance in the range of 10 to 100 µF. The internal compensation is optimized to operate with an output filter of L = 1.5 µH and C_{OUT} = 10 µF.

The buck boost converter (DCDC4) on TPS65218 is designed to operate with effective inductance values in the range of 1.2 to 2.2 µH. The internal compensation is optimized to operate with an output filter of L = 1.5 µH and C_{OUT} = 47 µF.

The two battery backup converters (DCDC5 and DCDC6) are designed to operate with effective inductance values in the range of 4.7 to 22 µH. The internal compensation is optimized with an output filter of L = 10 µH and C_{OUT} = 20 µF.

Larger or smaller inductor/capacitance values can be used to optimize performance of the device for specific operation conditions.

8.2.1.2 Inductor Selection for Buck Converters

The inductor value affects its peak to peak ripple current, the PWM to PFM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current (ΔL) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}. 方程式 1 calculates the maximum inductor current ripple under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with 方程式 2. This is recommended as during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{1}$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \tag{2}$$

where

- F = Switching frequency
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- I_{Lmax} = Maximum inductor current

The following inductors have been used with the TPS65218 (see 表 8-1).

表 8-1. List of Recommended Inductors

PART NUMBER	VALUE	SIZE (mm) [L × W × H]	MANUFACTURER
INDUCTORS FOR DCDC1, DCDC2, DCDC3, DCDC4			
SPM3012T-1R5M	1.5 µH, 2.8 A, 77 mΩ	3.2 × 3.0 × 1.2	TDK
IHLP1212BZER1R5M11	1.5 µH, 4.0 A, 28.5 mΩ	3.6 × 3.0 × 2.0	Vishay
INDUCTORS FOR DCDC5, DCDC6			
MLZ2012N100L	10 µH, 110 mA, 300 mΩ	2012 / 0805 (2.00 × 1.25 × 1.25)	TDK
LQM21FN100M80	10 µH, 100 mA, 300 mΩ	2012 / 0805 (2.00 × 1.25 × 1.25)	Murata

8.2.1.3 Output Capacitor Selection

The hysteretic PWM control scheme of the TPS65218 switching converters allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents the converter operates in power save mode, and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM mode.

The two battery backup converters (DCDC5 and DCDC6) always operate in PFM mode. For these converters, a capacitor of at least 20 µF is recommended on the output to help minimize voltage ripple.

The buck-boost converter requires additional output capacitance to help maintain converter stability during high load conditions. At least 40 µF of output capacitance is recommended and an additional 100-nF capacitor can be added to further filter output ripple at higher frequencies.

表 8-1 lists the recommended capacitors.

表 8-2. List of Recommended Capacitors

PART NUMBER	VALUE	SIZE (mm) [L × W × H]	MANUFACTURER
CAPACITORS FOR VOLTAGES UP TO 5.5 V(1)			
GRM188R60J105K	1 µF	1608 / 0603 (1.6 × 0.8 × 0.8)	Murata
GRM21BR60J475K	4.7 µF	2012 / 0805 (2.0 × 1.25 × 1.25)	Murata

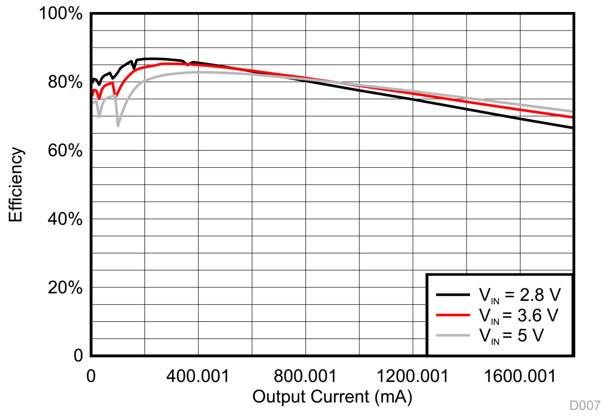
表 8-2. List of Recommended Capacitors (continued)

PART NUMBER	VALUE	SIZE (mm) [L × W × H]	MANUFACTURER
GRM31MR60J106K	10 µF	3216 / 1206 (3.2 × 1.6 × 1.6)	Murata
GRM31CR60J226K	22 µF	3216 / 1206 (3.2 × 1.6 × 1.6)	Murata
CAPACITORS FOR VOLTAGES UP TO 3.3 V(1)			
GRM21BR60J106K	10 µF	2012 / 0805 (2.0 × 1.25 × 1.25)	Murata
GRM31CR60J476M	47 µF	3216 / 1206 (3.2 × 1.6 × 1.6)	Murata

(1) The DC bias effect of ceramic capacitors must be considered when selecting a capacitor.

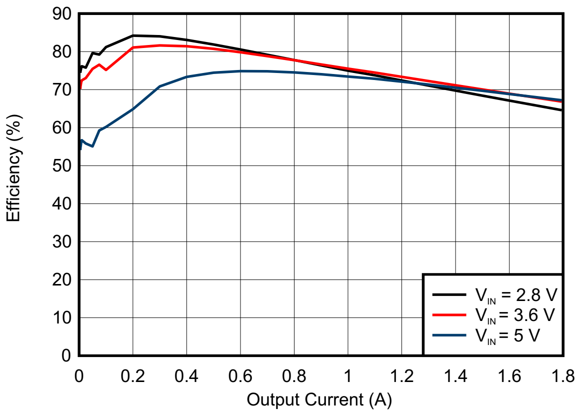
8.2.2 Application Curves

at T_J = 25°C unless otherwise noted



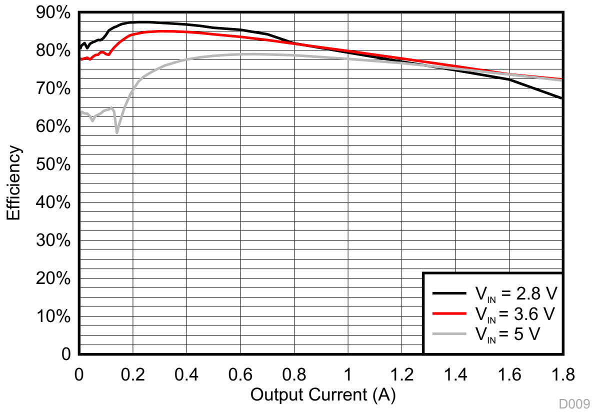
V_{OUT} = 1.1 V

图 8-4. DCDC1/DCDC2 Efficiency



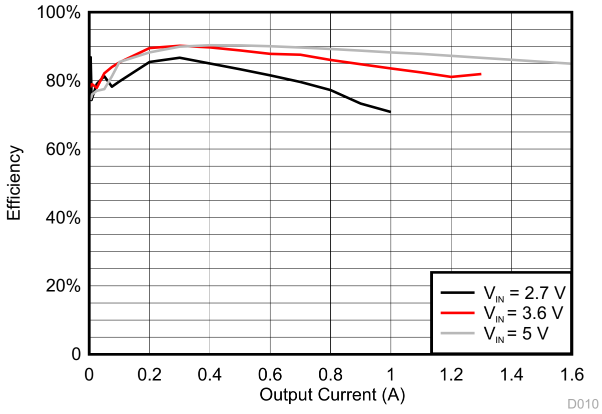
V_{OUT} = 1.2 V

图 8-5. DCDC3 Efficiency



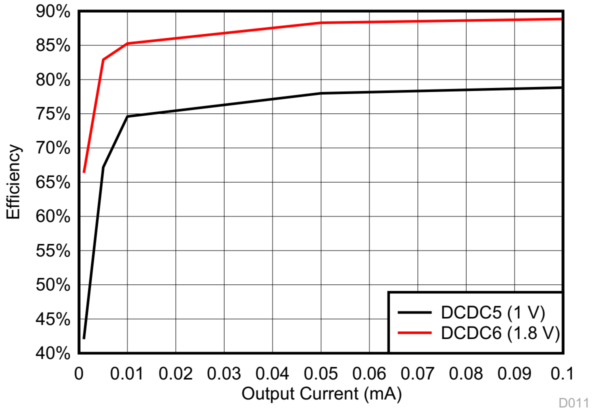
V_{OUT} = 1.5 V

图 8-6. DCDC3 Efficiency



V_{OUT} = 3.3 V

图 8-7. DCDC4 Efficiency



IN_BU = 0 V CC = 3 V

图 8-8. DCDC5/DCDC6 Efficiency

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.7 V and 5.5 V. This input supply can be from a single cell Li-Ion battery or other externally regulated supply. If the input supply is located more than a few inches from the TPS65218 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 μF is a typical choice.

The coin cell back up input is designed to operate with a input voltage supply between 2.2 V and 3.3 V This input should be supplied by a coin cell battery with 3-V nominal voltage.

10 Layout

10.1 Layout Guidelines

Follow these layout guidelines:

- The IN_X pins should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 4.7-μF with a X5R or X7R dielectric.
- The optimum placement is closest to the IN_X pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the IN_X pin, and the thermal pad (PowerPAD for the HTQFP packageof the device.
- The thermal pad should be tied to the PCB ground plane with a minimum of 25 vias. See 图 10-2 for an example.
- The LX trace should be kept on the PCB top layer and free of any vias.
- The FBX traces should be routed away from any potential noise source to avoid coupling.
- DCDC4 Output capacitance should be placed immediately at the DCDC4 pin. Excessive distance between the capacitance and DCDC4 pin may cause poor converter performance.

10.2 Layout Example

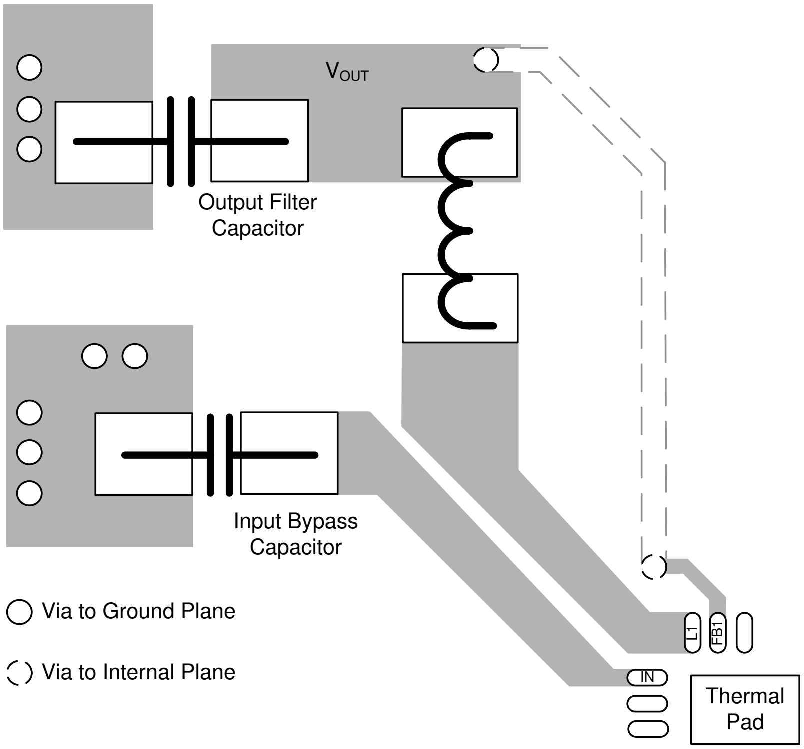
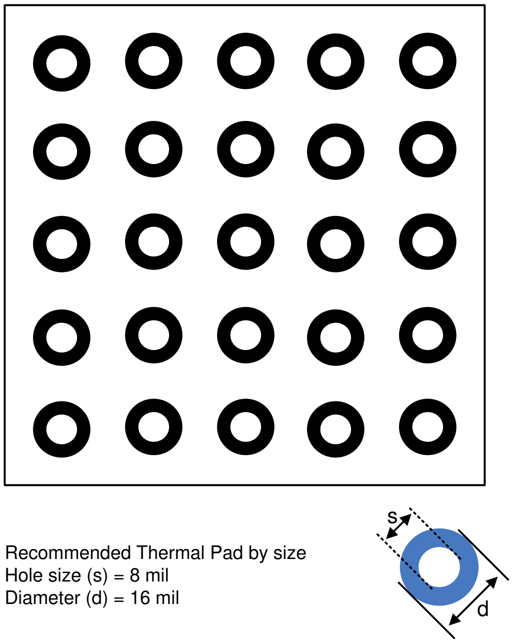


图 10-1. Layout Recommendation



Recommended Thermal Pad by size
Hole size (s) = 8 mil
Diameter (d) = 16 mil

图 10-2. PowerPAD™ Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage* application report
- Texas Instruments, *Design Calculations for Buck-Boost Converters* application report
- Texas Instruments, *Empowering Designs With Power Management IC (PMIC) for Processor Applications* application report
- Texas Instruments, *Powering the AM335x/AM437x with TPS65218* user's guide
- Texas Instruments, *TPS65218EVM* user's guide
- Texas Instruments, *TPS65218 Power Management Integrated Circuit (PMIC) for Industrial Applications* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65218B101PHPR	NRND	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	65218B101	
TPS65218B101PHPT	NRND	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	65218B101	
TPS65218B1PHPR	NRND	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	T65218B1	
TPS65218B1PHPT	NRND	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	T65218B1	
TPS65218B1RSLR	NRND	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65218B1	
TPS65218B1RSLT	NRND	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65218B1	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

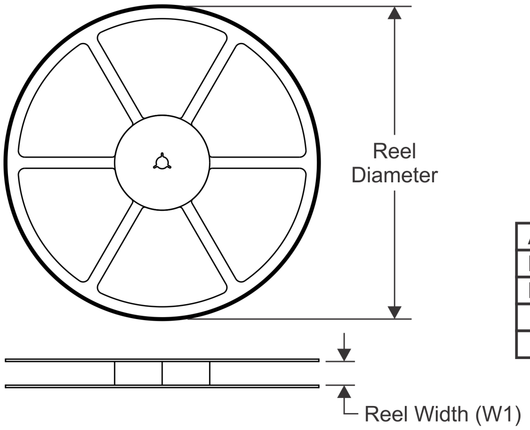
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

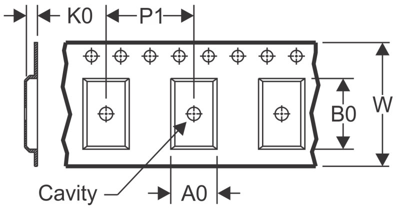
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

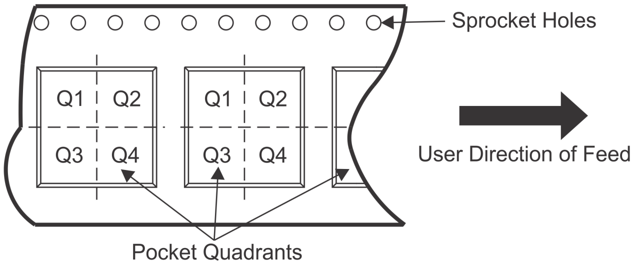


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

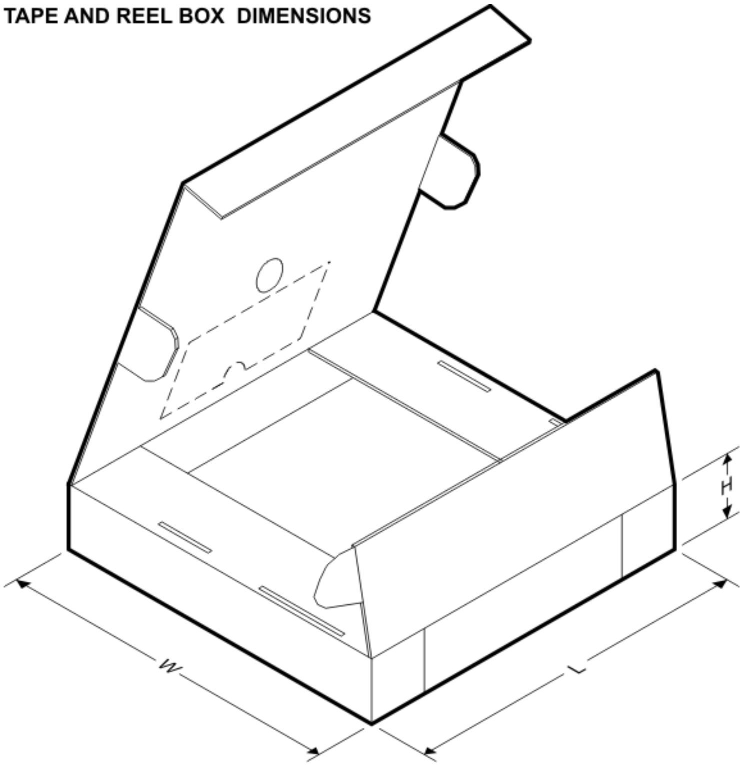
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65218B101PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B101PHPT	HTQFP	PHP	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1PHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1PHPT	HTQFP	PHP	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS65218B1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65218B1RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

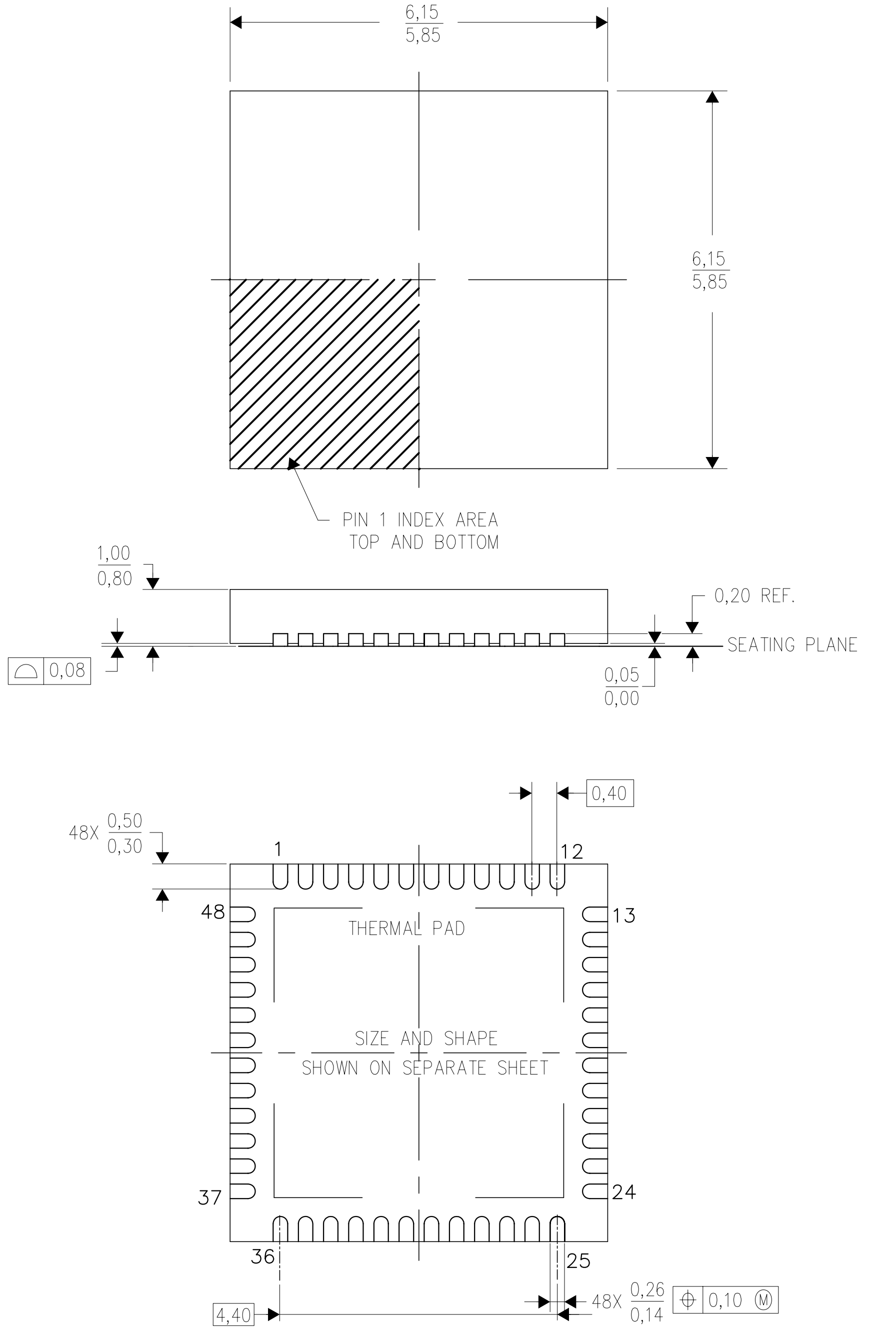
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

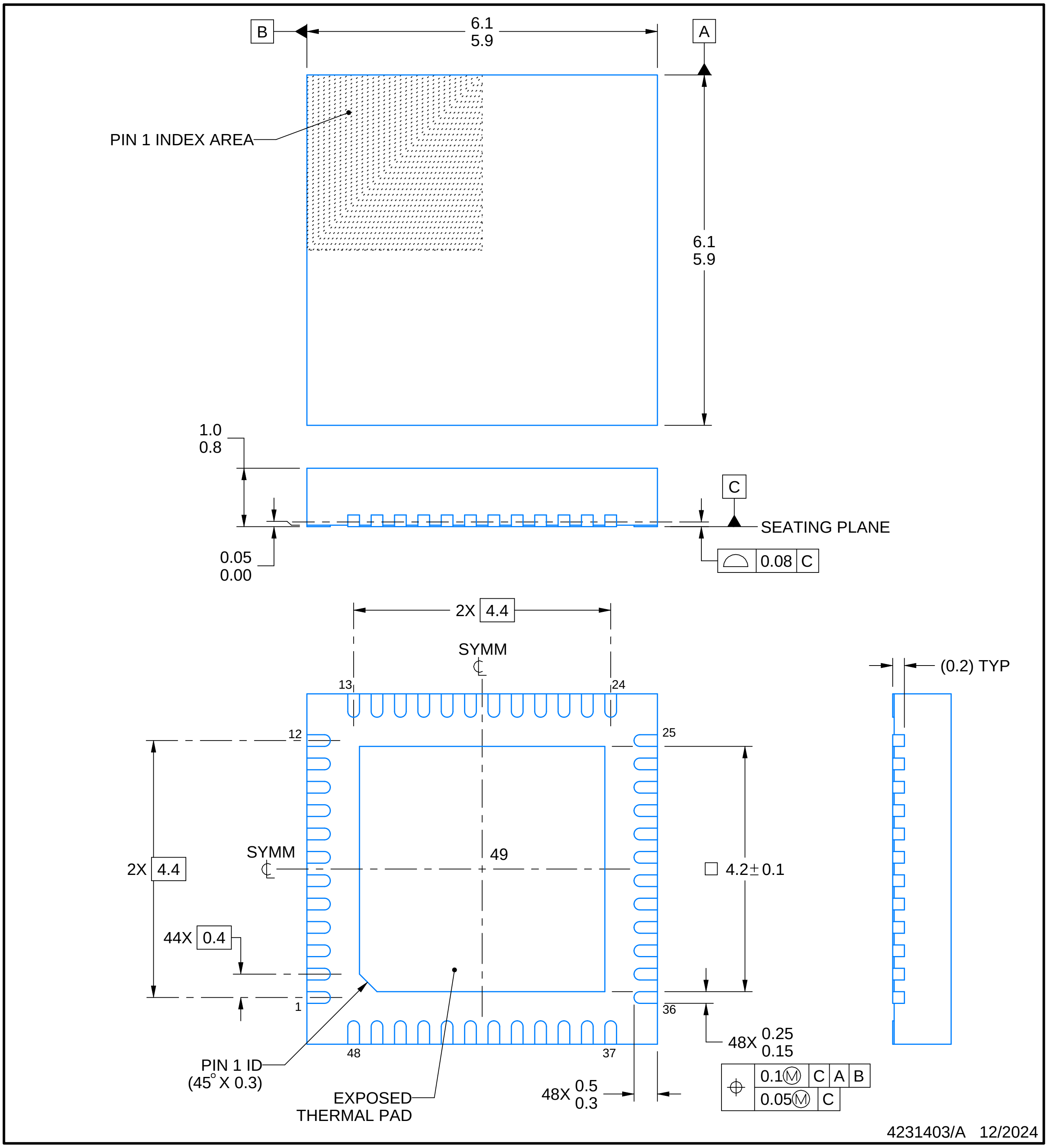
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65218B101PHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8
TPS65218B101PHPT	HTQFP	PHP	48	250	336.6	336.6	31.8
TPS65218B1PHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8
TPS65218B1PHPT	HTQFP	PHP	48	250	336.6	336.6	31.8
TPS65218B1RSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65218B1RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



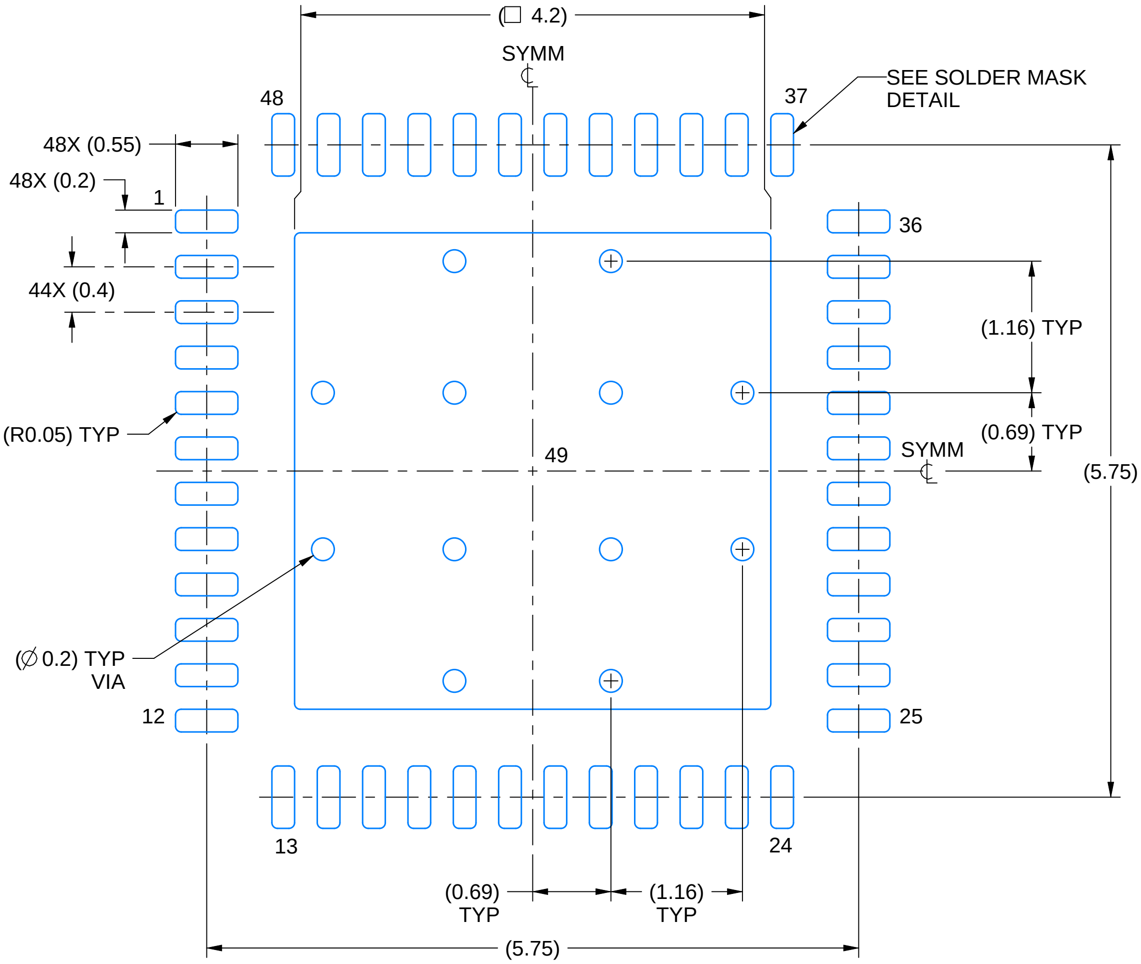
4207548/B 06/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No—leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

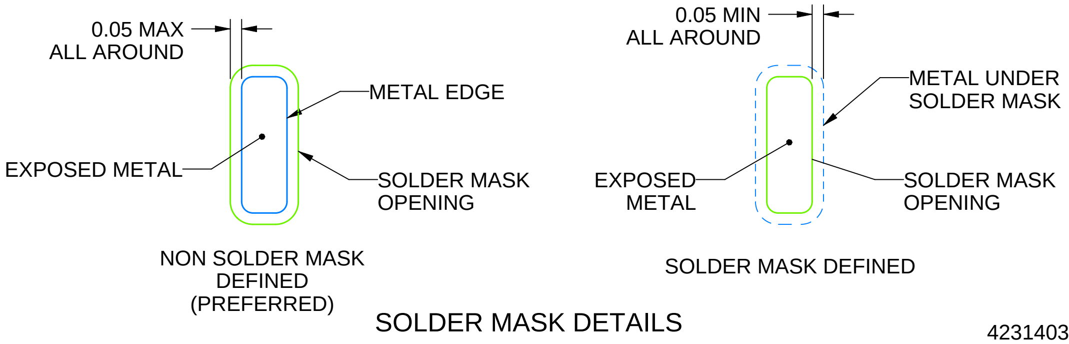


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

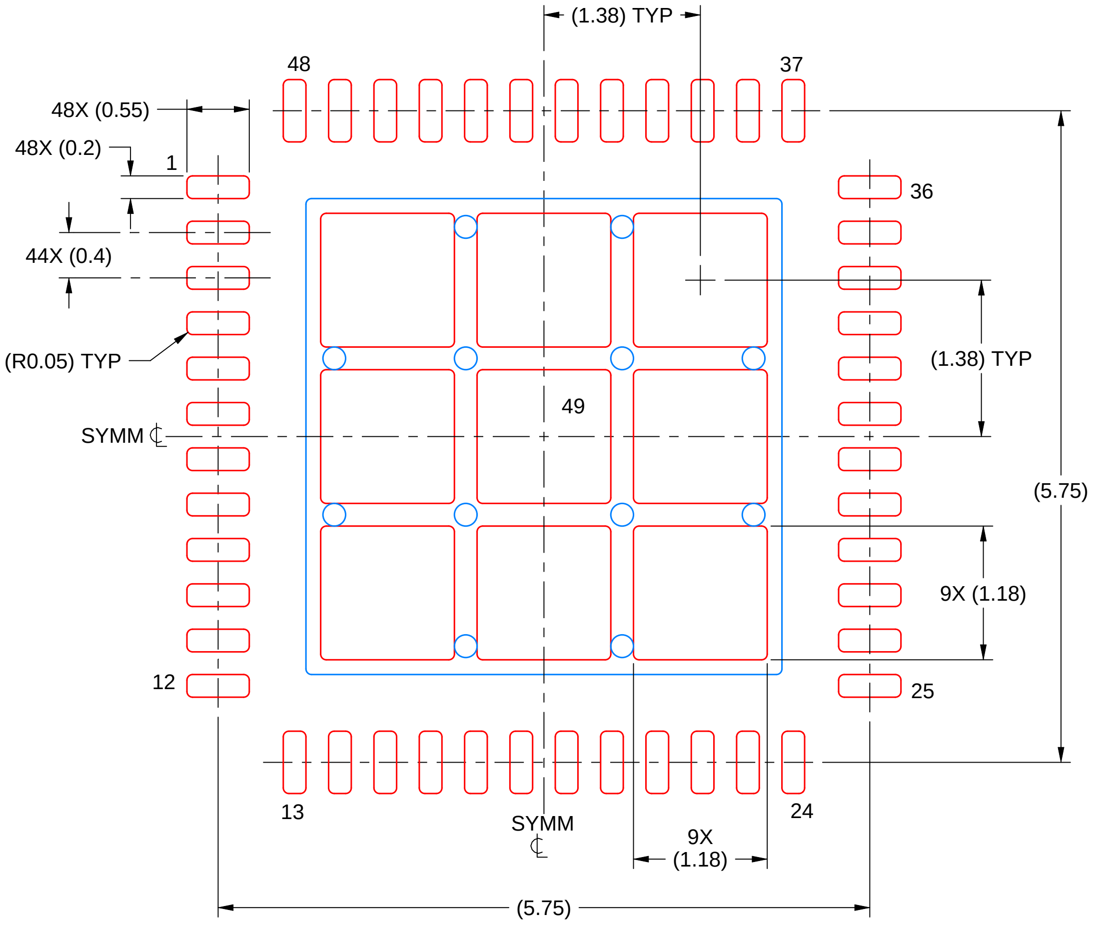


SOLDER MASK DETAILS

4231403/A 12/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

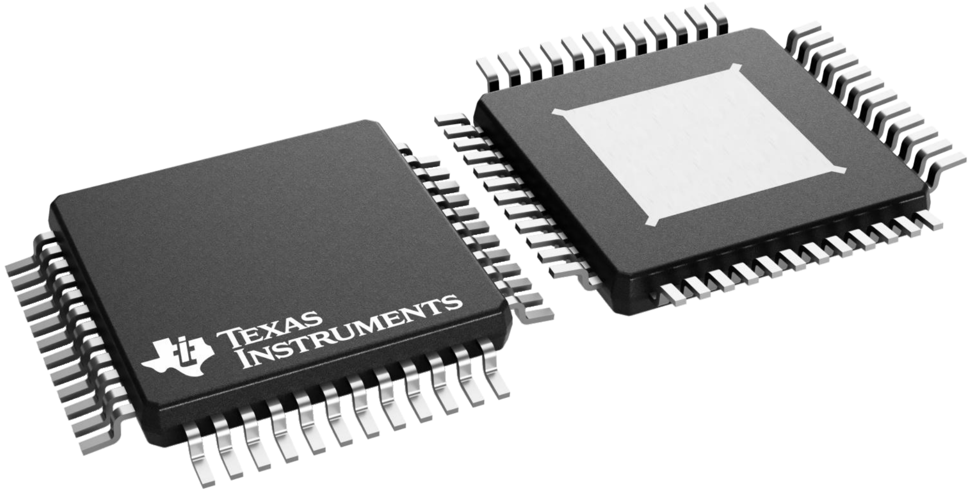
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

PHP 48 **TQFP - 1.2 mm max height**

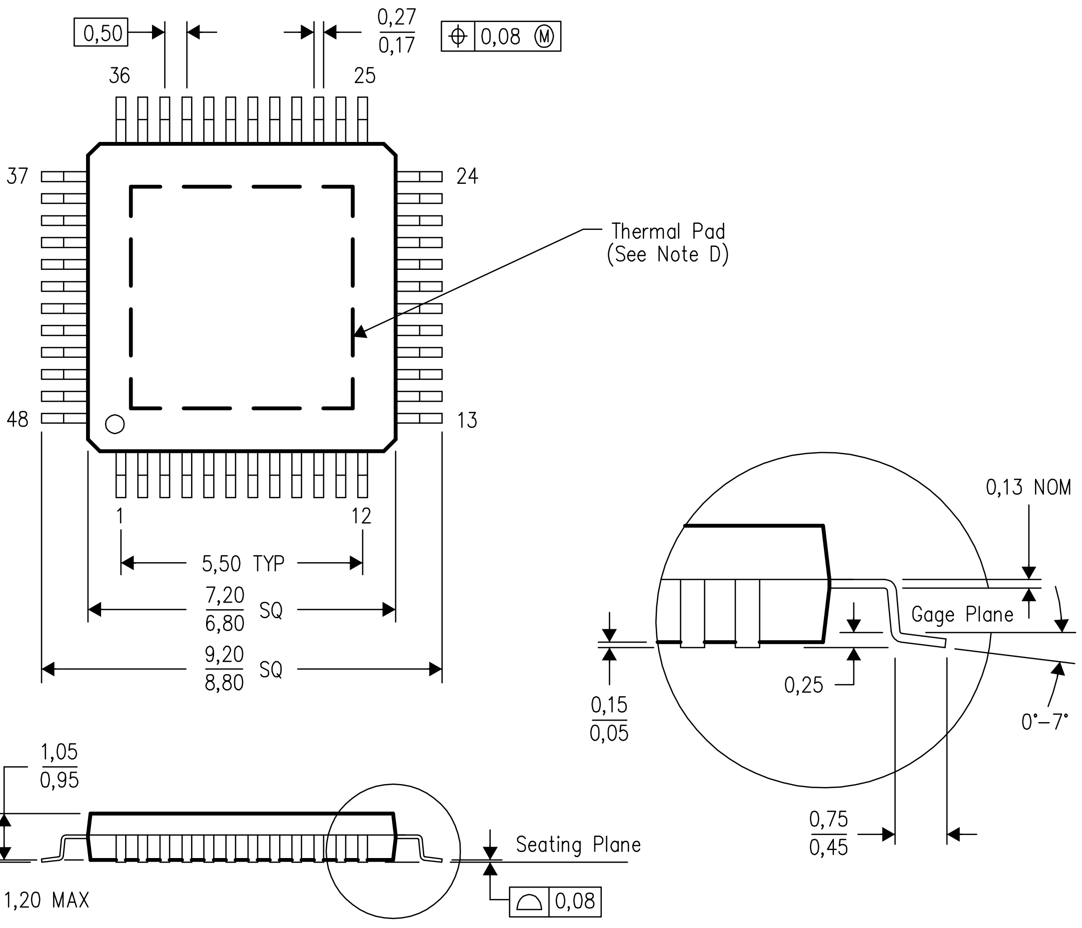
7 x 7, 0.5 mm pitch QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226443/A

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



4146927/B 08/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MS–026

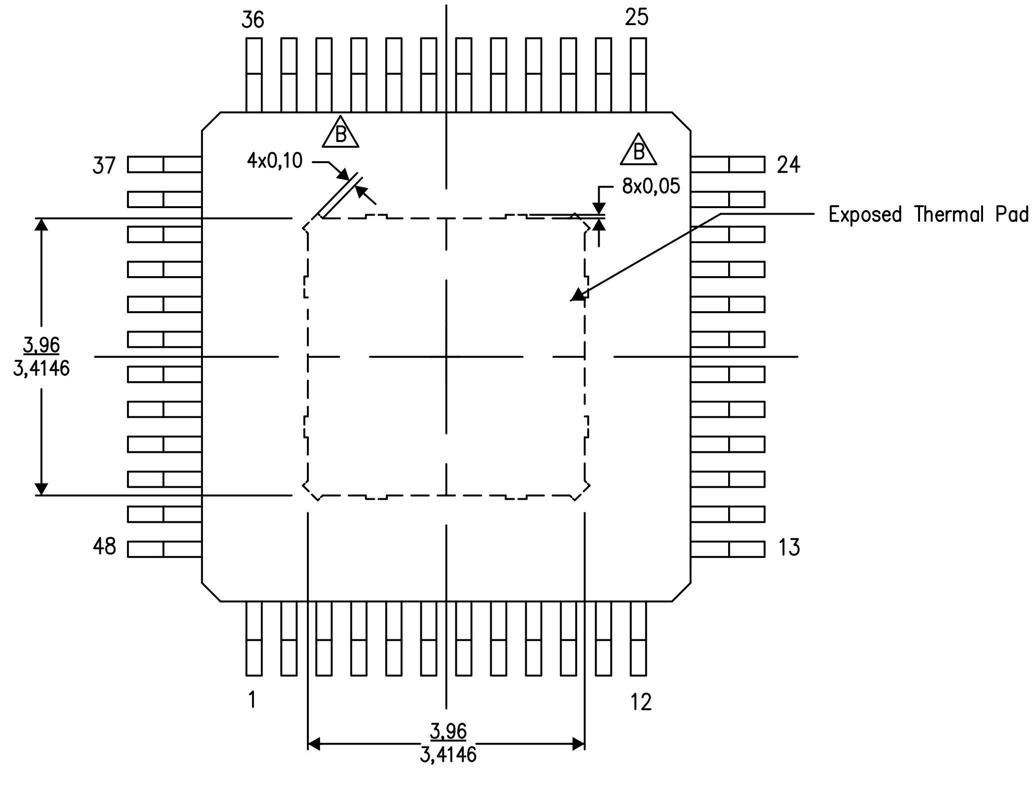
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206329–14/P 03/15

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265