

# 适用于安全相关应用中微控制器的 TPS653850A-Q1 and TPS653852A-Q1 多轨电源

## 1 特性

- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级 1：-40°C 至 +125°C 环境温度工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 符合功能安全标准
  - 专为功能安全应用开发
  - 可帮助使 ISO 26262 系统设计符合 ASIL D 的文档
  - 可满足 ASIL D 要求的系统功能和硬件完整性
- 输入电压范围
  - 电池初始加电电压为 7V 至 36V
  - 电池初始加电后正常运行电压为 4V 至 36V
  - 唤醒后的最低运行电压为 2.3V
- 电源轨 (具有内部 FET)
  - 6V 同步降压/升压前置稳压器
  - 5V、285mA LDO (CAN、外设或 ADC 基准 1% 精度, 带 20 至 120mA 负载)
  - 3.3V 或 5V、350mA LDO (MCU) TPS653850A-Q1。3.3V 350mA 或 5V 500mA LDO (MCU) TPS653852A-Q1
  - 用于传感器电源或外设的 2 个受保护的 LDO
    - 传感器电源 1 (VSOUT1) 为 120mA, 传感器电源 2 (VSOUT2) 为 100mA
    - 可配置跟踪模式 (跟踪输入引脚) 或 3.3V/5V 固定输出电压
    - 接地短路和电池保护
  - 电荷泵: 最小值 6V, 最大值 11V (高于电池电压)
- 监视和保护

- 独立监控所有稳压器输出、电池电压和内部电源的欠压和过压情况
- 电压监视电路 (包括独立的带隙基准) 由单独的电池电压输入引脚供电
- 针对所有电压监控进行自检 (上电期间以及在上电之后由外部 MCU 触发)
- 所有电源均具有电流限制和过热预警及关断保护
- 微控制器接口
  - 打开和关闭窗口或问答看门狗功能
  - 功能安全 MCU 故障输出 (PWM 或电平) 监控器、MCU 错误信号监控器
  - DIAGNOSTIC 状态, 用于辅助执行器件自检和系统诊断
  - SAFE 状态, 用于检测到错误事件时的器件和系统保护
  - 针对内部振荡器的时钟监视器
  - 模拟与逻辑内置自检
  - 支持对非易失性存储器、器件和系统配置寄存器以及 SPI 通信进行循环冗余校验 (CRC)
  - 针对 MCU 的复位电路
  - 诊断输出引脚
- SPI 支持对命令和数据进行 CRC
- 通过 SPI 寄存器报告系统级和器件级错误
- 使能驱动输出, 可在检测到任意系统故障时禁用外部功率级
- 通过 IGN 引脚 (点火) 或 CAN\_WU 引脚 (收发器或其他功能) 唤醒
- 48 引脚 HTSSOP PowerPAD™ IC 封装

## 2 应用

- 汽车安全相关应用
- 工业安全相关应用

## 3 说明

TPS653850A-Q1 and TPS653852A-Q1 器件是一款多轨电源, 旨在为安全相关应用中的微控制器供电, 例如汽车行业中的应用。该器件支持采用双核锁步 (LS) 和其他多核架构的功能安全微控制器。

TPS653850A-Q1 and TPS653852A-Q1 器件集成了多个为 MCU、CAN 或 FlexRay 以及外部传感器供电的电源轨。并且配有一个具有内部 FET 的降压-升压转换器, 可将 2.3V 至 36V 的输入电池电压转换为 6V 前置稳压器输出, 从而为其他稳压器供电。集成电荷泵可为内部稳压器提供过驱电压, 而且还可用于驱动外部 NMOS FET 以提供电池反向保护。该器件支持通过点火信号 (IGN 引脚) 或者通过 CAN 收发器或其他信号 (CAN\_WU 引脚) 唤醒。

该器件内部有一个独立的电压监测单元, 可监测所有内部电源轨以及电池电源稳压器输出的欠压和过压情况。此外, 该器件还实现了稳压器电流限制和过热保护。TPS653850A-Q1 and TPS653852A-Q1 器件具有问答看门狗、MCU 误差信号监控、针对内部振荡器的时钟监控、针对时钟监控器的自检、针对非易失性存储器和 SPI 通信的循环冗余校验 (CRC)、支持 MCU 监测器件内部模拟和数字信号的诊断输出引脚、针对 MCU 的复位电路 (NRES 引脚) 以及可在检测到任何系统故障时禁用外部功率级的保险输出 (ENDRV 引脚)。该器件在启动时自动运行内置



自检 (BIST), 如果需要, MCU 可以在系统运行期间通过软件控制重新运行 BIST。专用的 DIAGNOSTIC 状态可供 MCU 使用以检查 TPS653850A-Q1 and TPS653852A-Q1 功能性。

TPS653850A-Q1 and TPS653852A-Q1 器件还可通过 SPI 寄存器报告错误。此器件在 SPI 寄存器中有单独的状态位, 用于指示每个特定的系统级或器件级错误。当器件检测到特定错误条件时, 可将相应状态位置 1 并保持到 MCU 读取完该状态位所在 SPI 寄存器为止。根据置 1 的状态位, MCU 可以决定是否必须使系统保持安全状态或者是否可使系统恢复运行。

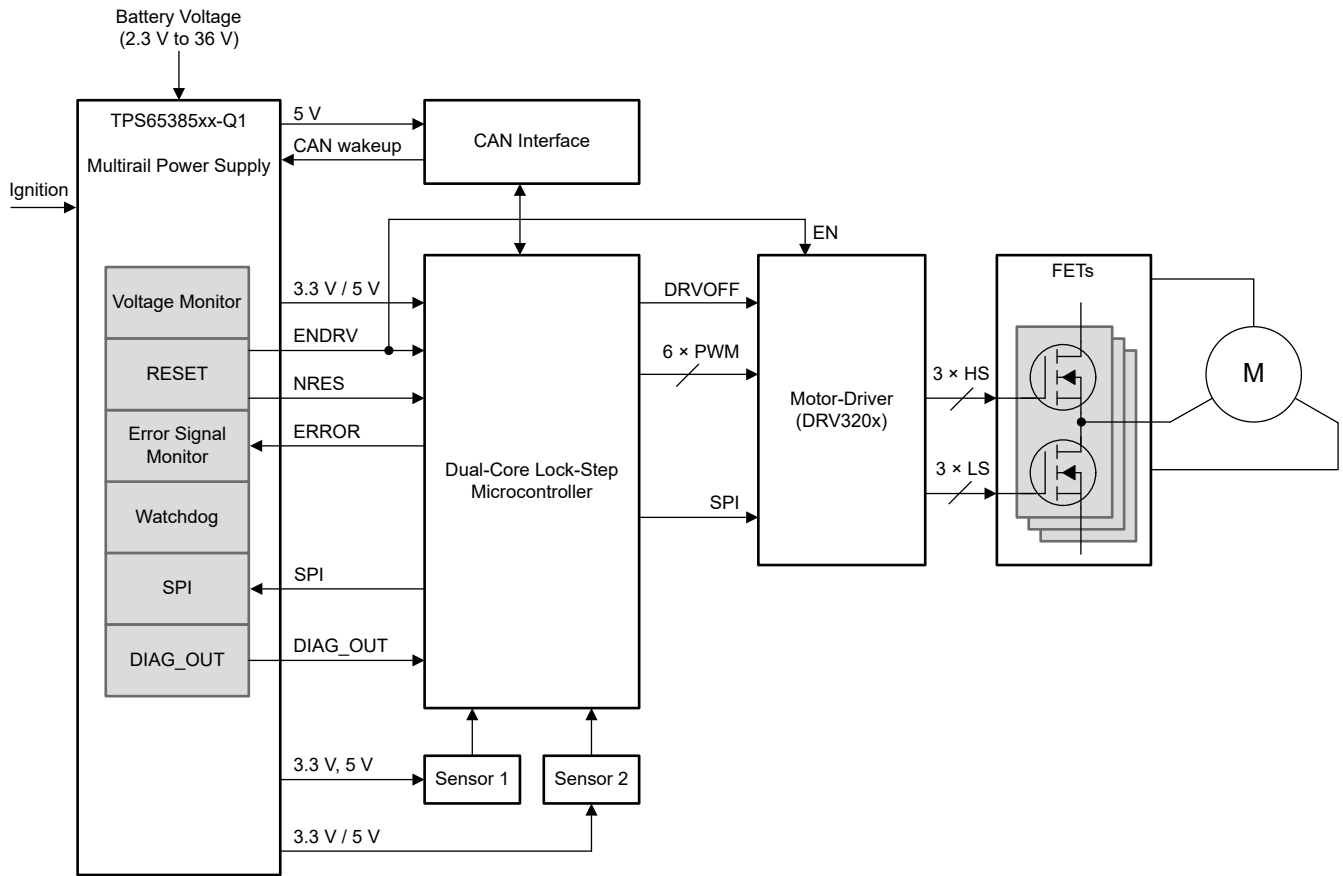
TPS653850A-Q1 and TPS653852A-Q1 器件采用 48 引脚 HTSSOP PowerPAD™ IC 封装。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸
TPS653850A-Q1	HTSSOP (48)	12.50mm x 6.10mm
TPS653852A-Q1		

(1) 如需更多信息, 请参阅节 6。

### 3.1 Typical Application Diagram



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from Revision \* (January 2020) to Revision A (February 2021)

Page

• 向特性部分添加了“符合功能安全标准”状态.....	<b>1</b>
• 更新了整个文档中的表、图和交叉参考的编号格式.....	<b>1</b>

## 5 Device and Documentation Support

### 5.1 Documentation Support

#### 5.1.1 Related Documentation

For related documentation see the following:

- Texas instruments, [A Guide to Board Layout for Best Thermal Resistance for Exposed Packages application report](#)
- Texas instruments, [PowerPAD™ Made Easy application report](#)
- Texas instruments, [PowerPad™ Thermally Enhanced Package application report](#)

#### 5.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.3 支持资源

**TI E2E™ 支持论坛**是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 5.4 Trademarks

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### 5.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 5.6 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
O3850AQDCARQ1	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O3850A	<a href="#">Samples</a>
O3852AQDCARQ1	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	O3852A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
O3850AQDCARQ1	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
O3852AQDCARQ1	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
O3850AQDCARQ1	HTSSOP	DCA	48	2000	350.0	350.0	43.0
O3852AQDCARQ1	HTSSOP	DCA	48	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

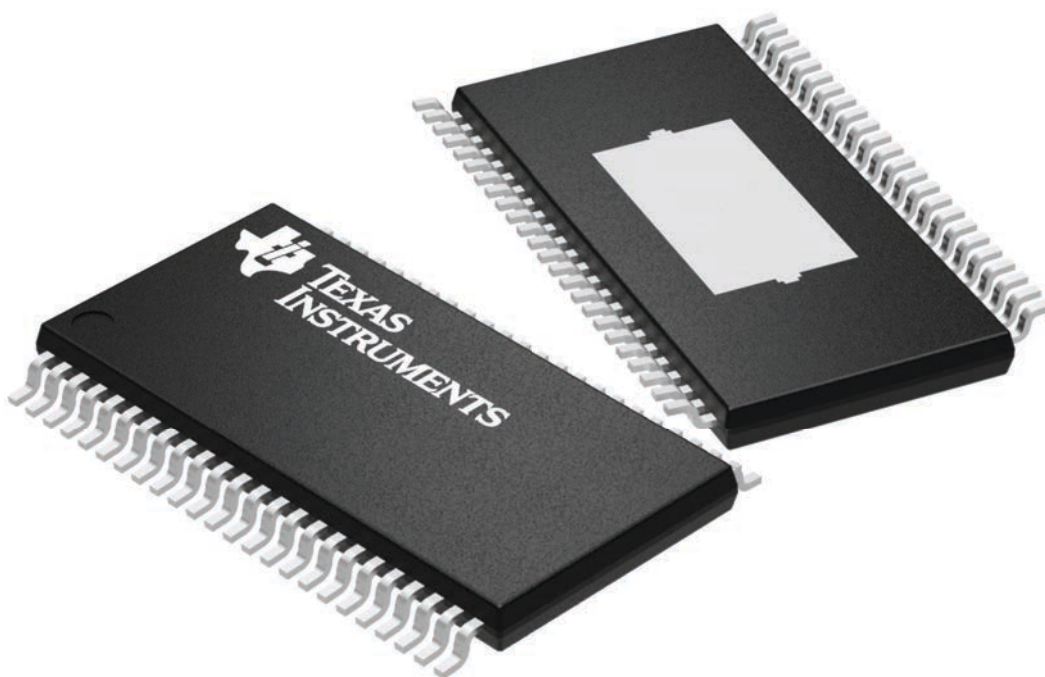
**DCA 48**

**HTSSOP - 1.2 mm max height**

12.5 x 6.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

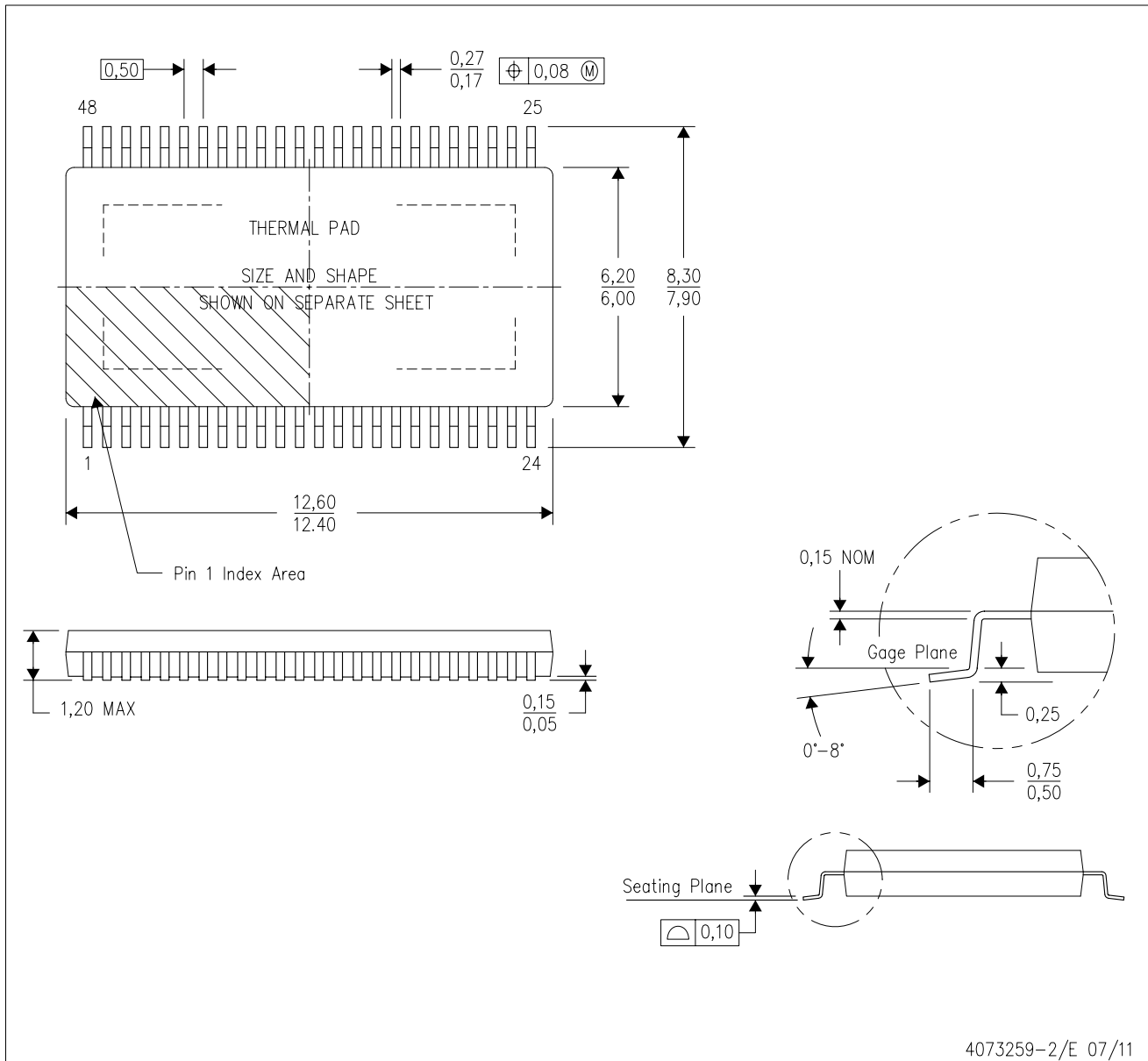


4224608/A

# MECHANICAL DATA

DCA (R-PDSO-G48)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

DCA (R-PDSO-G48)

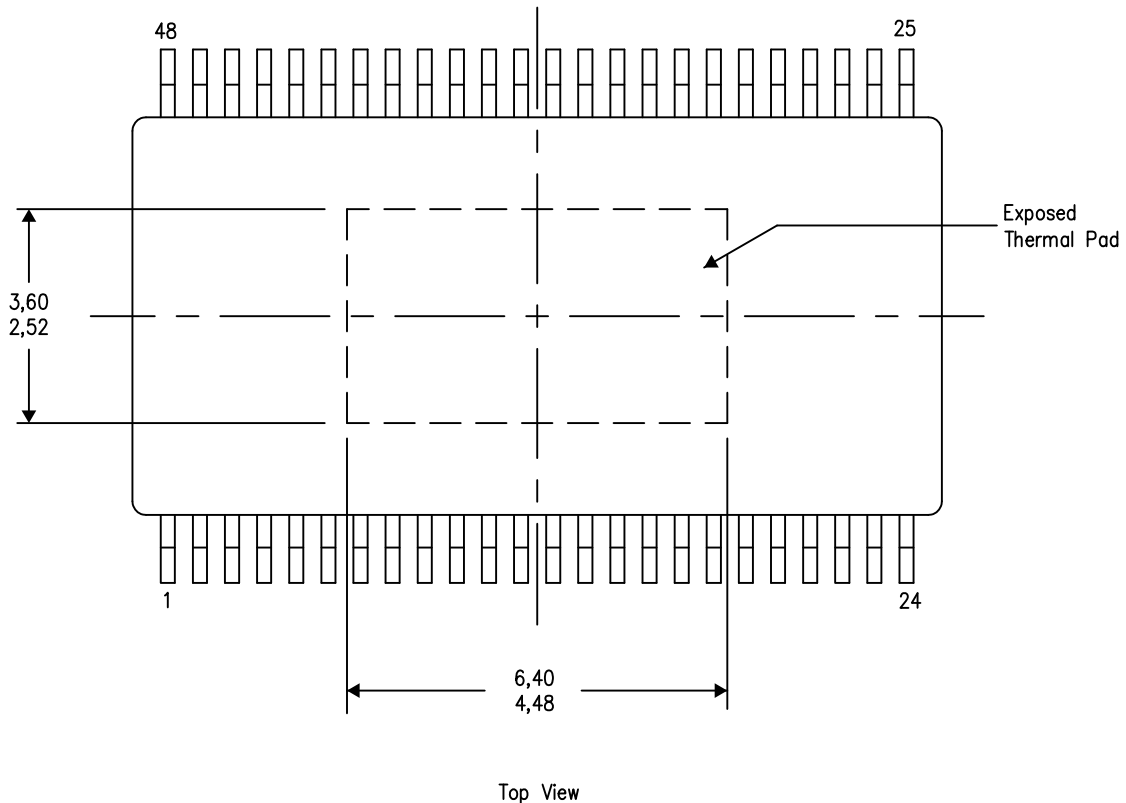
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

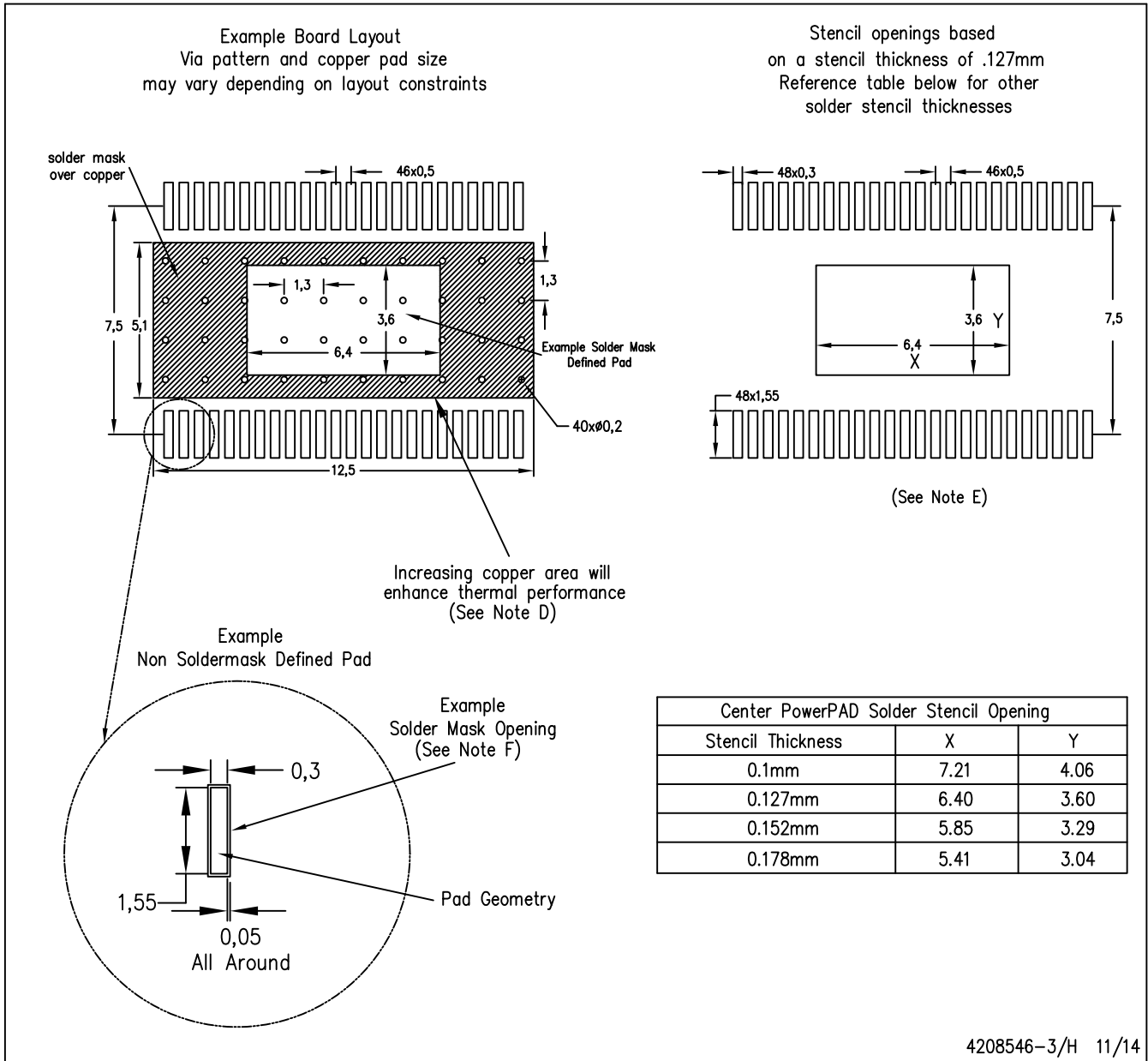


Exposed Thermal Pad Dimensions

4206320-4/S 11/14

NOTE: A. All linear dimensions are in millimeters

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4208546-3/H 11/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

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