TPS65980 Thunderbolt™ 总线电源降压/升压

1 特性

- 由 Thunderbolt™ 总线供电
- 2.5V 至 15.75V 输入
- 3.3V 输出
- 电缆电源输出电流限制
- 热关断

2 应用范围

- Thunderbolt™/Thunderbolt™ 2 系统
- 总线供电系统
- 电源管理系统

3 说明

TPS65980 是一款直流/直流开关稳压器，此稳压器由电压范围介于 2.5V 至 15.75V 之间的 Thunderbolt™ 或 Thunderbolt™ 2 电源总线供电，并且生成 3 个独立 3.3V 电源输出。

TBT_OUT 电源为本地外设 Thunderbolt™ 控制器和支持电路供电。 CBL_OUT 电源将电能输送回 Thunderbolt™ 电缆，并且具有可调电流限值。 DEV_OUT 电源为器件中的所有其他电路供电来执行其设计的功能。

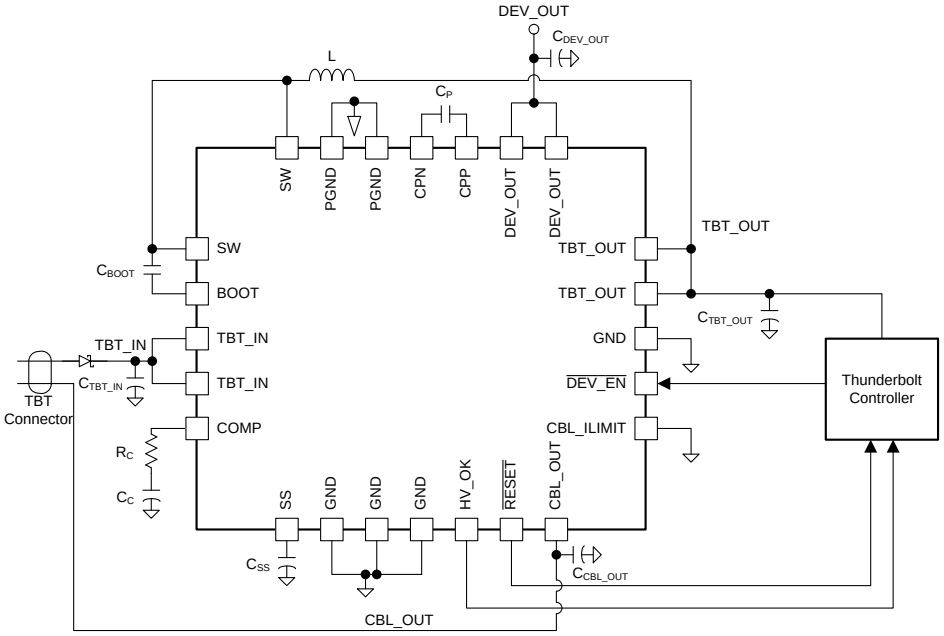
TPS65980 采用 24 引脚 5mm x 4mm x 0.9mm 超薄四方平面无引线 (VQFN) 封装。

器件信息(1)

器件名称	封装	封装尺寸
TPS65980	VQFN (24)	5mm x 4mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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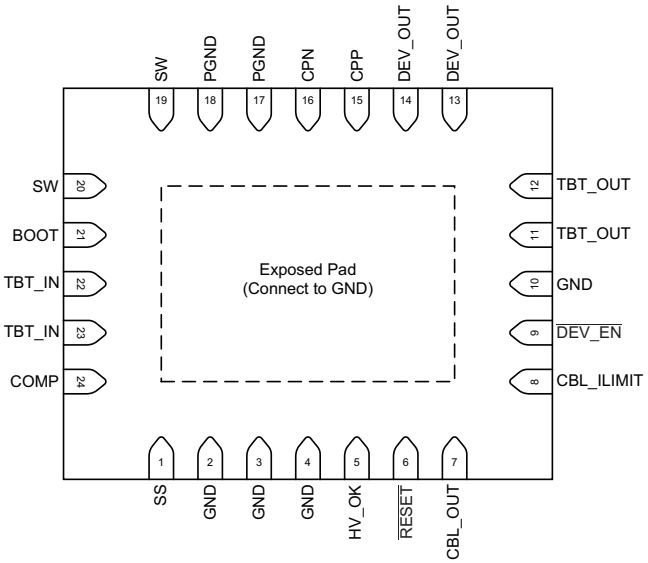
5 修订历史记录

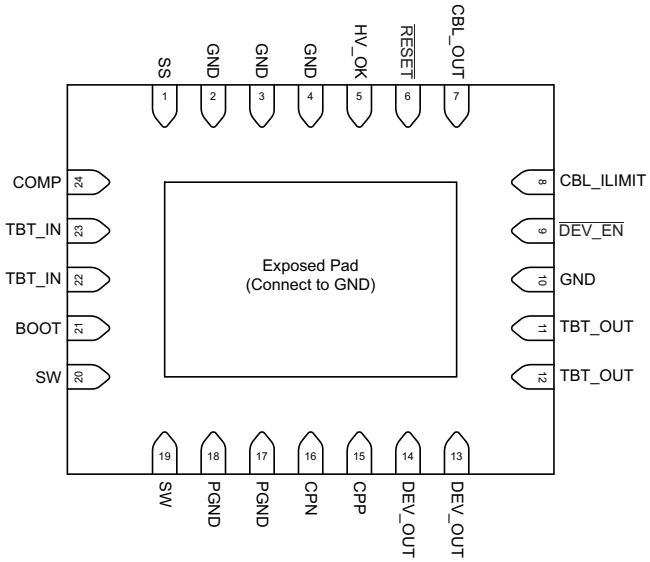
Changes from Original (April 2014) to Revision A	**Page**
• 已将文档修改为完整版。	1

6 Pin Configuration and Functions

VQFN (RHF) 24-Pin
TOP VIEW



VQFN (RHF) 24-Pin
BOTTOM



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SS	ANALOG	Soft Start Capacitance. This pin sets the soft start ramp rate when the TBT_IN voltage ramps from 0V to high voltage.
2, 3, 4	GND	GND	Device Ground
5	HV_OK	OUTPUT	High Voltage Present Indicator. This pin indicates that a high voltage is present on TBT_IN. The output asserts high when the TBT_IN pin is above the V_{HVT} voltage and the $\overline{RESET}$ output is asserting high.
6	$\overline{RESET}$	OUTPUT	Reset output indicator. This pin asserts low when TBT_OUT is in under-voltage.
7	CBL_OUT	PWROUT	Current Limited Power Output to Thunderbolt™ Cable. This pin supplies power to the Thunderbolt™ cable. The current limit of this pin is set by the CBL_ILIMIT pin.
8	CBL_ILIMIT	INPUT	Current Limit Set. Logic input that sets the current limit state on the CBL_OUT pin. Tie pin to TBT_OUT for a logic high input.
9	$\overline{DEV\_EN}$	INPUT	Device Enable Input. When input pin is high, DEV_OUT is high impedance. When input pin low, DEV_OUT is connected to TBT_OUT.
10	GND	ANALOG	Device Ground
11, 12	TBT_OUT	PWROUT	Power Output to Thunderbolt™ circuitry. This pin supplies power to the Thunderbolt™ controller.
13, 14	DEV_OUT	PWROUT	Power Output to peripheral device. This pin supplies power to circuitry not associated with the Thunderbolt™ controller or the Thunderbolt™ cable. It is intended to supply power to the peripheral device main function.
15	CPP	ANALOG	Charge Pump Capacitance Positive Output
16	CPN	ANALOG	Charge Pump Capacitance Negative Output
17, 18	PGND	GND	Buck Controller Power Ground
19, 20	SW	ANALOG	Buck Controller Switch Output
21	BOOT	ANALOG	Buck Controller Bootstrap
22, 23	TBT_IN	PWRIN	Power Input from Thunderbolt™ Cable. This pin is the power supply to the device.
24	COMP	ANALOG	Buck Converter Compensation. This pin provides compensation to the buck converter feedback loop.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
	Input voltage range[2]	TBT_IN	–0.3	18	V
		$\overline{\text{DEV\_EN}}$	–0.3	3.6	
		BOOT	–0.3	25	
		BOOT (10 ns transient)	–0.3	27	
		BOOT (vs SW)	–0.3	7	
		SW	–0.6	18	
		SW (10 ns transient)	–2	20	
		COMP	–0.3	3.6	
		SS	–0.3	3.6	
		CBL_ILIMIT	–0.3	3.6	
		CPP	–0.3	7.2	
		CPN	–0.3	3.6	
	Output voltage range[2]	TBT_OUT, CBL_OUT, DEV_OUT	–0.3	3.6	V
		$\overline{\text{RESET}}$, HV_OK	–0.3	3.6	
V_{diff}	Voltage from GND to Thermal Pad		–0.2	0.2	V
	Voltage from PGND to GND		–0.2	0.2	V
T_A	Operating ambient temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
TBT_IN	Supply input voltage range		2.5	15.75	V
V_I	Input voltage range	$\overline{\text{DEV\_EN}}$	–0.1	3.6	V
		BOOT	–0.1	25	
		SW	–0.6	16.5	
		COMP	–0.1	3.6	
		SS	–0.1	3.6	
		CBL_ILIMIT	–0.1	3.6	
		CPP	–0.1	7.2	
		CPN	–0.1	3.6	
V_O	Output voltage range	TBT_OUT, CBL_OUT, DEV_OUT	–0.1	3.6	V
		$\overline{\text{RESET}}$, HV_OK	–0.1	3.6	
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS65980 RHF 24 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	8.2	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	8.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted all specifications applies over the V_{TBT_IN} range and operating ambient temperature of –40°C ≤ T_A ≤ 85°C, C_{TBT_IN} = 22 µF, C_{TBT_OUT} = 10 µF, C_{CBL_OUT} = 1 µF, CSS = 10 nF, and 33 V/µs logic input transitions. Typical values are for V_{TBT_IN} = 12 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS						
V_{TBT_IN}	TBT_IN Input voltage range		2.5	12	15.75	V
V_{REF_RSTN}	TBT_OUT to $\overline{RESET}$ clear high	TBT_OUT rising	3	3.1	3.2	V
	TBT_OUT to $\overline{RESET}$ assert low	TBT_OUT falling	2.5	2.6	2.7	
V_{HVTR}	TBT_IN to HV_OK assert	TBT_IN rising	4.36	4.5	4.64	V
$V_{HVTHYST}$	TBT_IN to HV_OK clear	TBT_IN Falling hysteresis		100		mV
SR_{02L}	TBT_IN Input slew rate	TBT_IN transition from 0 V to 3.3 V	0.1		30	kV/s
SR_{L2H}	TBT_IN Input slew rate	TBT_IN transition from 3.3 V to 15 V	0.1		30	kV/s
I_{RAMP}	Combined output di/dt(1)				5	kA/s
Efficiency	Buck converter efficiency	$I_{LOADTOTAL}$ = 3 A, V_{TBT_IN} = 12 V		87%		
	Charge pump efficiency	V_{TBT_IN} = 3.3 V, $I_{LOADTOTAL}$ = 25 mA		47%		
POWER OUTPUT PINS (LOW VOLTAGE INPUT)(2)						
V_{TBT_IN}	TBT_IN Input voltage range		2.5	3.3	3.4	V
V_{TBT_OUT}	TBT_OUT Output voltage range(3)		3.135	3.25	3.4	V
I_{TBT_OUT}	TBT_OUT Load current(4)(5)	$\overline{RESET}$ high	5		50	mA
		$\overline{RESET}$ low			100	µA
POWER OUTPUT PINS (HIGH VOLTAGE INPUT)(6)						
V_{TBT_IN}	TBT_IN Input voltage range		10	12	15.75	V
V_{TBT_OUT}	TBT_OUT Output voltage range(3)	I_LOADTOTAL = 1 A to 3.5 A	3.221	3.27	3.319	V
		I_LOADTOTAL = 0.235 A to 3.5 A	3.221	3.27	3.42	
I_{TBT_OUT}	TBT_OUT Load current(4)		235		1000	mA
V_{CBL_OUT}	CBL_OUT Output voltage range(3)	ILIMIT = 0, I_{CBL_OUT} = 0 to 720 mA	3.171	3.27	3.319	V
		ILIMIT = 1, I_{CBL_OUT} = 0 to 1.44 A	3.12	3.27	3.319	
V_{DEV_OUT}	DEV_OUT Output Voltage Range	I_{DEV_OUT} = 0 to 2500 mA	3	3.27	3.319	V
POWER OUTPUT PINS (HIGH VOLTAGE INPUT DURING SYSTEM SLEEP)						
V_{TBT_IN}	TBT_IN Input voltage range		5.2	12	15.75	V
V_{TBT_OUT}	TBT_OUT DC Output voltage range	I_LOADTOTAL = 1 A to 3.5 A	3.221	3.27	3.319	V
		I_LOADTOTAL = 0.235 A to 3.5 A	3.221	3.27	3.42	
I_{TBT_OUT}	TBT_OUT Load current		5		31	mA
V_{CBL_OUT}	CBL_OUT Output voltage range(3)	I_{CBL_OUT} = 0 to 235 mA	3.171	3.27	3.319	V
V_{DEV_OUT}	DEV_OUT Output voltage range	I_{DEV_OUT} = 0 to 700 mA	3	3.3	3.319	V
CABLE OUTPUT (HIGH VOLTAGE INPUT & HIGH VOLTAGE INPUT DURING SLEEP)						
$V_{CBL\_OUT\_MON}$	CBL_OUT Ramp-up monotonicity(7)	CBL_OUT ramp from off to on			0	mV
$V_{CBL\_OUT\_RIP}$	CBL_OUT Voltage ripple	After settling All output combined Load > 1 mA			2	$\%_{P-P}$
		All output combined Load < 1 mA			40	$mV_{P=P}$
I_{LIM_CBLOUT}	CBL_OUT Current limit	ILIMIT = 0	0.8	1.1	1.4	A
		ILIMIT = 1	1.6	2.2	2.8	
t_{LIM_CBLOUT}	Short circuit response time	RCBL_OUT = 0.5 Ω to GND, ILIMIT = 0			500	µs
		RCBL_OUT = 0.01 Ω to GND, ILIMIT = 0			8	

(1) The three voltage outputs (TBT_OUT, CBL_OUT, DEV_OUT) all pull current from a single node. Therefore, the total combined current cannot exceed the maximum di/dt.
(2) CBL_OUT and DEV_OUT are open (high impedance) for this input voltage range.
(3) During light load conditions, the average output voltage may reach 3.5 V with peaks not exceeding 3.42 V.
(4) TBT_OUT load current flows from the TBT_OUT pin when the device is in charge pump mode and pulls the buck converter inductor when the device is in buck mode.
(5) TBT_OUT load current will not go higher than 50mA until after the device asserts HV_OK.
(6) The maximum current supplied by the TPS65980 to all outputs is limited to 3.5 A. Max power depends on the Thunderbolt™ system and how much power is supplied to the input.
(7) A monotonicity of 0 mV means that the output does not have a negative going ramp at anytime during its power up ramp. A ripple of up to 62 mV from the DC/DC will occur.

Electrical Characteristics (continued)

Unless otherwise noted all specifications applies over the V_{TBT_IN} range and operating ambient temperature of –40°C ≤ T_A ≤ 85°C, C_{TBT_IN} = 22 µF, C_{TBT_OUT} = 10 µF, C_{CBL_OUT} = 1 µF, CSS = 10 nF, and 33 V/µs logic input transitions. Typical values are for V_{TBT_IN} = 12 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{DEV\_EN}$ AND ILIMIT INPUT LOGIC						
V_{IH}	High-level input voltage		2.6			V
V_{IL}	Low-level input voltage				0.6	V
I_{IN}	Input leakage to GND	$V_{\overline{DEV\_EN}}$ = 3.3V			1	mA
$\overline{RESET}$ AND HV_OK OUTPUT LOGIC						
V_{OH}	High-level output voltage	I_L = –1.5 mA, Referenced to V_{TBT_OUT}	–250		0	mV
V_{OL}	Low-level output voltage	I_L = 1.5 mA	0		250	mV
SOFT START(8)						
I_{INRUSH}	Inrush current di/dt				250	kA/s
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature		120	135	150	°C
T_{SDHYST}	Shutdown hysteresis			10		°C

(8) The charge pump will limit the normal ramp of current. Soft start will control the inrush current when the input ramps from 0 V to high voltage (not a normal operating condition). See recommended components section for required soft-start cap.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
t_{IN2OR}	TBT_IN to TBT_OUT On Time	V_{TBT_IN} ≥ 0.9 × $V_{TBT\_IN(min)}$) to V_{TBT_OUT} ≥ 0.99 × $V_{TBT\_OUT(min)}$ R_{TBT_OUT} = 100 Ω			20	ms
t_{IN2OF}	TBT_IN to TBT_OUT Off Time	V_{TBT_IN} ≤ 0.9 × $V_{TBT\_IN(min)}$ to V_{TBT_OUT} ≤ 0.1 × $V_{TBT\_OUT(min)}$ R_{TBT_OUT} = 100 Ω		2.4	4	ms
t_{OUT2RR}	TBT_OUT to RESETZ High time	V_{TBT_OUT} ≥ $V_{REF\_RSTN(max)}$ rising to $V_{\overline{RESET}}$ = 0.9 × VOH, C_{RESETN} = 100 pF			20	µs
t_{IN2RF}	TBT_IN to RESETZ Low time	V_{TBT_IN} ≤ 0.9 × $V_{TBT\_IN(min)}$ to $V_{\overline{RESET}}$ = 0.1 × V_{OH}, C_{RESETN} = 100 pF			20	ms
t_{HV2OKR}	TBT_IN Rise to HV_OK	V_{TBT_IN} ≥ V_{HVTR} to V_{HV_OK} = 0.9 × V_{OH} C_{HV_OK} = 100 pF			10	µs
t_{HV2OKF}	TBT_IN Fall to HV_OK	V_{TBT_IN} ≤ V_{HVTR}-$V_{HVTHYST}$ to V_{HV_OK} = 0.1 × V_{OH}, C_{HV_OK} = 100 pF			10	µs
t_{HV2CR}(1)(2)	HV_OK to CBL_OUT On time	V_{HV_OK} ≥ 1.65 V to V_{CBL_OUT} = 2.95 V R_{CB_OUT} = 100 Ω, C_{HV_OK} = 100 pF	0.1		10	ms
t_{HV2CF}	HV_OK to CBL_OUT Off time	V_{HV_OK} ≤ 1.65 V to V_{CBL_OUT} = 2.95 V R_{CB_OUT} = 100 Ω, C_{HV_OK} = 100 pF			40	µs
t_{RCBL}	CABLE_OUT Ramp time	V_{CBL_OUT} ramp 10% to 90% C_{CBL_OUT} = 0 to 52 µF	0.1		10	ms
t_{DEVEN}	$\overline{DEV\_EN}$ to DEV_OUT On time	$V_{\overline{DEV\_EN}}$ ≤ 1.65 V to V_{DEV_OUT} = 2.7 V R_{DEV_OUT} = 100 Ω	0.1		10	ms
t_{DEVDIS}	$\overline{DEV\_EN}$ to DEV_OUT Off time	$V_{\overline{DEV\_EN}}$ ≥ 1.65V to V_{DEV_OUT} = 2.7 V RDEV_OUT = 100 Ω			50	ms
$t_{HV2DEVEN}$	Wait time from HV_OK High before $\overline{DEV\_EN}$ can be asserted low(2)	V_{HV_OK} ≥ 1.65 V to $V_{\overline{DEV\_EN}}$ ≤ 1.65 V C_{HV_OK} = 100 pF	2			ms

(1) TBT_IN must transition from 3.3 V to high voltage, not from 0 V to high voltage
(2) During the transition from low voltage input to high voltage input, the total load of all outputs combined can not exceed 85 mA until 2 ms after HV_OK asserts high.

7.7 Timing Diagrams

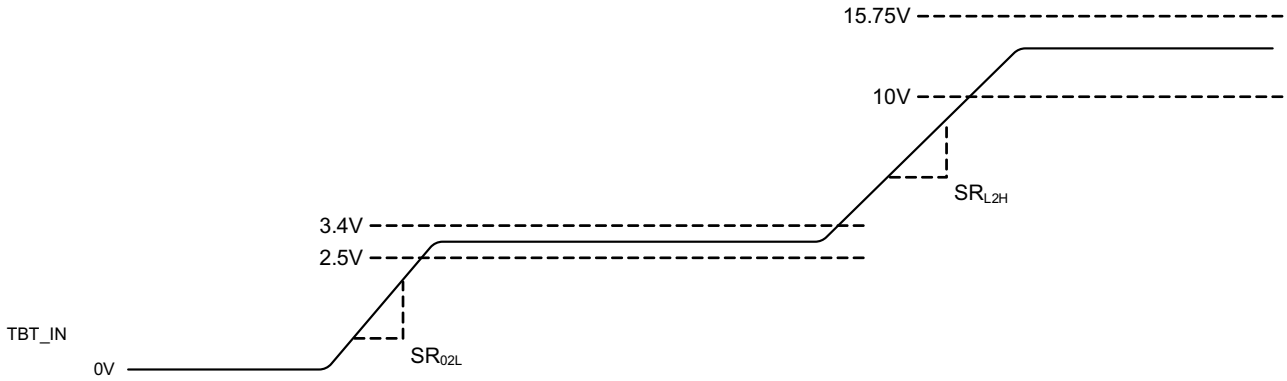


Figure 1. TBT_IN Slew Rates

The TPS65980 has two normal operating regions. The first region is when 2.5 V ≤ V_{TBT_IN} ≤ 3.4 V. This is the normal power-up state and is termed the low-voltage state. When the input transitions to this range, the input slew rate must meet the SR_{02L} limits. In this voltage range, the TPS65980 operates with a charge pump to generate the nominally 3.3 V output. When the input voltage moves to the higher end of this range, the buck converter takes over to produce the 3.3 V. In normal operation, the TPS65980 input voltage will transition from the low-voltage range to a high-voltage range where 10 V ≤ V_{TBT_IN} ≤ 15.75 V. This is the high-voltage state and is the state where the TPS65980 will operate most of the time. In this state, the device operates as a buck converter providing a nominally 3.3 V output. Figure 1 shows the input voltage transitions and states.

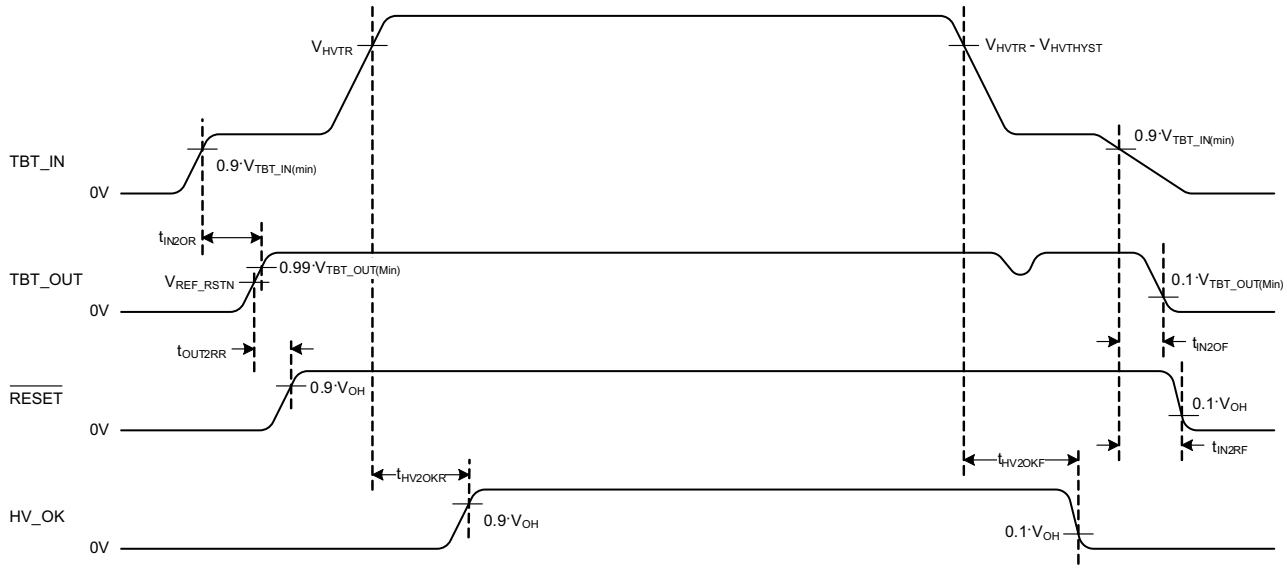


Figure 2. Timing Diagram

Figure 2 shows normal operating timing diagram for the TBT_OUT output voltage and the $\overline{RESET}$ and HV_OK output indicator signals. When TBT_IN transitions to the low-voltage range, TBT_OUT will power up a short time later. Once TBT_OUT reaches the normal output range, $\overline{RESET}$ will transition high. However, timing for $\overline{RESET}$ is measured from the input TBT_IN transitioning high. When TBT_IN transitions from the low-voltage input range to the high-voltage input range, HV_OK will transition high. $\overline{RESET}$ is an active-high output indicating that the TBT_OUT voltage is valid and. HV_OK is an active-high output indicating that the TBT_IN voltage is in the high-voltage range. When in the high-voltage state, the TPS65980 can provide much higher output current than when in the low-voltage state.

Timing Diagrams (continued)

When the TBT_IN input transitions from high-voltage to low-voltage, HV_OK will de-assert to a logic low. When the TBT_IN input voltage falls below the minimum operating voltage, the RESET output will de-assert low.

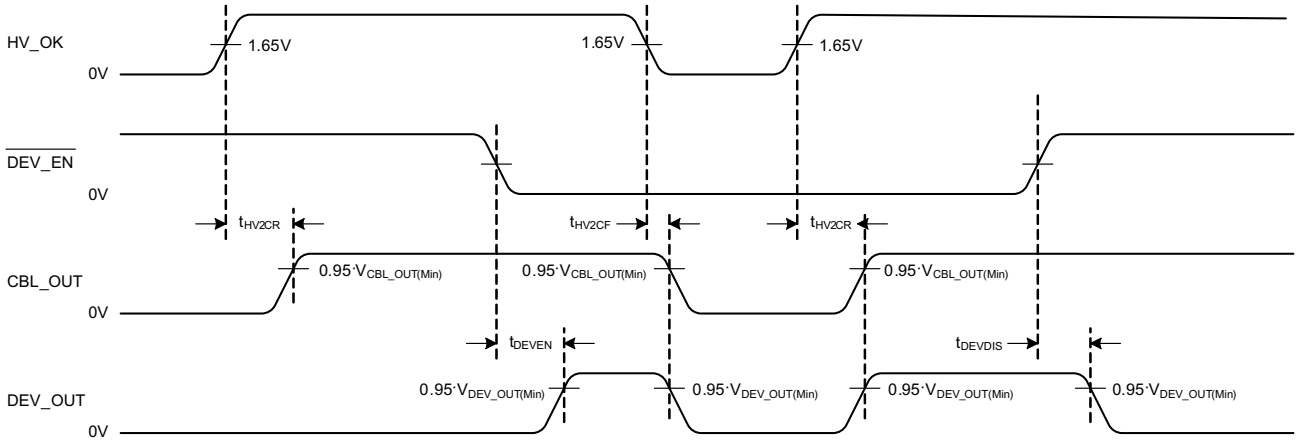


Figure 3. Timing Diagram

Figure 3 shows the CBL_OUT and DEV_OUT outputs and timing based on the HV_OK signal and the DEV_ENZ input. The CBL_OUT output will be connected to TBT_OUT and supplying 3.3V when HV_OK is asserting high. The DEV_OUT output will be connected to TBT_OUT and supplying 3.3 V when HV_OK is asserting high and the DEV_ENZ input is low.

7.8 Typical Characteristics

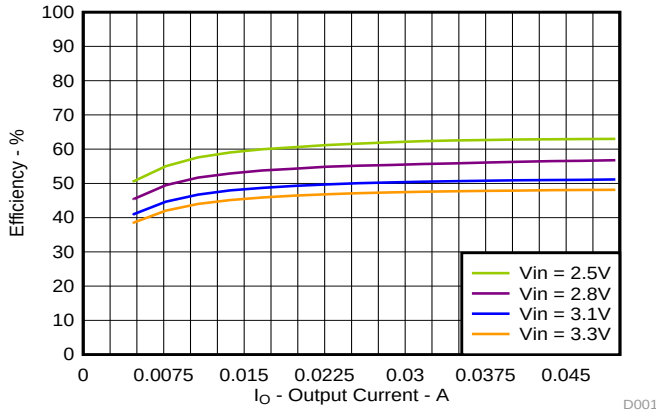


Figure 4. Low Voltage Efficiency

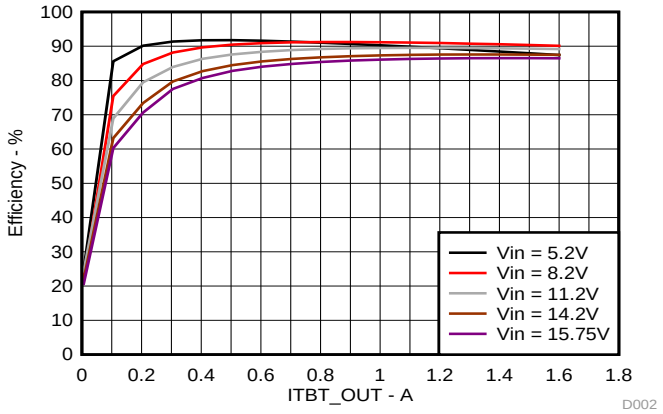


Figure 5. High Voltage Efficiency (System Sleep)

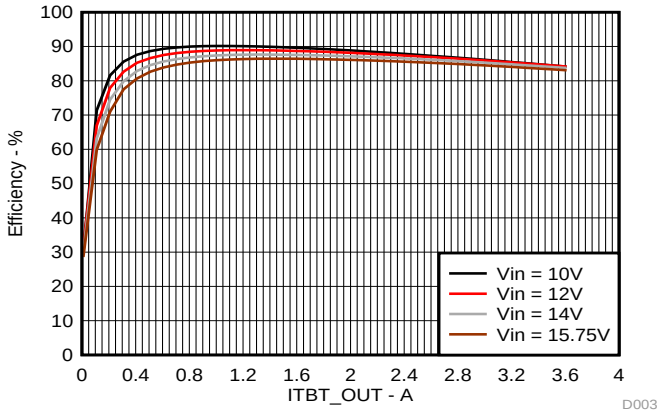


Figure 6. High Voltage Efficiency (Active)

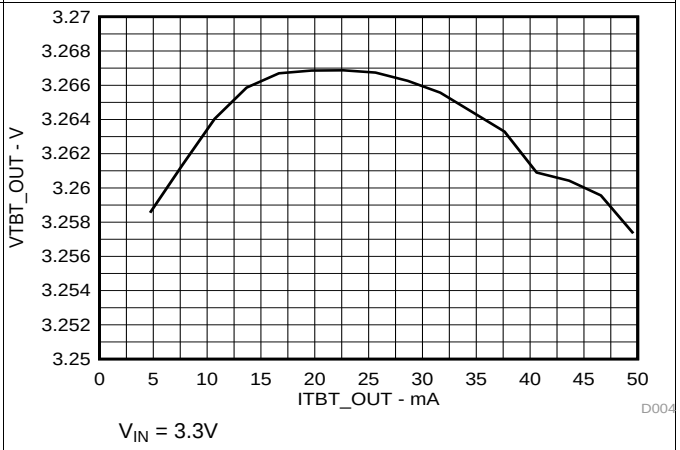


Figure 7. TBT_OUT Load Regulation

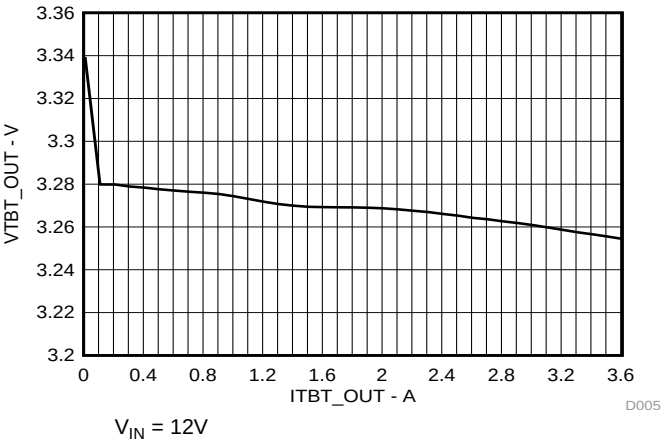


Figure 8. TBT_OUT Load Regulation

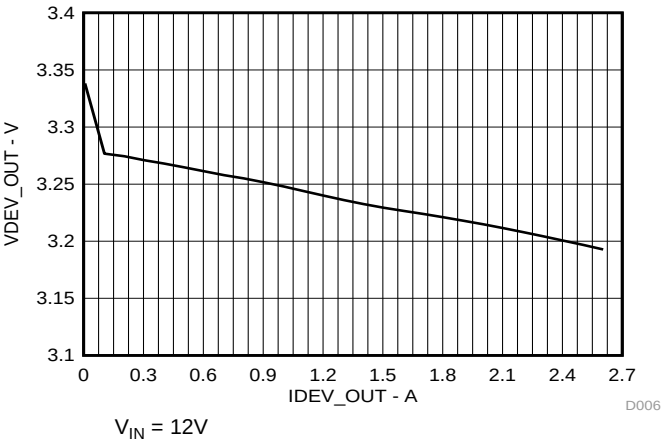


Figure 9. DEV_OUT Load Regulation

Typical Characteristics (continued)

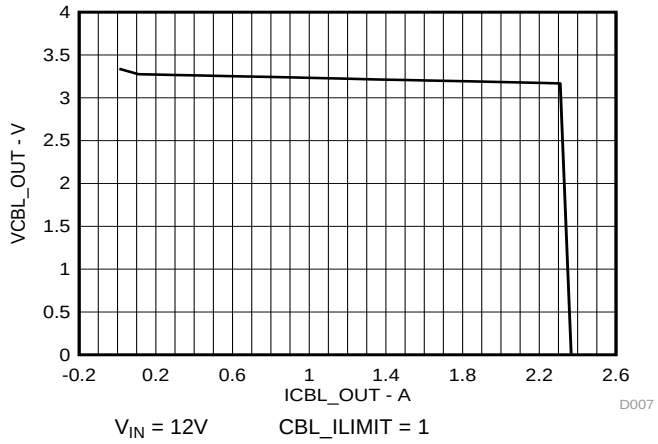


Figure 10. CBL_OUT Load Regulation

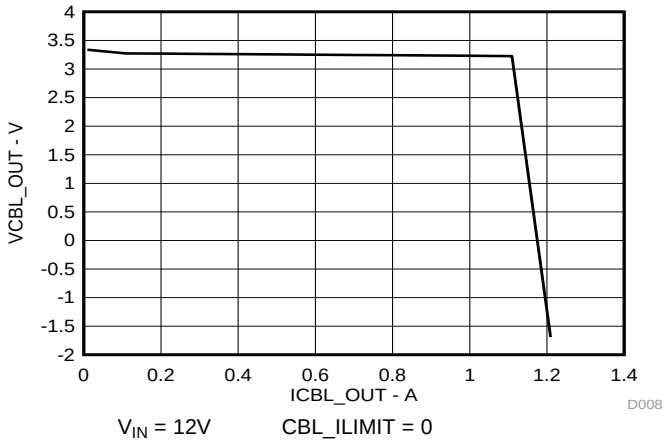


Figure 11. CBL_OUT Load Regulation

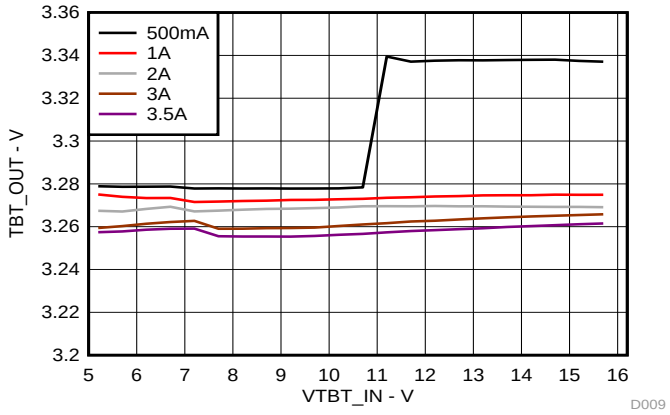


Figure 12. TBT_OUT Line Regulation

8 Detailed Description

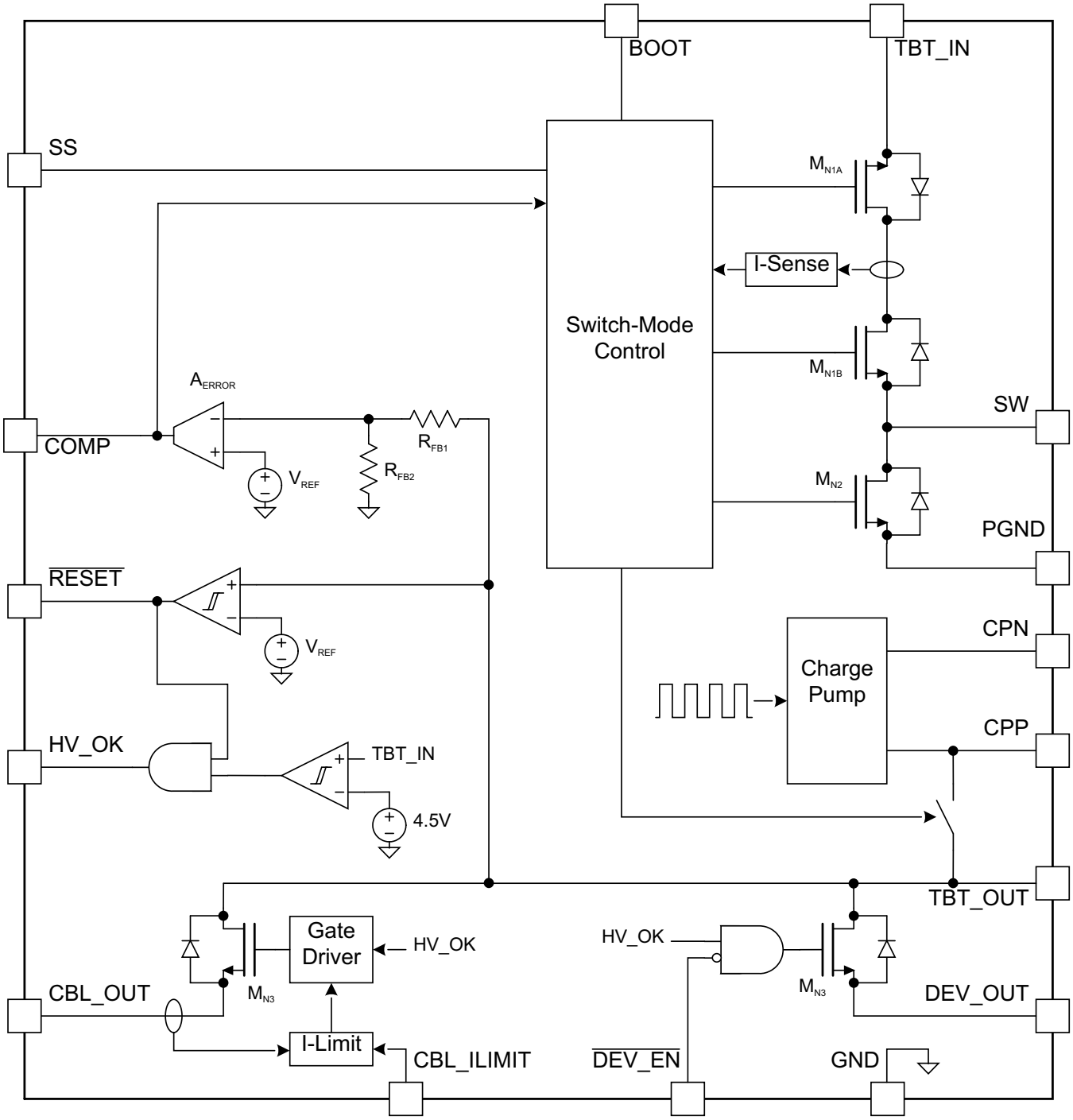
8.1 Overview

The TPS65980 is a switching regulator designed for Thunderbolt™ and Thunderbolt™ 2 bus-powered systems. The TPS65980 receives power from a Thunderbolt™ host in the range of 2.5 V to 15.75 V and produces three separate 3.3 V outputs. TBT_OUT is the main output from the regulator. This output is generated from a switched-cap charge pump when the input is in the low-voltage range. The output is generated from a switching buck converter when the input voltage is in the high-voltage range. The TBT_OUT output powers the local Thunderbolt™ controller and any additional Thunderbolt™ circuitry. Once in the input has settled in the high-voltage range, the other two outputs can be powered from the TBT_OUT output. When the TBT_OUT is supplying 3.3 V, the $\overline{\text{RESET}}$ output asserts high. When the TBT_OUT voltage is below the valid output range, $\overline{\text{RESET}}$ asserts low. When TBT_IN is in the high-voltage input range and $\overline{\text{RESET}}$ is asserting high (valid output), HV_OK will assert high indicating that high-voltage has been received.

The CBL_OUT output supplies power back to the Thunderbolt™ cable for powering the active cable circuitry. This output is connected to the TBT_OUT output with a FET switch and is current limited.

The CBL_ILIMIT logic input pin sets the current limit level. The DEV_OUT output provides power to all other circuitry in the system. This output is not current limited and is enabled/disabled by the $\overline{\text{DEV\_EN}}$ logic input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 2.5-V to 15.75-V Input

The TPS65980 is powered from a Thunderbolt™ Bus. This is typically an input to a port from Thunderbolt™ cable. This input will start at 3.3 V (2.5 V ≤ V_{TBT_IN} ≤ 3.4 V) until a link is established between a host and the peripheral device containing the TPS65980. Once the link is established, the voltage at the input can transition to a higher operating voltage (10 V ≤ V_{TBT_IN} ≤ 15.75 V).

8.3.2 3.3-V Outputs

The TPS65980 has three separate 3.3 V outputs. One output, TBT_OUT, is the output from the buck/boost and the other outputs, CBL_OUT and DEV_OUT, are outputs that through load switches from TBT_OUT.

The TBT_OUT supply provides power to the local peripheral Thunderbolt™ controller and support circuitry. The CBL_OUT supply provides power back to the Thunderbolt™ cable and has adjustable current limit. The DEV_OUT supply provides power to all other circuitry in the device to perform its designed function.

8.3.3 Thermal Shutdown

The TPS65980 as a thermal shutdown feature preventing the device from over heating during current limiting situations. The thermal shutdown occurs at a 135°C junction temperature typically. A 10°C hysteresis occurs before the thermal shutdown is cleared.

8.3.4 Cable Power Out Current Limit

The CBL_OUT output is current limited internally. The current limit has two values which are set by the CBL_ILIMIT logic input. When CBL_ILIMIT = 0, the current limit will bet set to 1.1 A typically. When CBL_ILIMIT = 1, the current limit will be set to 2.2 A typically.

8.4 Device Functional Modes

8.4.1 Operation with 2.5 V ≤ V_{TBT_IN} ≤ 3.4 V

The TPS65980 has two normal operating regions. The first region is when 2.5 V ≤ V_{TBT_IN} ≤ 3.4 V. This is the normal power-up state and is termed the low-voltage state. When the input transitions to this range, the input slew rate must meet the SR02L limits. In this voltage range, the TPS65980 operates with a charge pump to generate the nominally 3.3 V output. When the input voltage moves to the higher end of this range, the buck converter takes over to produce the 3.3 V.

8.4.2 Operation with 10 V ≤ V_{TBT_IN} ≤ 15.75 V

In normal operation, the TPS65980 input voltage will transition from the low-voltage range to a high-voltage range where 10 V ≤ V_{TBT_IN} ≤ 15.75 V. This is the high-voltage state and is the state where the TPS65980 will operate most of the time. In this state, the device operates as a buck converter providing a nominally 3.3 V output.

9 Application and Implementation

9.1 Application Information

The TPS65980 DC/DC switching regulator that receives power from a Thunderbolt™ or Thunderbolt™ 2 power bus ranging from 2.5 V to 15.75 V and generates three separate 3.3-V supply outputs.

9.2 Typical Application

9.2.1 Single-Port Bus-Powered Thunderbolt™ Device

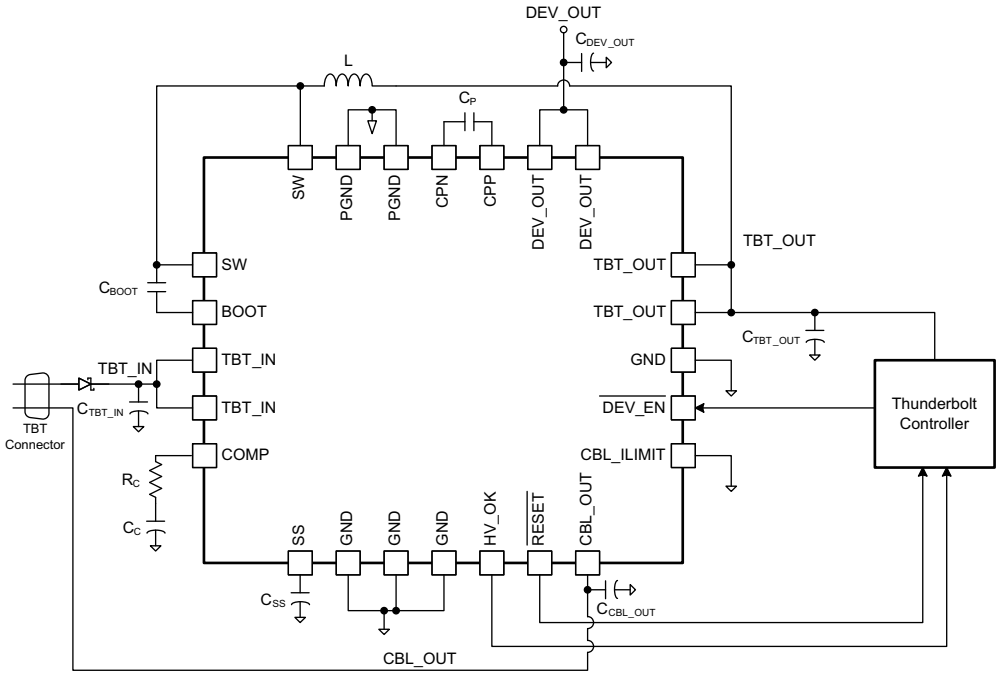


Figure 13. Typical Application (Single-Port Bus-Powered Thunderbolt™ Device)

9.2.1.1 Design Requirements

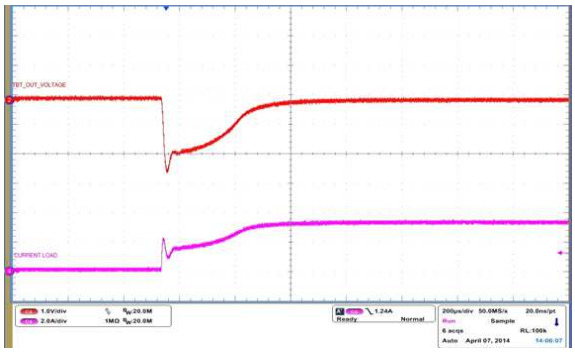
Table 1. Recommended Component Values

COMPONENT	DESCRIPTION	MIN	TYP	MAX	UNIT
C_{IN}	TBT_IN Input Capacitance	17.6	22	52	µF
C_{BOOT}	Converter Bootstrap Capacitance	8	10	12	nF
C_{CP}	Charge Pump Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_{SS}	Soft Start Capacitance	8	10	12	nF
C_{TBT}	TBT_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	16	20	24	µF
C_{CBL}	CBL_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_{DEV}	DEV_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_C	Compensation Capacitance	8	10	12	nF
R_C	Compensation Resistance	8	10	12	kΩ
L	Inductor SRR1280 (ESR ≤ 20 mΩ)	8	10	12	µH

9.2.1.2 Detailed Design Procedure

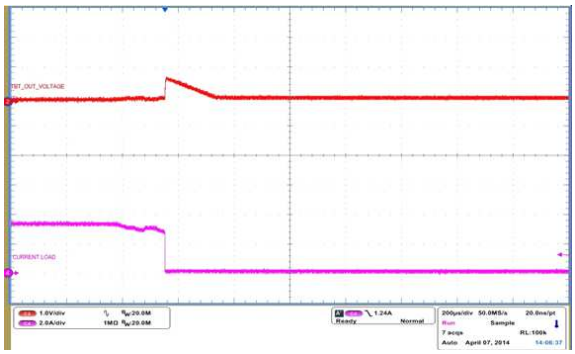
The TPS65980 should use the recommended component values in Table 1. The device is designed to fit the needs of a Thunderbolt™ bus powered peripheral and the recommended component values are chosen to satisfy those conditions. The input capacitance C_{IN} can be as high as 52 µF, but this maximum capacitance must include all capacitances seen at the input to the Thunderbolt™ port.

9.2.1.3 Application Performance Plots



C_{TBT_OUT} = 10 µF V_{TBT_IN} = 12 V

Figure 14. TBT_OUT Load Transient Response (0.5A to 3.5A Step)



C_{TBT_OUT} = 10 µF V_{TBT_IN} = 12 V

Figure 15. TBT_OUT Load Transient Response (3.5A to 0.5A Step)

Figure 16. 0V to 3.3V Power Up With 50mA Load

Figure 17. 3.3V to 0V Power Down With 50mA Load

Figure 18. 3.3V to 15.75V Vin Step With 50mA Load

Figure 19. 15.75 to 3.3V Vin Step With 50mA Load

CBL_ILIMIT = 0

Figure 20. Short Circuit Current Limit Response

CBL_ILIMIT = 1

Figure 21. Short Circuit Current Limit Response

9.2.2 Dual-Port Bus-Powered Thunderbolt™ Device

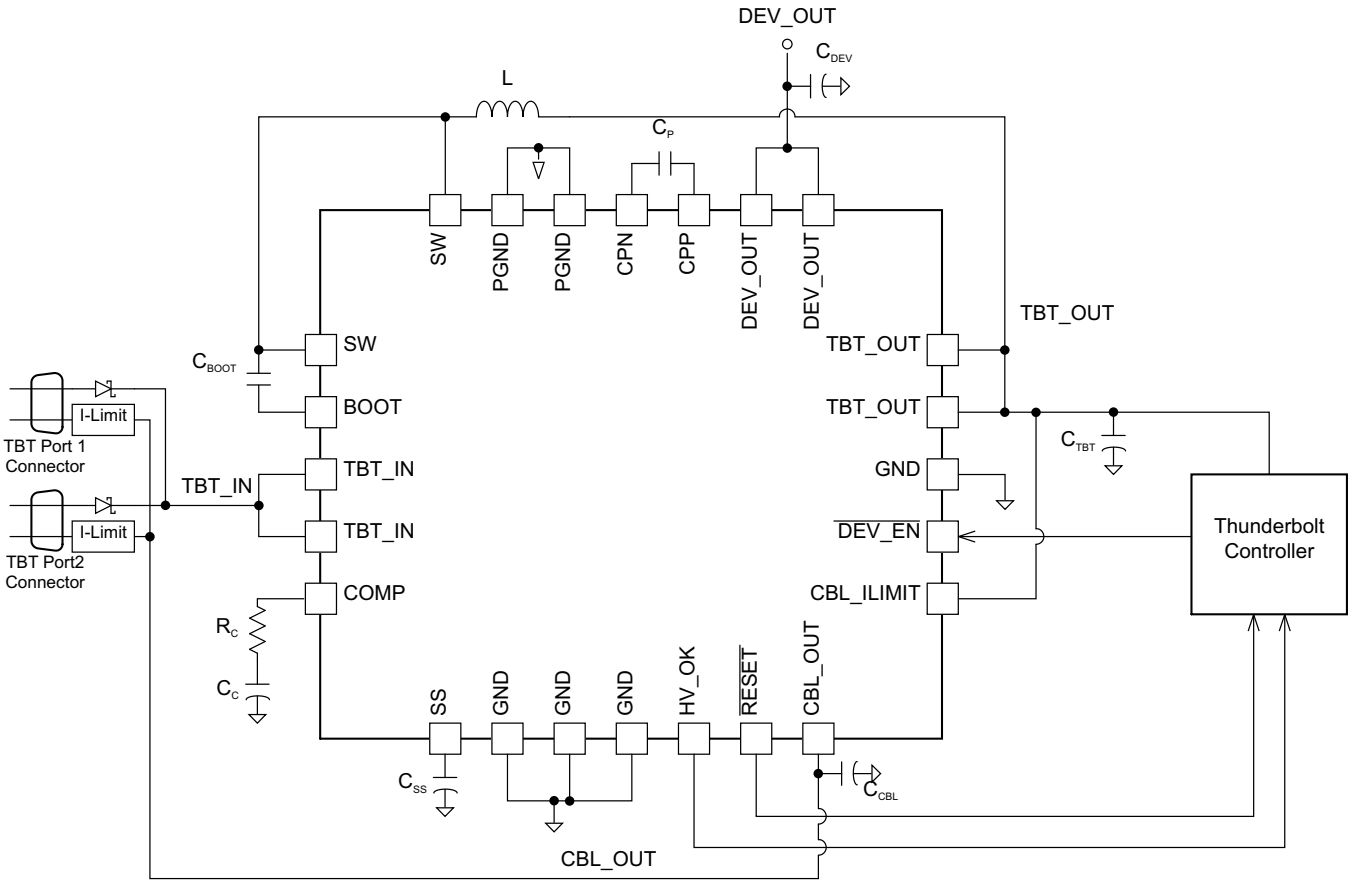


Figure 22. Typical Application (Dual-Port Bus-Powered Thunderbolt™ Device)

9.2.2.1 Design Requirements

In a dual-port application, the TBT_IN input voltage will be selected from either port. A simple diode-or function will produce TBT_IN from the higher of the two inputs. The diode-or selection will allow the high-voltage supply to be at TBT_IN.

In a dual port system, the TPS65980 must provide cable power to both ports. In this case, a second current limiting device (TPS22920) connected between TBT_OUT and the port is recommended. The CBL_OUT pin can also supply current to both ports. In this case, tying CBL_ILIMIT to TBT_OUT will double the amount of current that can be supplied before current limiting. When using this method, the voltage drop to the CBL_OUT pin will increase and care must be taken that other systems resistance do not cause the cable voltage to drop below the allowed pin voltage specified in the Thunderbolt™ specification. To avoid issues with voltage drop in the system, it is recommended that the second port be powered from TBT_OUT as shown in Figure 22. This relieves the voltage drop due to extra current through the CBL_OUT load switch.

Table 2. Recommended Component Values

COMPONENT	DESCRIPTION	MIN	TYP	MAX	UNIT
C_{IN}	TBT_IN Input Capacitance	17.6	22	52	µF
C_{BOOT}	Converter Bootstrap Capacitance	8	10	12	nF
C_{CP}	Charge Pump Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_{SS}	Soft Start Capacitance	8	10	12	nF
C_{TBT}	TBT_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	16	20	24	µF
C_{CBL}	CBL_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_{DEV}	DEV_OUT Output Capacitance (ceramic with ESR ≤ 10 mΩ)	0.8	1	1.2	µF
C_C	Compensation Capacitance	8	10	12	nF
R_C	Compensation Resistance	8	10	12	kΩ
L	Inductor SRR1280 (ESR ≤ 20 mΩ)	8	10	12	µH

9.2.2.2 Detailed Design Procedure

Refer to Detailed Design Procedure in the Single-Port Bus-Powered Thunderbolt™ Device section.

9.2.2.3 Application Performance Plots

Refer to Application Performance Plots in the Single-Port Bus-Powered Thunderbolt™ Device section.

10 Power Supply Recommendations

The TPS65980 is designed to operate from a Thunderbolt™ bus. The input will range from 2.5 V to 15.75 V. The input should be placed as near to the port connector as possible.

11 Layout

11.1 Layout Guidelines

Proper placement and routing will maximize the performance of the TPS65980. Follow Figure 23 for optimized layout and routing (hashed planes indicate bottom layer).

11.2 Layout Example

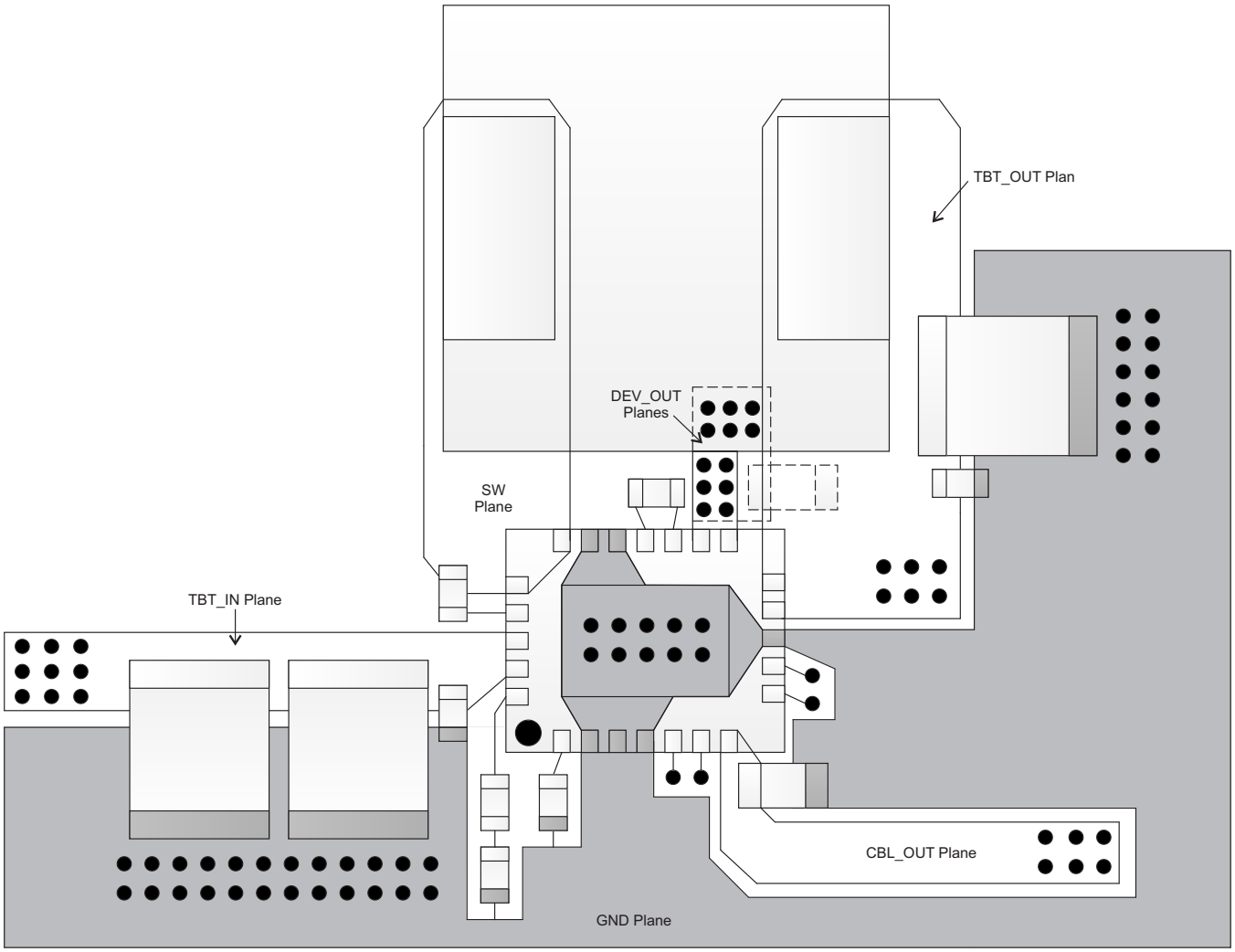


Figure 23. Top View Board Layout

Layout Example (continued)

For TBT_IN, the input capacitors must be placed close to the device with an inductance less than 1nH from input capacitors to the TBT_IN pins. Layout tools and calculators are available to approximate the inductance. The input capacitors must have their GND side area via stitched to the GND plane. The GND side of the input cap should also share the same polygon as the PGND/PowerPad on the top layer. PowerPad should be connected to the GND plane through multiple vias.

Inductor placement should be above the TPS65980, slightly to the left of the device. The SW pins to the inductor must be connected though a plane as shown in Figure 23. The TBT_OUT pins also have to be connected to the other side of the inductor with a plane. This plane should be wide to overlap the output capacitors. The GND side of the output capacitors should be stitched to the GND plane.

The CBL_OUT output capacitor should be placed close to the device on the top layer with an inductance less than 1 nH from the capacitor to the CBL_OUT pin. The DEV_OUT capacitor is best placed on the bottom side of the board with two planes (top and bottom) connect through a set of vias. The number of vias placed should be able to carry at least 3 A (DEV_OUT = 2.5 A max) for margin and inductance path less than 1nH from DEV_OUT pins to capacitor. When routing DEV_OUT to an internal power plane, follow Figure 24 for via paths.

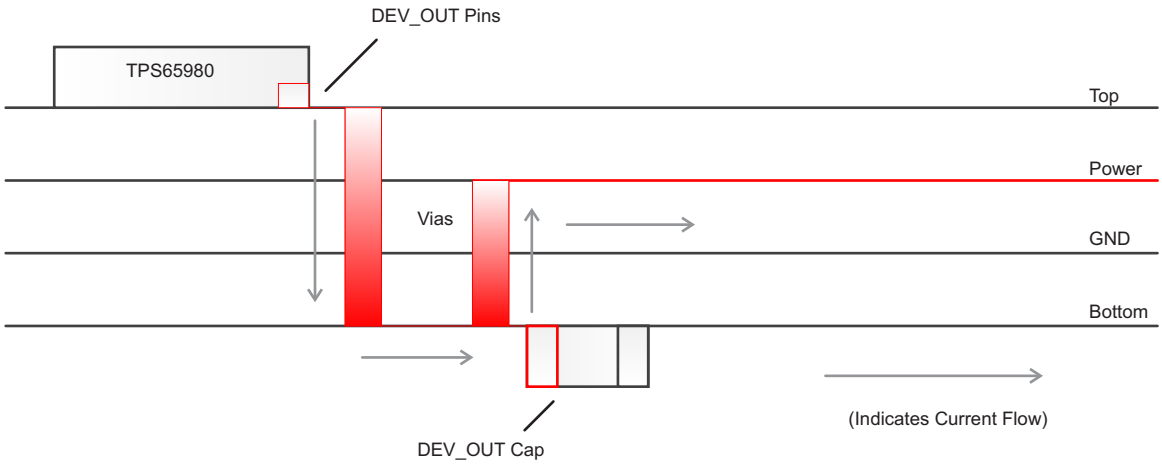


Figure 24. DEV_OUT Recommended Routing

The charge pump capacitor must be placed on the top layer close to the CPP and CPN pins. The inductance paths from capacitor to the pins must be less than 1 nH. SS and Compensation components should be placed on the top layer close to the device.

12 器件和文档支持

12.1 Trademarks

Thunderbolt is a trademark of Intel Corporation.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65980RHFR	ACTIVE	VQFN	RHF	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65980	Samples
TPS65980RHFT	ACTIVE	VQFN	RHF	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65980	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

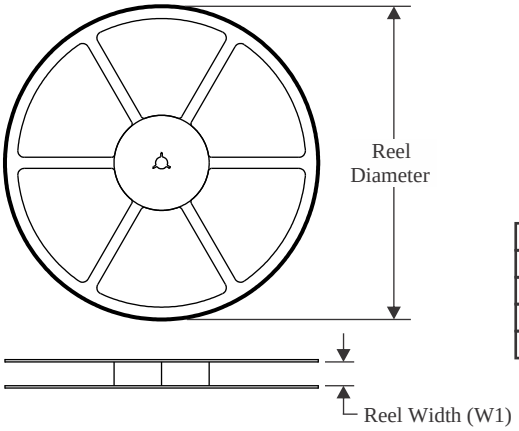
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

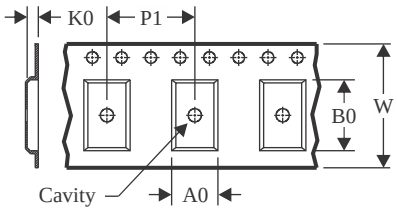
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

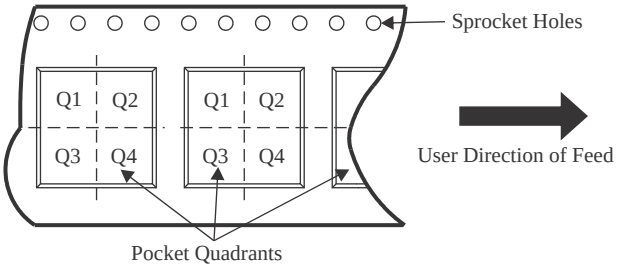


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

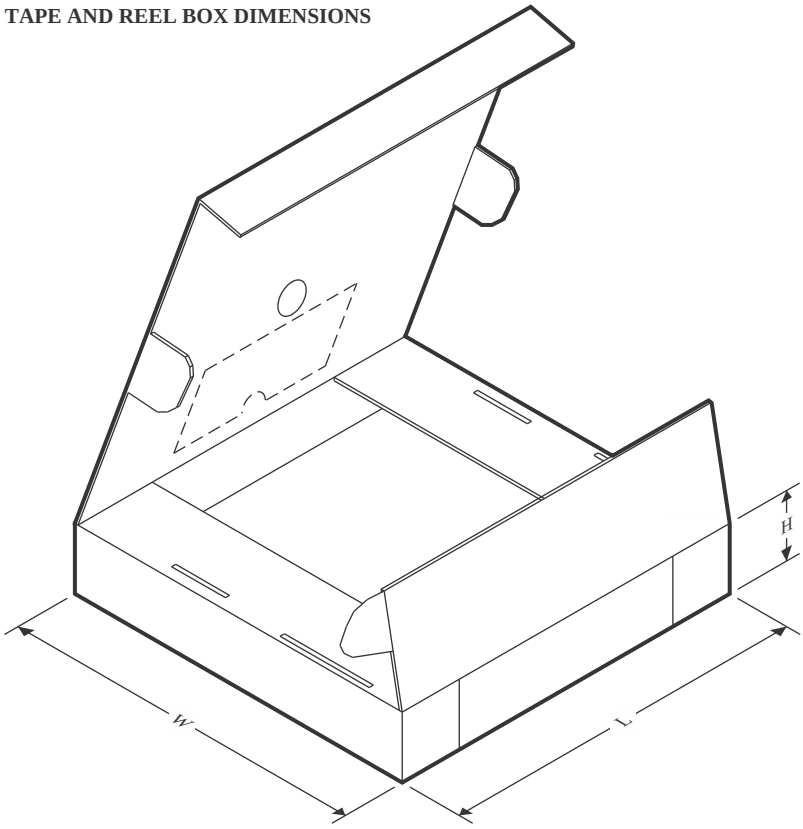
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65980RHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
TPS65980RHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

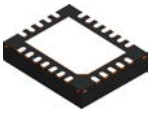
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65980RHFR	VQFN	RHF	24	3000	346.0	346.0	33.0
TPS65980RHFT	VQFN	RHF	24	250	210.0	185.0	35.0

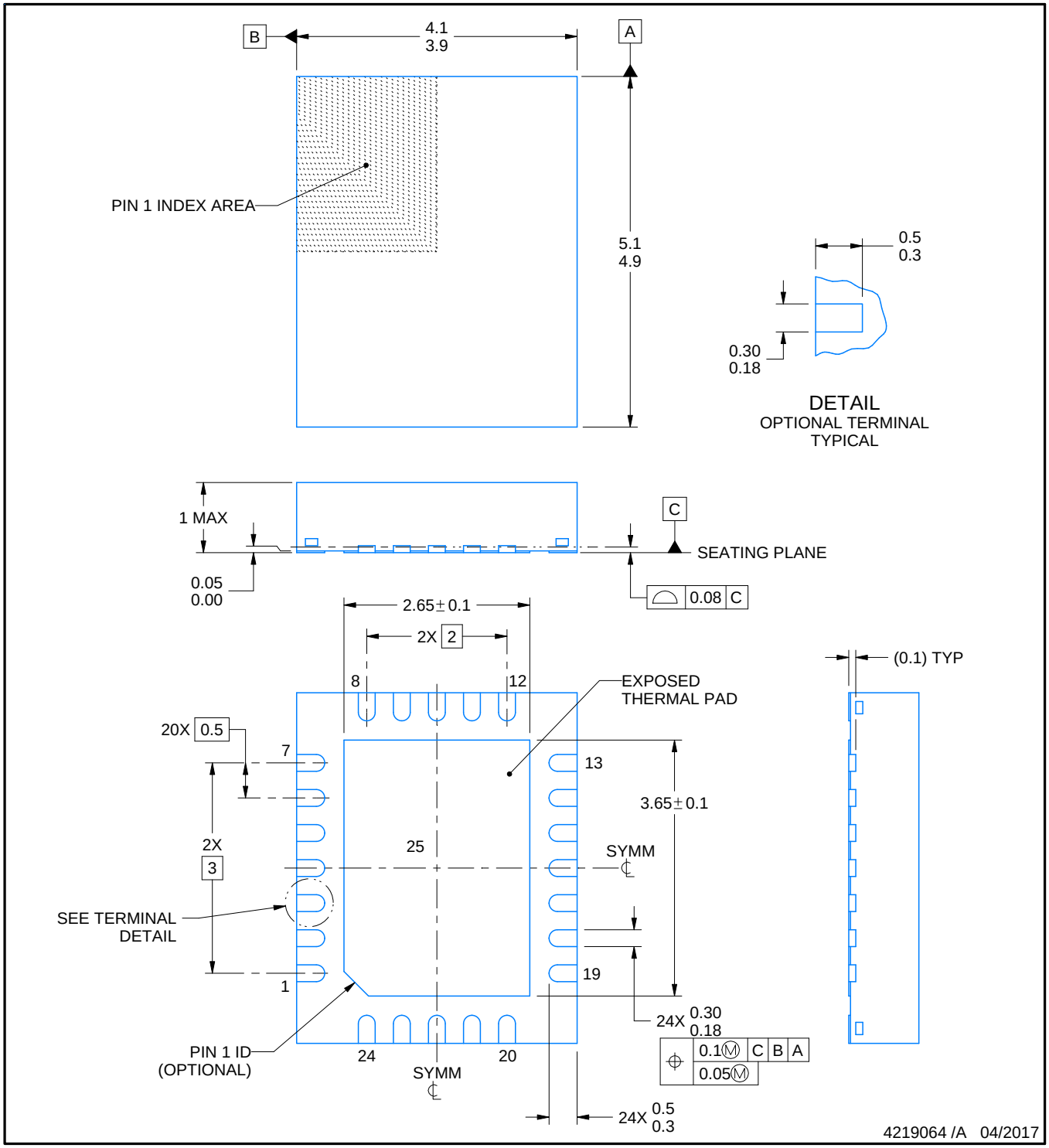
RHF0024A



PACKAGE OUTLINE

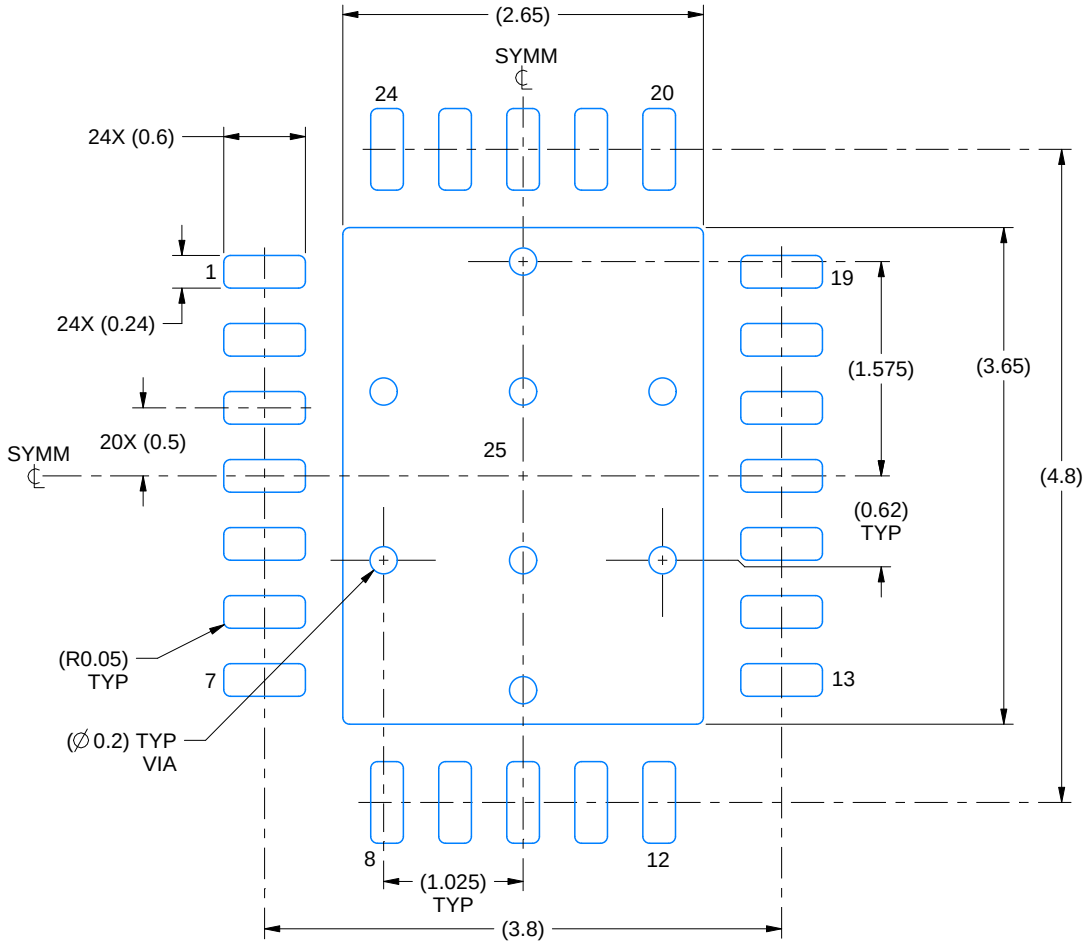
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

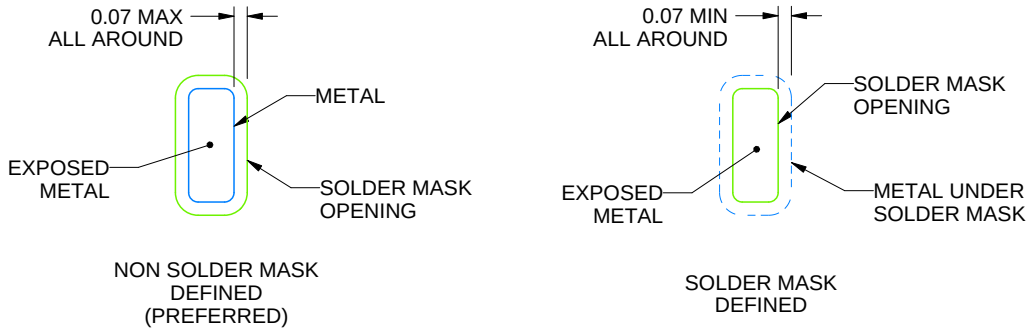


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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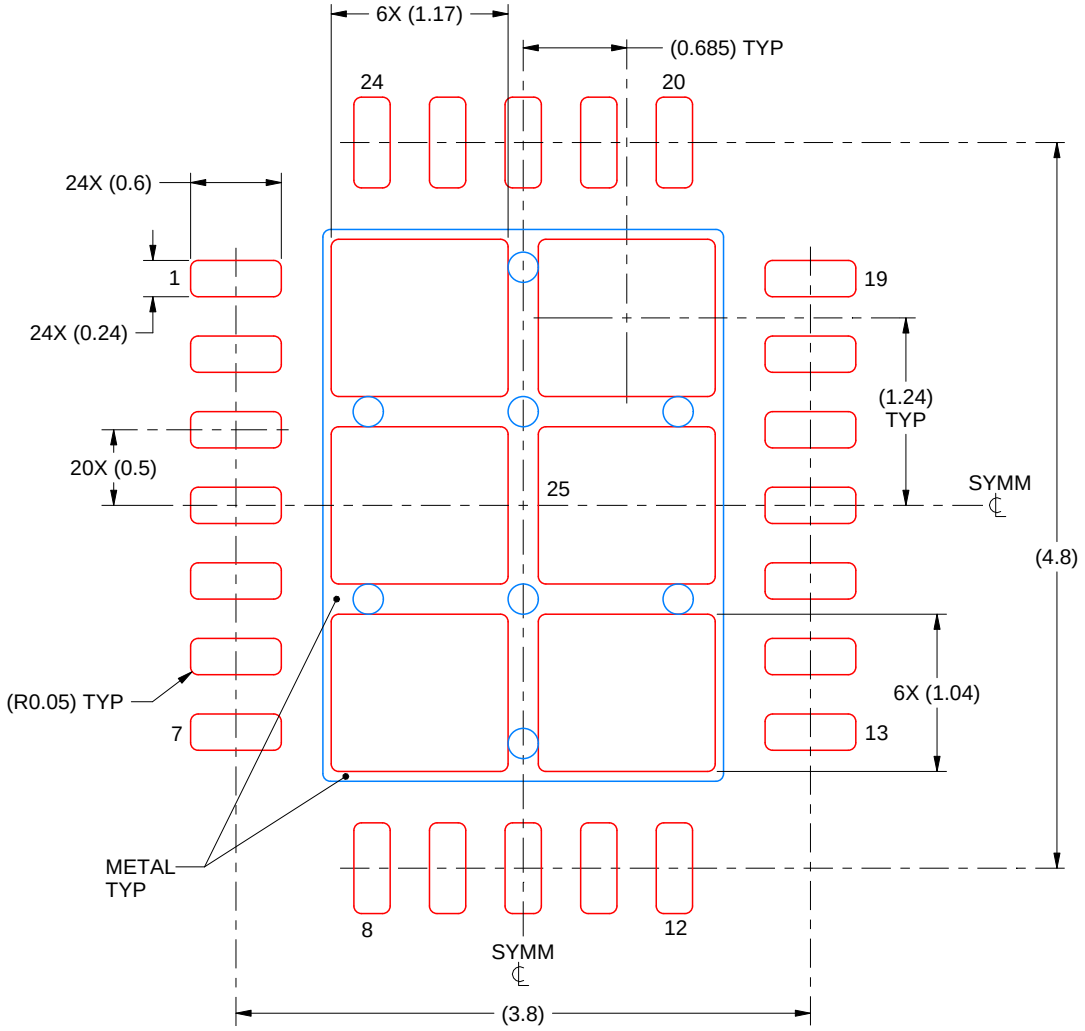
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219064 /A 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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