TPS748A-Q1 具有可编程软启动功能的汽车类 1.5A 低压降线性稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C ≤ T_A ≤ +125°C
  - HBM ESD 分类等级 2
  - CDM ESD 分类等级 C4A
- 扩展结温 (T_J) 范围：
  - –40°C 至 +150°C
- 输入电压范围：
  - IN: V_{IN} + V_{DO} 至 6.0V
  - BIAS：V_{OUT} + $V_{DO(BIAS)}$ 至 6.0V
- V_{OUT} 范围：0.8V 至 3.6V
- 低压降：1.5A、V_{BIAS} = 5V 下的典型值为 60mV
- 电源正常 (PG) 输出可实现电源监视或为其他电源提供时序信号
- 线路、负载和温度范围内的精度为 2%
- 可编程软启动可提供线性电压启动
- V_{BIAS} 支持低 V_{IN} 运行，具有良好的瞬态响应
- 与 ≥ 2.2 µF 的任何输出电容器一起工作时可保持稳定
- 采用小型 3mm × 3mm × 1mm VSON-10 封装

2 应用

- 远程信息处理控制单元
- 信息娱乐系统与仪表组
- 成像雷达

3 说明

TPS748A-Q1 低压降 (LDO) 线性稳压器可面向多种应用提供易于使用的稳健型电源管理解决方案。用户可编程软启动通过减少启动时的电容涌入电流，最大限度地减少了输入电源上的应力。软启动具有单调性，旨在为各类处理器和专用集成电路 (ASIC) 供电。借助使能输入和电源正常输出，可通过外部稳压器轻松实现上电排序。凭借全方位的灵活性，该器件可为现场可编程门阵列 (FPGA)、数字信号处理器 (DSP) 和其他具有特殊启动要求的应用配置可满足其时序要求的解决方案。

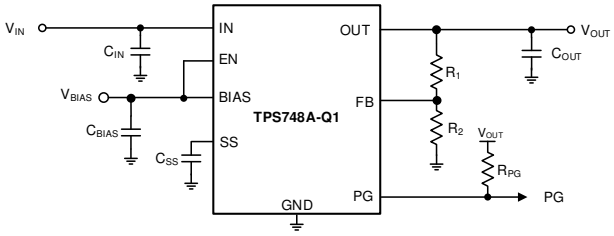
该器件还具有高精度的参考电压电路和误差放大器，可在整个负载、线路、温度和过程范围内提供 2% 精度。该器件在使用大于或等于 2.2 µF 的任何类型的电容器时都能保持稳定运行，并具有 T_J = –40°C 至 +150°C 的额定结温范围。TPS748A-Q1 采用小型 3mm × 3mm VSON-10 封装，可实现高度紧凑的解决方案总尺寸。

封装信息

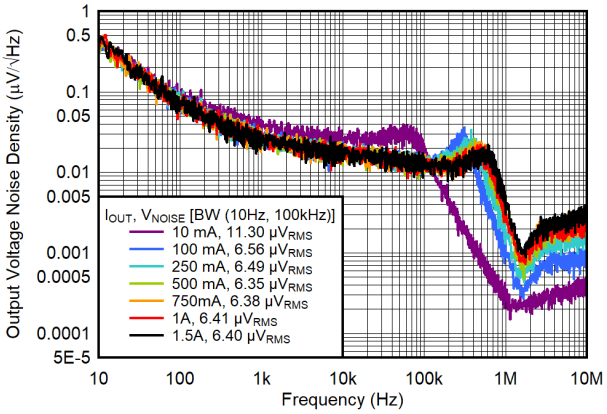
器件型号	封装(1)	封装尺寸(2)
TPS748A-Q1	DRC（VSON，10）	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用电路（可调节）



输出电压噪声密度与频率间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2022) to Revision A (May 2023)	Page
• 将文档状态从*预告信息*更改为*量产数据*	1

5 Pin Configuration and Functions

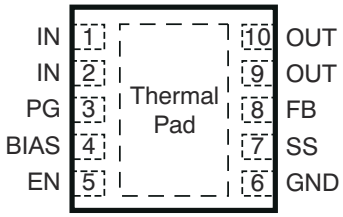


图 5-1. DRC Package, 10-Pin VSON With Thermal Pad (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	VSON		
BIAS	4	I	Bias input voltage for the error amplifier, reference, and internal control circuits. Use a 1-µF or larger input capacitor for optimal performance. If IN is connected to BIAS, a 4.7-µF or larger capacitor must be used.
EN	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
FB	8	I	Feedback pin. This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	6	—	Ground
IN	1, 2	I	Input to the device. Use a 1-µF or larger input capacitor for optimal performance.
NC	N/A	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	9, 10	O	Regulated output voltage. A small capacitor (total typical capacitance ⩾ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
PG	3	O	Power-good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. Connect a pullup resistor (10 kΩ to 1 MΩ) from this pin to a supply of up to 6.0 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
SS	7	—	Soft-start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 µs.
Thermal pad		—	Must be soldered to the ground plane for increased thermal performance. Internally connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, BIAS	–0.3	6.5	V
	EN	–0.3	6.5	
	PG	–0.3	6.5	
	SS	–0.3	6.5	
	FB	–0.3	V_{BIAS}	
	OUT	–0.3	V_{IN} + 0.3	
Current	PG	0	1.5	mA
	OUT	Internally limited		
	Output short-circuit duration	Indefinite		
	Continuous total power dissipation, P_{DISS}	See Thermal Information		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC specification Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	VOUT + 0.3	6.0	V
V_{EN}	Enable supply voltage		V_{IN}	6.0	V
V_{BIAS}	BIAS supply voltage	V_{OUT} + V_{DO} (VBIAS)(1)	V_{OUT} + 1.6(1)	6.0	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor (3)	10			µF
C_{IN}	Input capacitor (1) (2)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
C_{SS}	Soft-start capacitor	1	10	100	nF
T_J	Operating junction temperature	–40		150	℃

(1) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.
(3) A maximum capacitor derating of 25% is considered for minimum capacitance

6.4 Thermal Information

THERMAL METRIC(1)		TPS748A-Q1 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{SS} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V (4), and T_J = –40°C to 150°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		6.0	V
V_{BIAS}	BIAS pin voltage range		2.7		6.0	V
V_{REF}	Internal reference (Adj.)	T_A = +25°C	0.796	0.8	0.804	V
$V_{BIAS(UVLO)}$	Rising bias supply UVLO		1.0	1.25	1.75	V
$V_{BIAS(UVLO),HYST}$	Bias supply UVLO hysteresis		20	43	65	mV
ΔV_{OUT} (ΔVIN)	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A	V_{REF}		3.6	V
	Accuracy (1) (5)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 1.5 A	–1.25	±0.5	1.25	%
ΔV_{OUT} (ΔIOUT)	Line regulation	$V_{OUT(nom)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.03		%/V
V_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 1.5 A		0.09		%/A
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT(nom)}$ ≥ 3.25 V(3)		75	150	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}		1.14	1.35	V
I_{CL}	Output current limit	V_{OUT} = 80% × $V_{OUT(nom)}$	2.3		3.1	A
I_{BIAS}	BIAS pin current	I_{OUT} = 50 mA		0.67	1.1	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 1.1 V, V_{OUT} = 0.8 V		0.9	15	µA
I_{FB}	Feedback pin current		–0.22	±0.12	0.22	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{OUT} = 0.8 V		69		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{OUT} = 0.8 V		30		dB
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{OUT} = 0.8 V		59		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.1 V, V_{OUT} = 0.8 V		33		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 1 nF		7		µVrms x Vout
t_{STR}	Minimum startup time	R_{LOAD} for I_{OUT} = 1.0 A, C_{SS} = open		170		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		7.5		µA
t_{SS}	Soft-start time	Css = 10 nF		1.2		ms
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis			55		mV

6.5 Electrical Characteristics (continued)

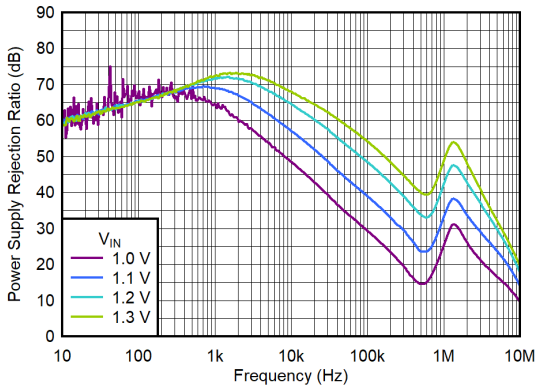
At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 μF, C_{IN} = C_{OUT} = 10 μF, C_{SS} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V (4), and T_J = –40°C to 150°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EN(dg)}$	Enable pin deglitch time			17		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	0.3	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	%V_{OUT}
V_{HYS}	PG trip hysteresis			2.5		%V_{OUT}
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.125	V
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.01	0.1	μA
T_J	Operating junction temperature		–40		125	℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		℃
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) 3.25 V is a test condition of this device and can be adjusted by referring to Figure 12.
(4) V_{BIAS} = $V_{DO\_MAX(BIAS)}$ + V_{OUT} for V_{OUT} ≥ 3.4 V
(5) The device is not tested under conditions where V_{IN} > V_{OUT} + 1.65 V and I_{OUT} = 1.5 A, because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test.

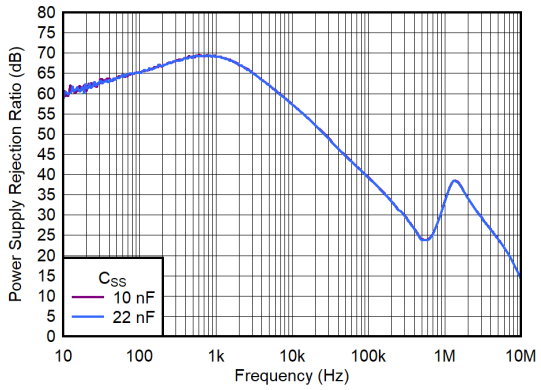
6.6 Typical Characteristics: I_{OUT} = 50 mA

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



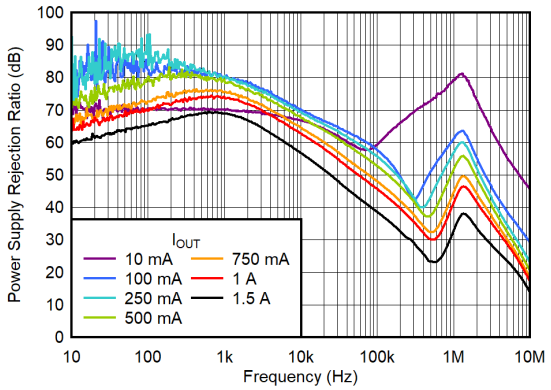
V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{EN} = V_{BIAS} = 6 V

图 6-1. IN PSRR vs Frequency and V_{IN}



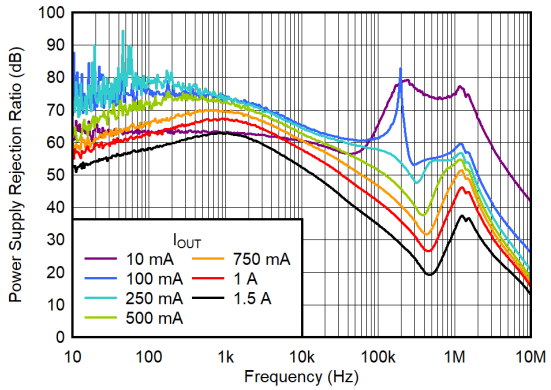
V_{IN} = 1.1 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, V_{EN} = V_{BIAS} = 6 V

图 6-2. IN PSRR vs Frequency and C_{SS}



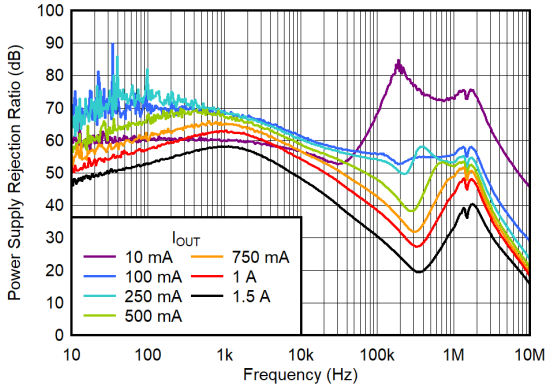
V_{IN} = 1.1 V, V_{OUT} = 0.8 V, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{EN} = V_{BIAS} = 6 V

图 6-3. IN PSRR vs Frequency and I_{OUT} for V_{OUT} = 0.8 V



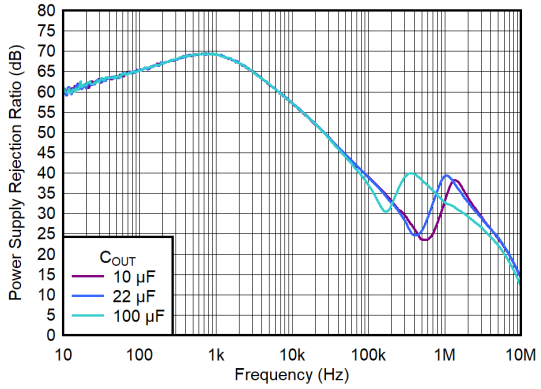
V_{IN} = 2.1 V, V_{OUT} = 1.8 V, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{EN} = V_{BIAS} = 6 V

图 6-4. PSRR vs Frequency and I_{OUT} for V_{OUT} = 1.8 V



V_{IN} = 3.6 V, V_{OUT} = 3.3 V, C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{EN} = V_{BIAS} = 6 V

图 6-5. IN PSRR vs Frequency and I_{OUT} for V_{OUT} = 3.3 V

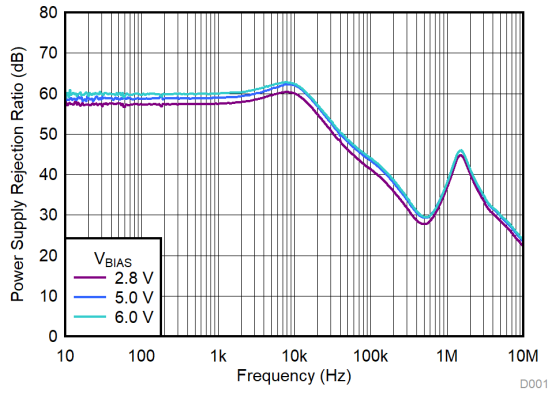


V_{IN} = 1.1 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{BIAS} = 0.1 µF, C_{SS} = 10 nF, V_{EN} = V_{BIAS} = 6 V

图 6-6. IN PSRR vs Frequency and C_{OUT}

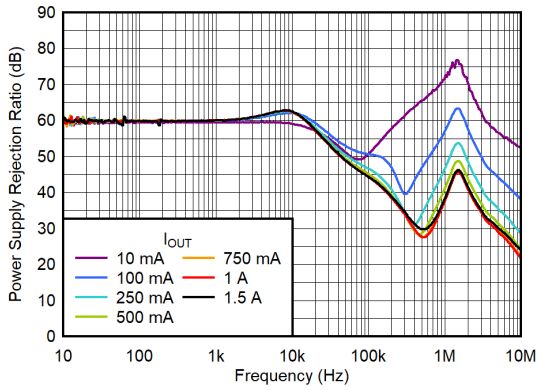
6.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



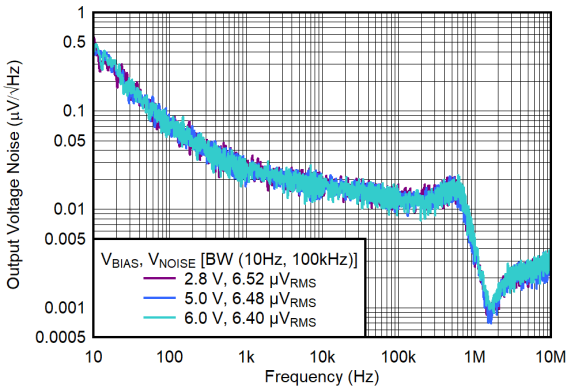
V_{IN} = 1.1 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{EN} = 6 V

图 6-7. BIAS PSRR vs Frequency and V_{BIAS}



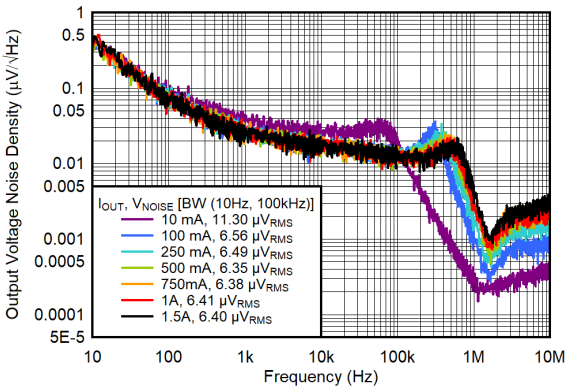
V_{EN} = V_{IN} = 1.1 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, V_{BIAS} = 6 V

图 6-8. BIAS PSRR vs Frequency and I_{OUT}



V_{EN} = V_{BIAS}, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, I_{OUT} = 1.5 A, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{BIAS} = 0.1 µF

图 6-9. Output Voltage Noise Density vs Frequency and V_{BIAS}

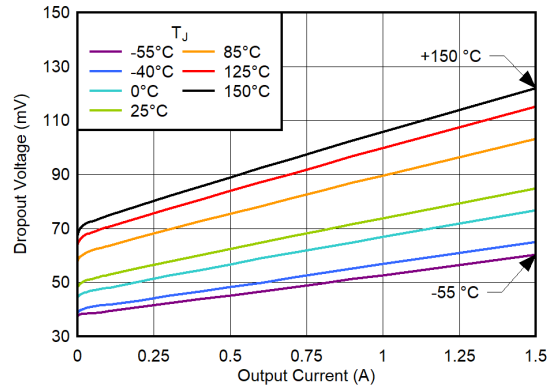


V_{EN} = V_{BIAS}, V_{IN} = 1.1 V, V_{OUT} = 0.8 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 10 nF, C_{BIAS} = 0.1 µF

图 6-10. Output Voltage Noise Density vs Frequency and I_{OUT}

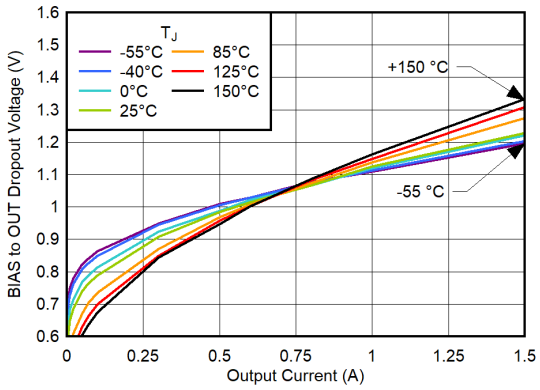
6.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)



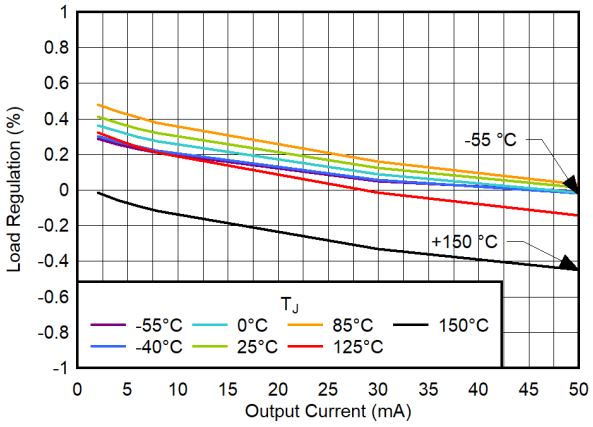
V_{BIAS} = 5 V, V_{OUT} = 0.8 V

图 6-11. IN-to-OUT Dropout Voltage vs I_{OUT} and Temperature (T_J)



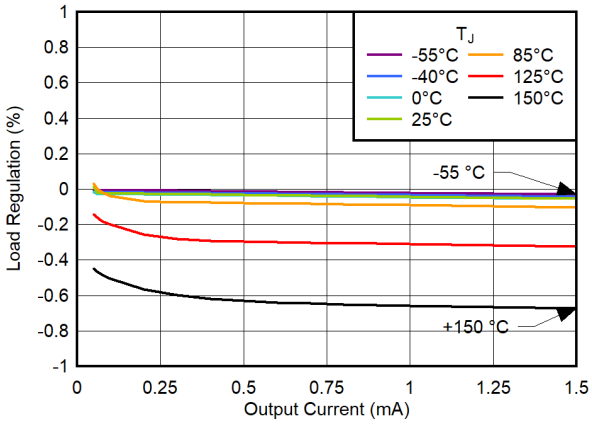
V_{IN} = 1.1 V, V_{OUT} = 0.8 V

图 6-12. BIAS-to-OUT Dropout Voltage vs I_{OUT} and Temperature (T_J)



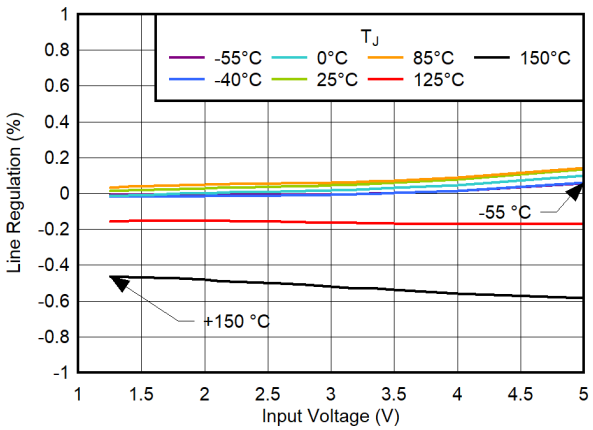
V_{IN} = 1.1 V, V_{BIAS} = 5 V, V_{OUT} = 0.8 V

图 6-13. Load Regulation vs 0-mA to 50-mA Output Current



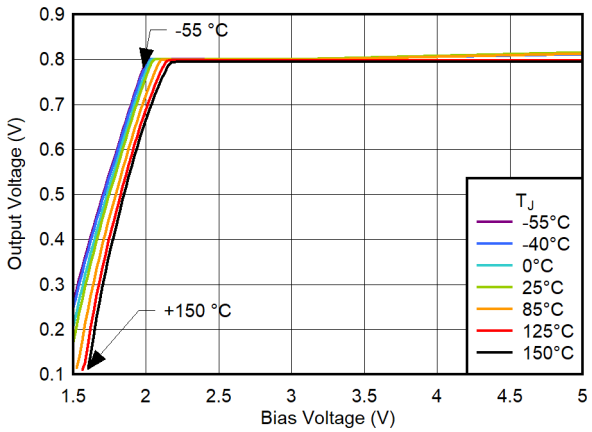
V_{IN} = 1.1 V, V_{BIAS} = 5 V, V_{OUT} = 0.8 V

图 6-14. Load Regulation vs ⩾50-mA Output Current



V_{OUT} = 0.8 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA

图 6-15. Line Regulation vs Input Voltage

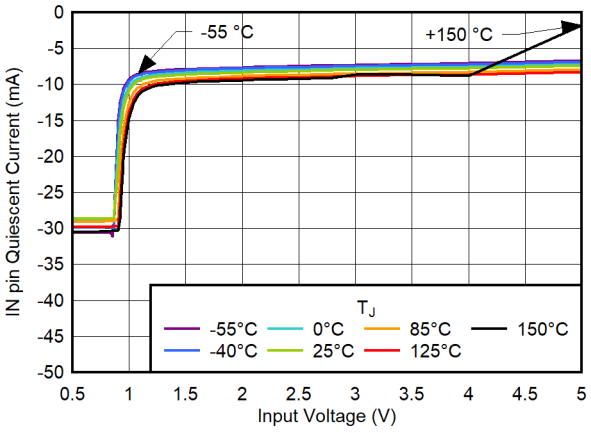


V_{BIAS} = 5 V, V_{OUT} = 0.8 V, I_{OUT} = 50 mA

图 6-16. Output Voltage vs Bias Voltage

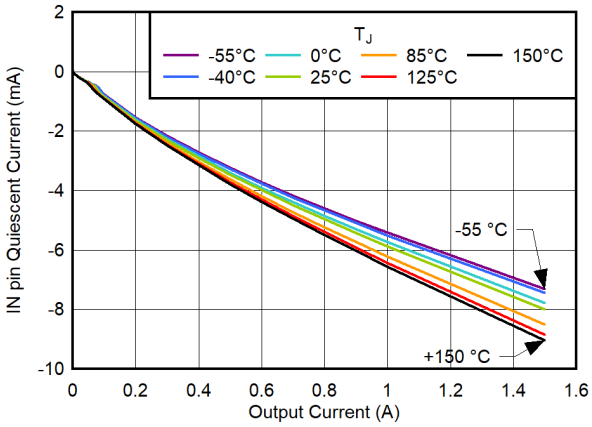
6.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 4.7 μF, and C_{OUT} = 10 μF (unless otherwise noted)



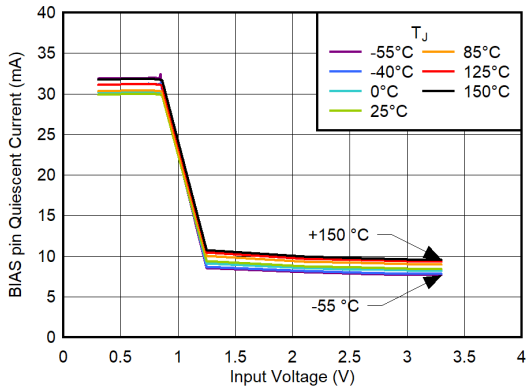
V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 50 mA

图 6-17. IN Pin Quiescent Current vs Input Voltage



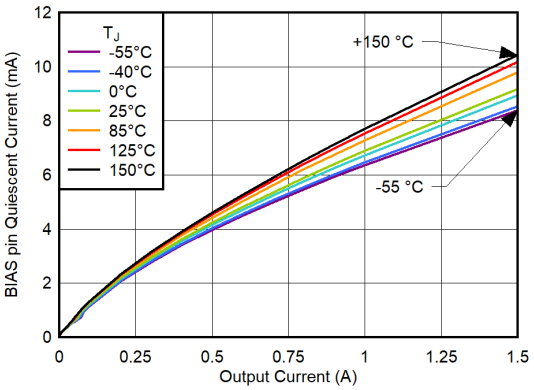
V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V

图 6-18. IN Pin Quiescent Current vs Output Current



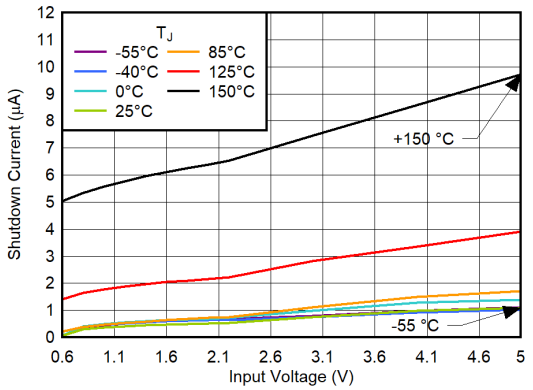
V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V, I_{OUT} = 1.5 A

图 6-19. BIAS Pin Quiescent Current vs Input Voltage



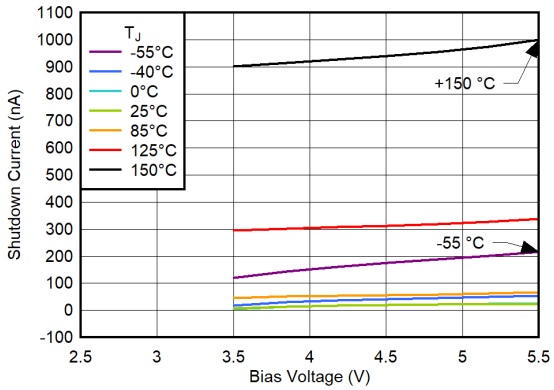
V_{IN} = 1.1 V, V_{OUT} = 0.8 V, V_{BIAS} = 5.0 V

图 6-20. BIAS Pin Quiescent Current vs Output Current



V_{BIAS} = 5 V, V_{EN} = 0 V

图 6-21. Shutdown Current (GND Pin) vs Input Voltage



V_{IN} = 1.1 V, V_{EN} = 0 V

图 6-22. Shutdown Current (GND Pin) vs Bias Voltage

6.6 Typical Characteristics: I_{OUT} = 50 mA (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF (unless otherwise noted)

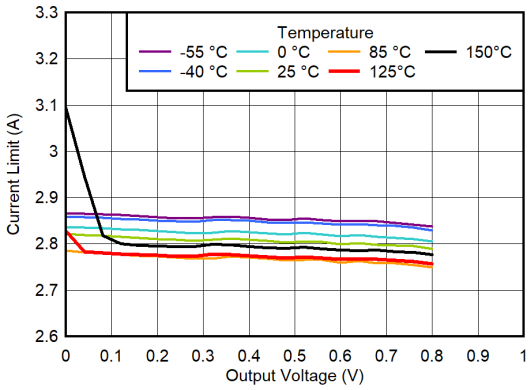


图 6-23. Current Limit vs Output Voltage

7 Detailed Description

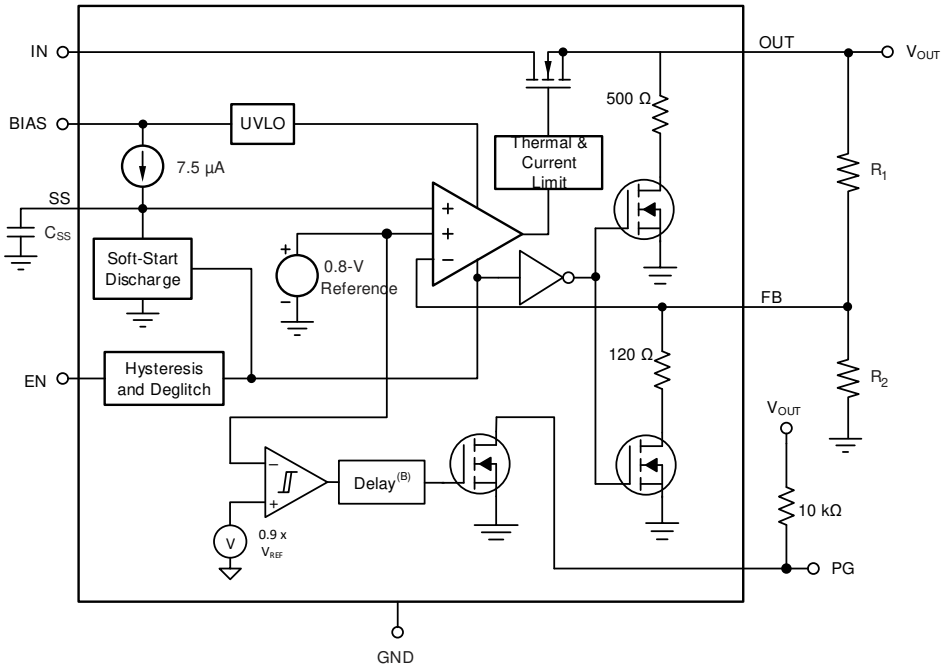
7.1 Overview

The TPS748A-Q1 is a low-input, low-output (LILO), low-quiescent-current linear regulator optimized to support excellent transient performance. This regulator uses a low-current bias rail to power all internal control circuitry, allowing the n-type field effect transistor (NMOS) pass transistor to regulate very-low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a p-channel metal-oxide-semiconductor field effect transistor (PMOS) topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS748A-Q1 to be stable with any ceramic capacitor 10 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS748A-Q1 features a programmable, voltage-controlled, soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and compatible with standard digital-signaling levels. Setting V_{EN} below 0.4 V turns the regulator off, and setting V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the device to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 70 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.75 V and varies with temperature and process variations. Temperature variation is approximately –1.2 mV/°C; process variation accounts for most of the remaining variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used.

If not used, EN can be connected to BIAS. Place the connection as close as possible to the bias capacitor.

7.3.2 Active Discharge

The TPS748A-Q1 has an internal active pulldown circuits on the OUT pin.

Each active discharge function uses an internal metal-oxide-semiconductor field-effect transistor (MOSFET) that connects a resistor ($R_{PULLDOWN}$) to ground when the low-dropout resistor (LDO) is disabled in order to actively discharge the output voltage. The active discharge circuit is activated when the device is disabled by driving EN to logic low, when the voltage at IN or BIAS is below the UVLO threshold, or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

The first active pulldown circuit connects the output to GND through a 600-Ω resistor when the device is disabled.

The second circuit connects FB to GND through a 120-Ω resistor when the device is disabled. This resistor discharges the FB pin. 方程式 1 calculates the output capacitor discharge time constant when OUT is shorted to FB, or when the output voltage is set to 0.65 V.

$$\tau_{OUT} = (600 \,||\, 120 \times R_L / (600 \,||\, 120 + R_L) \times C_{OUT} \quad (1)$$

If the LDO is set to an output voltage greater than 0.65 V, a resistor divider network is in place and minimizes the FB pin pulldown. 方程式 2 and 方程式 3 calculate the time constants set by these discharge resistors.

$$R_{DISCHARGE} = (120 \,||\, R_2) + R_1 \quad (2)$$

$$\tau_{OUT} = R_{DISCHARGE} \times R_L / (R_{DISCHARGE} + R_L) \times C_{OUT} \quad (3)$$

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input and can cause damage to the device. Limit reverse current to no more than 5% of the device-rated current.

7.3.3 Power-Good Output (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG signals when the output nears the nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 图 7-1 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage and, because the PG circuit monitors the FB pin, the PG signal can indicate a false positive.

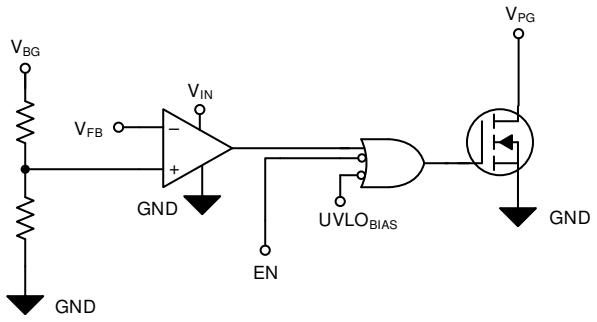


图 7-1. Simplified PG Circuit

7.3.4 Internal Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current when the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the *short-circuit current limit* (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in a brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. When the device sufficiently cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note. 图 7-2 shows a diagram of the foldback current limit.

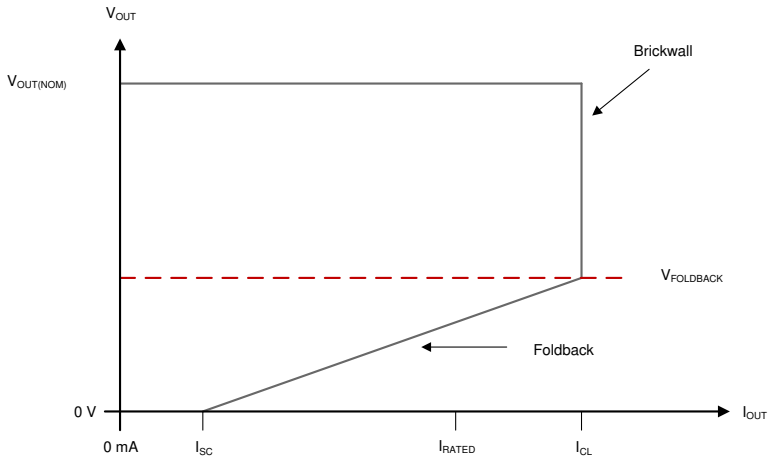


图 7-2. Foldback Current Limit

7.3.5 Thermal Shutdown Protection (T_{SD})

The internal thermal shutdown protection circuit disables the output when the thermal junction temperature (T_J) of the pass transistor rises to the thermal shutdown temperature threshold, $T_{SD(shutdown)\ (typical)}$. The thermal shutdown circuit hysteresis makes sure that the LDO resets (turns on) when the temperature falls to $T_{SD(reset)\ (typical)}$.

The thermal time constant of the semiconductor die is fairly short; thus, the device can cycle on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown, or above the maximum recommended junction temperature, reduces long-term reliability.

7.4 Device Functional Modes

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geqslant V_{OUT\ (nom)} + V_{DO(IN)}$ and $V_{IN} \geqslant V_{IN(min)}$	$V_{BIAS} \geqslant V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geqslant V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{HI(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{LO(EN)}$	—	$T_J \geqslant T_{SD}$ for shutdown

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(IN)}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO(BIAS)}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and functions as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state, defined as when the device is in dropout ($V_{IN} < V_{OUT} + V_{DO(IN)}$ or $V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO(IN)}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

7.4.3 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold
- The device junction temperature is greater than the thermal shutdown temperature

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS748A-Q1 is a low-input, low-output (LILO), low-dropout regulator (LDO) that features soft-start capability. This regulator uses a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

Using an NMOS pass transistor offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows stability with ceramic capacitors of 10 μF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

A programmable voltage-controlled, soft-start circuit provides a smooth, monotonic start-up and limits start-up inrush currents that can be caused by large capacitive loads. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often required by processor-intensive systems.

8.1.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for ceramic capacitor of values ≥ 10 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} is 1 μF and the minimum recommended capacitor for V_{BIAS} is 0.1 μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF. Use good quality, low equivalent series resistance (ESR) and equivalent series inductance (ESL) capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close the pins as possible for optimum performance.

Low ESR and ESL capacitors improve high-frequency PSRR.

8.1.2 Dropout Voltage

The TPS748A-Q1 offers very low dropout performance, making the device designed for high-current, low V_{IN} and low V_{OUT} applications. The low dropout allows the device to be used in place of a dc/dc converter and still achieve good efficiency. 方程式 4 provides a quick estimate of the efficiency.

$$\text{Efficiency} \approx \frac{V_{OUT} \times I_{OUT}}{\left[V_{IN} \times (I_{IN} + I_Q)\right]} \approx \frac{V_{OUT}}{V_{IN}} \text{ at } I_{OUT} >> I_Q \tag{4}$$

This efficiency provides designers with the power architecture for applications to achieve the smallest, simplest, and lowest cost solutions.

For this architecture, there are two different specifications for dropout voltage. The first specification (see 图 6-11) is referred to as *V_{IN} dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 2.8 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5.0-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} + 2.8 V, the V_{IN} dropout is less than specified.

备注

2.8 V is a test condition of this device and can be adjusted by referring to the *Electrical Characteristics* table.

The second specification (illustrated in 图 6-12) is referred to as V_{BIAS} *dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass transistor; therefore, V_{BIAS} must be 1.9 V above V_{OUT}. Because of this usage, having IN and BIAS tied together become a highly inefficient solution that can consume large amounts of power. Pay attention not to exceed the power rating of the device package.

8.1.3 Output Noise

The TPS748A-Q1 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 10-nF, soft-start capacitor, the output noise is reduced by half and is typically 7.1 μV_{RMS} for a 0.8-V output (10 Hz to 100 kHz). Increasing C_{SS} has no effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. 方程式 5 gives the RMS noise with a 10-nF, soft-start capacitor:

$$V_N(\mu V_{RMS}) = 7.1 \cdot \left(\frac{\mu V_{RMS}}{V}\right) \cdot V_{OUT}(V) \tag{5}$$

The low output noise makes this LDO a good choice for powering transceivers, phase-locked loops (PLLs), or other noise-sensitive circuitry.

8.1.4 Estimating Junction Temperature

By using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in 方程式 6). For backwards compatibility, an older $\theta_{JC(top)}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

where:

- P_D is the power dissipation
- T_T is the temperature at the center-top of the package
- T_B is the PCB temperature measured 1 mm away from the package *on the PCB surface*

备注

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the *Using New Thermal Metrics* application note, available for download at www.ti.com. For further information, see the *Semiconductor and IC Package Thermal Metrics* application note, also available on the TI website.

8.1.5 Soft Start, Sequencing, and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The soft start current is fixed for fixed output voltage versions.

Although the device does not have any sequencing requirement, following the sequencing order of BIAS, IN, and EN makes sure that the soft start starts from zero.

图 8-1 shows an example of the device behavior when the EN pin is enabled prior to having either power supply up. Under this condition, the output jumps from 0 V to approximately 0.3 V almost instantly when the IN voltage is sufficient to power the circuit.

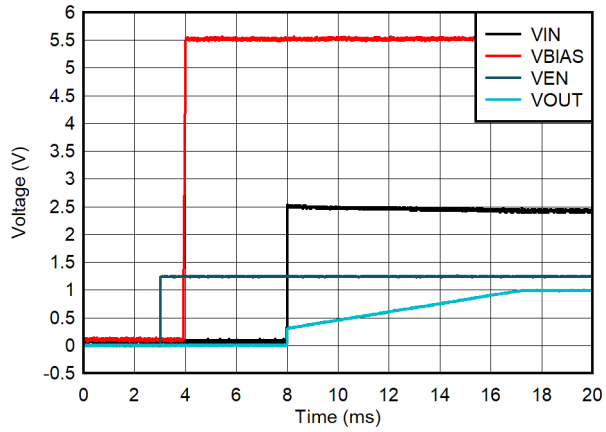


图 8-1. Sequencing and Soft-Start Behavior for V_{OUT} = 1 V

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to

measure because the input capacitor must be removed, which is not recommended. However, 方程式 7 can estimate this soft-start current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (7)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

8.1.6 Power-Good Operation

For proper operation of the power-good circuit, the pullup resistor value must be between 10 kΩ and 100 kΩ. The lower limit of 10 kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100 kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside of this range, then the power-good signal can possibly not read a valid digital logic level.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

8.2 Typical Application

This section discusses the implementation of the TPS748A-Q1 to regulate a 1-A load requiring good PSRR at high frequency with low noise. 图 8-2 provides a schematic for this typical application circuit.

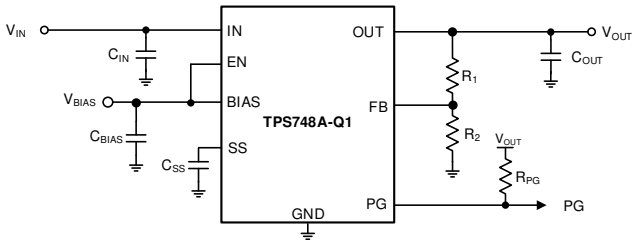


图 8-2. Typical ADJ Voltage Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.1 V, ±3%, provided by the dc/dc converter switching at 500 kHz
Bias voltage	5.0 V
Output voltage	1.8 V, ±1%
Output current	1.0 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 10 μV_{RMS}
PSRR at 500 kHz	> 40 dB
Start-up time	< 25 ms

8.2.2 Detailed Design Procedure

At 1.0 A and 1.8 V_{OUT}, the dropout of the TPS748A-Q1 has a 105-mV maximum dropout over temperature; thus, a 300-mV headroom is sufficient for operation over both input and output voltage accuracy. At full load and high temperature on some devices, the TPS748A can enter dropout if both the input and output supply are beyond the edges of the respective accuracy specification.

To satisfy the required start-up time and still maintain low noise performance, a 10-nF C_{SS} is selected. 方程式 8 calculates this value.

$$t_{SS} = (V_{SS} \times C_{SS}) / I_{SS} \quad (8)$$

At the 1.0-A maximum load, the internal power dissipation is 0.3 W and corresponds to a 13.3°C junction temperature rise for the DRC package on a standard JEDEC board. With an 55°C maximum ambient temperature, the junction temperature is at 68.3°C.

8.2.3 Application Curve

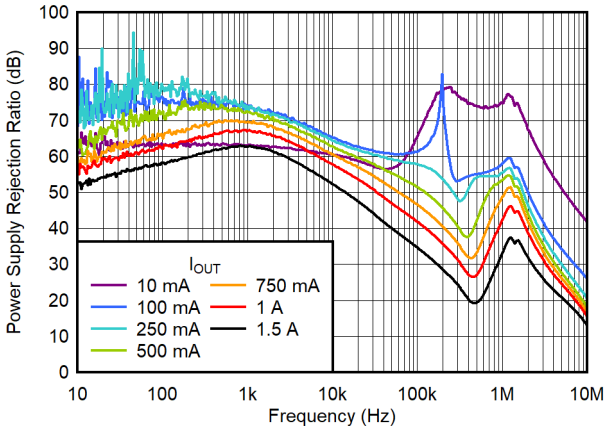


图 8-3. PSRR vs Frequency for V_{OUT} = 1.8 V

8.3 Power Supply Recommendations

The TPS748A-Q1 is designed to operate from an input voltage up to 6.0 V, provided the bias rail is at least 1.3 V higher than the input supply and dropout requirements are met. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally. Connect a low output impedance power supply directly to the IN pin. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the BIAS rail with a separate 0.1 µF or larger capacitor. If the IN pin is tied to the BIAS pin, a minimum 4.7-µF capacitor is required for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

8.4 Layout

8.4.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in 图 8-2 must be connected as close as possible to the load. If BIAS is connected to IN, connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device can be calculated using 方程式 9 and depends on input voltage and load conditions.

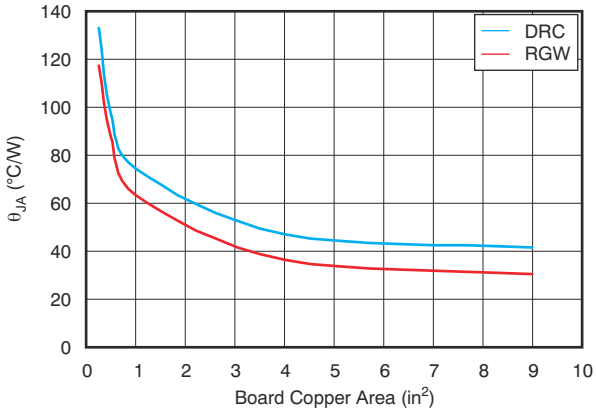
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{9}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRC) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or left floating; however, the thermal pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance can be calculated using 方程式 10 and depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device.

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (10)$$

The minimum amount of PCB copper area needed for appropriate heat sinking (which can be estimated using 图 8-4) is determined by knowing the maximum $R_{\theta JA}$.



The $R_{\theta JA}$ value at board size of 9 in^2 (that is, 3 in × 3 in) is a JEDEC standard.

图 8-4. $R_{\theta JA}$ vs Board Size

图 8-4 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and is not intended to be used to estimate actual thermal performance in real application environments.

备注

When the device is mounted on an application PCB, use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

8.4.2 Layout Example

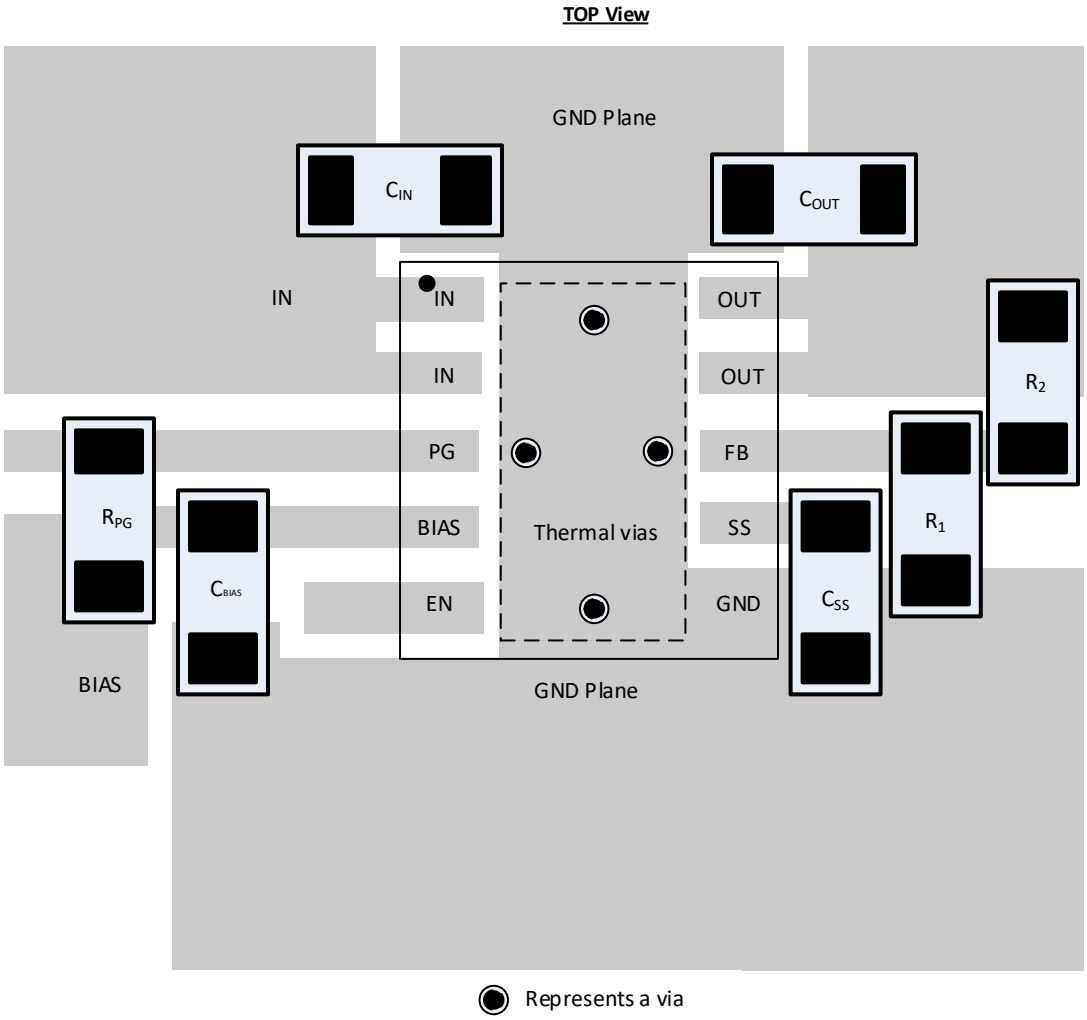


图 8-5. Example Layout

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

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9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

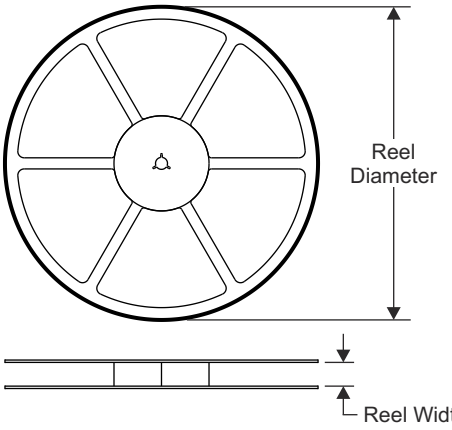
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

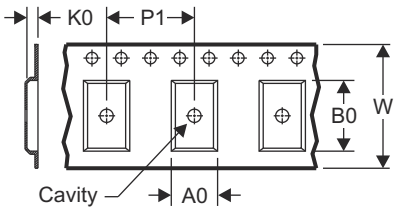
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

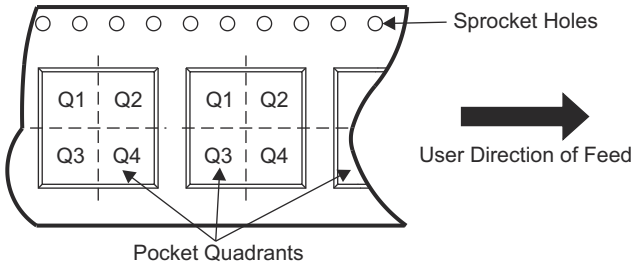


TAPE DIMENSIONS



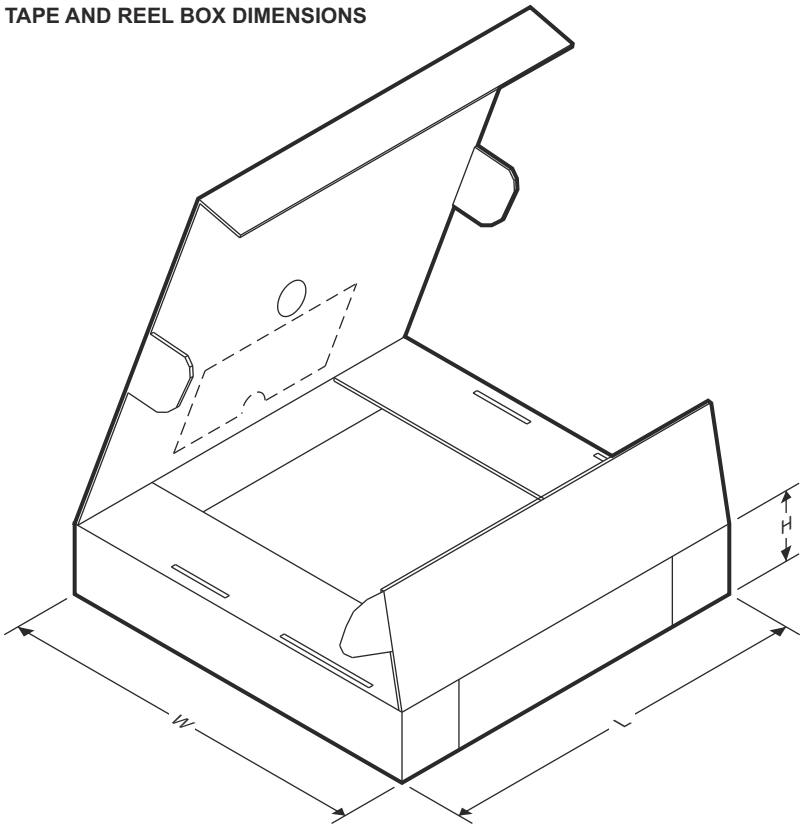
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



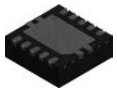
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801AQWDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801AQWDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

10.2 Mechanical Data

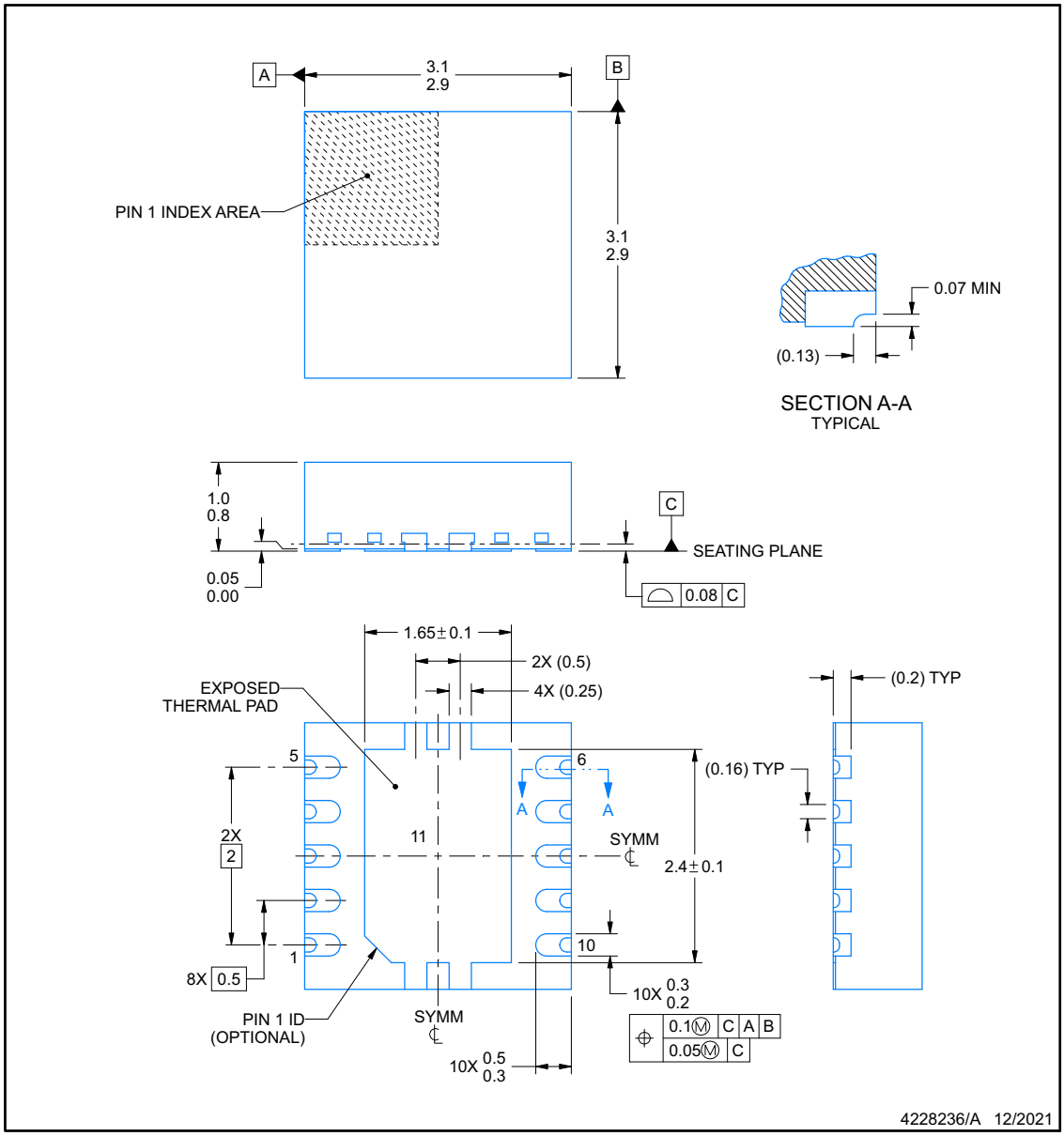


DRC0010W

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

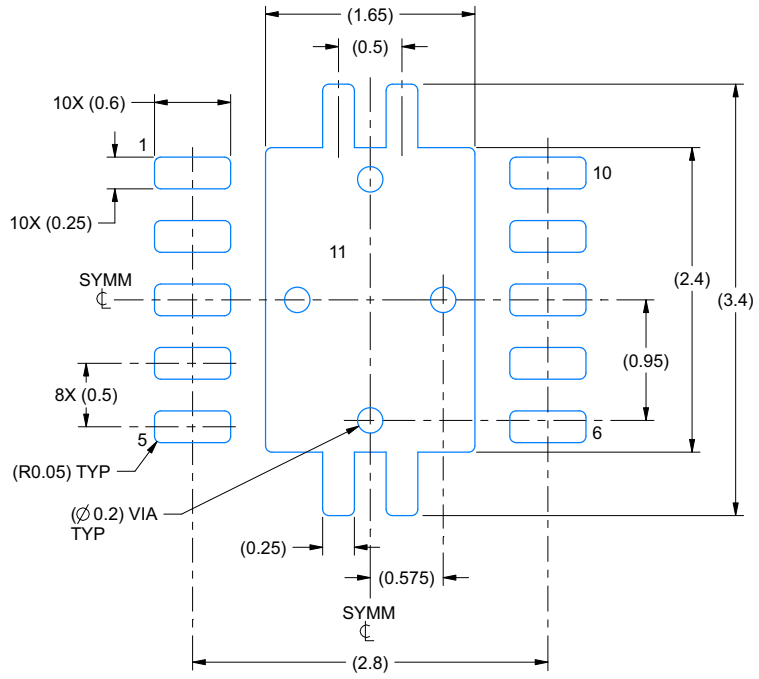
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

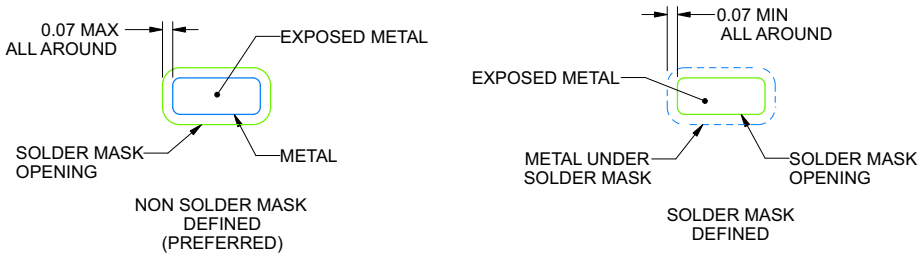
DRC0010W

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

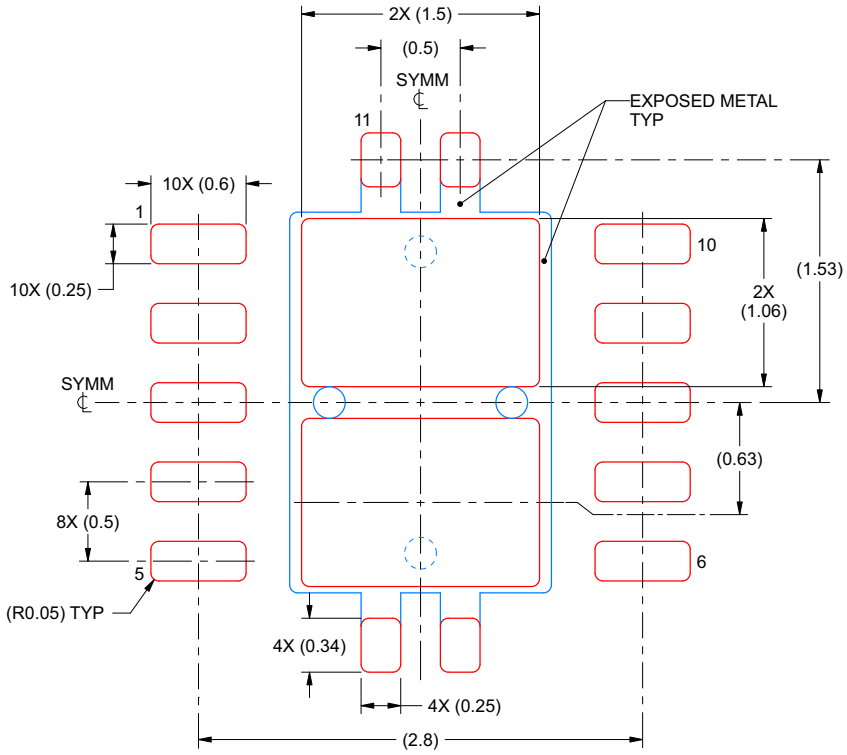
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010W

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74801AQWDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	74801A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS748A-Q1 :

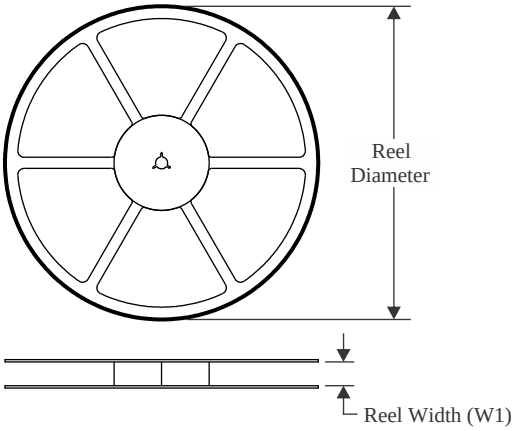
- Catalog : TPS748A

NOTE: Qualified Version Definitions:

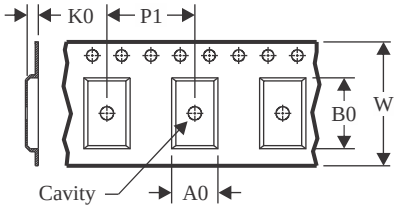
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
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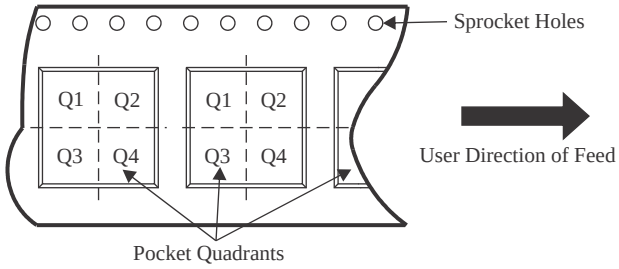
P1	Pitch between successive cavity centers

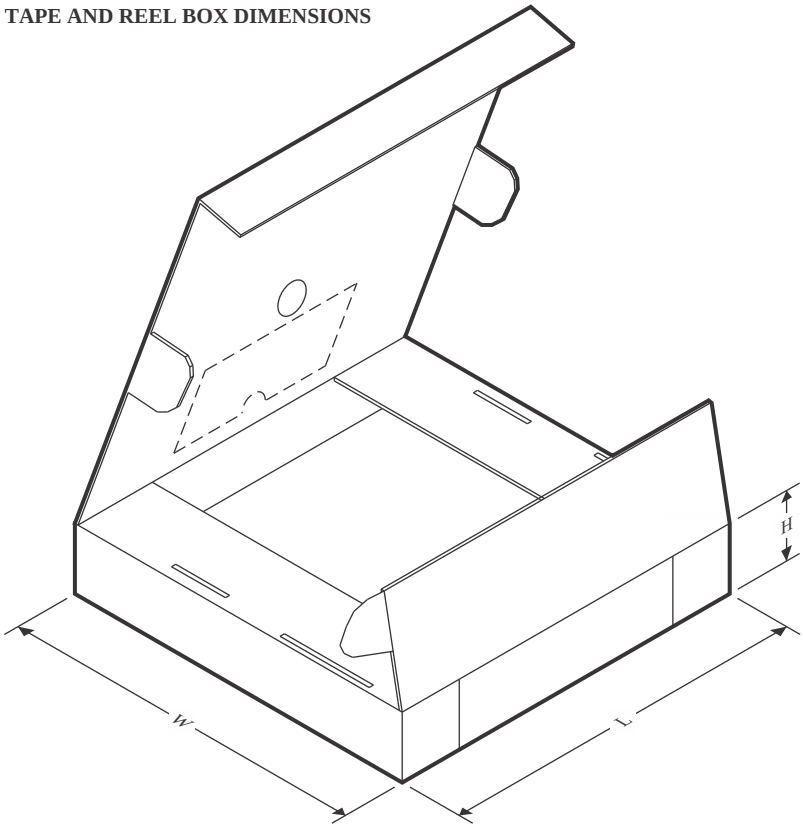
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801AQWDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801AQWDRCRQ1	VSON	DRC	10	3000	360.0	360.0	36.0

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