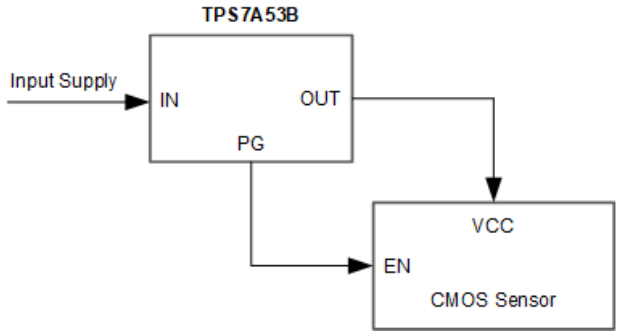
TPS7A53B 3A、低输入电压、低噪声、高精度、低压降 (LDO) 稳压器

1 特性

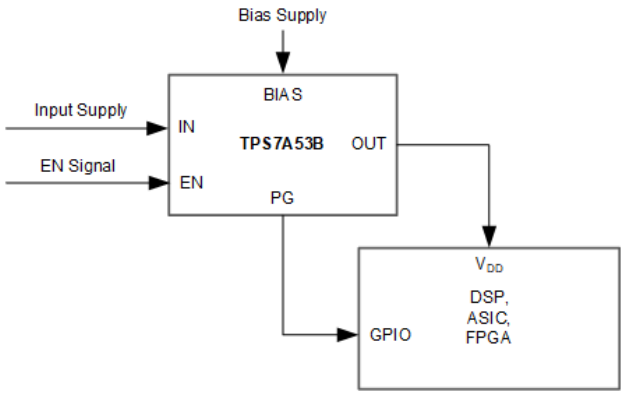
- 线路、负载和温度范围内的精度（有偏置）：0.5%
- 输出电压噪声：4.6 μ V_{RMS}
- 低压降：3A 电流时为 110mV（最大值），有偏置
- 电源抑制比：
  - 500kHz 时为 48dB
- 输入电压范围：
  - 无偏置：1.4V 至 6.5V
  - 有偏置：1.1V 至 6.5V
- 可调输出电压范围：0.5V 至 5.15V
- 可调软启动浪涌控制
- 开漏电源正常状态 (PG) 输出
- 2.5mm × 2.2mm，12 引脚 VQFN 封装

2 应用

- 宏远程无线电单元 (RRU)
- 室外回程单元
- 有源天线系统 mMIMO (AAS)
- 超声波扫描仪
- 实验室和现场仪表
- 传感器、成像和雷达



为射频组件供电



为数字负载供电

3 说明

TPS7A53B 是一款低噪声 (4.6 μ V_{RMS})、超低压降线性稳压器 (LDO)，可提供 3A 电流，最大压降仅为 110mV。该器件的输出电压可通过外部电阻分压器进行调节，范围为 0.5V 至 5.15V。

TPS7A53B 集低噪声 (4.6 μ V_{RMS})、高 PSRR 和高输出电流能力等特性于一体，非常适合为噪声敏感型元件供电。应用包括高速通信、视频、医疗或测试和测量。该器件具有高 PSRR 和低噪声性能，可抑制电源产生的相位噪声和时钟抖动，因此适合为高性能串行器和解串器 (SerDes)、模数转换器 (ADC) 和数模转换器 (DAC) 供电。具体来说，射频放大器将从该器件的高性能和 5.15V 输出能力受益。

对于需要以低输入和低输出 (LILO) 电压运行的数字负载（例如专用集成电路 (ASIC)、现场可编程门阵列 (FPGA) 和数字信号处理器 (DSP)），TPS7A53B 所具备的出色精度（在负载和温度范围内可达 0.5%）、遥感功能、卓越的瞬态性能和软启动功能可实现最优的系统性能。

作为可调节稳压器，TPS7A53B 可实现多用途设计，因此适用于压控振荡器 (VCO)、ADC、DAC 和成像传感器等模拟负载以及 SerDes、FPGA 和 DSP 等数字负载。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS7A53B	RPS（VQFN，12）	2.5mm × 2.2mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

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4 Pin Configuration and Functions

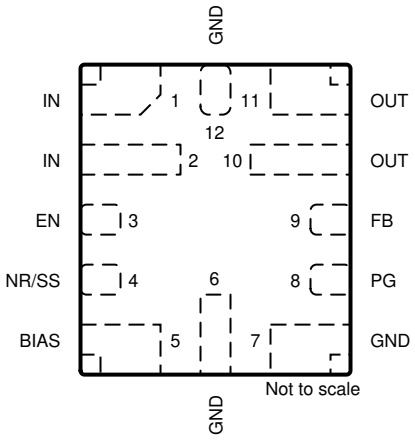


图 4-1. RPS Package, 2.5mm × 2.2mm, 12-Pin VQFN (Top View)

表 4-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	I/O	
BIAS	5	I	BIAS pin. This pin enables using low-input voltage, low-output (LILO) voltage conditions (that is, V_{IN} = 1.2V, V_{OUT} = 1V) to reduce power dissipation across the die. Using a BIAS voltage improves dc and ac performance for $V_{IN} \leqslant$ 2.2V. A 1µF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
EN	3	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. This pin must be connected to IN or BIAS if not driven externally.
FB	9	I	Feedback pin. Although not required, use a 10nF feed-forward capacitor from FB to OUT (as close to the device as possible) to maximize ac performance. A feed-forward capacitor can disrupt power-good (PG) functionality. See the *Adjustable Operation* section for more details.
GND	6, 7, 12	—	Ground pin. These pins must be connected to ground and each other with a low-impedance connection.
IN	1, 2	I	Input supply voltage pin. Use a 10µF or larger ceramic capacitor (5µF or greater of capacitance) from IN to ground to reduce input supply impedance. Place the input capacitor as close to the input as possible. See the *Input and Output Capacitor Requirements* section for more details.
NR/SS	4	—	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, connect a 10nF or larger capacitor from NR/SS to GND (as close to the pin as possible) to maximize ac performance. See the *Noise-Reduction and Soft-Start Capacitor* section for more details.
OUT	10, 11	O	Regulated output pin. A 47µF or larger ceramic capacitor (25µF or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load. See the *Input and Output Capacitor Requirements* section for more details.
PG	8	O	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches $V_{IT(PG)}$ of the target. A feed-forward capacitor can disrupt PG (power good) functionality. See the *Power-Good Output* section for more details.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, BIAS, PG, EN	–0.3	7.0	V
	OUT	–0.3	V_{IN} + 0.3(2)	
	NR/SS, FB	–0.3	3.6	
Current	OUT	Internally limited		A
	PG (sink current into device)		5	mA
Temperature	Operating junction, T_J	–55	125	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3V or 7.0V, whichever is smaller.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.1		6.5	V
V_{BIAS}	Bias supply voltage range	3.0		6.5	V
V_{OUT}	Output voltage range(1)	0.5		5.15	V
V_{EN}	Enable voltage range	0		6.5	V
I_{OUT}	Output current	0		3	A
C_{IN}	Input capacitor	10	47	3000	µF
C_{OUT}	Output capacitor	47	47||10||10(3)	3000	µF
C_{BIAS}	Bias pin capacitor		1		µF
R_{PG}	Power-good pullup resistance	10		100	kΩ
$C_{NR/SS}$	NR/SS capacitor		10		nF
C_{FF}	Feed-forward capacitor		10		nF
R_1	Top resistor value in feedback network for adjustable operation		12.1		kΩ
R_2	Bottom resistor value in feedback network for adjustable operation			160(2)	kΩ
T_J	Operating junction temperature	–40		125	°C

(1) This output voltage range does not include device accuracy or accuracy of the feedback resistors.
(2) The upper limit for the R_2 resistor is to provide accuracy by making the current through the feedback network much larger than the leakage current into the feedback node.

(3) The recommended output capacitors are selected to optimize PSRR for the frequency range of 400kHz to 700kHz. This frequency range is a typical value for dc/dc supplies.

5.4 Thermal Information

THERMAL METRIC[1]		RPS (VQFN) 12 PINS		UNIT
		JEDEC[2]	EVM[3]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.7	46.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.8	43.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	4.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.9	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	11.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) JEDEC standard. (2s2p, no vias to internal plane and bottom layer).
(3) EVM thermal model using the TPS7A53EVM-031 for thermal analysis, see the TPS7A53EVM Thermal Analysis section for more information.

5.5 Electrical Characteristics

over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.5 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up toV_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage			0.5		V
$V_{NR/SS}$	NR/SS pin voltage			0.5		V
$V_{UVLO+(IN)}$	Rising input supply UVLO with BIAS	V_{IN} rising with V_{BIAS} = 3V		1.02	1.085	V
$V_{UVLO-(IN)}$	Falling input supply UVLO with BIAS	V_{IN} falling with V_{BIAS} = 3V	0.55	0.7		V
$V_{UVLO+(IN)}$	Rising input supply UVLO without BIAS	V_{IN} rising		1.31	1.39	V
$V_{UVLO-(IN)}$	Falling input supply UVLO without BIAS	V_{IN} falling	0.65	1.057		V
$V_{UVLO+(BIAS)}$	Rising bias supply UVLO	V_{BIAS} rising, V_{IN} = 1.1V		2.83	2.9	V
$V_{UVLO-(BIAS)}$	Falling bias supply UVLO	V_{BIAS} falling, V_{IN} = 1.1V	2.45	2.54		V
V_{OUT}	Output voltage range		0.5		5.15	V
	Output voltage accuracy	1.4 V ≤ V_{IN} ≤ 6.5 V, 0.5V ≤ V_{OUT} ≤ 5.15V, 5mA ≤ I_{OUT} ≤ 3A	-0.75		0.75	%
		V_{IN} =1.1V, 5mA ≤ I_{OUT} ≤ 3A, 3V ≤ V_{BIAS} ≤ 6.5V	-0.5		0.5	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 5mA, 1.4V ≤ V_{IN} ≤ 6.5V		0.03		mV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	5mA ≤ I_{OUT} ≤ 3A, 3V ≤ V_{BIAS} ≤ 6.5V, V_{IN} = 1.1V		0.07		mV/A
		5mA ≤ I_{OUT} ≤ 3A		0.012		mV/A

5.5 Electrical Characteristics（续）

over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.5 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up toV_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Error amplifier offset voltage	V_{IN} = 1.4V, I_{OUT} = 5mA	-2.5		2.5	mV
V_{DO}	Dropout voltage	V_{IN} = 1.4V, I_{OUT} = 3A, V_{FB} = 0.5V – 3%		105	175	mV
		V_{IN} = 5.4V, I_{OUT} = 3A, V_{FB} = 0.5V – 3%		170	280	
		V_{IN} = 5.6V, I_{OUT} = 3A, V_{FB} = 0.5V – 3%		215	375	
		V_{IN} = 1.1V, 3.0V ≤ V_{BIAS} ≤ 6.5V, I_{OUT} = 3A, V_{FB} = 0.5V – 3%		60	110	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, $V_{OUT(nom)}$ = 5.0V	3.6	4.2	4.9	A
I_{SC}	Short-circuit current limit	R_{LOAD} = 20mΩ		2		
I_{GND}	GND pin current	V_{IN} = 6.5V, I_{OUT} = 5mA		3	4.3	mA
		V_{IN} = 1.4 V, I_{OUT} = 3 A		4.3	5.5	
		Shutdown, PG = open, V_{IN} = 6.5V, V_{EN} = 0.5V			25	µA
I_{EN}	EN pin current	V_{IN} = 6.5V, V_{EN} = 0V and 6.5V			0.5	µA
I_{BIAS}	BIAS pin current	V_{IN} = 1.1V, V_{BIAS} = 6.5V, $V_{OUT(nom)}$ = 0.5V, I_{OUT} = 3A		2.3	3.5	mA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)		0		0.5	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1		6.5	V
$V_{IT-(PG)}$	Falling PG pin threshold	For falling V_{OUT}	80% × V_{OUT}	86% × V_{OUT}	91% × V_{OUT}	V
$V_{IT+(PG)}$	Rising PG pin threshold	For rising V_{OUT}	85% × V_{OUT}	91% × V_{OUT}	96% × V_{OUT}	V
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5V			1	µA
$I_{NR/SS}$	NR/SS pin charging current	$V_{NR/SS}$ = GND, V_{IN} = 6.5V	4	6.2	9	µA
I_{FB}	FB pin leakage current	V_{IN} = 6.5V			100	nA
R_{NR}	NR resistor value			250		kΩ
PSRR	Power-supply rejection ratio	V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF, f = 10kHz		53		dB
		V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF, f = 500kHz		48		

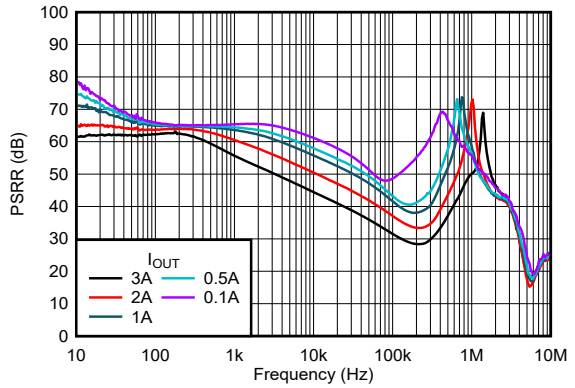
5.5 Electrical Characteristics（续）

over operating junction temperature range (T_J = –40°C to +125°C), V_{IN} = 1.4 V or V_{IN} = $V_{OUT(nom)}$ + 0.5 V (whichever is greater), V_{BIAS} = open, $V_{OUT(nom)}$ = 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{IN} = 10 µF, C_{OUT} = 47 µF, $C_{NR/SS}$ = 0 nF, C_{FF} = 0 nF, and PG pin pulled up toV_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Output noise voltage	Bandwidth = 10Hz to 100kHz, V_{IN} = 1.1V, V_{OUT} = 0.5V, V_{BIAS} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF		4.6		μV_{RMS}
		Bandwidth = 10Hz to 100kHz, V_{OUT} = 5V, I_{OUT} = 3A, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF		13.9		
T_{sd+}	Thermal shutdown temperature increasing	Shutdown, temperature increasing		160		°C
T_{sd-}	Thermal shutdown temperature decreasing	Reset, temperature decreasing		140		

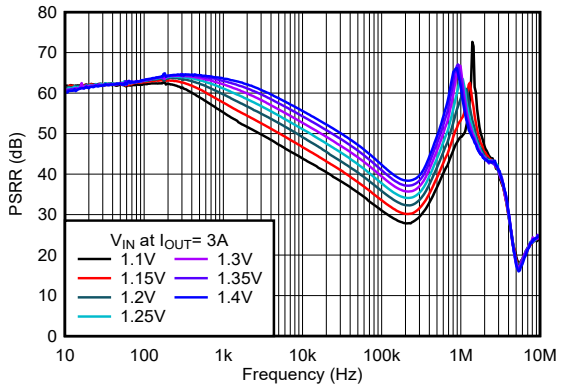
5.6 Typical Characteristics

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



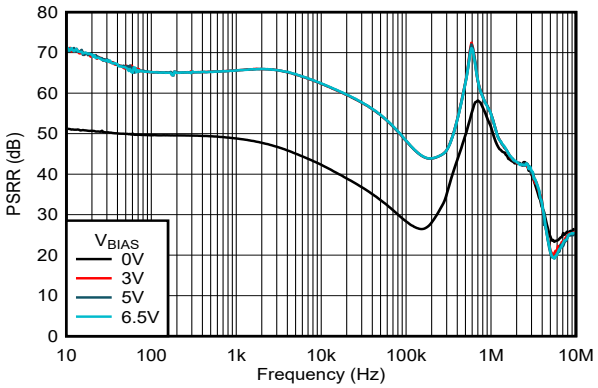
V_{IN} = 1.1V, V_{OUT} = 0.7V, V_{BIAS} = 5V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-1. PSRR vs Frequency and I_{OUT}



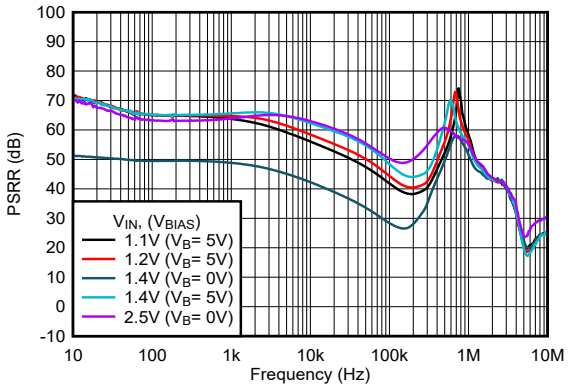
V_{BIAS} = 5V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-2. PSRR vs Frequency and V_{IN} With Bias



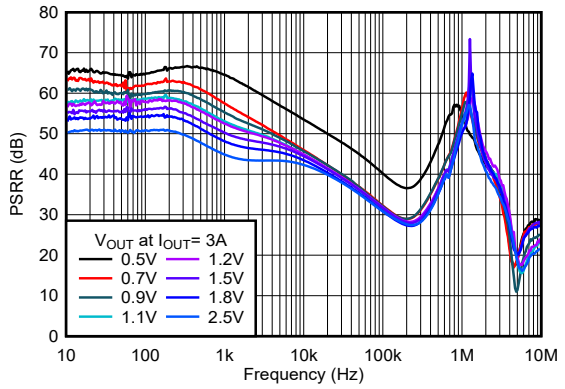
V_{IN} = 1.4V, I_{OUT} = 1A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-3. PSRR vs Frequency and V_{BIAS}



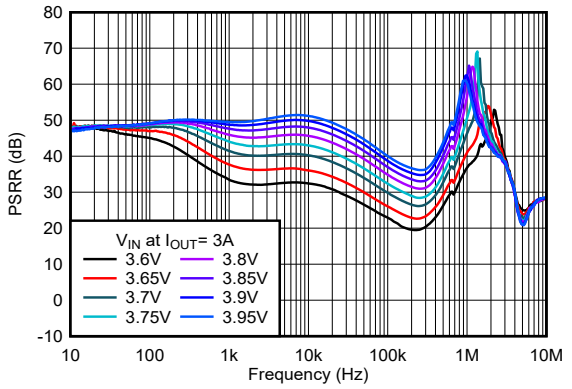
I_{OUT} = 1A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-4. PSRR vs Frequency and V_{IN}



V_{IN} = V_{OUT} + 0.4V, V_{BIAS} = 5.0V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-5. PSRR vs Frequency and V_{OUT} With Bias

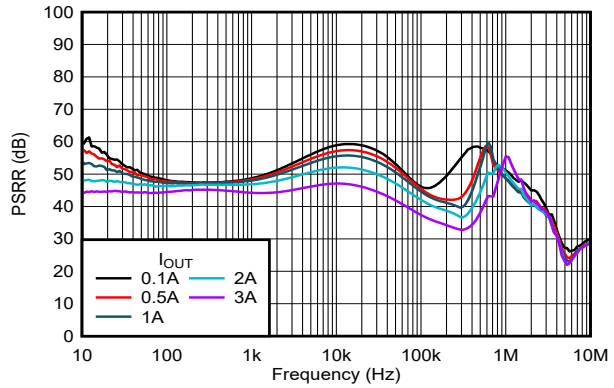


I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-6. PSRR vs Frequency and V_{IN} for V_{OUT} = 3.3V

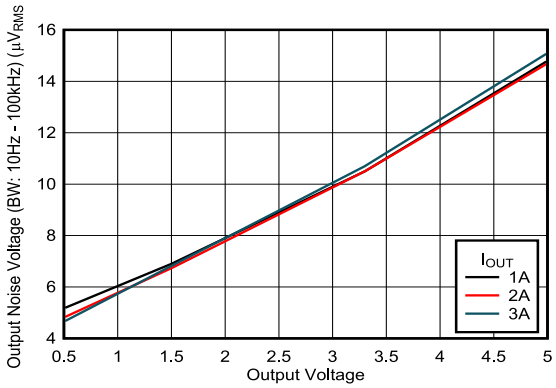
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



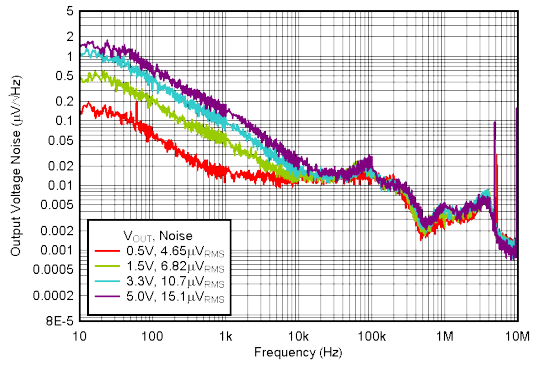
V_{IN} = 5.6V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF

图 5-7. PSRR vs Frequency and I_{OUT} for V_{OUT} = 5V



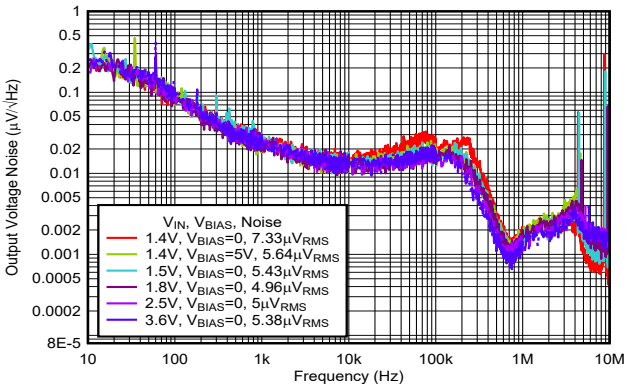
V_{IN} = V_{OUT} + 0.4V and V_{BIAS} = 5V for V_{OUT} ≤ 2.2V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-8. Output Voltage Noise vs Output Voltage and I_{OUT}



V_{IN} = V_{OUT} + 0.4V and V_{BIAS} = 5V for V_{OUT} ≤ 2.2V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-9. Output Voltage Noise vs Frequency and V_{OUT}

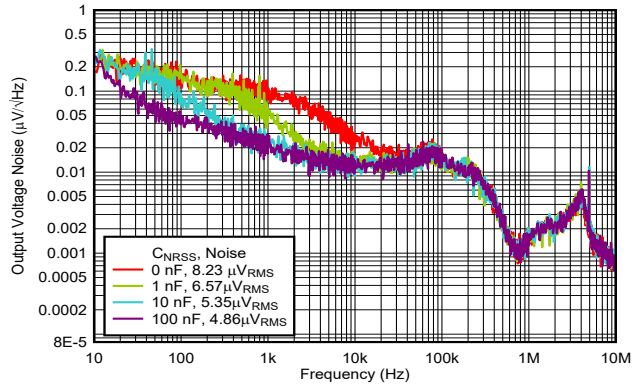


I_{OUT} = 1A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-10. Output Voltage Noise vs Frequency and V_{IN}

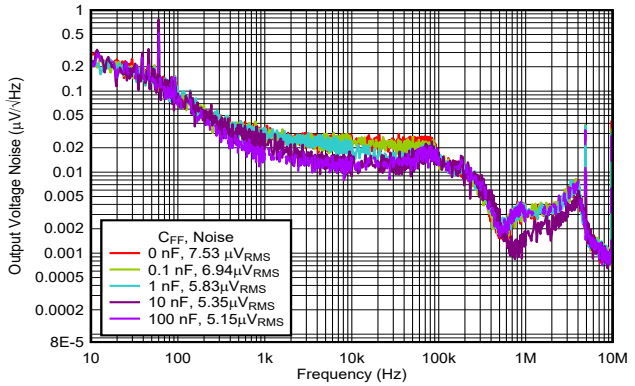
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



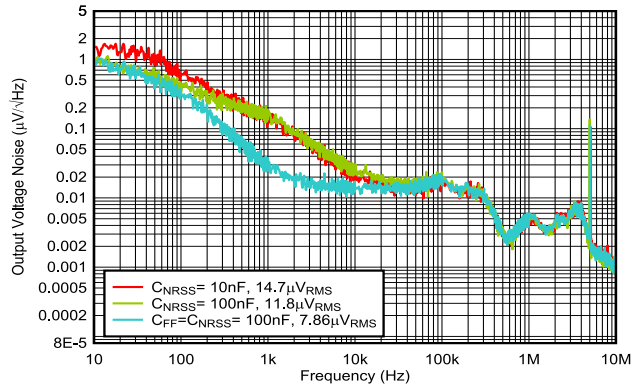
V_{IN} = V_{OUT} + 0.4V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-11. Output Voltage Noise vs Frequency and $C_{NR/SS}$



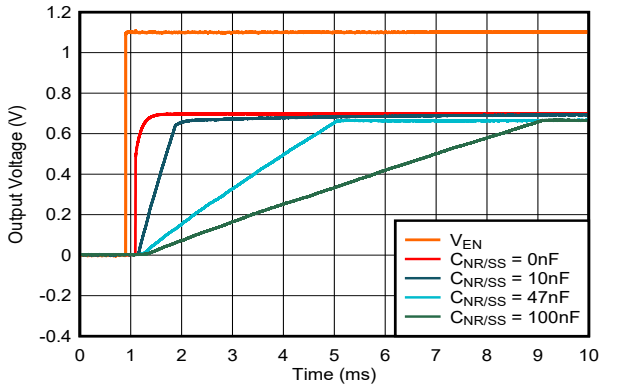
V_{IN} = 1.1V, V_{OUT} = 0.7V, V_{BIAS} = 5V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-12. Output Voltage Noise vs Frequency and C_{FF}



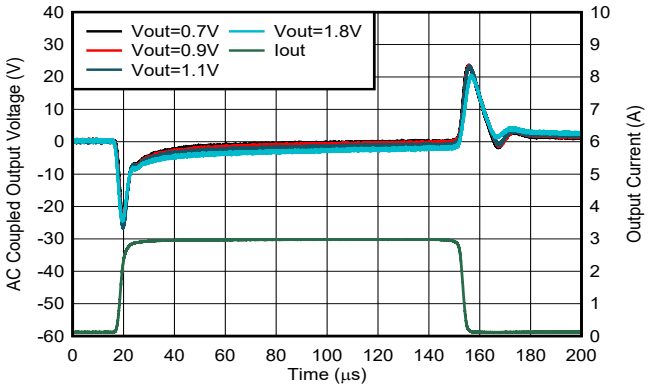
V_{IN} = 5.6V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{FF} = 10nF, RMS noise BW = 10Hz to 100kHz

图 5-13. Output Voltage Noise vs Frequency at 5V Output



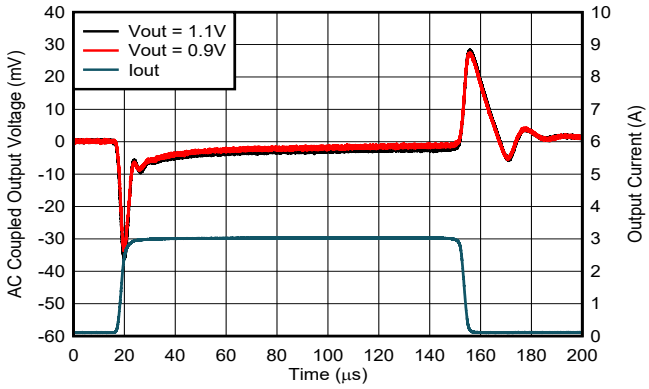
V_{IN} = 1.1V, V_{OUT} = 0.7V, V_{BIAS} = 5.0V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF

图 5-14. Start-Up Waveform vs Time and $C_{NR/SS}$



V_{IN} = V_{OUT} + 0.4V, V_{BIAS} = 5V, $I_{OUT, DC}$ = 100mA, slew rate = 1A/µs, $C_{NR/SS}$ = C_{FF} = 10nF, C_{OUT} = 47µF || 10µF || 10µF

图 5-15. Load Transient vs Time and V_{OUT} With Bias

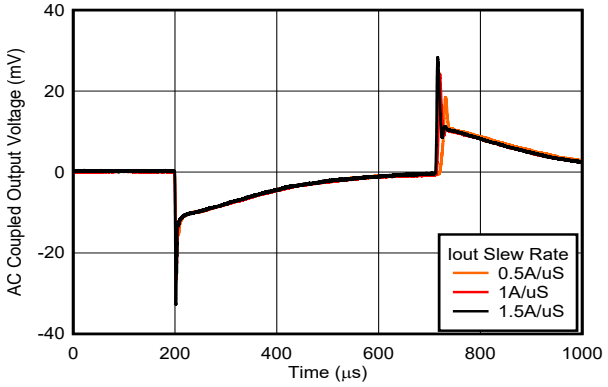


$I_{OUT, DC}$ = 100mA, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF, slew rate = 1A/µs

图 5-16. Load Transient vs Time and V_{OUT} Without Bias

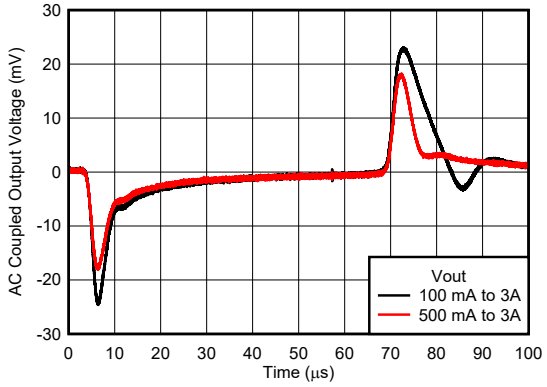
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



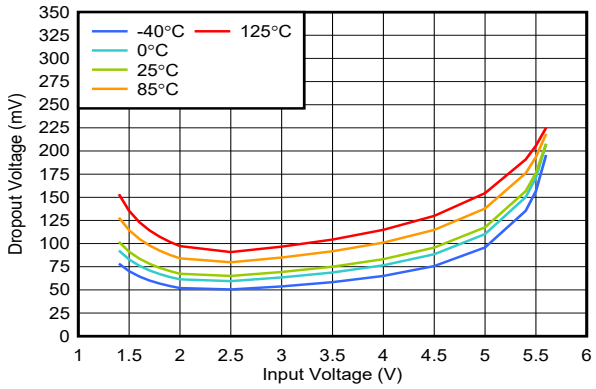
V_{OUT} = 5V, $I_{OUT, DC}$ = 100mA, I_{OUT} = 100mA to 3A, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF

图 5-17. Load Transient vs Time and Slew Rate



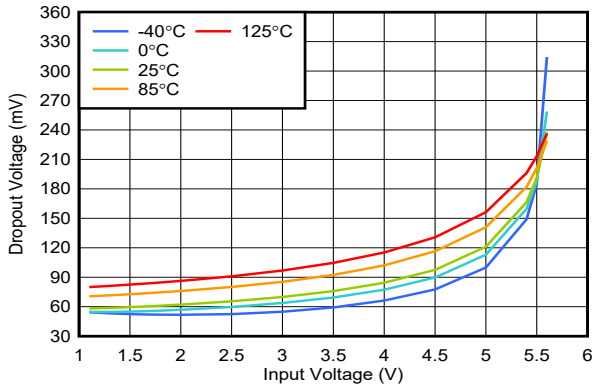
V_{IN} = 1.4V, V_{BIAS} = 5.0V, C_{OUT} = 47µF || 10µF || 10µF, $C_{NR/SS}$ = C_{FF} = 10nF, slew rate = 1A/µs

图 5-18. Load Transient vs Time and DC Load (V_{OUT} = 0.7V)



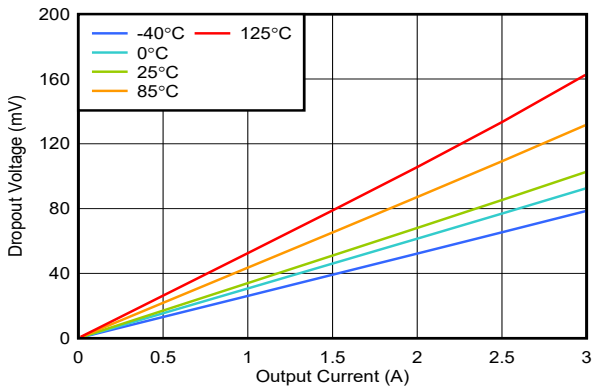
I_{OUT} = 3A, V_{BIAS} = 0V

图 5-19. Dropout Voltage vs Input Voltage Without Bias



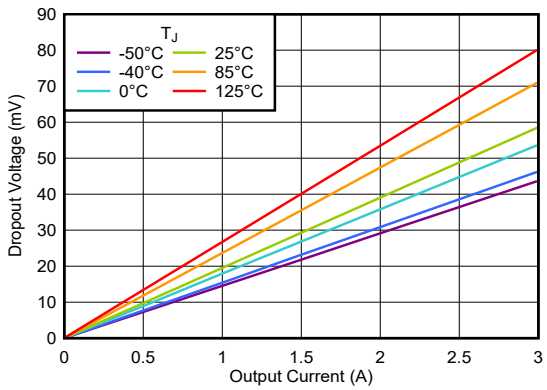
I_{OUT} = 3A, V_{BIAS} = 6.5V

图 5-20. Dropout Voltage vs Input Voltage With Bias



V_{IN} = 1.4V, V_{BIAS} = 0V

图 5-21. Dropout Voltage vs Output Current Without Bias

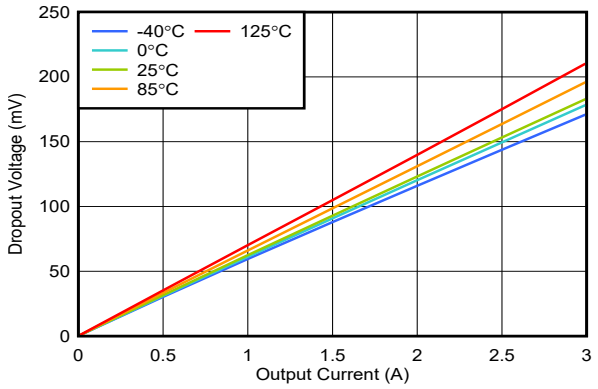


V_{IN} = 1.1V, V_{BIAS} = 3V

图 5-22. Dropout Voltage vs Output Current With Bias

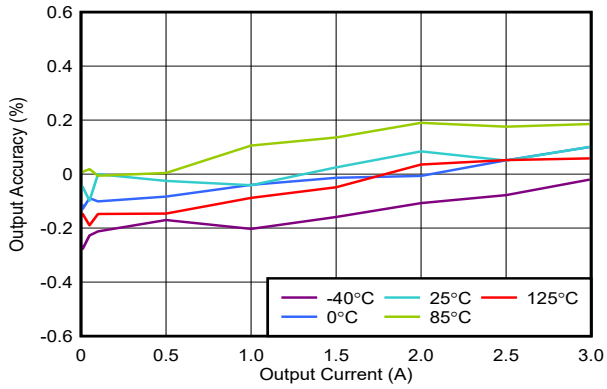
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



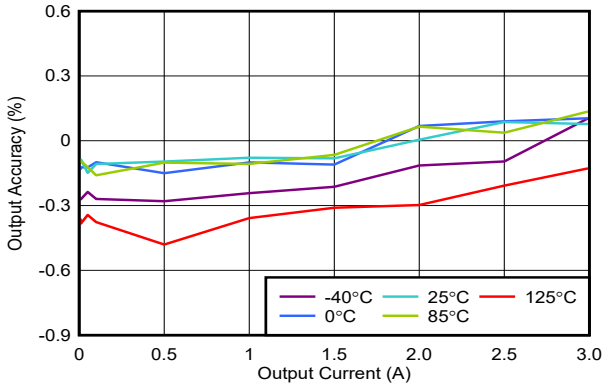
V_{IN} = 5.5V

图 5-23. Dropout Voltage vs Output Current (High V_{IN})



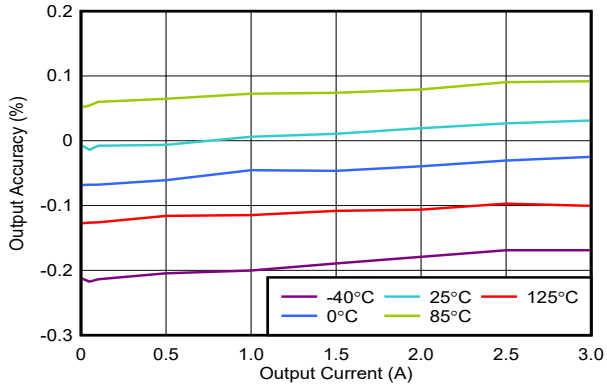
V_{IN} = 1.1V, V_{BIAS} = 3.0V

图 5-24. Load Regulation With Bias



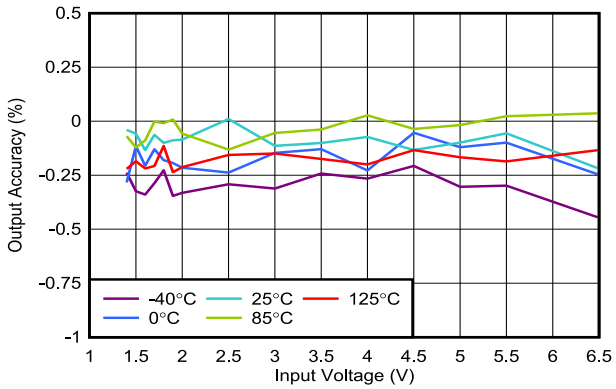
V_{IN} = 1.4V

图 5-25. Load Regulation Without Bias



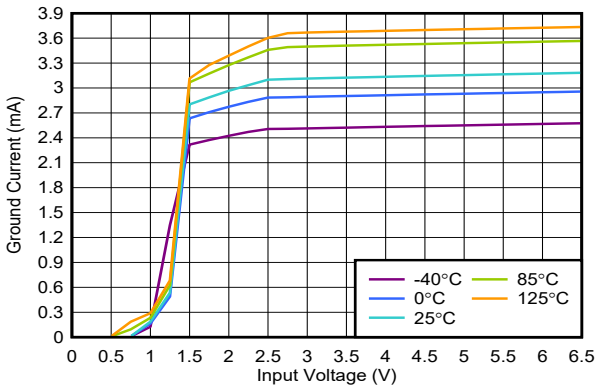
V_{IN} = 5.5V, V_{OUT} = 5.15V, V_{BIAS} = 0V

图 5-26. Load Regulation Without Bias



V_{OUT} = 0.5V, I_{OUT} = 5mA

图 5-27. Line Regulation Without Bias

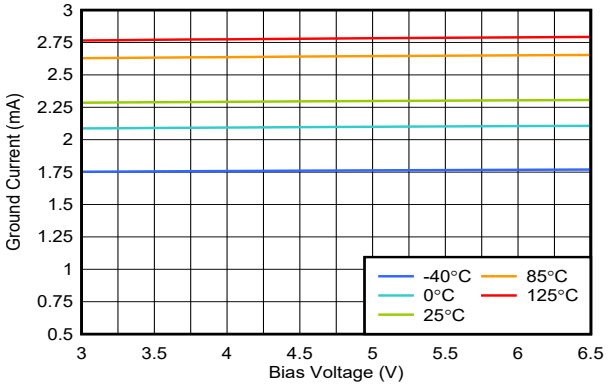


V_{BIAS} = 0V, I_{OUT} = 5mA

图 5-28. Quiescent Current vs Input Voltage

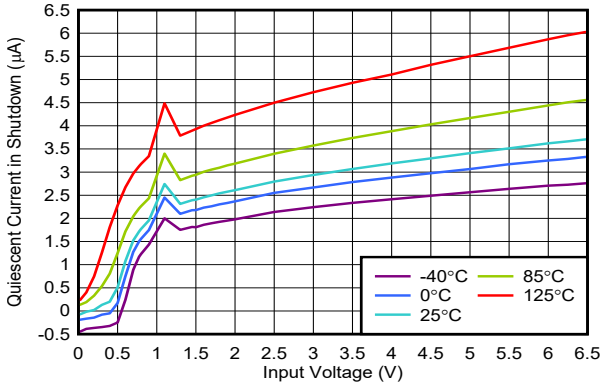
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



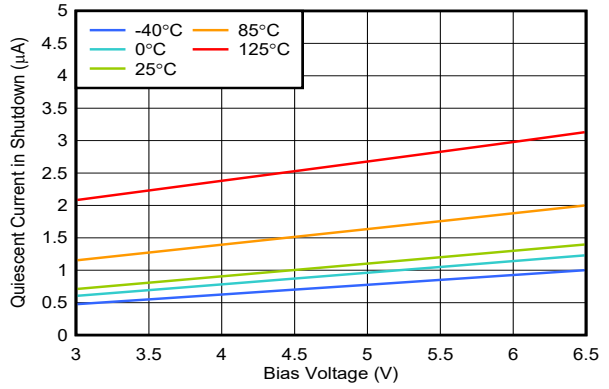
V_{IN} = 1.1V, I_{OUT} = 5mA

图 5-29. Quiescent Current vs Bias Voltage



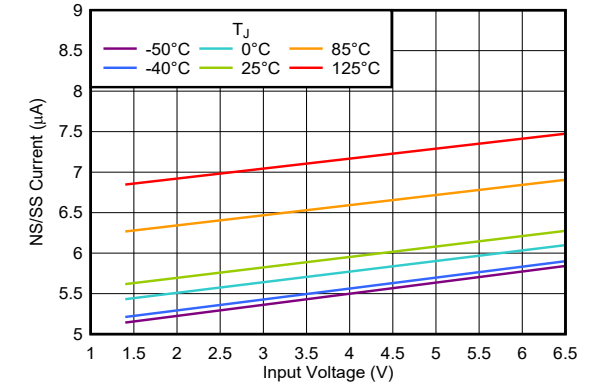
V_{BIAS} = 0V

图 5-30. Shutdown Current vs Input Voltage



V_{IN} = 1.1V

图 5-31. Shutdown Current vs Bias Voltage



V_{BIAS} = 0V

图 5-32. NR/SS Current vs Input Voltage

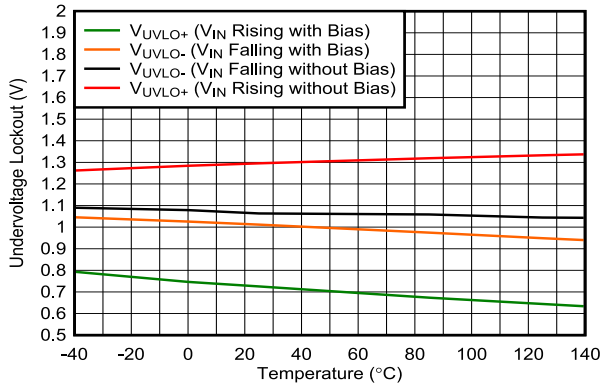
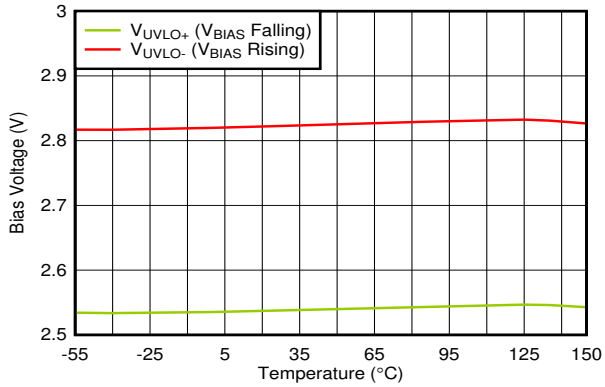


图 5-33. V_{IN} UVLO vs Temperature

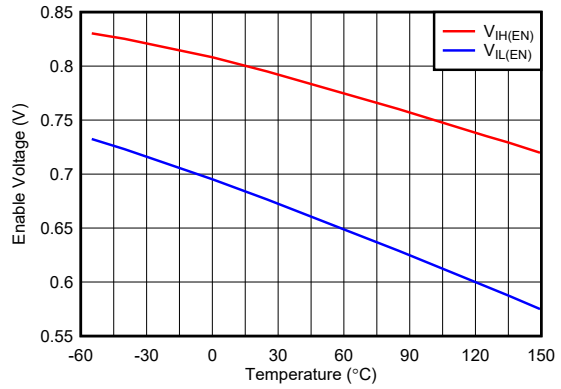


V_{IN} = 1.1V

图 5-34. V_{BIAS} UVLO vs Temperature

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = 1.4V or V_{IN} = $V_{OUT(NOM)}$ + 0.5V (whichever is greater), V_{BIAS} = open, $V_{OUT(NOM)}$ = 0.5V, V_{EN} = 1.1V, C_{OUT} = 47µF, $C_{NR/SS}$ = 0nF, C_{FF} = 0nF, and PG pin pulled up to V_{IN} with 100kΩ (unless otherwise noted)



V_{IN} = 1.4V, 6.5V

图 5-35. Enable Threshold vs Temperature

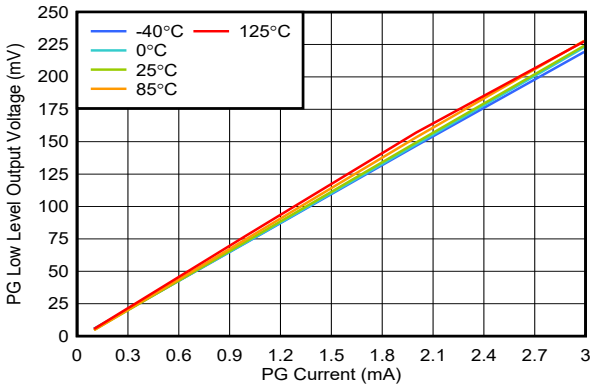
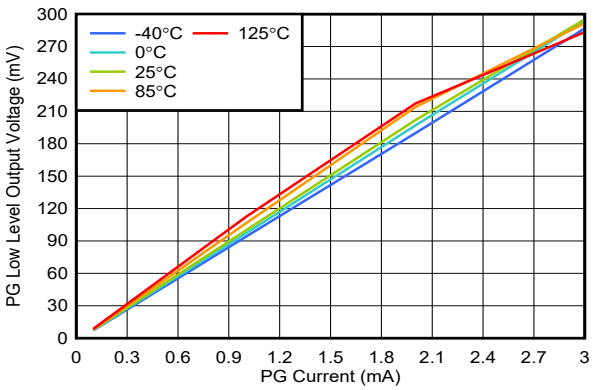


图 5-36. PG Voltage vs PG Current Sink



V_{IN} = 6.5V

图 5-37. PG Voltage vs PG Current Sink Without Bias

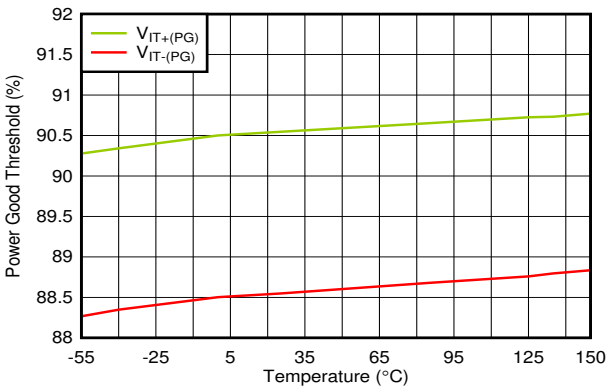
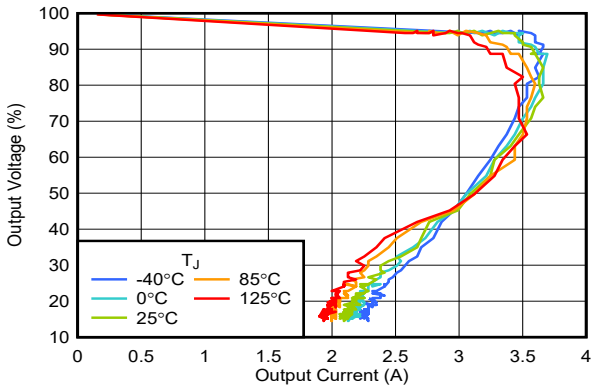


图 5-38. PG Threshold vs Temperature



V_{IN} = 1.1V, V_{BIAS} = 3V

图 5-39. Foldback Current Limit vs Temperature

6 Detailed Description

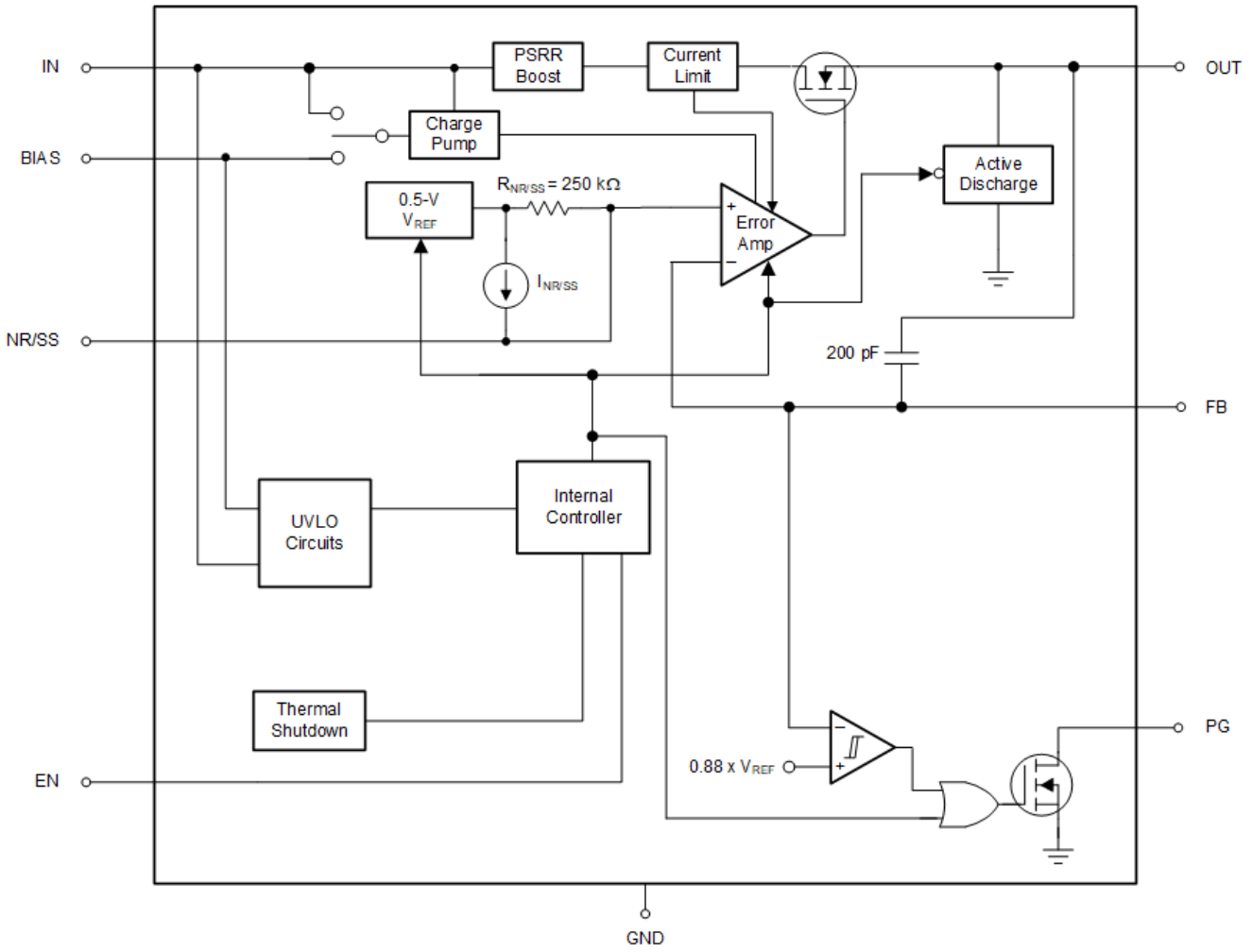
6.1 Overview

The TPS7A53B is a high-current (3A), low-noise (4.6μV_{RMS}), high-accuracy (0.75%) low-dropout linear voltage regulator with an input range of 1.1V to 6.5V and an output voltage range of 0.5V to 5.15V. The TPS7A53B has an integrated charge pump for ease of use, and an external bias rail to allow for the lowest dropout across the entire output voltage range. 表 6-1 categorizes the functions shown in the *Functional Block Diagram*. These features make the TPS7A53B a robust solution to solve many challenging problems by generating a clean, accurate power supply in a variety of applications.

表 6-1. Device Features

VOLTAGE REGULATION	SYSTEM START-UP	INTERNAL PROTECTION
High accuracy	Programmable soft-start	Foldback current limit
Low-noise, high-PSRR output	No sequencing requirement between BIAS, IN, and EN	Thermal shutdown
Fast transient response	Power-good output	
	Start-up with negative bias on OUT	

6.2 Functional Block Diagram



6.3 Feature Description

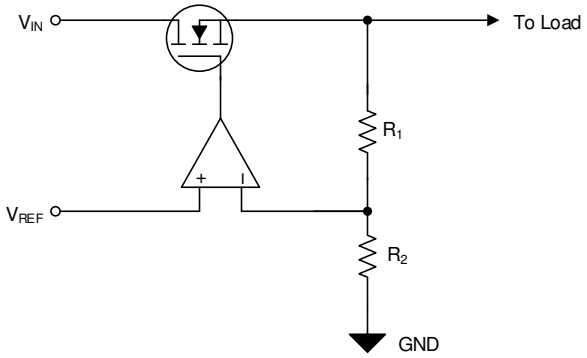
6.3.1 Voltage Regulation Features

6.3.1.1 DC Regulation

A low-dropout regulator (LDO) functions as a class-B amplifier, as shown in 图 6-1, in which the input signal is the internal reference voltage (V_{REF}). V_{REF} is designed to have very low bandwidth at the input to the error amplifier by using a low-pass filter ($V_{NR/SS}$).

As such, the reference can be considered as a pure dc input signal. The low output impedance of an LDO comes from the combination of the output capacitor and pass transistor. The pass transistor also presents a high input impedance to the source voltage when operating as a current source. A positive LDO can only source current because of the class-B architecture.

This device achieves a maximum of 0.75% output voltage accuracy primarily because of the high-precision band-gap voltage (V_{BG}) that creates V_{REF}. The low dropout voltage (V_{DO}) reduces the thermal power dissipation required by the device to regulate the output voltage at a given current level, thereby improving system efficiency. These features combine to make this device a good approximation of an optimal voltage source.



$V_{OUT} = V_{REF} \times (1 + R_1 / R_2)$.

图 6-1. Simplified Regulation Circuit

6.3.1.2 AC and Transient Response

The LDO responds quickly to a transient (large-signal response) on the input supply (line transient) or the output current (load transient) resulting from the LDO high-input impedance and low output impedance across frequency. This same capability also means that the LDO has a high power-supply rejection ratio (PSRR) and, when coupled with a low internal noise-floor (V_n), the LDO approximates an optimal power supply in ac (small-signal) and large-signal conditions.

The choice of external component values optimizes the small- and large-signal response. The NR/SS capacitor ($C_{NR/SS}$) and feed-forward capacitor (C_{FF}) easily reduce the device noise floor and improve PSRR.

6.3.2 System Start-Up Features

In many different applications, the power-supply output must turn on within a specific window of time to either provide proper operation of the load or to minimize the loading on the input supply or other sequencing requirements. The LDO start-up is well-controlled and user-adjustable, solving the demanding requirements faced by many power-supply design engineers in a simple fashion.

6.3.2.1 Programmable Soft-Start (NR/SS Pin)

Soft-start directly controls the output start-up time and indirectly controls the output current during start-up (inrush current).

As shown in 图 6-2, the external capacitor at the NR/SS pin ($C_{NR/SS}$) sets the output start-up time by setting the rise time of the internal reference ($V_{NR/SS}$).

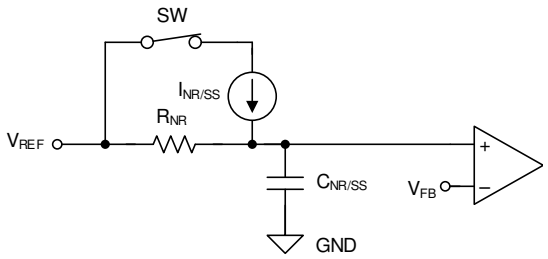


图 6-2. Simplified Soft-Start Circuit

6.3.2.2 Internal Sequencing

Controlling when a single power supply turns on can be difficult in a power distribution network (PDN), because of the high power levels inherent in a PDN and the variations between the supplies. As shown in 图 6-3 and 表 6-2, the LDO turn-on and turn-off time is set by the enable circuit (EN) and undervoltage lockout circuits ($UVLO_{1,2(IN)}$ and $UVLO_{BIAS}$).

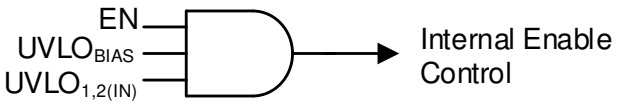


图 6-3. Simplified Turn-On Control

表 6-2. Internal Sequencing Functionality Table

INPUT VOLTAGE	BIAS VOLTAGE	ENABLE STATUS	LDO STATUS	ACTIVE DISCHARGE	POWER GOOD
$V_{IN} \geq V_{UVLO\_1,2(IN)}$	$V_{BIAS} \geq V_{UVLO(BIAS)}$	EN = 1	On	Off	PG = 1 when $V_{OUT} \geq V_{IT(PG)}$
		EN = 0	Off	On	PG = 0
	$V_{BIAS} < V_{UVLO(BIAS)} + V_{HYS(BIAS)}$	EN = Don't care	Off	On(1)	
$V_{IN} < V_{UVLO\_1,2(IN)} - V_{HYS1,2(IN)}$	BIAS = Don't care		Off		
IN = Don't care	$V_{BIAS} \geq V_{UVLO(BIAS)}$		Off		

(1) The active discharge remains on as long as V_{IN} or V_{BIAS} provide enough headroom for the discharge circuit to function.

6.3.2.2.1 Enable (EN)

The enable signal (V_{EN}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geqslant V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leqslant V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. Connect EN to V_{IN} if enable functionality is not needed.

6.3.2.2.2 Undervoltage Lockout (UVLO) Control

The UVLO circuits respond quickly to glitches on IN or BIAS and attempts to disable the output of the device if either of these rails collapse.

6.3.2.2.3 Active Discharge

When either EN or UVLO are low, the device connects a resistor of several hundred ohms from V_{OUT} to GND, discharging the output capacitance.

Do not rely on the active discharge circuit for discharging large output capacitors when the input voltage drops below the targeted output voltage. Current flows from the output to the input (reverse current) when $V_{OUT} > V_{IN}$, which can cause damage to the device (when $V_{OUT} > V_{IN} + 0.3V$).

6.3.2.3 Power-Good Output (PG)

The PG signal provides an easy solution to meet demanding sequencing requirements because PG signals when the output nears the nominal value. PG can be used to signal other devices in a system when the output voltage is near, at, or above the set output voltage ($V_{OUT(nom)}$). 图 6-4 shows a simplified schematic.

The PG signal is an open-drain digital output that requires a pullup resistor to a voltage source and is active high. The PG circuit sets the PG pin into a high-impedance state to indicate that the power is good.

Using a large feed-forward capacitor (C_{FF}) delays the output voltage and, because the PG circuit monitors the FB pin, the PG signal can indicate a false positive.

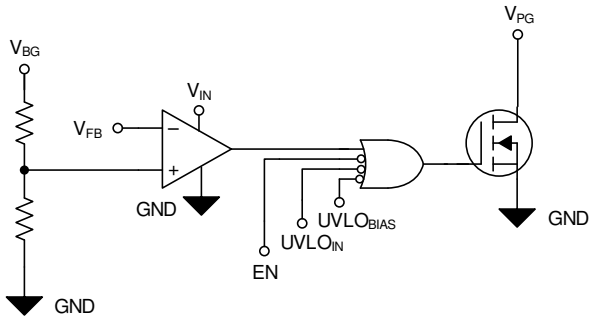


图 6-4. Simplified PG Circuit

6.3.3 Internal Protection Features

In many applications, fault events can occur that damage devices in the system. Short circuits and excessive heat are the most common fault events for power supplies. The TPS7A53B implements circuitry to protect the device and the load during these events. Do not continuously operate in these fault conditions or above a junction temperature of 140°C because the long-term reliability of the device is reduced.

6.3.3.1 Foldback Current Limit (I_{CL})

The internal current limit circuit protects the LDO against high load-current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. For proper operation of the current limit, minimize the inductances to the input and load. Do not run continuous operation in current limit.

6.3.3.2 Thermal Protection (T_{sd})

The thermal shutdown circuit protects the LDO against excessive heat in the system, either resulting from current limit or high ambient temperature.

The output of the LDO turns off when the LDO temperature (junction temperature, T_J) exceeds the rising thermal shutdown temperature. The output turns on again after T_J decreases below the falling thermal shutdown temperature.

A high power dissipation across the device, combined with a high ambient temperature (T_A), can cause T_J to be greater than or equal to T_{sd}, triggering the thermal shutdown and causing the output to fall to 0V. The LDO can cycle on and off when thermal shutdown is reached under these conditions.

6.4 Device Functional Modes

表 6-3 provides a quick comparison between the regulation and disabled operation.

表 6-3. Device Functional Modes Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	EN	I_{OUT}	T_J
Regulation(1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{BIAS} \geq V_{UVLO(BIAS)}$ (3)	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J \leq T_{J(maximum)}$
Disabled(2)	$V_{IN} < V_{UVLO\_1,2(IN)}$	$V_{BIAS} < V_{UVLO(BIAS)}$	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.
(3) V_{BIAS} is only required for V_{IN} < 1.4V.

6.4.1 Regulation

The device regulates the output to the nominal output voltage when all conditions in 表 6-3 are met.

6.4.2 Disabled

When disabled, the pass transistor is turned off, the internal circuits are shut down, and the output voltage is actively discharged to ground by an internal resistor from the output to ground. See the *Active Discharge* section for additional information.

6.4.3 Current Limit Operation

During a current-limit event, the LDO regulates the output current instead of the output voltage. Therefore, the output voltage falls with decreased load impedance.

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

7.1.1 Recommended Capacitor Types

The TPS7A53B is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 4). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (V_{IN} = 5.5V to V_{OUT} = 5.0V), the derating can be greater than 50%, and must be taken into consideration.

7.1.1.1 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A53B is designed and characterized for operation with ceramic capacitors of 47µF or greater (22µF or greater of capacitance) at the output and 10µF or greater (5µF or greater of capacitance) at the input. Use at least a 47µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins to minimize trace parasitics. If the trace inductance from the input supply to the TPS7A53B is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by additional input capacitors to dampen and keep the ringing below the device absolute maximum ratings.

A combination of multiple output capacitors boosts the high-frequency PSRR. The combination of one 0805-sized, 47µF ceramic capacitor in parallel with two 0805-sized, 10µF ceramic capacitors with a sufficient voltage rating (in conjunction with the PSRR boost circuit) optimizes PSRR for the frequency range of 400kHz to 700kHz, a typical range for dc/dc supply switching frequency. This 47µF || 10µF || 10µF capacitor combination also makes certain that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47µF ceramic capacitors have a voltage derating of approximately 60% to 80% at 5.0V, so the addition of the two 10µF capacitors makes sure that the capacitance is at or above 22µF.

7.1.1.2 Noise-Reduction and Soft-Start Capacitor ($C_{NR/SS}$)

The TPS7A53B features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ($C_{NR/SS}$). Use an external $C_{NR/SS}$ to minimize inrush current into the output capacitors. This soft-start feature eliminates power-up initialization problems when powering field-programmable gate arrays (FPGAs), digital signal processors (DSPs), or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a monotonic start-up, the TPS7A53B error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage approaches the internal reference. The soft-start ramp time depends on the soft-start charging current ($I_{NR/SS}$), the soft-start capacitance ($C_{NR/SS}$), and the internal reference ($V_{NR/SS}$). Use 方程式 1 to calculate the soft-start ramp time:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (1)$$

$I_{NR/SS}$ is provided in the *Electrical Characteristics* table and has a typical value of 6.2 μA.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low-pass filter (LPF) that filters out noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and 方程式 2 calculates the cutoff frequency. The typical value of R_{NR} is 250kΩ. Increasing the $C_{NR/SS}$ capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, use a 10nF to 1μF $C_{NR/SS}$.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR} \times C_{NR/SS}) \quad (2)$$

7.1.1.3 Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled. For a detailed description, see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note.

7.1.2 Soft-Start and Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO achieve threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current into the LDO at the IN pin during start-up. Inrush current then consists primarily of the sum of load current and the current used to charge the output capacitor. This current is difficult to measure because the input capacitor must be removed, which is not recommended. However, 方程式 3 can estimate this soft-start current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (3)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the V_{OUT} ramp
- R_{LOAD} is the resistive load impedance

7.1.3 Optimizing Noise and PSRR

Improve the ultra-low noise floor and PSRR of the device by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range
- C_{FF} in the mid-band frequency range
- C_{OUT} for the high-frequency range
- V_{IN} – V_{OUT} for all frequencies
- V_{BIAS} at lower input voltages

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. To improve mid-band PSRR, use the feed-forward capacitor to place a zero-pole pair near the edge of the loop bandwidth and push out the loop bandwidth. Use larger output capacitors to improve high-frequency PSRR.

A higher input voltage improves PSRR by giving the device more headroom to respond to noise on the input. A bias rail also improves PSRR at lower input voltages because greater headroom is provided for the internal circuits.

The noise-reduction capacitor filters out low-frequency noise from the reference, and the feed-forward capacitor reduces output voltage noise by filtering out mid-band frequency noise. However, a large feed-forward capacitor can create new issues that are discussed in the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note.

Use a large output capacitor to reduce high-frequency output voltage noise. Additionally, a bias rail or higher input voltage improves noise because greater headroom is provided for the internal circuits.

表 7-1 lists the output voltage noise for the 10Hz to 100kHz band at a 5.0V output for a variety of conditions with an input voltage of 5.5V, an R_1 of 12.1kΩ, and a load current of 3.0A. The 5.0V output is used because this output is the worst-case condition for output voltage noise.

表 7-1. Output Noise Voltage at a 5.0V Output

OUTPUT VOLTAGE NOISE (μV_{RMS})	$C_{NR/SS}$ (nF)	C_{FF} (nF)	C_{OUT} (µF)
11.7	10	10	47 || 10 || 10
7.7	100	10	47 || 10 || 10
6	100	100	47 || 10 || 10
7.4	100	10	1000
5.8	100	100	1000

7.1.4 Charge Pump Noise

The device internal charge pump generates a minimal amount of noise. Use a bias rail to minimize the internal charge pump noise when the internal voltage is clamped, thereby reducing the overall output noise floor.

The high-frequency components of the output voltage noise density curve are filtered out in most applications by using 10nF to 100nF bypass capacitors close to the load. Using a ferrite bead between the LDO output and the load input capacitors forms a pi-filter, further reducing the high-frequency noise contribution.

7.1.5 Current Sharing

There are two main current sharing implementations:

1. Through the use of external ballast resistors. For more details of this implementation, see the *Scalable, High-Current, Low-Noise Parallel LDO Reference Design* design guide, *Parallel LDO Architecture Design Using Ballast Resistors* white paper, and *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors* white paper.
2. Through the use of external operational amplifiers. For more details, see the *Current-Sharing Dual LDOs* design guide and *6 A Current-Sharing Dual LDO* design guide.

7.1.6 Adjustable Operation

As shown in 图 7-1, the output voltage of the TPS7A53B is set using external resistors.

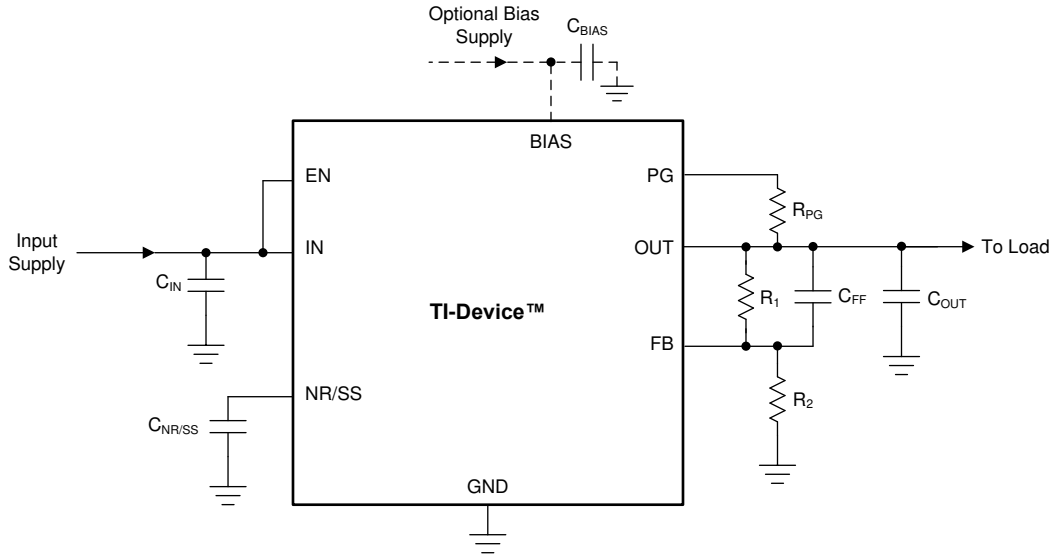


图 7-1. Adjustable Operation

Use 方程式 4 to calculate R_1 and R_2. This resistive network must provide a current equal to or greater than 5 μA for dc accuracy. To optimize noise and PSRR, use an R_1 of 12.1kΩ.

$$V_{OUT} = V_{NR/SS} \times (1 + R_1 / R_2) \quad (4)$$

表 7-2 shows the resistor combinations required to achieve several common rails using standard 1%-tolerance resistors.

表 7-2. Recommended Feedback-Resistor Values(1)

TARGETED OUTPUT VOLTAGE (V)	FEEDBACK RESISTOR VALUES		CALCULATED OUTPUT VOLTAGE (V)
	R_1 (kΩ)	R_2 (kΩ)	
0.6	12.4	62	0.600
0.7	12.4	31.2	0.699
0.75	12.4	24.8	0.750
0.8	12.4	20.8	0.799
0.9	12.4	15.5	0.90
1.0	12.4	12.4	1.00
1.05	12.4	11.3	1.048
1.1	12.4	10.4	1.096
1.2	12.4	8.87	1.19
1.5	12.4	6.2	1.50
1.8	12.4	4.7	1.81
3.30	12.4	2.21	3.30
5.00	12.4	1.38	4.99

(1) R_1 is connected from OUT to FB; R_2 is connected from FB to GND.

7.1.7 Power-Good Operation

For proper operation of the power-good circuit, the pullup resistor value must be between 10kΩ and 100kΩ. The lower limit of 10kΩ results from the maximum pulldown strength of the power-good transistor, and the upper limit of 100kΩ results from the maximum leakage current at the power-good node. If the pullup resistor is outside this range, then the power-good signal can possibly be unable to read a valid digital logic level.

Using a large C_{FF} with a small $C_{NR/SS}$ causes the power-good signal to incorrectly indicate that the output voltage has settled during turn-on. The C_{FF} time constant must be greater than the soft-start time constant for proper operation of the PG during start-up. For a detailed description, see the *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note.

The state of PG is only valid when the device operates above the minimum supply voltage. During short UVLO events and at light loads, power-good does not assert because the output voltage is sustained by the output capacitance.

7.1.8 Undervoltage Lockout (UVLO) Operation

The UVLO circuit makes sure that the device remains disabled before the input or bias supplies reach the minimum operational voltage range, and that the device shuts down when the input supply or bias supply falls too low.

The UVLO circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.8V causes the UVLO to assert for a short time; however, the UVLO circuit does not have enough stored energy to fully discharge the internal circuits inside the device. When the UVLO circuit does not fully discharge, the internal circuits of the output are not fully disabled.

The effect of the downward line transient can be mitigated by either using a larger input capacitor to limit the fall time of the input supply when operating near the minimum V_{IN}, or by using a bias rail.

图 7-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output can fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

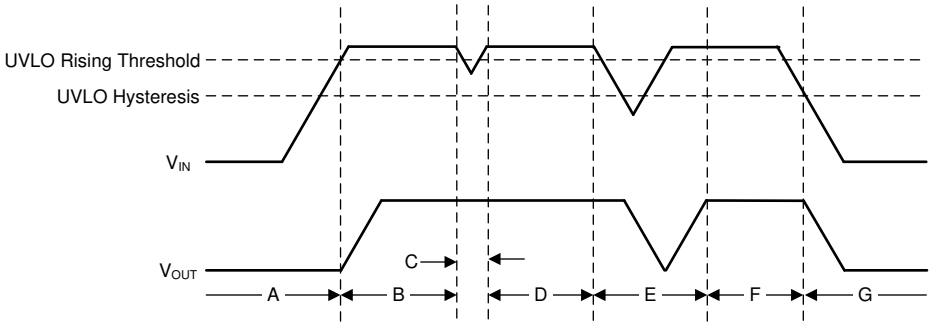


图 7-2. Typical UVLO Operation

7.1.9 Dropout Voltage (V_{DO})

Generally, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} - V_{OUT}$) required for regulation. When V_{IN} drops below the required V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. Dropout voltage is proportional to the output current because the device is operating as a resistive switch.

Dropout voltage is affected by the drive strength for the gate of the pass transistor, which is nonlinear with respect to V_{IN} on this device because of the internal charge pump. The charge pump causes a higher dropout voltage at lower input voltages when a bias rail is not used.

For this device, dropout voltage increases exponentially when the input voltage nears the maximum operating voltage because the charge pump is internally clamped to 8.0V.

7.1.10 Device Behavior During Transition From Dropout Into Regulation

Some applications have transients that place the device into dropout, especially with a device such as a high-current linear regulator. A typical application with these transient conditions can require setting $V_{IN} \leqslant (V_{OUT} + V_{DO})$ to keep the device junction temperature within the specified operating range. A load transient or line transient with these conditions can place the device into dropout (for example, a load transient from 1A to 3A at 1A/µs when operating with a V_{IN} of 5.4V and a V_{OUT} of 5.0V).

The load transient saturates the error amplifier output stage when the gate of the pass transistor is driven as high as possible by the error amplifier, thus making the pass transistor function as a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient (I_{OUT} = 3A to 1A at 1A/µs) is limited because the error amplifier must first recover from saturation, and then place the pass transistor back into active mode. During recovery from the load transient, V_{OUT} overshoots because the pass transistor is functioning as a resistor from V_{IN} to V_{OUT}. If operating under these conditions, apply a higher dc load or increase the output capacitance to reduce the overshoot.

7.1.11 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 图 7-3 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

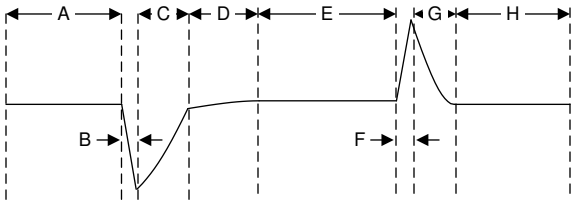


图 7-3. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)

- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the TPS7A53B is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This different output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.12 Reverse Current Protection Considerations

As with most LDOs, this device can be damaged by excessive reverse current.

Conditions where excessive reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3V$:

- If the device has a large C_{OUT}, then the input supply collapses quickly and the load current becomes very small
- The output is biased when the input supply is not established
- The output is biased above the input supply

If an excessive reverse current flow is expected in the application, then external protection must be used to protect the device. 图 7-4 shows one approach of protecting the device.

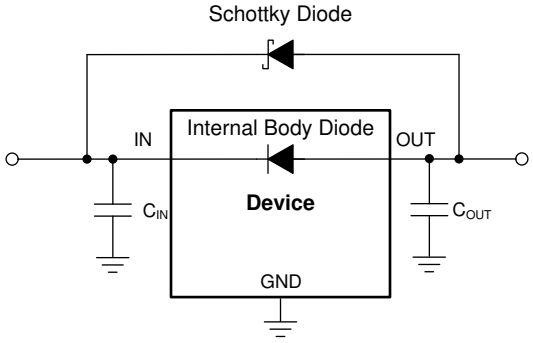


图 7-4. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.13 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 方程式 5 calculates P_D:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (5)$$

备注

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A53B allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 方程式 6. The equation is rearranged for output current in 方程式 7.

$$T_J = T_A = (R_{\theta JA} \times P_D) \quad (6)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (7)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance.

7.1.14 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 方程式 8 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (8)$$

where:

- P_D is the power dissipated as explained in 方程式 5
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.1.15 TPS7A53EVM Thermal Analysis

The RPS package is a 2.2mm × 2.5mm, 12-pin VQFN with 25µm plating on each via. The EVM is a 3 inch by 3 inch (7.62 mm × 7.62 mm) PCB comprised of four layers. 表 7-3 lists an overview of the EVM stackup. 图 7-5 to 图 7-9 provide layer details for the EVM.

表 7-3. Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.40
3	Top layer	Copper	1.40
4	Dielectric 1	FR-4, high T_G	18.50
5	Mid layer 1	Copper	1.40
6	Dielectric 2	FR-4, high T_G	18.60
7	Mid layer 2	Copper	1.40
8	Dielectric 3	FR-4, high T_G	18.50
9	Bottom layer	Copper	1.40
10	Bottom solder	Solder resist	0.40

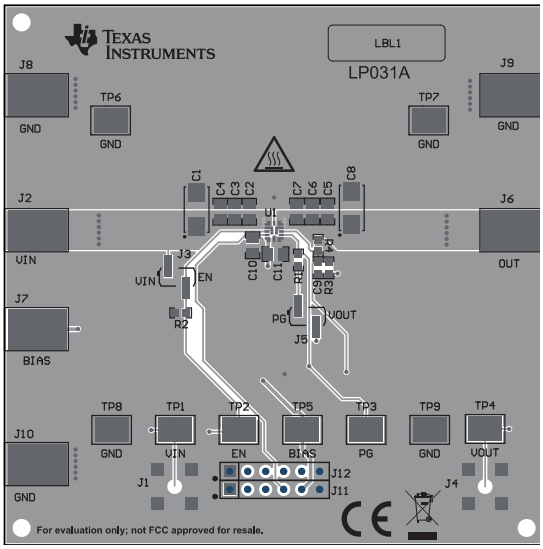


图 7-5. Top Composite View

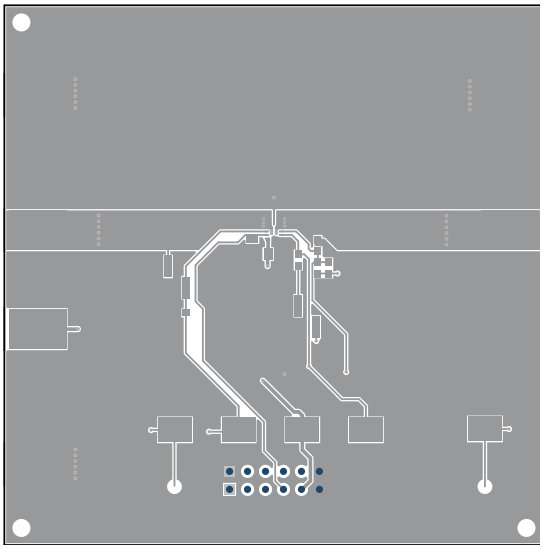


图 7-6. Top Layer Routing

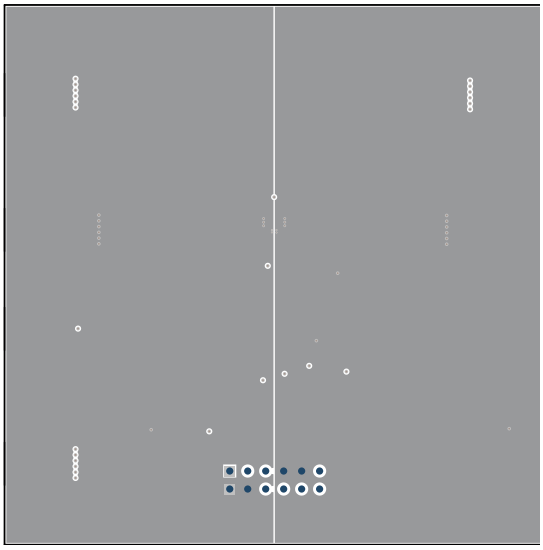


图 7-7. Mid Layer 1 Routing

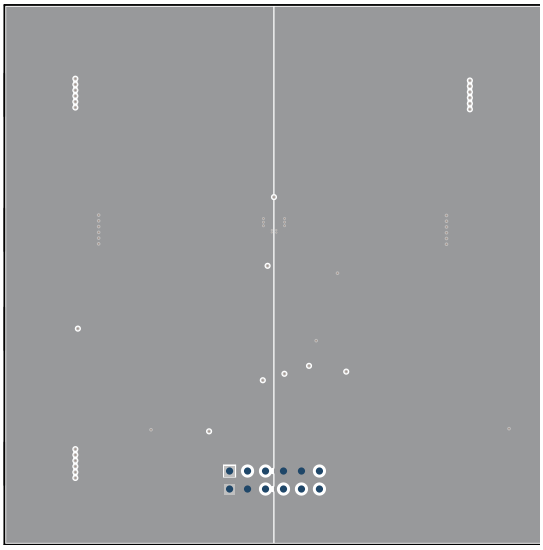


图 7-8. Mid Layer 2 Routing

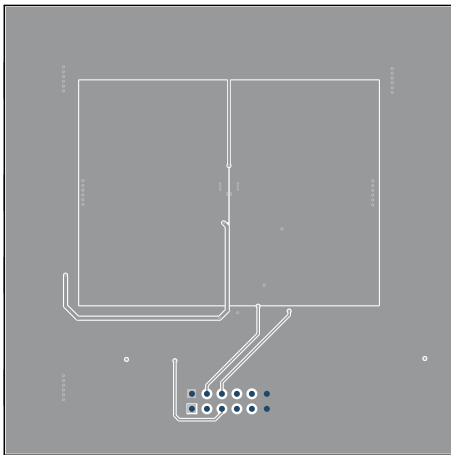


图 7-9. Bottom Layer Routing

图 7-10 shows the thermal gradient on the PCB that results when using a 1W power dissipation through the pass transistor with a 25°C ambient temperature.

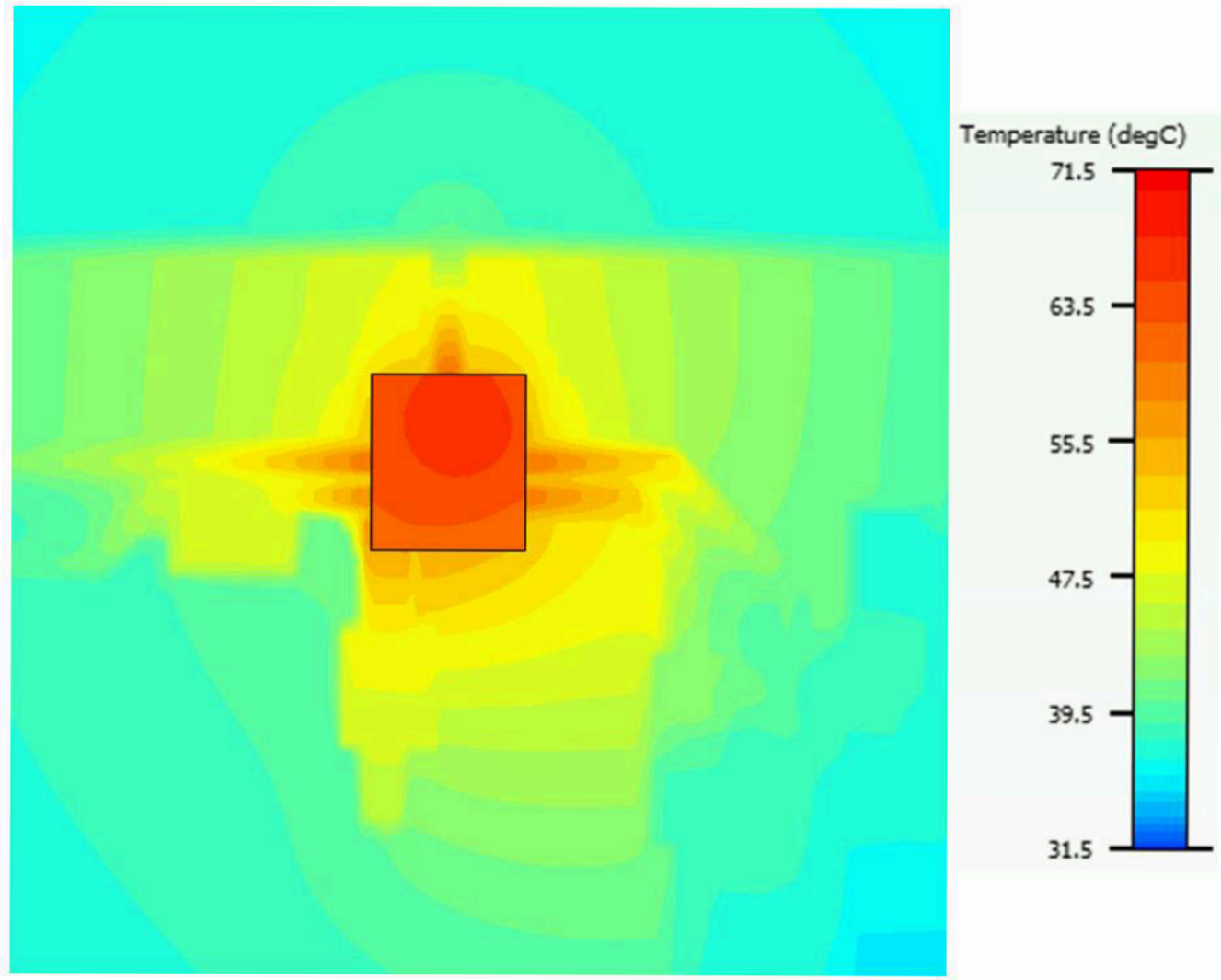


图 7-10. PCB Thermal Gradient

For additional information on the PCB, see the *TPS7A53EVM-031 Evaluation Module* user guide.

7.2 Typical Application

This section discusses the implementation of the TPS7A53B using an adjustable feedback network to regulate a 3A load requiring good PSRR at high frequency with low noise at an output voltage of 0.9V. 图 7-11 provides a schematic for this typical application circuit.

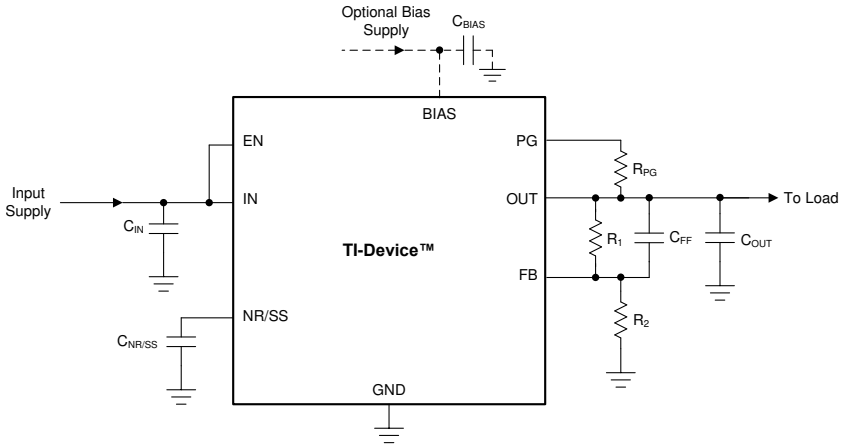


图 7-11. Typical Application for a 0.9V Rail

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-4 as the input parameters.

表 7-4. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.2V, ±3%, provided by the dc/dc converter switching at 500kHz
Bias voltage	5V, ±5%
Output voltage	0.9V, ±1%
Output current	3.0A (maximum), 100mA (minimum)
RMS noise, 10Hz to 100kHz	< 10μV_{RMS}
PSRR at 500kHz	> 40dB
Start-up time	< 25ms

7.2.2 Detailed Design Procedure

At 3.0A and given a V_{BIAS} of 5.0V, the TPS7A53B has a 110mV maximum dropout over temperature, Thus, a 300mV headroom is sufficient for operation over both input and output voltage accuracy. At full load and high temperature on some devices, the TPS7A53B can enter dropout if both the input and output supply are beyond the edges of the respective accuracy specification.

For a 0.9V output, use external adjustable resistors. See the resistor values listed in 表 7-2 for choosing resistors for a 0.9V output.

Input and output capacitors are selected in accordance with the *Recommended Capacitor Types* section. Ceramic capacitances of 47μF for the input and one 47μF capacitor in parallel with two 10μF capacitors for the output are selected.

To satisfy the required start-up time and still maintain low noise performance, a 100nF $C_{NR/SS}$ is selected. 方程式 9 calculates this value.

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (9)$$

At the 3.0A maximum load, the internal power dissipation is 0.9W and corresponds to a 61.8°C junction temperature rise for the RPS package on a standard JEDEC board. With a 55°C maximum ambient temperature, the junction temperature is at 116.8°C. To further minimize noise, a feed-forward capacitance (C_{FF}) of 10nF is selected.

7.2.3 Application Curves

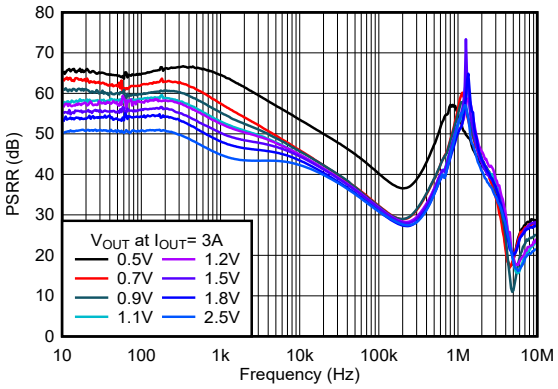


图 7-12. PSRR vs Frequency and V_{OUT} With Bias

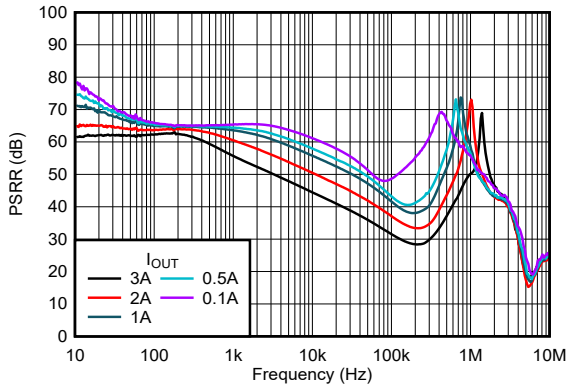


图 7-13. PSRR vs Frequency and I_{OUT}

7.3 Power Supply Recommendations

The TPS7A53B is designed to operate from an input voltage supply range between 1.1V and 6.5V. If the input supply is less than 1.4V, then a bias rail of at least 3.0V must be used. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, use additional input capacitors with low ESR to help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Board Layout

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in 图 7-14 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane provides accuracy of the output voltage, shields noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example

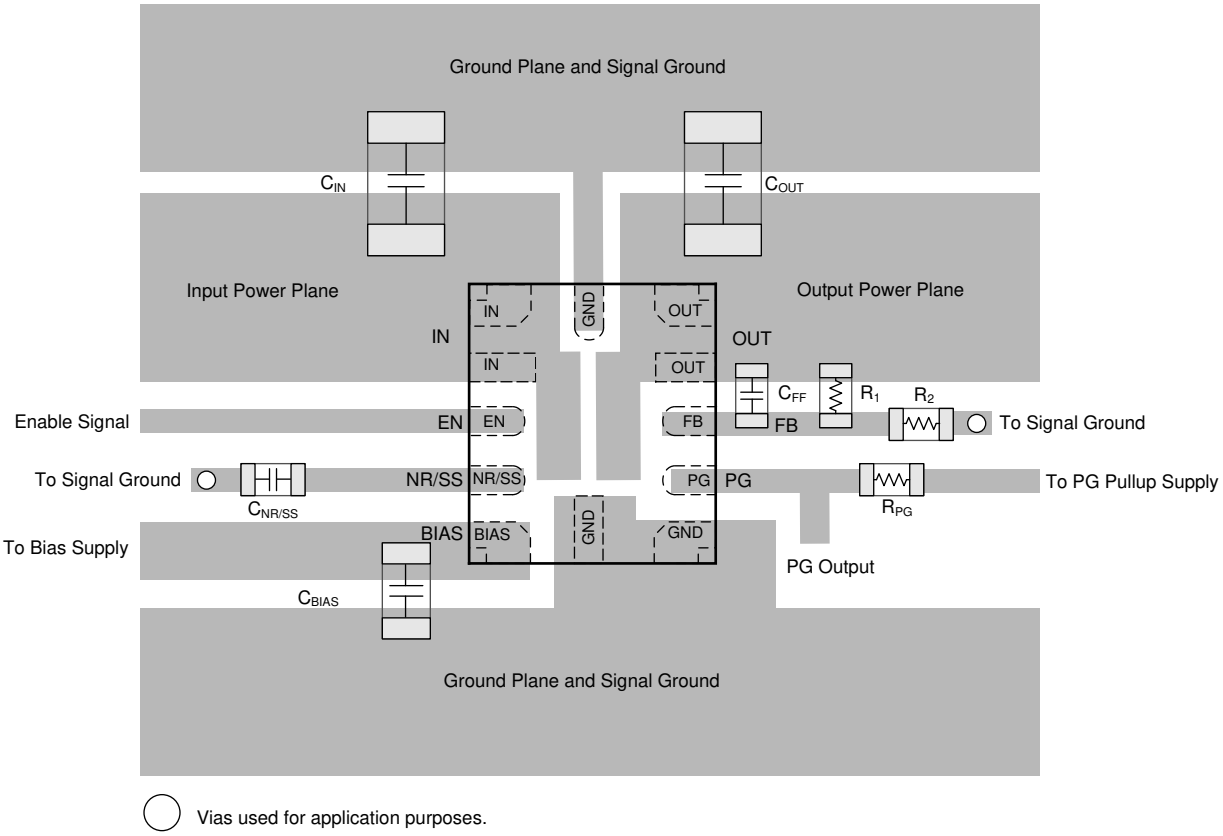


图 7-14. Example Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Ordering Information(1)

PRODUCT	DESCRIPTION
TPS7A5301B**YYYZ**	**YYY** is the package designator. **Z** is the package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS3702 High-Accuracy, Overvoltage and Undervoltage Monitor* data sheet
- Texas Instruments, *TPS7A53EVM-031 Evaluation Module* user guide
- Texas Instruments, *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application note
- Texas Instruments, *Scalable, High-Current, Low-Noise Parallel LDO Reference Design* design guide

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.5 Trademarks

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8.6 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2023) to Revision A (January 2024)	Page
• 将文档状态从 *预告信息* 更改为 *量产数据*	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A5301BRPSR	ACTIVE	VQFN-HR	RPS	12	3000	RoHS & Green	MATTE SN	Level-2-260C-1 YEAR	-40 to 125	39BH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

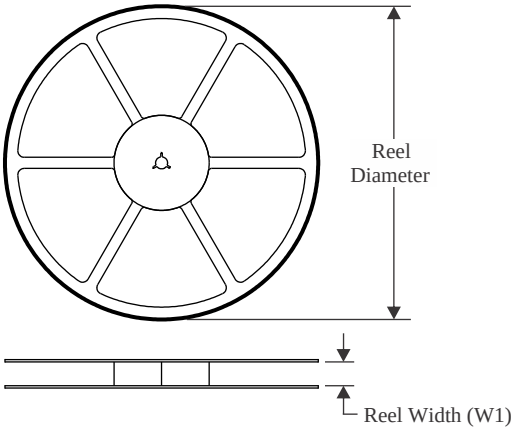
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

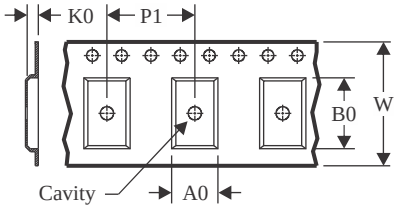
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

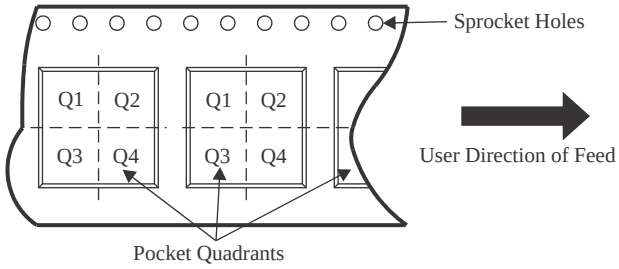


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

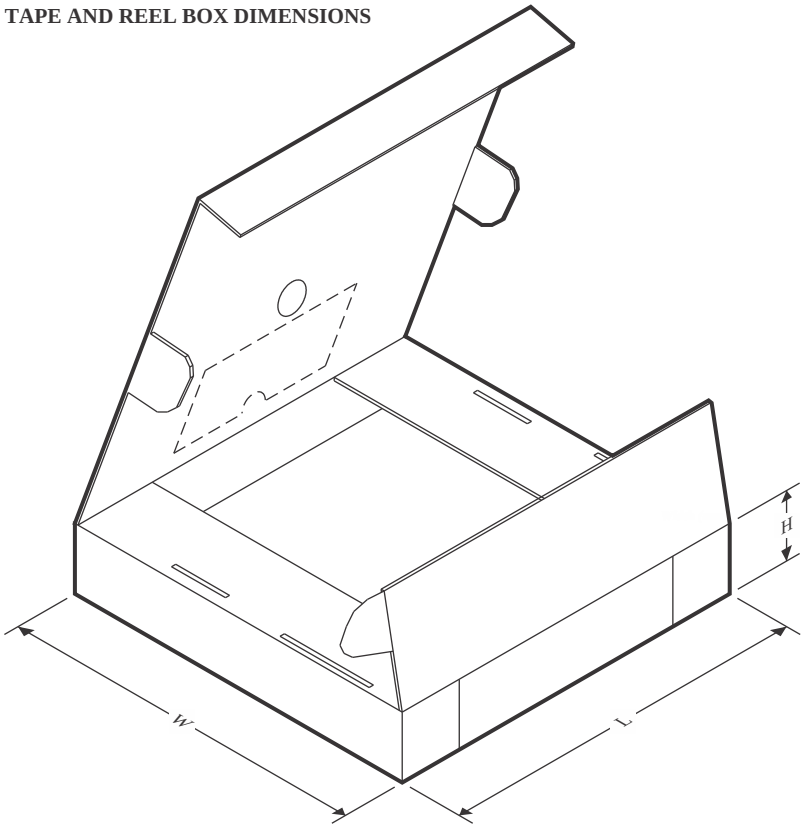
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A5301BRPSR	VQFN-HR	RPS	12	3000	180.0	12.4	2.45	2.75	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

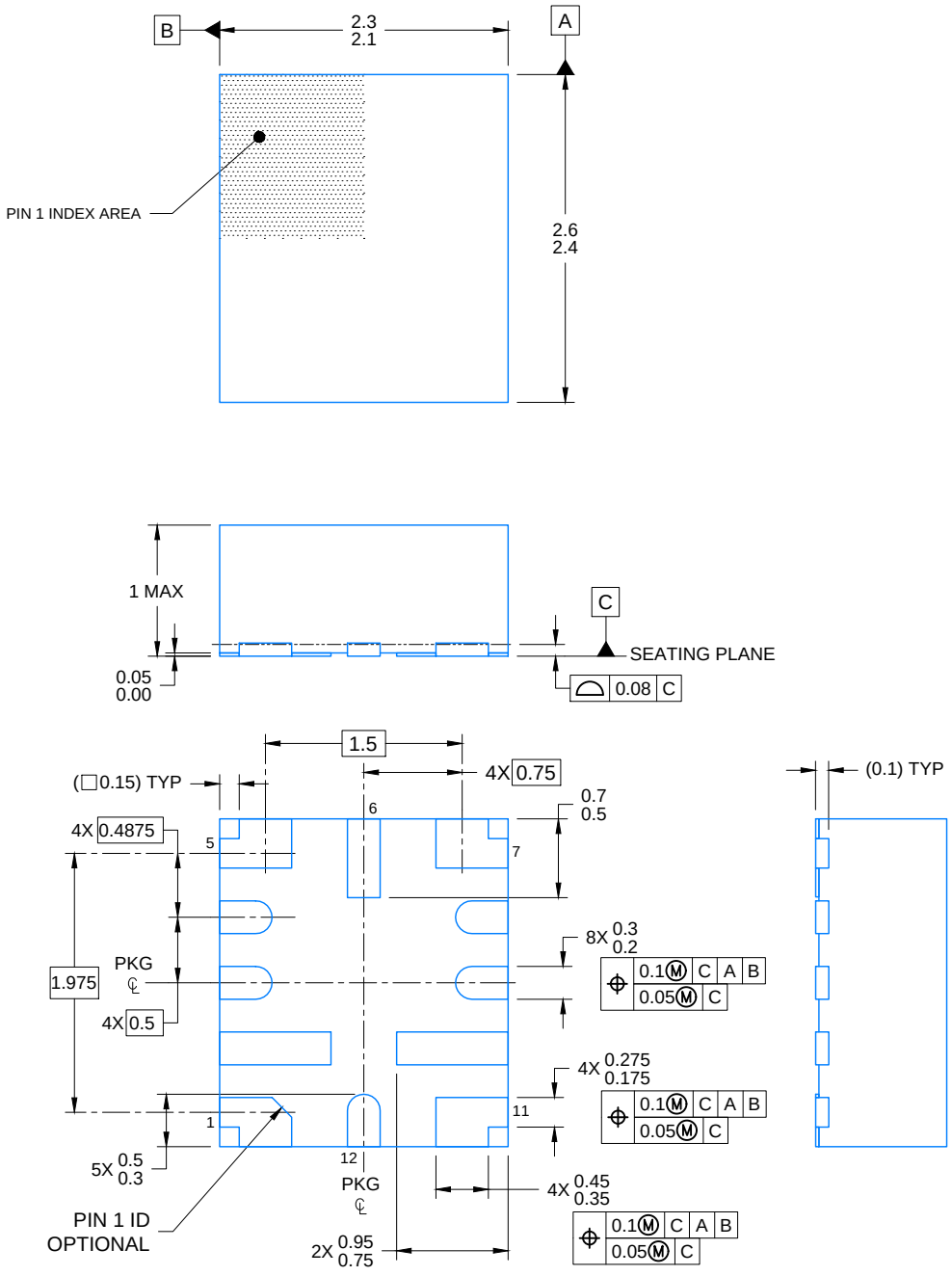
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A5301BRPSR	VQFN-HR	RPS	12	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPS0012A

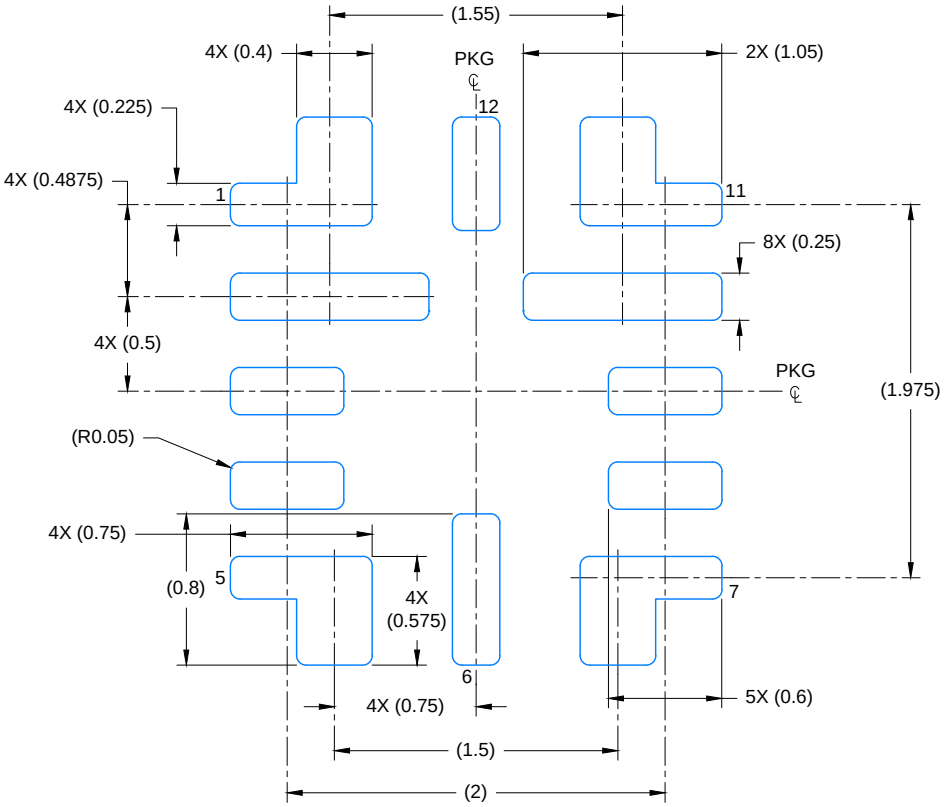
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

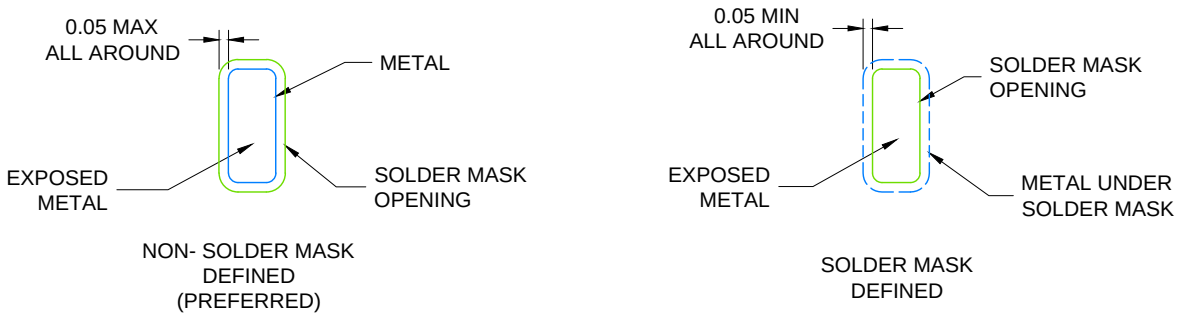
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 25X

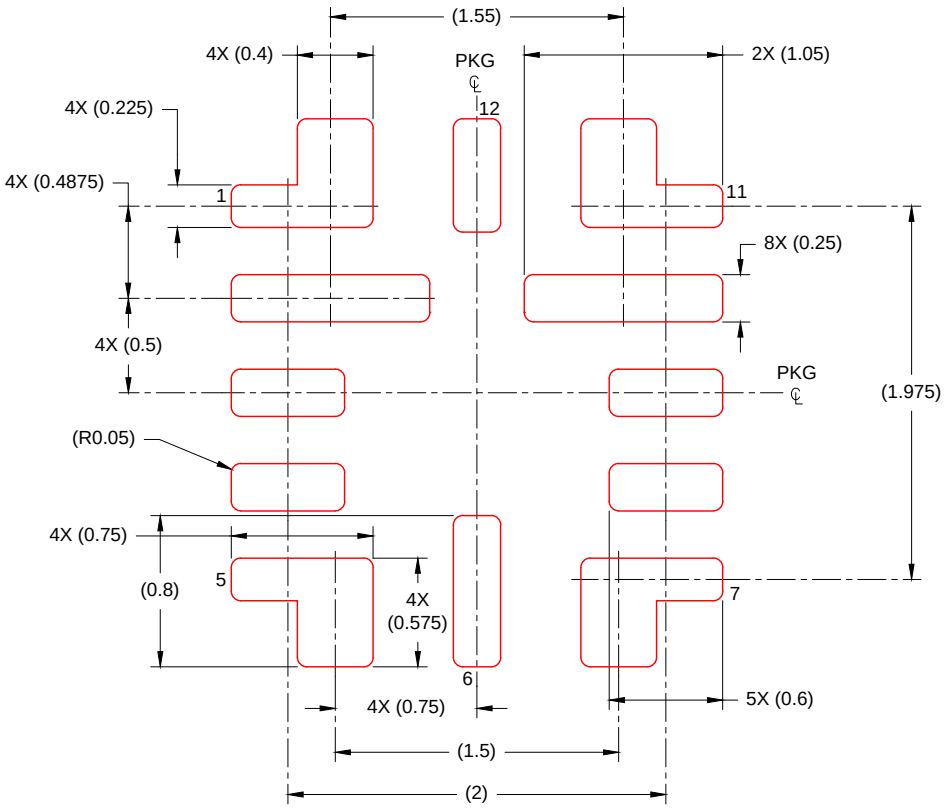


SOLDER MASK DETAILS

4224847/A 03/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4224847/A 03/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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