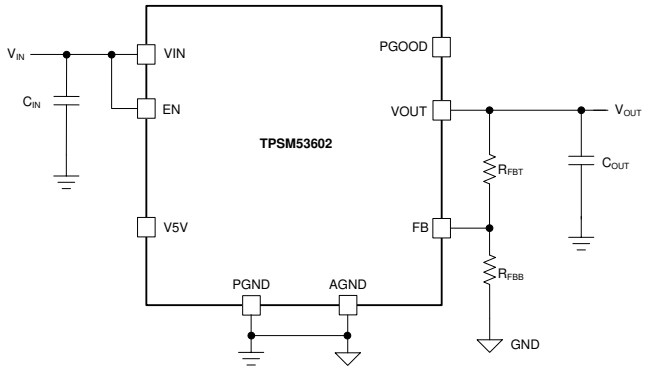
TPSM53602 采用 Enhanced HotRod™ QFN 封装的 36V 输入、2A 电源模块

1 特性

- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 5mm × 5.5mm × 4mm 增强型 HotRod™ QFN 封装
  - 85mm^2 解决方案尺寸（单面）
  - 低 EMI：符合 CISPR11 辐射发射标准
  - 优异的热性能：
    在 85°C 且无气流的情况下具有高达 14W 的输出功率
  - 标准封装尺寸：单个大型散热焊盘和所有引脚均分布在封装外围
- 输入电压范围：3.8V 至 36V
- 输出电压范围：1 V 至 7 V
- 效率高达 95%
- 电源正常状态标志
- 精密使能端
- 内置断续模式短路保护、过热保护、启动至预偏置输出、软启动和 UVLO
- IC 工作结温范围：–40°C 至 +125°C
- 工作环境温度范围：-40°C 至 +105°C
- 通过了 Mil-STD-883D 冲击和振动测试
- 与以下器件引脚兼容：3A TPSM53603 和 4A TPSM53604
- 使用 TPSM53602 并借助 WEBENCH® Power Designer 创建定制设计方案
- 下载 EVM 设计文件以快速进行电路板设计

2 应用

- 通用宽输入电压电源
- 工厂自动化和控制
- 测试和测量
- 航天和国防
- 负输出电压应用



简化版原理图

3 说明

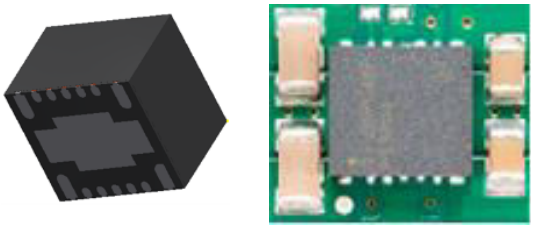
TPSM53602 电源模块是一款高度集成的 2A 电源解决方案，在热增强型 QFN 封装内整合了一个带有功率 MOSFET 的 36V 输入降压直流/直流转换器、一个屏蔽式电感器和多个无源器件。此 5mm × 5.5mm × 4mm、15 引脚封装采用*增强型 HotRod QFN* 技术来实现增强的热性能、小尺寸和低 EMI。该封装尺寸的所有引脚均分布在外围，具有单个大散热垫，实现简单的布局和制造中的轻松处理。

总体解决方案仅需四个外部组件，并且省去了设计流程中的环路补偿和磁性元件选择过程。TPSM53602 具有全套功能集，包括正常电源状态指示、可编程 UVLO、预偏置启动、过流和过热保护，因此是为各种应用供电的出色器件。

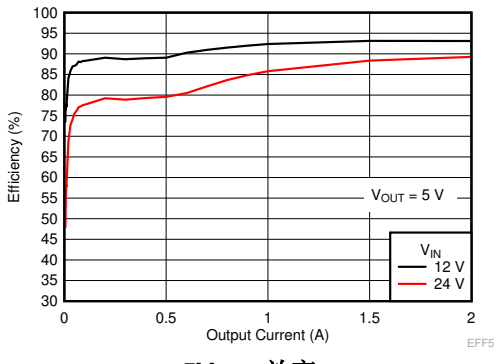
器件信息

器件型号 (1)	封装	封装尺寸（标称值）
TPSM53602	B3QFN (15)	5.0mm × 5.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



增强型 HotRod QFN 和典型布局



5V_{OUT} 效率

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (August 2020) to Revision B (September 2021)	Page
• 添加了功能安全项目符号	1

Changes from Revision * (December 2019) to Revision A (August 2020)	Page
• 将封装信息更新为正确的封装类型	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

5 Pin Configuration and Functions

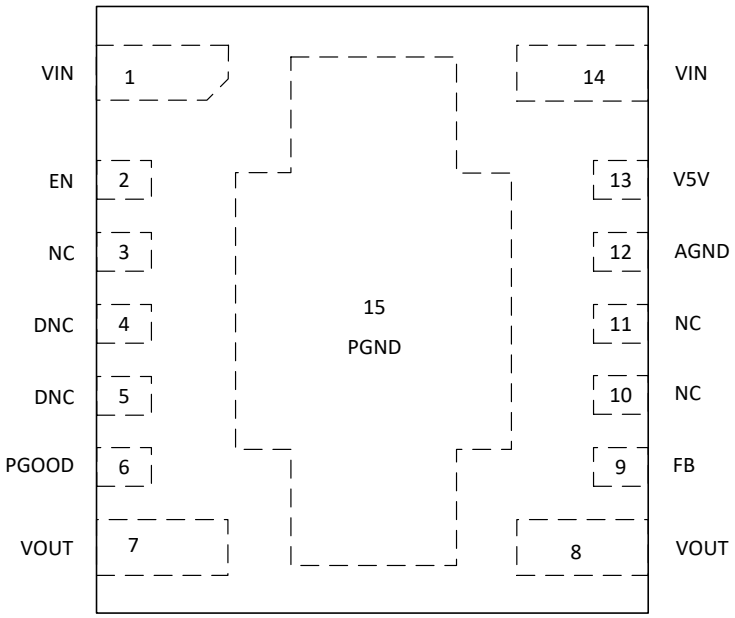


图 5-1. RDA Package 15-Pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
12	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. **This pin must be connected to PGND at a single point.** See 节 10 for a recommended layout.
4, 5	DNC	—	Do not connect. Do not connect these pins to ground, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
2	EN	I	Enable pin. This pin turns the converter on when pulled high and turns off the converter when pulled low. This pin can be connected directly to VIN. **Do not float.** This pin can be used to set the input under voltage lockout with two resistors. See 节 7.3.6.
9	FB	I	Feedback input. Connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
3, 10, 11	NC	—	Not connected. These pins are not connected to any circuitry within the module. It is recommended that these pins be connected to the PGND plane on the application board to enhance shielding and thermal performance.
15	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See 节 10 for a recommended layout.
6	PGOOD	O	Power-good pin. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required and can be tied to the V5V pin or other DC voltage less than 22 V. If not used, this pin can be left open or connected to PGND.
1, 14	VIN	I	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device.
7, 8	VOUT	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
13	V5V	O	Internal 5-V LDO output. Supplies internal control circuits. Do not connect to external loads. This pin can be used as logic supply for PGOOD pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	38	V
	EN to AGND(2)	–0.3	V_{IN} + 0.3	
	PGOOD to AGND(2)	–0.3	22	
	FB to AGND	–0.3	5.5	
	AGND to PGND	–0.3	0.3	
Output voltage	VOUT to PGND(2)	-0.3	V_{IN} + 0.3	V
	V5V to AGND	0	5.5	
Operating IC junction temperature, T_J (3)		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C
Peak reflow case temperature			245	°C
Maximum number or reflows allowed			3	
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	±2500	V
		Charged-device model (CDM)(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Input voltage, V_{IN}	3.8 (3)	36	V
Output voltage, V_{OUT}	1	7 (4)	V
Output current, I_{OUT}	0	2	A
EN voltage, V_{EN} (2)	0	V_{IN}	V
PGOOD pullup voltage, V_{PGOOD} (2)	0	18	V
PGOOD sink current		3	mA
Operating ambient temperature, T_A	–40	105	°C
Input capacitance, C_{IN} (5)	20		µF
Output capacitance, C_{OUT}	min (6)	1000	µF

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the 节 *6.5*.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) The recommended minimum V_{IN} is 3.8 V or (VOUT + 1 V), whichever is greater. See the 节 *7.3.9* section for more information.
(4) The recommended maximum output voltage varies depending input voltage. See the 节 *7.3.9* section for more information.
(5) Minimum C_{IN} of 20 µF must be ceramic type.
(6) The minimum amount of required output capacitance varies depending on the output voltage. See 表 7-1.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM53602 RDA (QFN) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	5.5	°C/W
T_{SHDN}	Thermal shutdown temperature	165	°C
	Recovery temperaure	148	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 75-mm x 75-mm four-layer PCB with 2-oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the *节 10.3* section.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Limits apply over T_A = –40°C to +105°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT} maximum, (unless otherwise noted); C_{IN1} = 2x10 µF, 50-V, 1206 ceramic; C_{IN2} = 100 nF, 50-V, 0603 ceramic; C_{OUT} = 3x22 µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage range	Over I_{OUT} range	3.8 (1)		36	V
	V_{IN} turn on	V_{IN} increasing, I_{OUT} = 0 A		3.55		V
	V_{IN} turn off	V_{IN} decreasing, I_{OUT} = 0 A		3.05		V
I_Q	Quiescient current	Non-switching, V_{FB} = 1.2 V		24		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, I_{OUT} = 0 A		5	10	µA
INTERNAL LDO (V5V)						
V5V	Internal LDO output voltage appearing at the V5V pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
FEEDBACK						
V_{FB}	Feedback voltage(2)	–40°C ≤ T_J ≤ +125°C, I_{OUT} = 0.75 A	0.985	1	1.015	V
	Load regulation	T_A = +25°C, 0.5 A ≤ I_{OUT} ≤ 2 A		0.06		%
	Line regulation	T_A = +25°C, I_{OUT} = 0.75 A, Over V_{IN} range		0.15		%
I_{FB}	Current into FB pin	FB = 1 V		0.2	50	nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		2	A
I_{OUT}	Over-current threshold			3.5		A
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
ENABLE (EN PIN)						
$V_{EN-VCC-H}$	EN input level required to turn on internal LDO	Rising threshold			1	V
$V_{EN-VCC-L}$	EN input level required to turn off internal LDO	Falling threshold	0.3			V
V_{EN-H}	EN input level required to start switching	Rising threshold	1.2	1.23	1.26	V
V_{EN-HYS}	Hysteresis below V_{EN-H}	Falling		100		mV

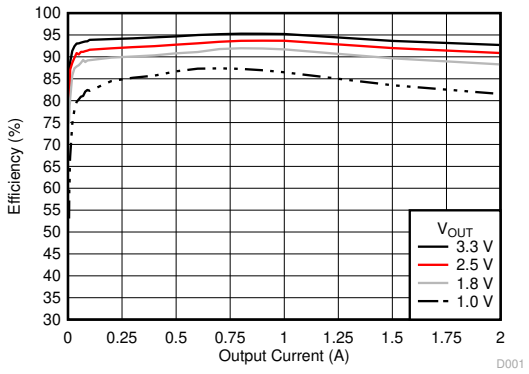
Limits apply over T_A = –40°C to +105°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = I_{OUT} maximum, (unless otherwise noted); C_{IN1} = 2x10 µF, 50-V, 1206 ceramic; C_{IN2} = 100 nF, 50-V, 0603 ceramic; C_{OUT} = 3x22 µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.2		nA
POWER GOOD (PGOOD PIN)						
$V_{PG-HIGH-UP}$	V_{OUT} rising (fault)	% of FB voltage		107		%
$V_{PG-HIGH-DN}$	V_{OUT} falling (good)	% of FB voltage		105		%
$V_{PG-LOW-UP}$	V_{OUT} rising (good)	% of FB voltage		94		%
$V_{PG-LOW-DN}$	V_{OUT} falling (fault)	% of FB voltage		92		%
R_{PG}	Power-good flag R_{DSON}	V_{EN} = 0 V		35		Ω
V_{IN-PG}	Minimum input voltage for proper PGOOD function	50-µA, EN = 0 V			2	V
V_{PG}	PGOOD logic low output	50-µA, EN = 0 V, V_{IN} = 2 V			0.2	V
PERFORMANCE						
η	Efficiency	I_{OUT} = 2 A, T_A = 25°C		91		%
SOFT START						
t_{SS}	Internal soft-start time			4		ms
SWITCHING FREQUENCY						
f_{SW-MAX}	Max switching frequency	I_{OUT} = 2 A, T_A = 25°C		1.4(3)		MHz

(1) The recommended minimum V_{IN} is 3.8 V or (VOUT + 1 V), whichever is greater. See the *井 7.3.9* section for more information.
(2) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.
(3) The typical switching frequency of this device will change based on operating conditions. See the *井 7.4.2* section for more information.

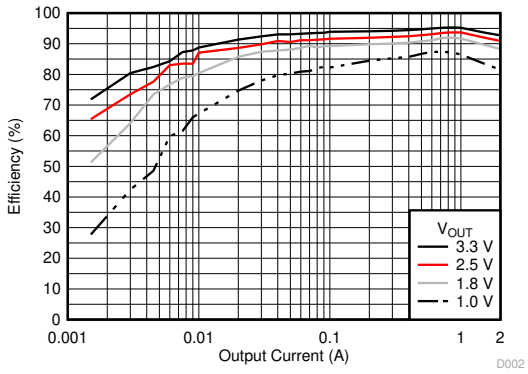
6.6 Typical Characteristics (V_{IN} = 5 V)

The typical characteristic data has been developed from actual products tested at T_A = 25°C. This data is considered typical for the device.



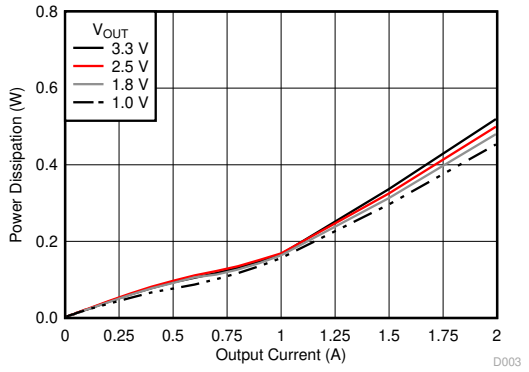
V_{IN} = 5 V Linear Scale

图 6-1. Efficiency versus Output Current



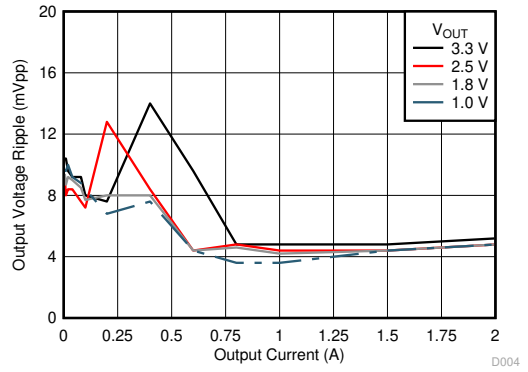
V_{IN} = 5 V Log Scale

图 6-2. Efficiency versus Output Current



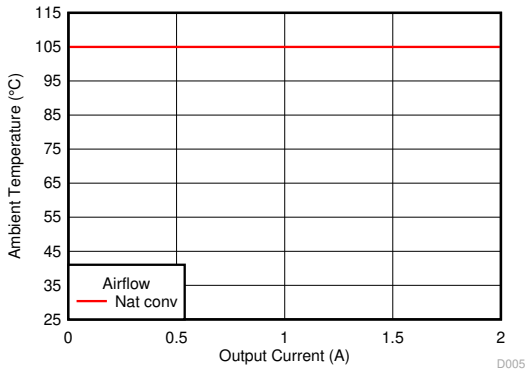
V_{IN} = 5 V

图 6-3. Power Dissipation versus Output Current



V_{IN} = 5 V C_{OUT} = 4x 47µF

图 6-4. Voltage Ripple versus Output Current



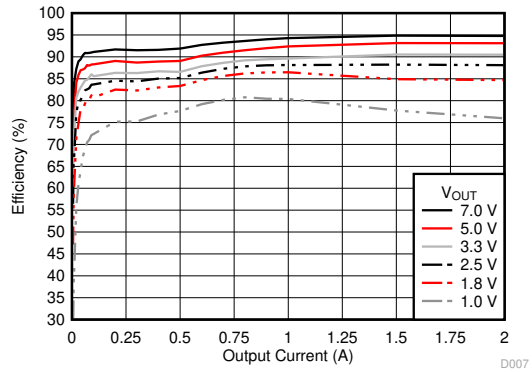
V_{IN} = 5 V $V_{OUT} \leq$ 4 V

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

图 6-5. Safe Operating Area

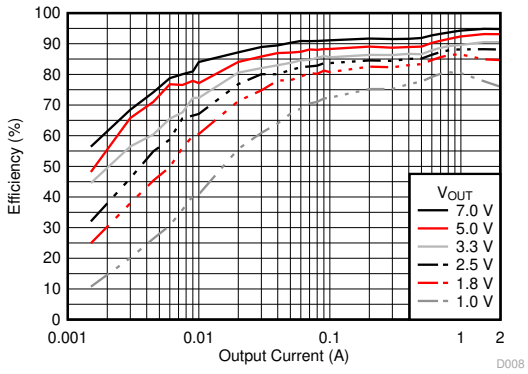
6.7 Typical Characteristics (V_{IN} = 12 V)

The typical characteristic data has been developed from actual products tested at T_A = 25°C. This data is considered typical for the device.



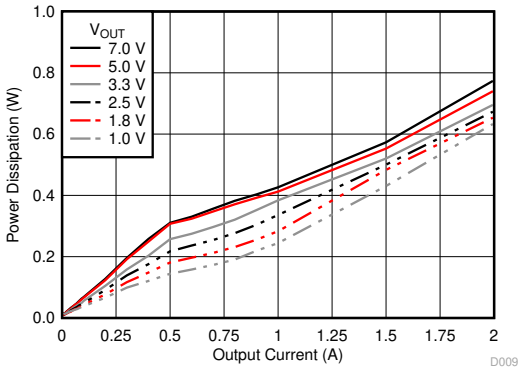
V_{IN} = 12 V Linear Scale

图 6-6. Efficiency versus Output Current



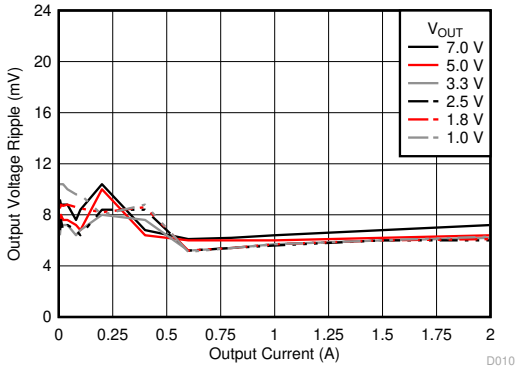
V_{IN} = 12 V Log Scale

图 6-7. Efficiency versus Output Current



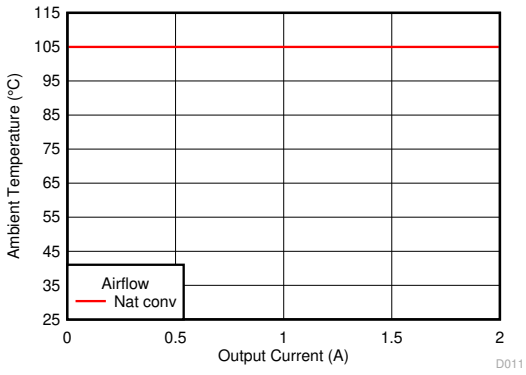
V_{IN} = 12 V

图 6-8. Power Dissipation versus Output Current



V_{IN} = 12 V C_{OUT} = 4x 47µF

图 6-9. Voltage Ripple versus Output Current



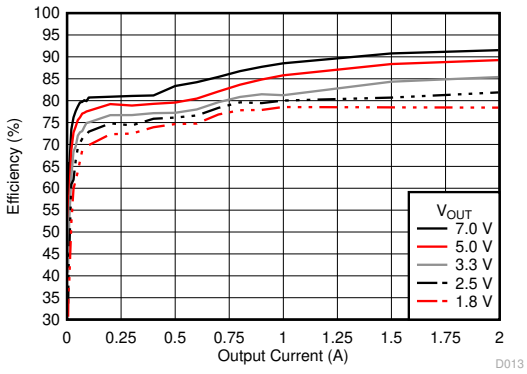
V_{IN} = 12 V All V_{OUT}

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

图 6-10. Safe Operating Area

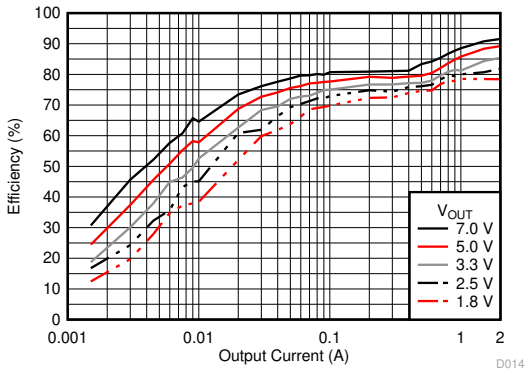
6.8 Typical Characteristics (V_{IN} = 24 V)

The typical characteristic data has been developed from actual products tested at T_A = 25°C. This data is considered typical for the device.



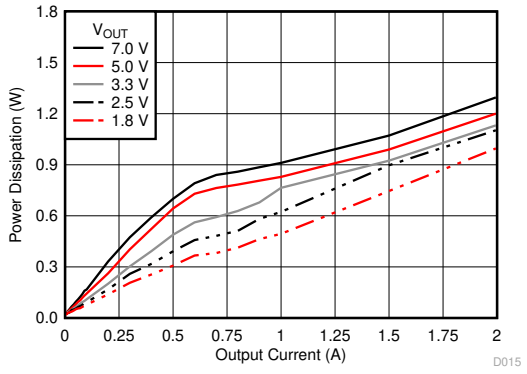
V_{IN} = 24 V

图 6-11. Efficiency versus Output Current



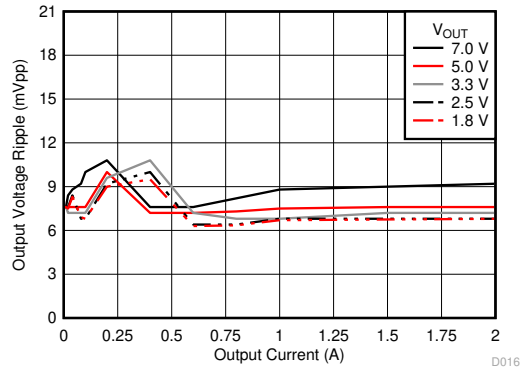
V_{IN} = 24 V

图 6-12. Efficiency versus Output Current



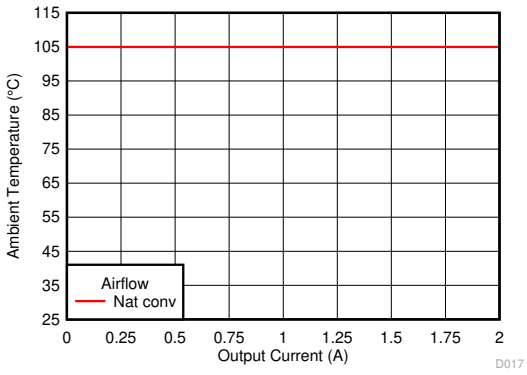
V_{IN} = 24 V

图 6-13. Power Dissipation versus Output Current



V_{IN} = 24 V C_{OUT} = 4x 47µF

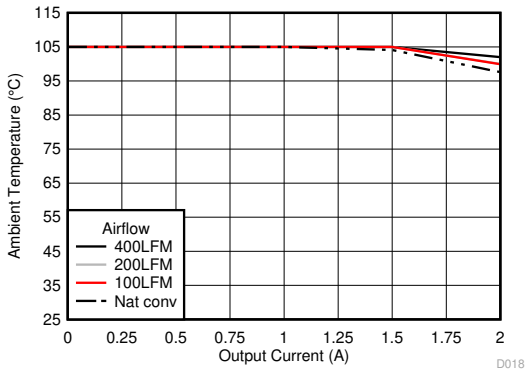
图 6-14. Voltage Ripple versus Output Current



V_{IN} = 24 V $V_{OUT} \leqslant$ 1.8 V

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

图 6-15. Safe Operating Area



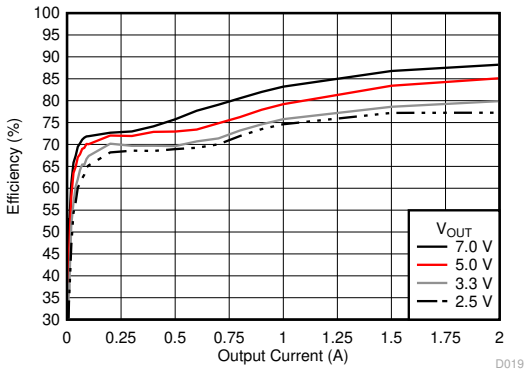
V_{IN} = 24 V V_{OUT} = 5 V

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

图 6-16. Safe Operating Area

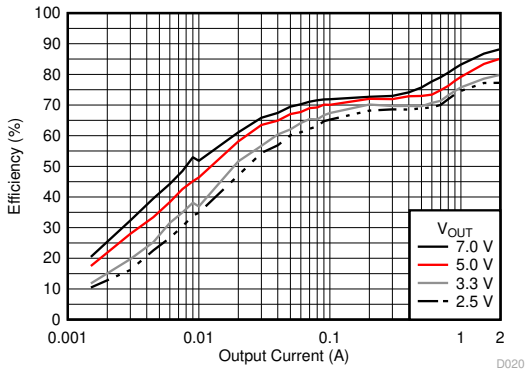
6.9 Typical Characteristics (V_{IN} = 36 V)

The typical characteristic data has been developed from actual products tested at T_A = 25°C. This data is considered typical for the device.



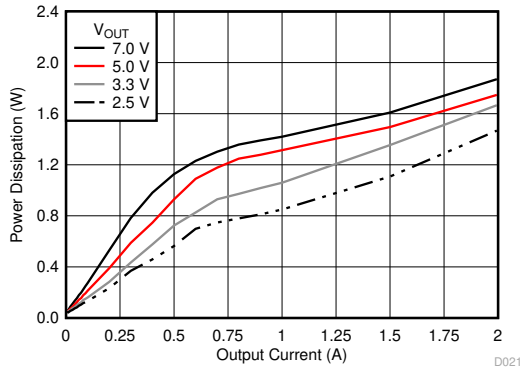
V_{IN} = 36 V

图 6-17. Efficiency versus Output Current



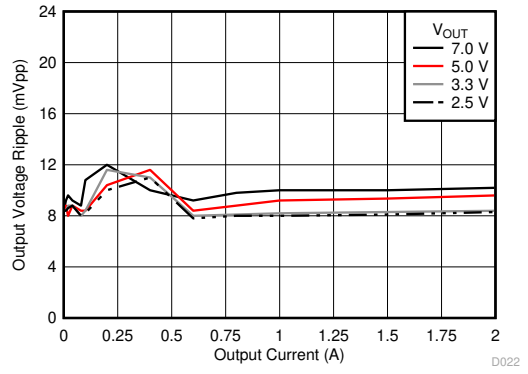
V_{IN} = 36 V

图 6-18. Efficiency versus Output Current



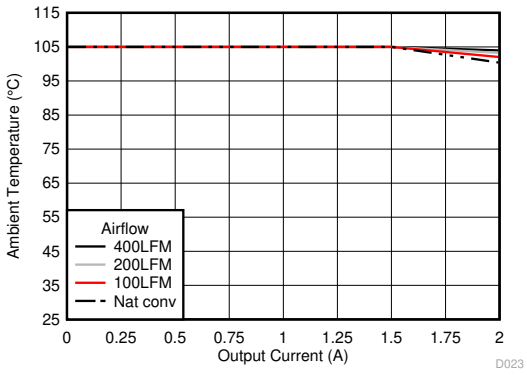
V_{IN} = 36 V

图 6-19. Power Dissipation versus Output Current



V_{IN} = 36 V C_{OUT} = 4x 47µF

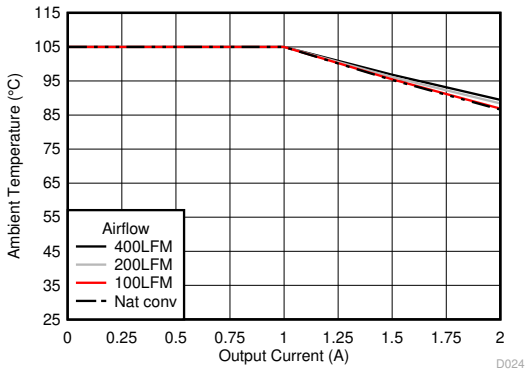
图 6-20. Voltage Ripple versus Output Current



V_{IN} = 36 V V_{OUT} = 1.8 V

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

图 6-21. Safe Operating Area



V_{IN} = 36 V V_{OUT} = 5 V

PCB = 85-mm × 65-mm, 4-layer, 2-oz. copper

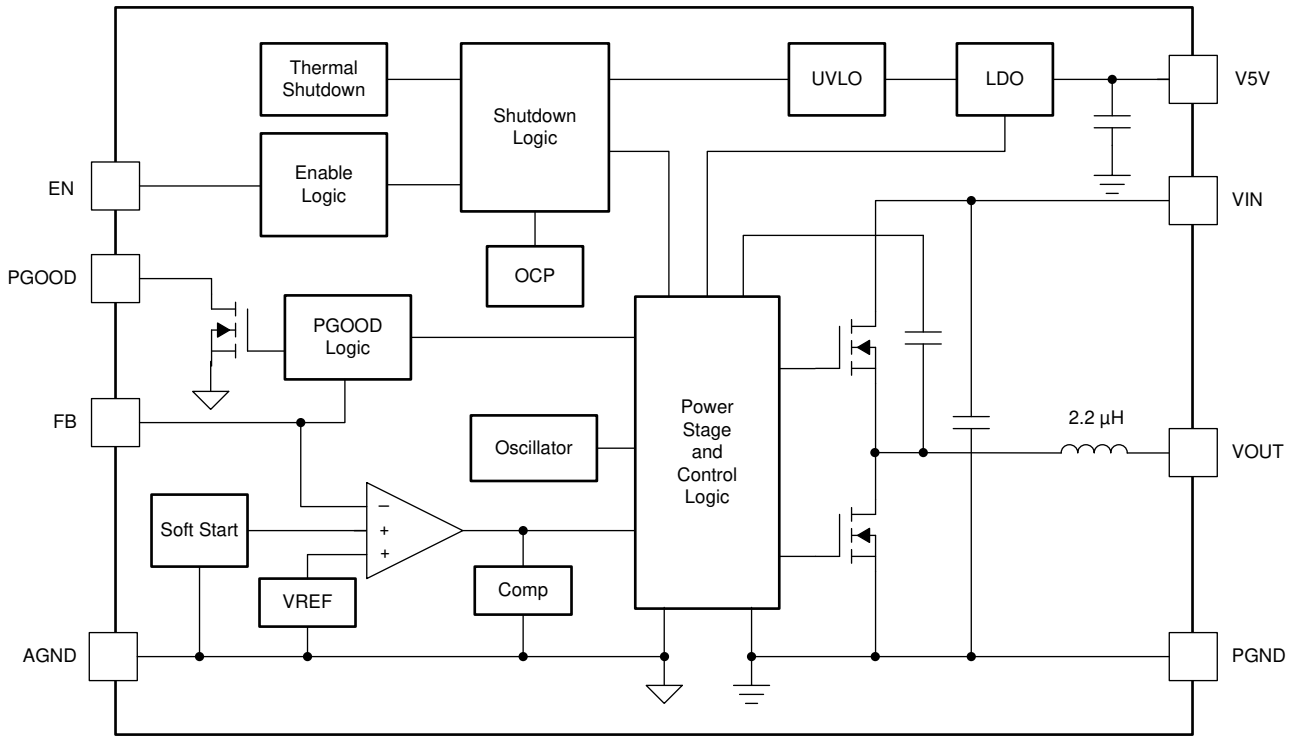
图 6-22. Safe Operating Area

7 Detailed Description

7.1 Overview

The TPSM53602 is a full-featured, 36-V input, 2-A, synchronous step-down converter with PWM, MOSFETs, shielded inductor, and control circuitry integrated into a low-profile, over-molded package. The device integration enables small designs while providing the ability to adjust key parameters to meet specific design requirements. The TPSM53602 provides an output voltage range of 1 V to 7 V. An external resistor divider is used to adjust the output voltage to the desired value. The device provides accurate voltage regulation over a wide load range by using a precision internal voltage reference. Input undervoltage lockout is internally set at 3.55 V (typical), but can be adjusted upward using a resistor divider on the EN pin of the device. The EN pin can also be pulled low to put the device into standby mode to reduce input current draw. A power-good signal is provided to indicate when the output is within its nominal voltage range. Thermal shutdown and current limit features protect the device during an overload condition. A 15-pin, QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 9) sets the output voltage of the TPSM53602. The output voltage adjustment range is from 1 V to 7 V. 图 7-1 shows the feedback resistor connections for setting the output voltage. The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be calculated using 方程式 1. 表 7-1 lists the standard resistor values for several output voltages. The minimum required output capacitance for each output voltage is also included in 表 7-1. The capacitance values listed represent the *effective* capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBB} = \frac{10}{(V_{OUT} - 1)} \ (k\Omega) \quad (1)$$

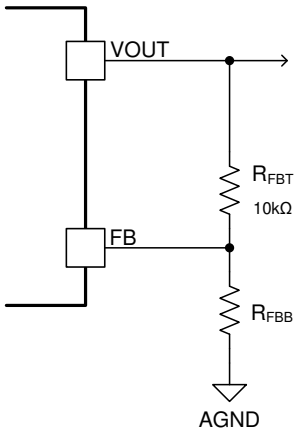


图 7-1. Setting the Output Voltage

表 7-1. Setting the Output Voltage

V_{OUT} (V)	R_{FBB} (kΩ)(1)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBB} (kΩ)(1)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	open	150	3.0	4.99	46
1.1	100	137	3.3	4.32	42
1.2	49.9	125	4.0	3.32	34
1.3	33.2	114	4.5	2.87	30
1.4	24.9	105	5.0	2.49	27
1.5	20.0	98	5.5	2.21	24
1.8	12.4	80	6.0	2.00	22
2.0	10.0	72	6.5	1.82	20
2.5	6.65	56	7.0	1.65	19

(1) R_{FBT} = 10.0 kΩ

7.3.2 Switching Frequency

The switching frequency of the TPSM53602 is set to 1.4 MHz, internal to the device. The switching frequency cannot be adjusted. When the load current is high enough and the device is operating in PWM mode, the device operates at a fixed frequency. As the load current drops and the device switches to PFM mode, the switching frequency is reduced resulting in reduced power dissipation. See 节 *7.4.2* for typical information on when the device switches from PWM mode to PFM mode.

7.3.3 Input Capacitors

The TPSM53602 requires a minimum input capacitance of 20 µF (2 × 10 µF) of ceramic type. High-quality, ceramic-type X5R or X7R capacitors with sufficient voltage rating are recommended. TI recommends an additional 47 µF of non-ceramic capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

表 7-2. Recommended Input Capacitors

VENDOR(1)	SERIES	SIZE	PART NUMBER	CAPACITOR CHARACTERISTICS	
				VOLTAGE RATING (V)	CAPACITANCE (3) (µF)
Murata	X5R	1206	GRT31CR61H106ME01L	50	10
TDK	X5R	1206	CGA5L3X5R1H106M160AB	50	10
TDK	X7R	1206	CGA5L1X7R1H106K160AC	50	10
Murata	X7R	1210	GRM32ER71H106KA12L	50	10
TDK	X7R	1210	C3225X7R1H106M250AC	50	10

(1) **Capacitor Supplier Verification, RoHS, Lead-free, and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C.
(3) Standard capacitance values

7.3.4 Output Capacitors

表 7-1 lists the TPSM53602 minimum output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contributes to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(min)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See 表 7-3 for a preferred list of output capacitors by vendor.

表 7-3. Recommended Output Capacitors

VENDOR(1)	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			VOLTAGE RATING (V)	CAPACITANCE (2) (µF)	ESR(2) (mΩ)
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X7R	GCM32ER70J476KE19L	6.3	47	2
Murata	X5R	GRM21BR61A476ME15L	10	47	2
TDK	X5R	C3216X5R1A476M160AB	10	47	2
Murata	X7R	GRM32ER71A476KE15L	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	10TPF150ML	10	150	15
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPF330M9L	6.3	330	9
Panasonic	POSCAP	6TPE470MAZU	6.3	470	35

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Standard capacitance values.

7.3.5 Output On/Off Enable (EN)

The voltage on the EN pin provides electrical ON/OFF control of the device. This input features precision thresholds, allowing the use of an external voltage divider to provide a programmable UVLO (see 节 *7.3.6*). Applying a voltage of $V_{EN} \geq V_{EN\text{-}LDO\_H}$ causes the device to enter standby mode, powering the internal LDO, but not producing an output voltage. Increasing the EN voltage to $V_{EN\text{-}H}$ fully enables the device, allowing it to enter start-up mode and beginning the soft-start period. When the EN input is brought below $V_{EN\text{-}H}$ by $V_{EN\text{-}HYS}$, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN\text{-}LDO\text{-}L}$ completely shuts down the device. 图 7-2 shows this behavior. The values for the various EN thresholds can be found in 节 *6.5*.

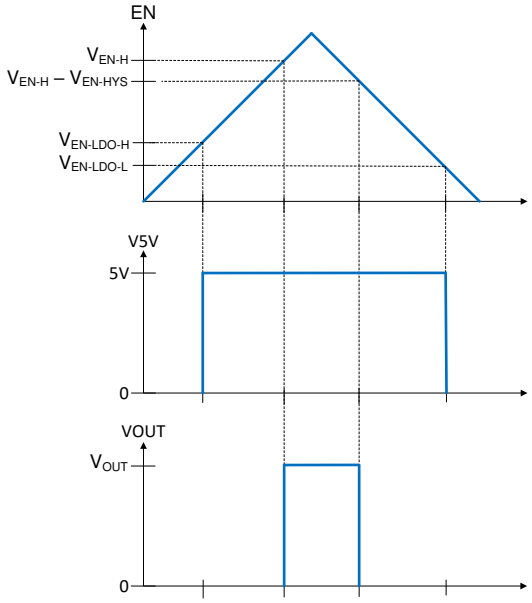


图 7-2. Precision Enable Behavior

The EN pin cannot be open circuit or floating. The simplest way to enable the operation of the TPSM53602 is to connect the EN pin to VIN directly as shown in 图 7-3. This allows self start-up of the TPSM53602 when VIN is within the operation range.

If an application requires controlling the EN pin, an external logic signal can be used to drive EN pin as shown in 图 7-4. Applications using an open drain/collector device to interface with this pin require a pullup resistor to a voltage above the enable threshold.

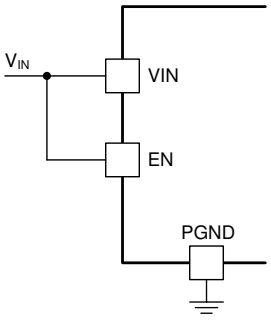


图 7-3. Enabling the Device

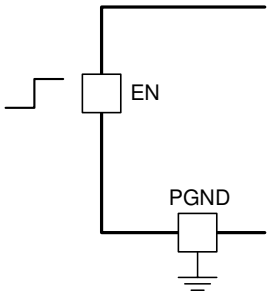


图 7-4. Typical Enable Control

7.3.6 Programmable Undervoltage Lockout (UVLO)

The TPSM53602 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 3.55 V (typical) with a typical hysteresis of 500 mV.

If an application requires a higher UVLO threshold, a resistor divider can be placed between VIN, the EN pin, and AGND as shown in 图 7-5. The enable rising threshold (V_{EN-H}) is 1.23 V (typ) with 100 mV (typ) hysteresis. 表 7-4 lists recommended resistor values for R_{ENT} and R_{ENB} to adjust the ULVO voltage.

To ensure proper start-up and reduce input current surges, TI recommends to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

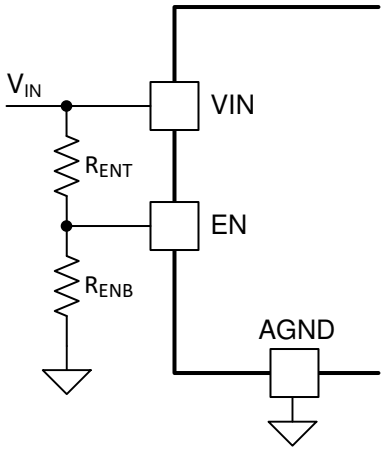


图 7-5. Adjustable UVLO

表 7-4. Resistor Values for Adjusting UVLO

VIN UVLO (V)	6.5	10	15	20	25	30
R_{ENT} (kΩ)	100	100	100	100	100	100
R_{ENB} (kΩ)	23.7	14.3	9.09	6.65	5.23	4.32

7.3.7 Power Good (PGOOD)

The TPSM53602 has a built-in power-good signal (PGOOD) which indicates whether the output voltage is within its regulation range. The PGOOD pin is an open-drain output that requires a pullup resistor to a nominal voltage source of 18 V or less. The internal 5-V LDO output (V5V pin) can be used as the pullup voltage source. A typical pullup resistor value is between 10 kΩ and 100 kΩ. The maximum recommended PGOOD sink current is 3 mA.

Once the output voltage rises above 94% of the set voltage, the PGOOD pin rises to the pullup voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 92% or rises higher than 107% of the nominal set voltage. See 图 7-6 for typical power-good thresholds.

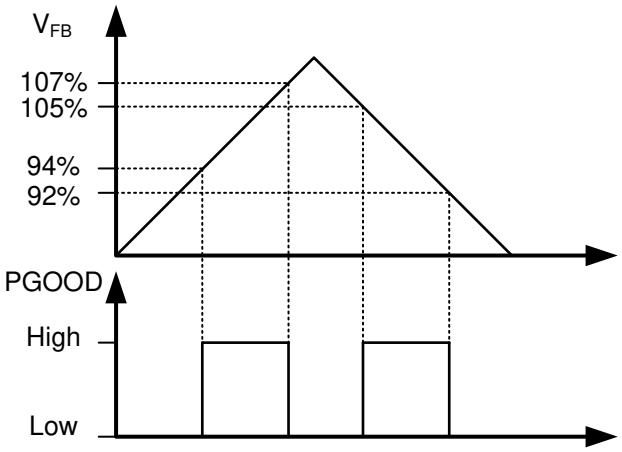


图 7-6. Power-good Flag

7.3.8 Light Load Operation

In light load conditions, the device turns on the high-side MOSFET until the inductor current reaches a controlled minimum value of approximately 1 A. As the input voltage decreases, reducing the voltage headroom between V_{IN} and V_{OUT}, the amount of time required to reach this minimum current increases. During this time, additional energy flows from V_{IN} to V_{OUT}, resulting in increased output voltage ripple. To eliminate this behavior, the EN UVLO function must be used to maintain at least 1 V of headroom above V_{OUT}. Alternatively, additional output capacitance can be added to reduce the output voltage ripple in applications that operate at light loads with very low V_{IN} to V_{OUT} headroom.

7.3.9 Voltage Dropout

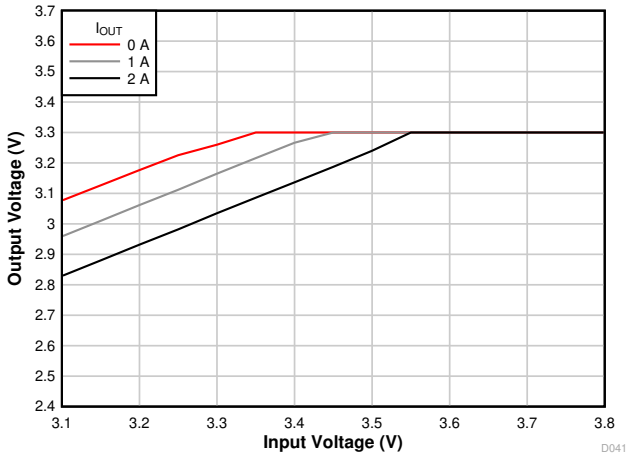
Voltage dropout is the difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

To ensure the TPSM53602 maintains output voltage regulation over the operating temperature range, the minimum V_{IN} is 3.8 V or (V_{OUT} + 1 V), whichever is greater.

The TPSM53602 operates in a frequency foldback mode when the dropout voltage is less than the recommendation above. Frequency foldback reduces the switching frequency to allow the output voltage to maintain regulation as input voltage decreases. At light load, the TPSM53602 operates in PFM mode which is a reduced frequency operation. See *节 7.4.2* for more information on PFM mode. 图 7-7 through 图 7-12 show typical dropout voltage and frequency foldback curves for 3.3 V, 5 V, and 7 V outputs at T_A = 25°C.

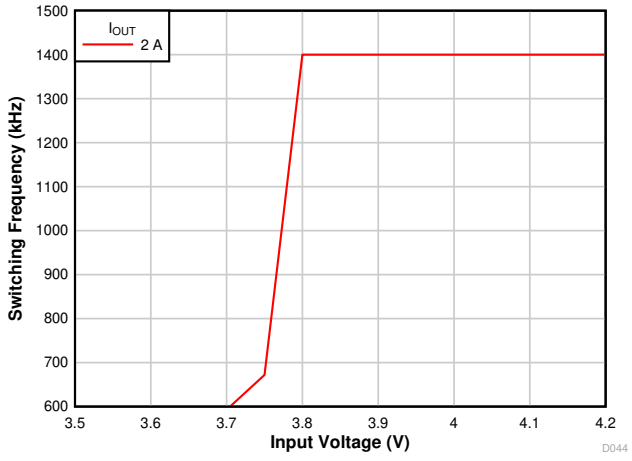
Note

As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltage.



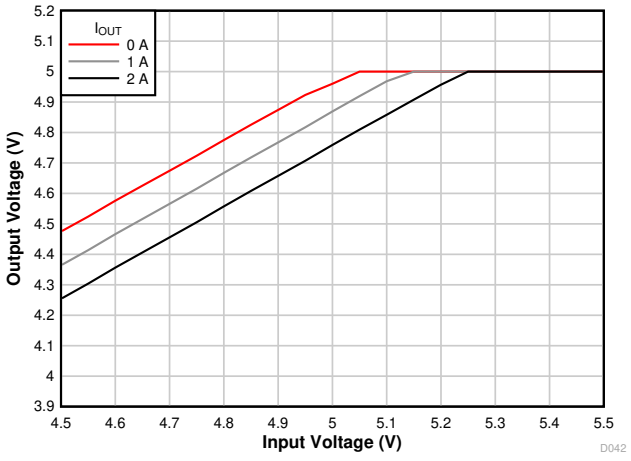
V_{OUT} = 3.3 V

图 7-7. Voltage Dropout



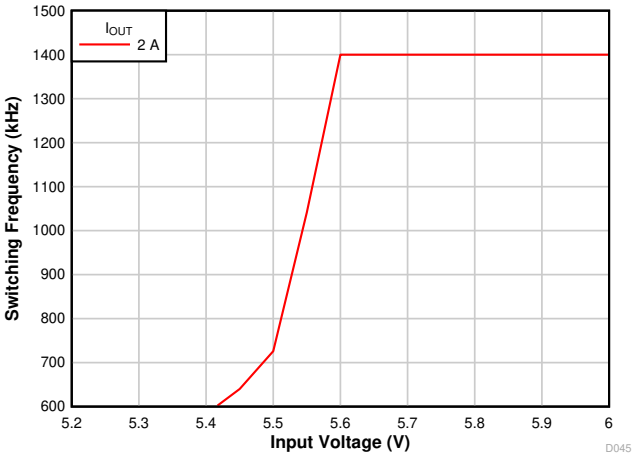
V_{OUT} = 3.3 V

图 7-8. Frequency Foldback



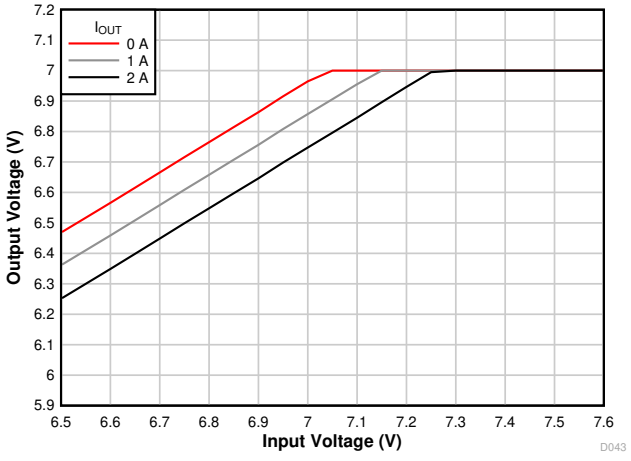
V_{OUT} = 5 V

图 7-9. Voltage Dropout



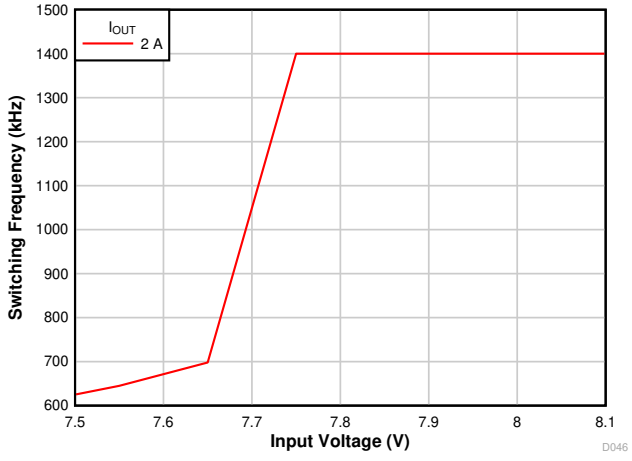
V_{OUT} = 5 V

图 7-10. Frequency Foldback



V_{OUT} = 7 V

图 7-11. Voltage Dropout



V_{OUT} = 7 V

图 7-12. Frequency Foldback

7.3.10 Overcurrent Protection (OCP)

The TPSM53602 is protected from overcurrent conditions. Cycle-by-cycle current limit is used for overloads while hiccup mode is used for short circuits. Hiccup mode is activated if a fault condition persists on the output. Hiccup mode reduces power dissipation under severe overcurrent conditions and prevents overheating and potential damage to the device. In hiccup mode, the regulator is shut down and kept off for 94 ms typical before the TPSM53602 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Once the fault is removed, the module automatically recovers with a normal soft-start power up.

The typical current limit threshold for the TPSM53602 varies slightly as a function of input voltage and output voltage. 图 7-13 shows the typical current limit threshold for several output voltages over the input voltage range.

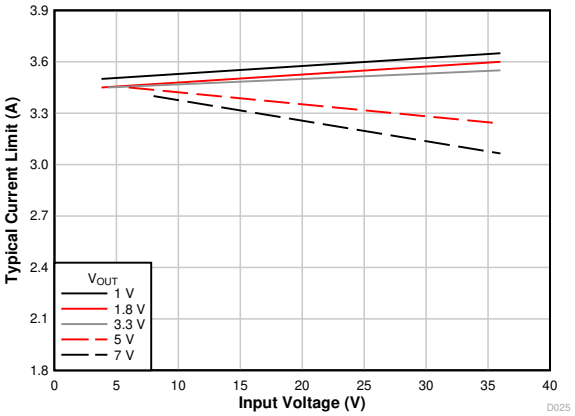


图 7-13. Current Limit Threshold

7.3.11 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 148°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The TPSM53602 is in active mode when VIN is above the turnon threshold and the EN pin voltage is above the EN high threshold. The most direct way to enable the TPSM53602 is to connect the EN pin to VIN. This allows self start-up of the TPSM53602 when the input voltage is in the operation range of 3.8 V to 36 V. Connecting a resistor divider between VIN, EN, and AGND adjusts the UVLO to delay the turn on until V_{IN} is closer to its regulated voltage.

7.4.2 Auto Mode

In auto mode, the device moves between Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM) as the load changes. At light loads, the regulator operates in PFM mode. At higher loads, the mode changes to PWM mode. The typical load current for which the device moves from PFM to PWM can be found in 图 7-14 and 图 7-15. The output current at which the device changes modes depends on the input voltage and the output voltage. For output currents above the curve, the device is in PWM mode. If the curve is a solid line, the PWM switching frequency is 1.4 MHz nominal. If the curve is a dashed line, the PWM switching frequency is reduced due to the minimum on-time of the internal controller to maintain output voltage regulation. For currents below the curves, the device is in PFM mode. For applications where the switching frequency must be known for a given condition, the above mentioned effects must be carefully tested before the design is finalized.

In PWM mode, the regulator operates at a constant frequency using PWM to regulate the output voltage. While operating in this mode, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM mode, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst and the actual switching frequency depends on the input voltage, output voltage, and load current. The frequency of these bursts is adjusted to regulate the output while diode emulation is used to maximize efficiency. This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. However, in this mode, expect larger output voltage ripple and variable switching frequency.

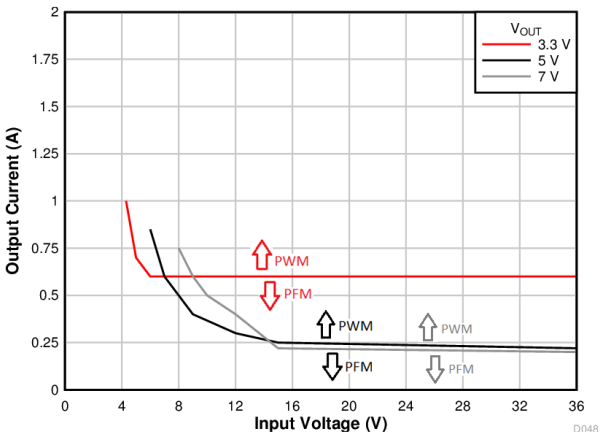


图 7-14. PFM/PWM Thresholds (3.3 V, 5 V, and 7 V)

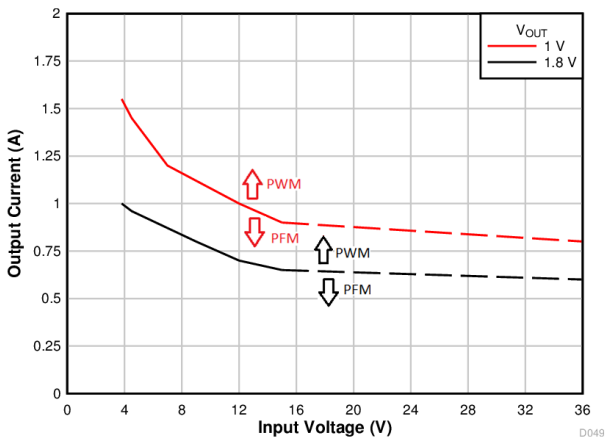


图 7-15. PFM/PWM Thresholds (1 V and 1.8 V)

7.4.3 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPSM53602. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode, the standby current is 5 μA typical.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPSM53602 is a synchronous, step-down, DC/DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The TPSM53602 can be configured in a negative output voltage, inverting buck-boost (IBB) topology. For more details, see the *Negative Output Voltage using the TPSM53602/3/4* application note. The following design procedure can be used to select components for the TPSM53602. Alternately, the WEBENCH® software can be used to generate complete designs. When generating a design, the WEBENCH® software uses an iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application

The TPSM53602 only requires a few external components to convert from a wide input voltage supply range to a wide range of output voltages. 图 8-1 shows a basic TPSM53602 schematic for a typical design.

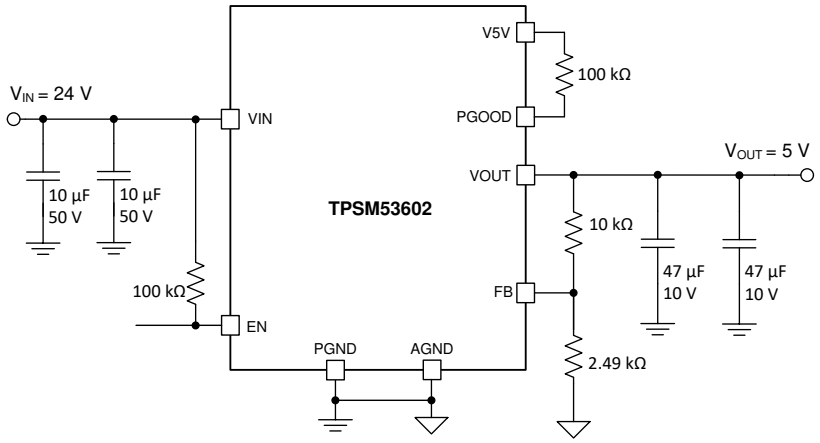


图 8-1. TPSM53602 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters and follow the design procedures in *节 8.2.2*.

表 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM53602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Setpoint

The output voltage of the TPSM53602 device is externally adjustable using a resistor divider. The recommended value of R_{FBT} is 10 kΩ. The value for R_{FBB} can be selected from 表 7-1 or calculated using 方程式 2:

$$R_{FBB} = \frac{10}{(V_{OUT} - 1)} \text{ (k}\Omega\text{)} \quad (2)$$

For the desired output voltage of 5 V, the formula yields a value of 2.5 kΩ. Choose the closest available value of 2.49 kΩ for R_{FBB}.

8.2.2.3 Input Capacitors

The TPSM53602 requires a minimum input capacitance of 20 µF (or 2 × 10 µF) ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 47 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage.

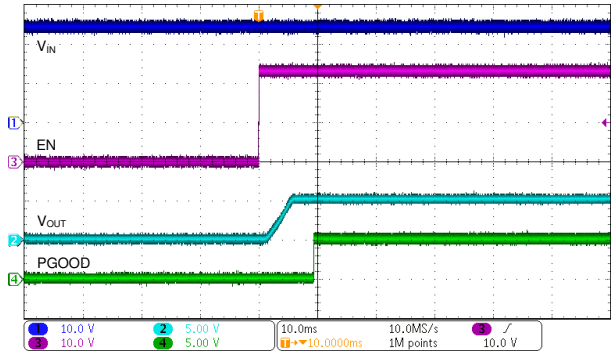
For this design example, two 10-µF, 50-V, ceramic capacitors are used.

8.2.2.4 Output Capacitor Selection

The TPSM53602 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See 表 7-1 for the required output capacitance.

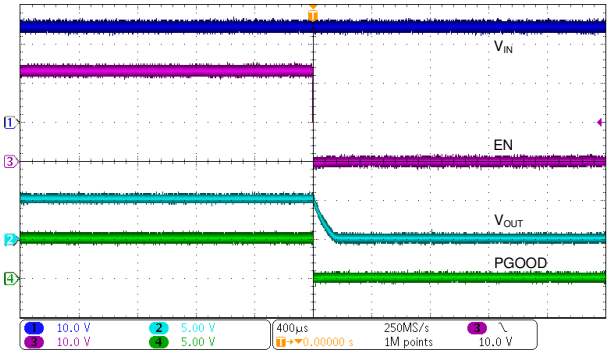
For this design example, two 47-µF, 10-V, ceramic capacitors are used.

8.2.3 Application Curves



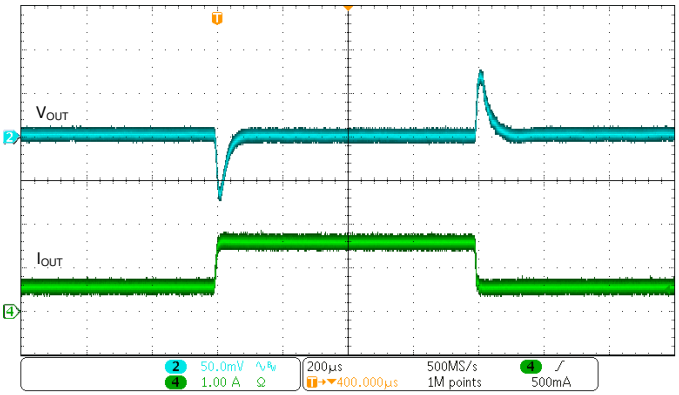
V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 2 × 47 µF

图 8-2. Enable Turn-ON



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 2 × 47 µF

图 8-3. Enable Turn-OFF



V_{IN} = 24 V V_{OUT} = 5 V C_{OUT} = 2 × 47 µF
I_{OUT} = 0.5 A to 1.5 A Slew rate: 1 A/µs

图 8-4. Transient Response

9 Power Supply Recommendations

The TPSM53602 is designed to operate from an input voltage supply range between 3.8 V and 36 V. This input supply must be well-regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPSM53602 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few centimeters from the TPSM53602, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 47-µF electrolytic capacitor.

10 Layout

The performance of any switching power supply depends as much on the layout of the PCB as the component selection. The following guidelines help users design a PCB with the best power conversion performance, optimal thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 10-1 through 图 10-3 shows a typical PCB layout. The following are some considerations for an optimized layout.

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.
- Download the EVM Design Files for fast board design

10.2 Layout Examples

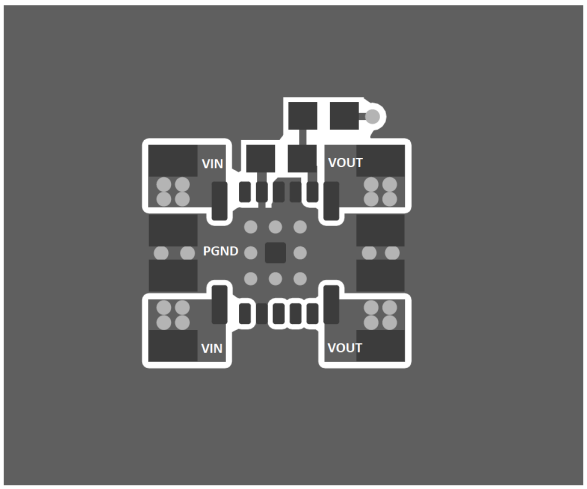


图 10-1. Typical Top-Layer Layout

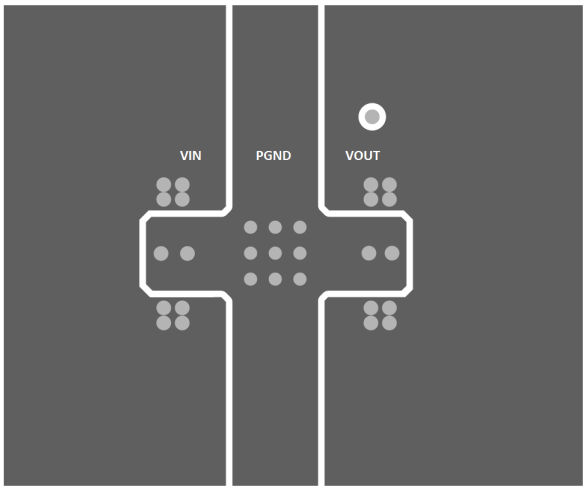


图 10-2. Typical Layer-2 Layout

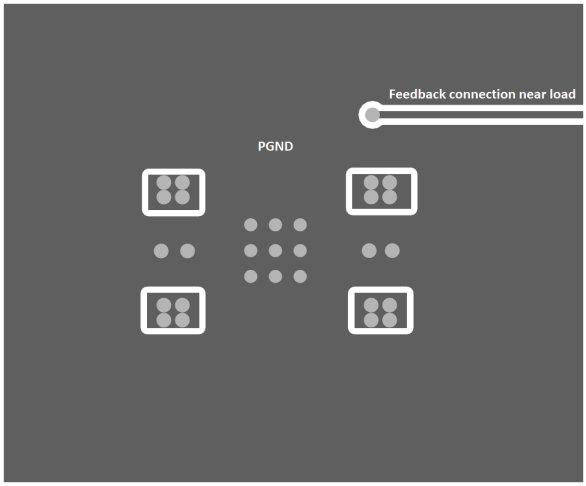


图 10-3. Typical PGND Layer

10.3 Theta JA versus PCB Area

The amount of PCB copper affects the thermal performance of the device. 图 10-4 shows the effects of copper area on the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the TPSM53602. The junction-to-ambient thermal resistance is plotted for a 4-layer PCB with PCB area from 30 cm^2 to 80 cm^2.

To determine the required copper area for an application:

1. Determine the maximum power dissipation of the device in the application by referencing the power dissipation graphs in *节 6.6* through *节 6.9*.
2. Calculate the maximum $R_{\theta JA}$ using 方程式 3 and the maximum ambient temperature of the application.

$$R_{\theta JA} = \frac{(125°C - T_{A(max)})}{P_{D(max)}} (°C/W) \quad (3)$$

3. Reference 图 10-4 to determine the minimum required PCB area for the application conditions.

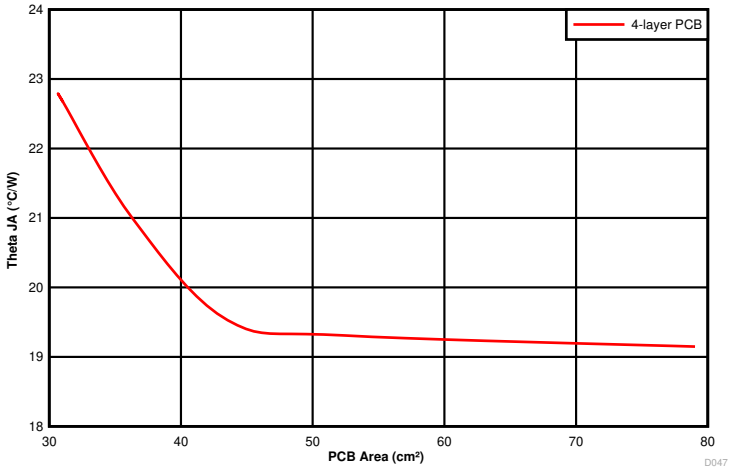


图 10-4. $R_{\theta JA}$ versus PCB Area (per layer)

10.4 Package Specifications

TPSM53602		VALUE	UNIT
Weight		429	mg
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	89.3	MHrs

10.5 EMI

The TPSM53602 is compliant with EN55011 Class-B radiated emissions. 图 10-5 and 图 10-6 show typical examples of radiated emissions plots for the TPSM53602. The graphs include the plots of the antenna in the horizontal and vertical positions.

EMI plots were measured using the standard TPSM53602EVM with no input filter.

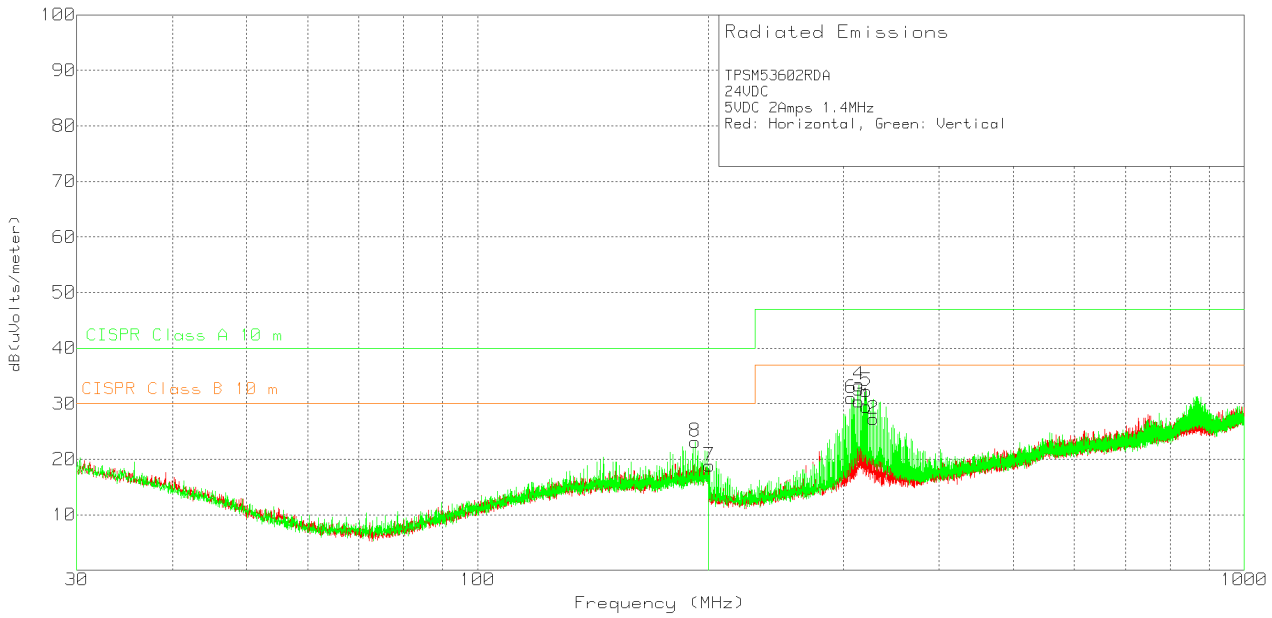


图 10-5. Radiated Emissions 24-V Input, 5-V Output, 2-A Load

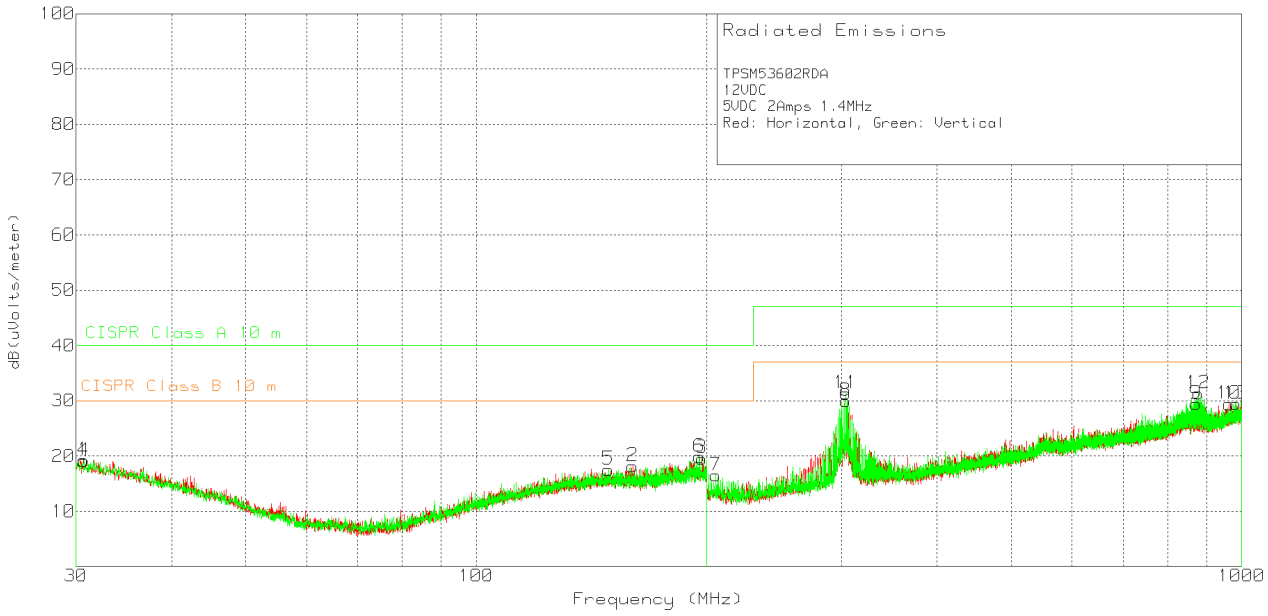


图 10-6. Radiated Emissions 12-V Input, 5-V Output, 2-A Load

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM53602 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Negative Output Voltage using the TPSM53602/3/4* application report

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM53602RDAR	ACTIVE	B3QFN	RDA	15	1000	RoHS & Green	NIPDAU	Level-3-245C-168 HR	-40 to 125	TPSM53602	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

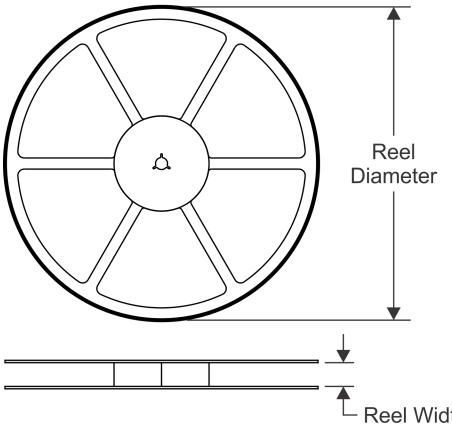
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

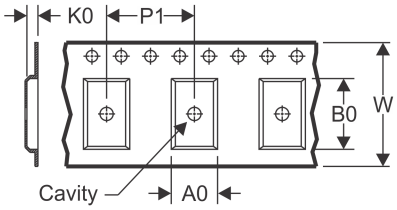
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

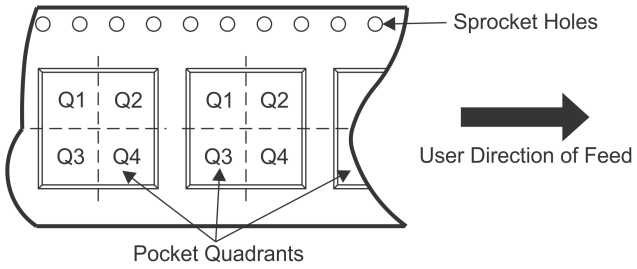


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

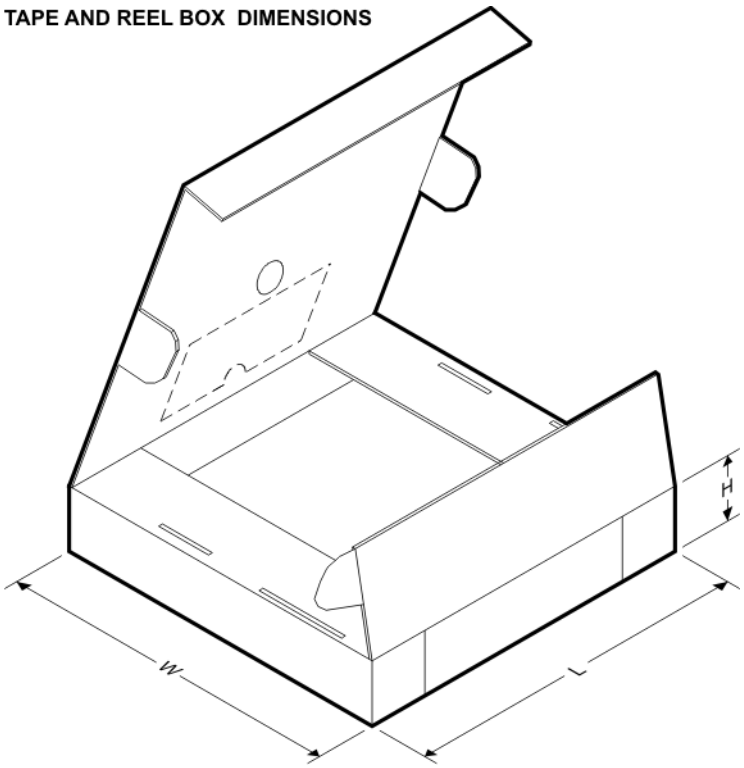
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM53602RDAR	B3QFN	RDA	15	1000	330.0	16.4	5.28	5.78	4.28	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

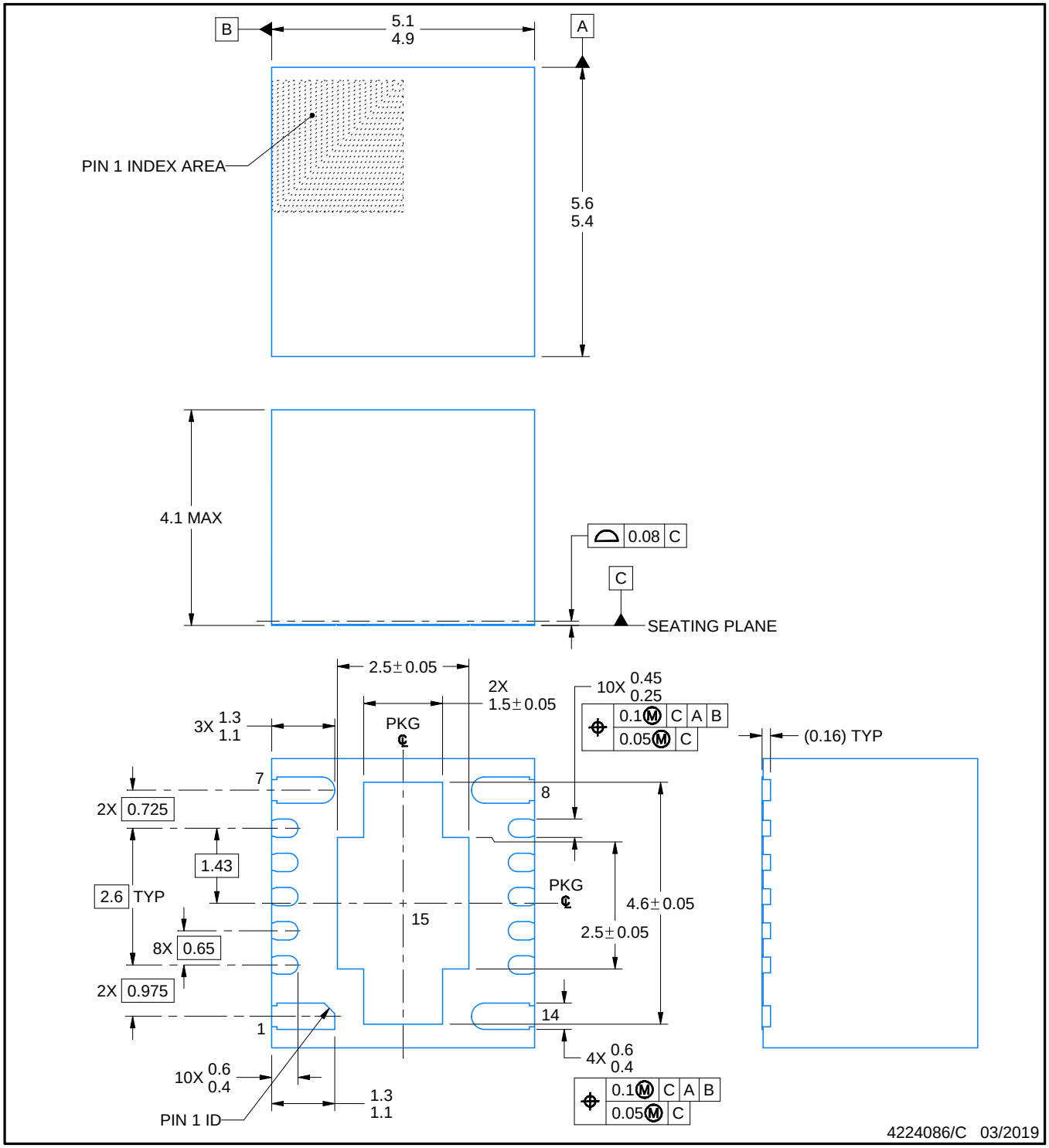
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM53602RDAR	B3QFN	RDA	15	1000	336.0	336.0	48.0

RDA0015A

PACKAGE OUTLINE

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

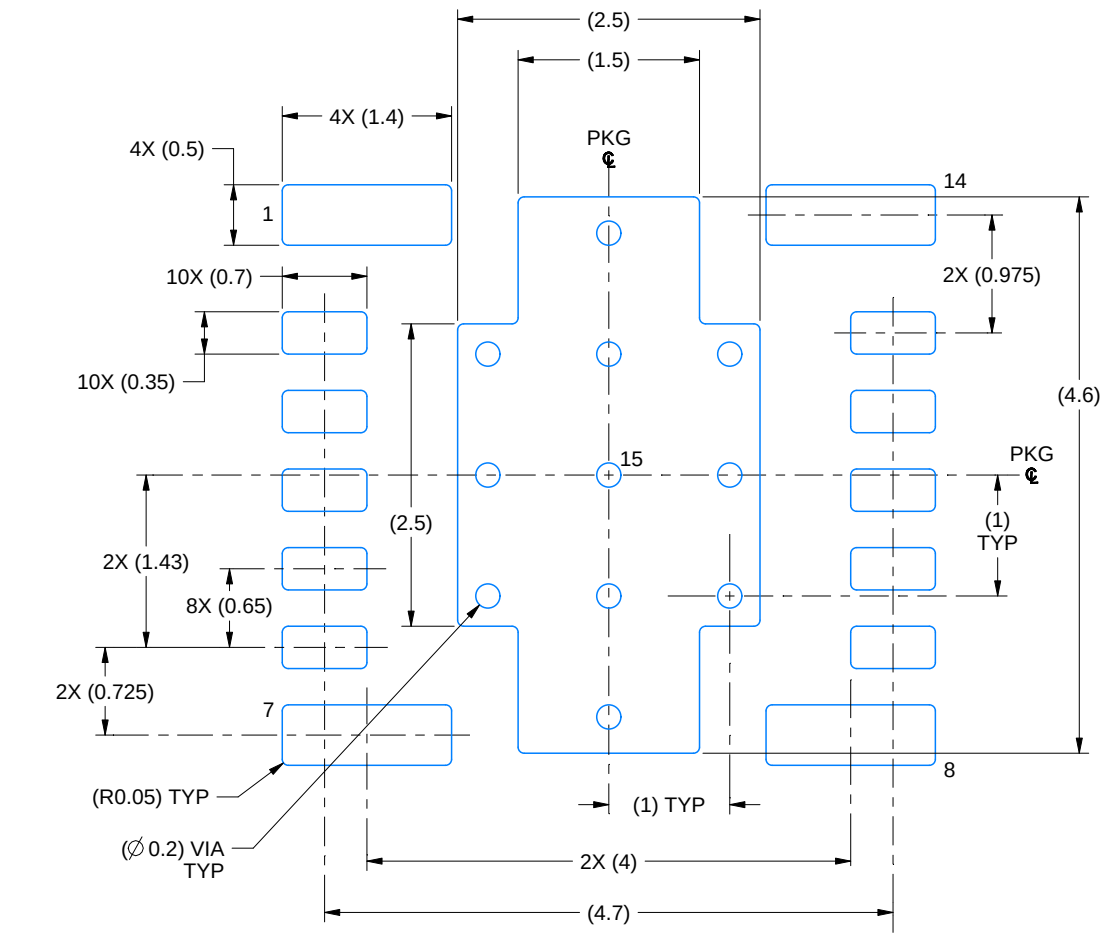
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RDA0015A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 16X

SOLDER MASK DETAILS

4224086/C 03/2019

NOTES: (continued)

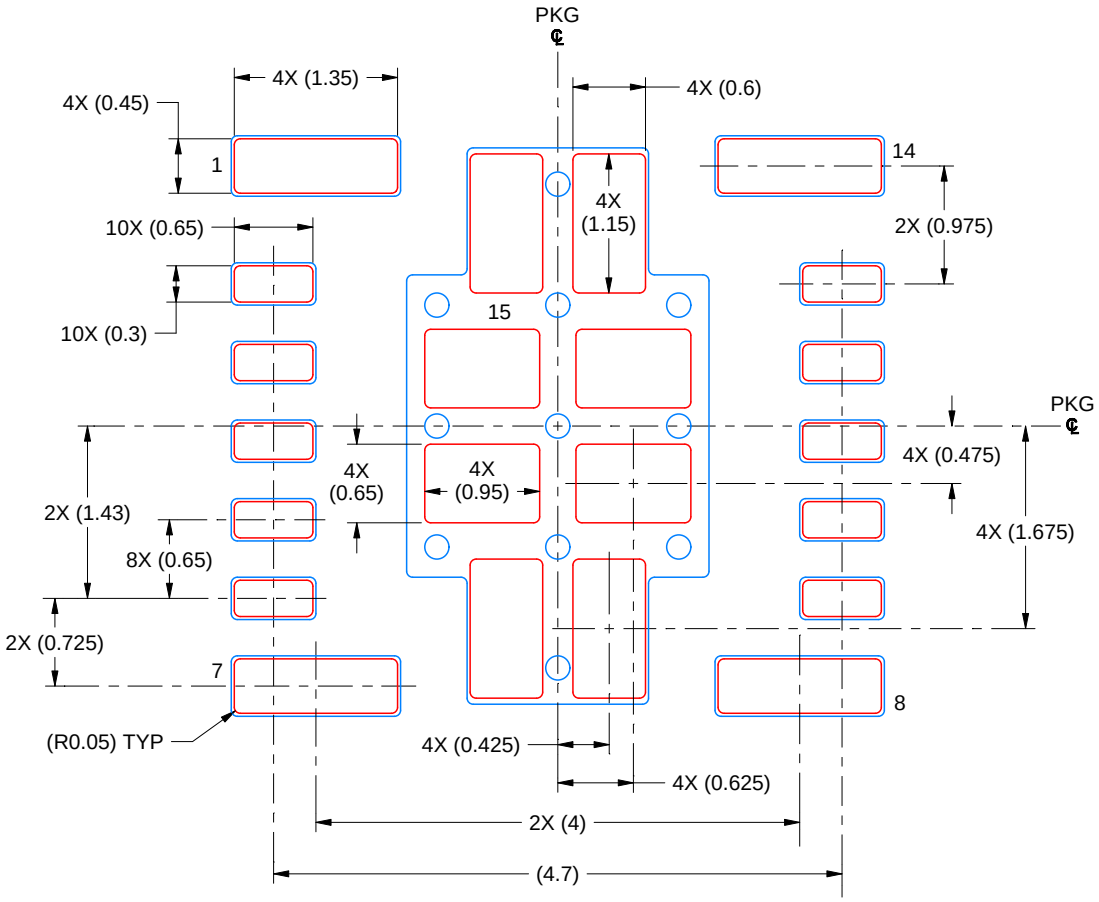
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RDA0015A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15:
56% PRINTED SOLDER COVERAGE BY AREA
SCALE: 16X

4224086/C 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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