

# TS5A63157 12Ω SPDT 模拟开关

## 5V/3.3V 单通道 2:1 多路复用器/多路解复用器

### 1 特性

- 过冲和下冲电压保护
- 断电模式下的隔离,  $V_{+} = 0V$
- 指定的先断后合开关
- 低通态电阻 (12Ω)
- 控制输入可承受 5V 电压
- 低电荷注入
- 出色的通态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA (符合 JESD 78, II 类规范的要求)
- ESD 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型 (A114-B, II 类)
  - 1000V 充电器件模型 (C101)

### 2 应用

- 采样和保持电路
- 电池供电类设备
- 音频和视频信号路由
- 通信电路

### 3 说明

TS5A63157 是一种单刀双掷 (SPDT) 模拟开关, 设计在 1.65V 至 5.5V 的电压范围内运行。此器件可处理数字信号和模拟信号。高达  $V_{+}$  (峰值) 的信号可在任一方向传输。

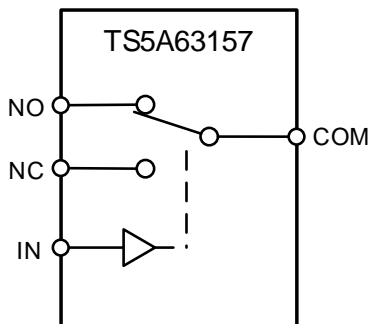
TI 已集成了过冲和下冲保护电路。TS5A63157 可检测 I/O 上的过冲和下冲事件, 并且通过防止电压差产生并打开开关来进行响应。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TS5A63157	SOT-23 (DBV)	2.90mm x 1.60mm
	SC-70 (DCK)	2.00mm x 1.25mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

方框图



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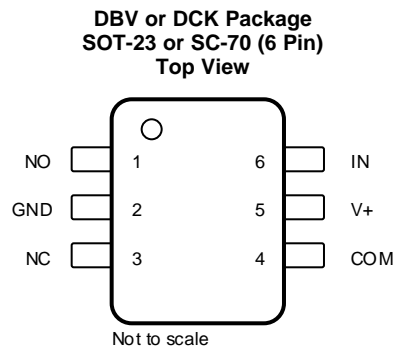
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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2009) to Revision B	Page
• 添加了器件信息表、ESD 额定值表、建议运行条件表、热性能信息表、特性说明部分、器件功能模式、应用和实施方案部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 .....	1
• Deleted the YEP or YZP package option .....	3
• Deleted 2 table notes from the <i>Absolute Minimum and Maximum Ratings</i> : "The input and output voltage ratings..." and "This value is limited to 5.5 V maximum." .....	4

## 5 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NO	1	Normally open
GND	2	Digital ground
NC	3	Normally closed
COM	4	Common
V+	5	Power supply
IN	6	Digital control. Logic H = COM to NO, Logic = L COM to NC

## 6 Specifications

### 6.1 Absolute Minimum and Maximum Ratings<sup>(1) (2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range <sup>(3)</sup>	-0.5	6.5	V
$V_{NO}$ $V_{NC}$ $V_{COM}$	Analog voltage range <sup>(3)</sup>	-0.5	$V_+ + 0.5$	V
$I_K$	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NO}, V_{NC}, V_{COM} > V_+$		mA
$I_{NO}$ $I_{NC}$ $I_{COM}$	On-state switch current	$V_{NC}, V_{NO}, V_{COM} = 0$ to $V_+$		mA
$V_I$	Digital input voltage range <sup>(3)</sup>	-0.5	6.5	V
$I_{IK}$	Digital input clamp current	$V_I < 0$		mA
$I_+$	Continuous current through $V_+$	-100	100	mA
$I_{GND}$	Continuous current through GND	-100	100	mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or V ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_+$	Supply voltage range	1.65	5.5	V
$V_{NO}$ $V_{NC}$ $V_{COM}$	Analog voltage range	0	$V_+$	V
$V_I$	Digital input voltage range	0	5.5	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TS5A63157		UNIT
		DBV	DCK	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209.9	298.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.1	103.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.8	107.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	65.3	2.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	82.5	106.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

## 6.5 Electrical Characteristics for 5-V Supply

 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Voltage undershoot	$V_{IKU}$	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50\text{ mA}$		5.5 V			-2	V
Peak ON-state resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		4.6	11	$\Omega$
			Full					
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 0$ , $I_{COM} = 30\text{ mA}$ Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		4	6.5	$\Omega$
			Full					
			25°C					
			Full					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 3.15\text{ V}$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		0.1	0.14	$\Omega$
			Full					
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		1.5	2	$\Omega$
			Full					
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V		0.001	0.03	$\mu\text{A}$
			Full					
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{COM} = 0 \text{ to } 5.5\text{ V}$ , $V_{NC} \text{ or } V_{NO} = 5.5\text{ V to } 0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	0		0.2	1	$\mu\text{A}$
			Full					
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V		0.001	0.01	$\mu\text{A}$
			Full					
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$ , Switch ON, See <a href="#">Figure 15</a>	25°C	5.5 V		0.003	0.03	$\mu\text{A}$
			Full					
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full			$V_+ \times 0.7$	5.5	V
Input logic low	$V_{IL}$		Full			0	$V_+ \times 0.3$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$	25°C	5.5 V		0.05	0.1	$\mu\text{A}$
			Full					

## Electrical Characteristics for 5-V Supply (continued)

 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	2	3.4	5	ns
				Full	4.5 V to 5.5 V	2		5.5	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	5 V	1	2.8	3.4	ns
				Full	4.5 V to 5.5 V	1		3.8	
Output voltage during undershoot	$V_{OUTU}$	See <a href="#">Figure 18</a>			2.5	$V_{OH}$ –0.3		V	
Output voltage during overshoot	$V_{OUTO}$	See <a href="#">Figure 18</a>				$V_{OL}$ +0.3	2	V	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	5 V	0.5	5	12	ns
				Full	4.5 V to 5.5 V	0.5		14	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 0.1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	5 V		–21	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	5 V		5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	5 V		14.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	5 V		14.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	5 V		2.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	5 V		371	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	5 V		–61	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	5 V		–61	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	5 V		0.06%		
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V	0.01	0.1	$\mu\text{A}$	
				Full			0.75		

## 6.6 Electrical Characteristics for 3.3-V Supply

 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Voltage undershoot	$V_{IKU}$	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50\text{ mA}$		3.6 V				V
Peak ON-state resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3 V		6.4	14	$\Omega$
			Full			18		
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 0$ , $I_{COM} = 24\text{ mA}$	25°C	3 V		4.8	8	$\Omega$
			Full			10		
		25°C	6.3			12		
		Full	15					
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 2.1\text{ V}$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3 V		0.1	0.2	$\Omega$
			Full			0.2		
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3 V		2.8	4	$\Omega$
			Full			7		
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V		0	0.03	$\mu\text{A}$
			Full			0.05		
	$I_{NC(PWROFF)}, I_{NO(PWROFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 3.6\text{ V}$ , $V_{COM} = 3.6\text{ V to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	0		0.15	0.50	
			Full			2		
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{COM} = 0 \text{ to } 3.6\text{ V}$ , $V_{NC} \text{ or } V_{NO} = 3.6\text{ V to } 0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	0		0.2	0.5	$\mu\text{A}$
			Full			5		
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V		0.001	0.01	$\mu\text{A}$
			Full			0.02		
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$ , Switch ON, See <a href="#">Figure 15</a>	25°C	3.6 V		0.003	0.03	$\mu\text{A}$
			Full			0.05		
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.7$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.3$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$	25°C	3.6 V		0.005	0.01	$\mu\text{A}$
			Full			0.02		

## Electrical Characteristics for 3.3-V Supply (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	2	4.3	6.6	ns
				Full	3 V to 3.6 V	2		7	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	1	3.3	6.3	ns
				Full	3 V to 3.6 V	1		7	
Output voltage during undershoot	$V_{OUTU}$	See <a href="#">Figure 18</a>			2.5	$V_{OH}$ –0.3		V	
Output voltage during overshoot	$V_{OUTO}$	See <a href="#">Figure 18</a>				$V_{OL}$ +0.3	2	V	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	3.3 V	0.5	7	17	ns
				Full	3 V to 3.6 V	0.5		19.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	25°C	3.3 V		–11.5		pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	25°C	3.3 V		5		pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	25°C	3.3 V		15		pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	25°C	3.3 V		15		pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	25°C	3.3 V		2.5		pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	25°C	3.3 V		370		MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	25°C	3.3 V		–60		dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	25°C	3.3 V		–60		dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	25°C	3.3 V		0.1%			
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V	0.05	0.1	$\mu\text{A}$	
				Full			0.6		



## 6.7 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Voltage undershoot	$V_{IKU}$	$0 \text{ mA} \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50 \text{ mA}$		2.7 V				V
Peak ON-state resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		9.2 30	35	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 0$ , $I_{COM} = 8 \text{ mA}$ Switch ON, See <a href="#">Figure 13</a> $V_{NO} \text{ or } V_{NC} = 2.3 \text{ V}$ , $I_{COM} = -8 \text{ mA}$	25°C Full 25°C Full	2.3 V		5.4 12 8.6	8.5 15.5 25	$\Omega$
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.6 \text{ V}$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		0.05	0.3 0.5	$\Omega$
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -8 \text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C Full	2.3 V		5	9 15	$\Omega$
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	2.7 V		0	0.03 0.05	$\mu\text{A}$
	$I_{NC(PWROFF)}, I_{NOPWROFF}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 2.7 \text{ V}$ , $V_{COM} = 2.7 \text{ V to } 0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C Full	0		0.15	0.50 0.75	
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{COM} = 0 \text{ to } 2.7 \text{ V}$ , $V_{NC} \text{ or } V_{NO} = 2.7 \text{ V to } 0$ , Switch ON, See <a href="#">Figure 14</a>	25°C Full	0		0.2	0.5 1	$\mu\text{A}$
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = \text{Open}$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	2.7 V		0.001	0.01 0.02	$\mu\text{A}$
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$ , Switch ON, See <a href="#">Figure 15</a>	25°C Full	2.7 V		0.003	0.03 0.05	$\mu\text{A}$
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.75$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.25$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$	25°C	2.7 V		0.005	0.01	$\mu\text{A}$
			Full					

## Electrical Characteristics for 2.5-V Supply (continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ or GND, $R_L = 500 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	3	5.8	9.6	ns
				Full	2.3 V to 2.7 V	3		12	
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ or GND, $R_L = 500 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	1.5	4.5	7.3	ns
				Full	2.3 V to 2.7 V	1.5		7.5	
Output voltage during undershoot	$V_{OUTU}$	See <a href="#">Figure 18</a>			2.5	$V_{OH}$ –0.3		V	
Output voltage during overshoot	$V_{OUTO}$	See <a href="#">Figure 18</a>				$V_{OL}$ +0.3	2	V	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50 \Omega$ ,	$C_L = 50 \text{ pF}$ , See <a href="#">Figure 19</a>	25°C	2.5 V	0.5	10	25	ns
				Full	2.3 V to 2.7 V	0.5		28.5	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 0.1 \text{ nF}$ , See <a href="#">Figure 23</a>	25°C	2.5 V		–8	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	2.5 V		5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		15	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	2.5 V		15	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		2.5	pF	
Bandwidth	BW	$R_L = 50 \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	2.5 V		367	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	2.5 V		–60	dB	
Crosstalk	$X_{TALK}$	$R_L = 50 \Omega$ , $f = 10 \text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	2.5 V		–60	dB	
Total harmonic distortion	THD	$R_L = 600 \Omega$ , $C_L = 50 \text{ pF}$ ,	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	2.5 V		0.15%		
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V	0.05	0.1	nA	
				Full			0.5		

## 6.8 Electrical Characteristics for 1.8-V Supply

 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

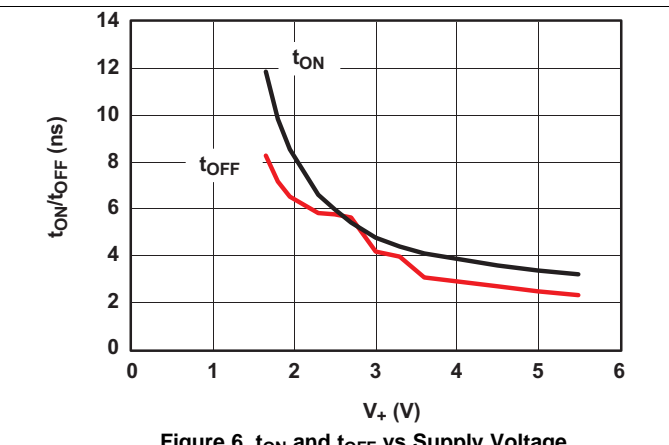
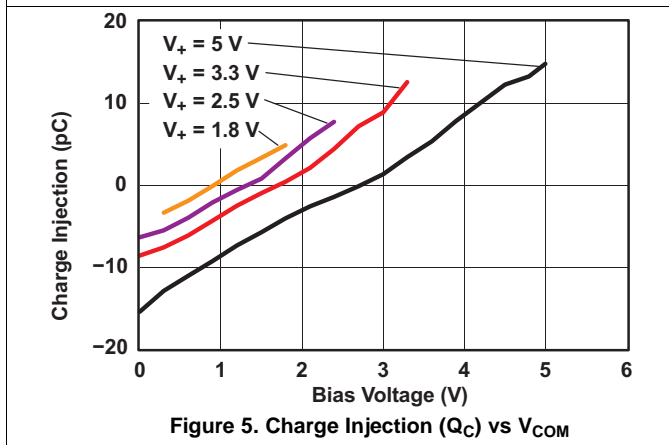
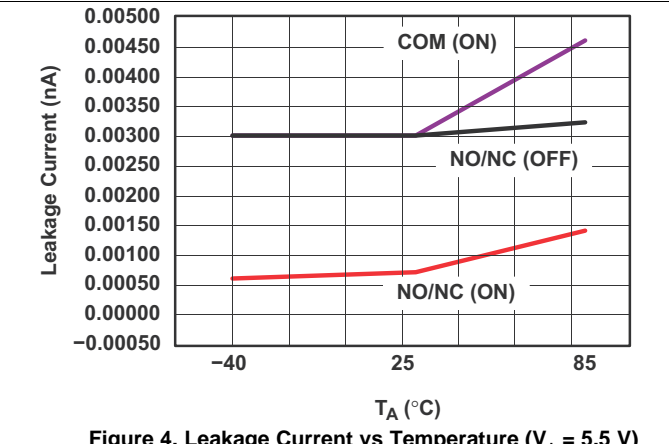
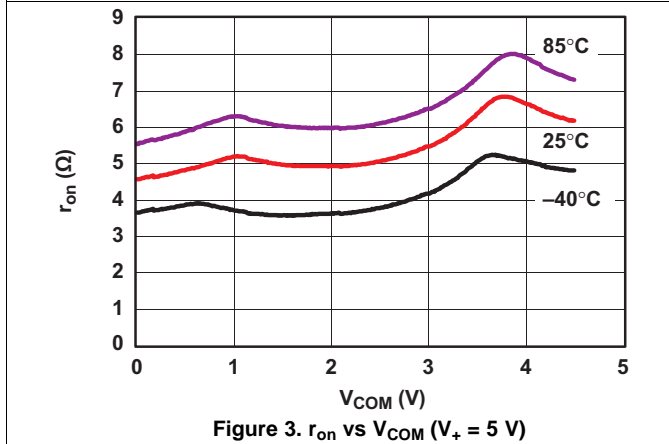
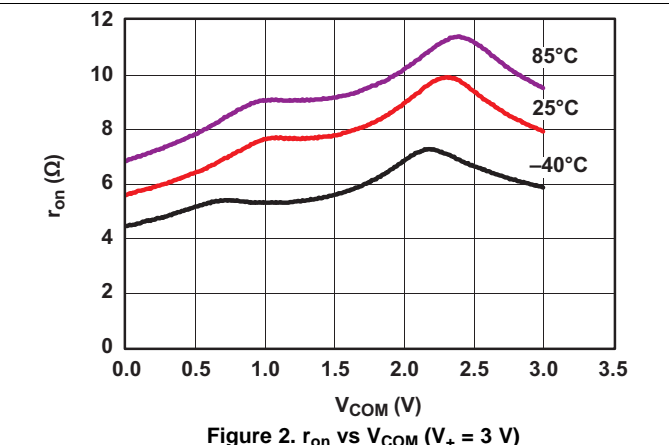
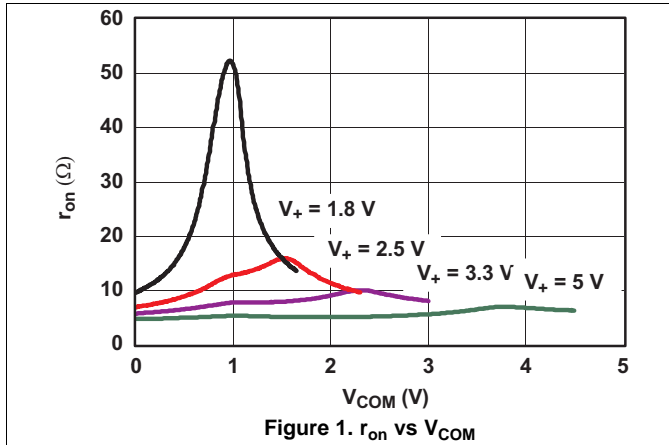
PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Analog signal range	$V_{COM}, V_{NO}, V_{NC}$				0		$V_+$	V
Voltage undershoot	$V_{IKU}$	$0 \geq (I_{NC}, I_{NO}, \text{ or } I_{COM}) \geq -50\text{ mA}$		1.95 V				V
Peak ON-state resistance	$r_{peak}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -4\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	13.8	60	$\Omega$
				Full			120	
ON-state resistance	$r_{on}$	$V_{NO} \text{ or } V_{NC} = 0$ , $I_{COM} = 4\text{ mA}$	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	5.9	15	$\Omega$
				Full			15	
		25°C				12.8	40	
		Full				45		
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} \text{ or } V_{NC} = 1.15\text{ V}$ , $I_{COM} = -4\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	0.1	0.5	$\Omega$
				Full			0.8	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$ , $I_{COM} = -4\text{ mA}$ ,	Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V	26.5	60	$\Omega$
				Full			80	
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V	0	0.03	$\mu\text{A}$
				Full			0.05	
	$I_{NC(PWROFF)}, I_{NOPWROFF}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } 1.95\text{ V}$ , $V_{COM} = 1.95\text{ V to } 0$ ,	Switch OFF, See <a href="#">Figure 14</a>	25°C	0	0.15	0.50	
				Full			0.75	
COM OFF leakage current	$I_{COM(PWROFF)}$	$V_{COM} = 0 \text{ to } 1.95\text{ V}$ , $V_{NC} \text{ or } V_{NO} = 1.95\text{ V to } 0$ ,	Switch ON, See <a href="#">Figure 14</a>	25°C	0	0.2	0.5	$\mu\text{A}$
				Full			1	
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = \text{Open}$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	1.95 V	0.001	0.01	$\mu\text{A}$
				Full			0.02	
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$ ,	Switch ON, See <a href="#">Figure 15</a>	25°C	1.95 V	0.003	0.03	$\mu\text{A}$
				Full			0.05	
<b>Digital Control Input (IN)</b>								
Input logic high	$V_{IH}$		Full		$V_+ \times 0.75$		5.5	V
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.25$	V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or } 0$	25°C	1.95 V	0.005	0.01	$\mu\text{A}$	
			Full			0.02		

## Electrical Characteristics for 1.8-V Supply (continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Dynamic</b>									
Turn-on time	$t_{ON}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	9.5	23	ns	
				Full	1.65 V to 1.95 V		24		
Turn-off time	$t_{OFF}$	$V_{COM} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	5.9	10	ns	
				Full	1.65 V to 1.95 V		12		
Output voltage during undershoot	$V_{OUTU}$	See <a href="#">Figure 18</a>			2.5	$V_{OH}$ –0.3		V	
Output voltage during overshoot	$V_{OUTO}$	See <a href="#">Figure 18</a>				$V_{OL}$ +0.3	2	V	
Break-before-make time	$t_{BBM}$	$V_{NC} = V_{NO} = V_+/2$ , $R_L = 50\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 19</a>	25°C	1.8 V	0.5	18	50	ns
				Full	1.65 V to 1.95 V	0.5		55	
Charge injection	$Q_C$	$V_{GEN} = 0$ , $R_{GEN} = 0$ ,	$C_L = 0.1\text{ nF}$ , See <a href="#">Figure 23</a>	25°C	1.8 V		–5	pC	
NC, NO OFF capacitance	$C_{NC(OFF)}$ , $C_{NO(OFF)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 16</a>	25°C	1.8 V		5.5	pF	
NC, NO ON capacitance	$C_{NC(ON)}$ , $C_{NO(ON)}$	$V_{NC}$ or $V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	1.8 V		15.5	pF	
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 16</a>	25°C	1.8 V		15.5	pF	
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 16</a>	25°C	1.8 V		2.5	pF	
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 20</a>	25°C	1.8 V		369	MHz	
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 21</a>	25°C	1.8 V		–60	dB	
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 22</a>	25°C	1.8 V		–60	dB	
Total harmonic distortion	THD	$R_L = 600\ \Omega$ , $C_L = 50\text{ pF}$ ,	$f = 20\text{ Hz to }20\text{ kHz}$ , See <a href="#">Figure 24</a>	25°C	1.8 V		0.4%		
<b>Supply</b>									
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V	0.05	0.06	$\mu\text{A}$	
				Full			0.3		

### 6.9 Typical Characteristics



Typical Characteristics (continued)

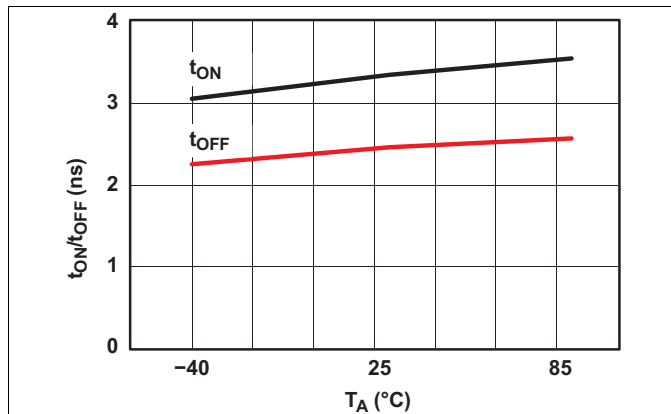


Figure 7.  $t_{ON}$  and  $t_{OFF}$  vs Temperature ( $V_+ = 5\text{ V}$ )

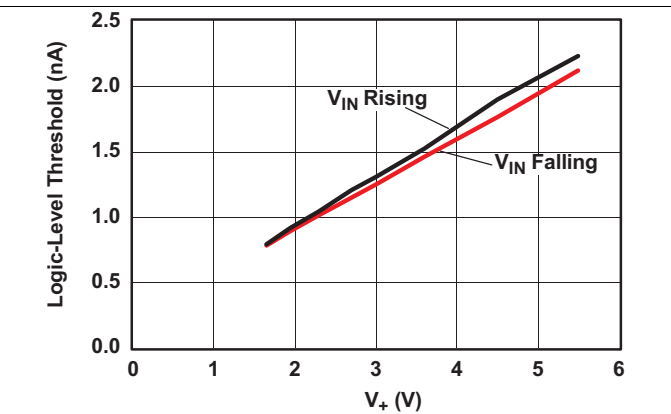


Figure 8. Logic-Level Threshold vs  $V_+$

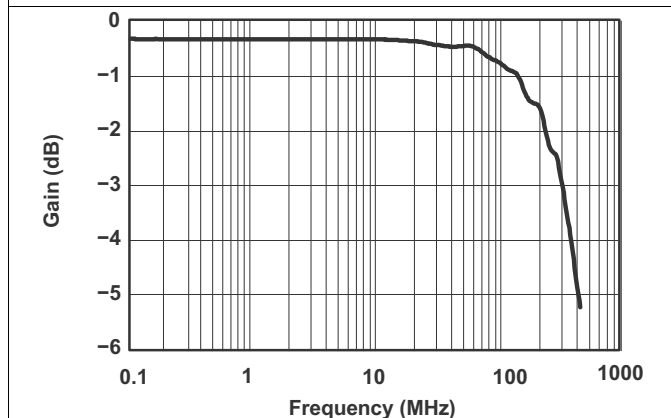


Figure 9. Bandwidth ( $V_+ = 3.3\text{ V}$ )

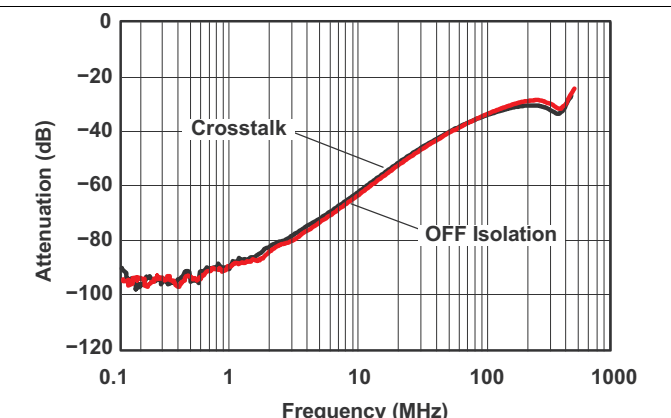


Figure 10. OFF Isolation and Crosstalk ( $V_+ = 3.3\text{ V}$ )

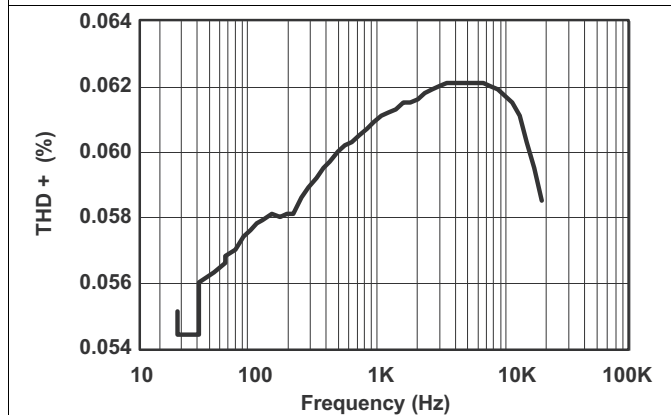


Figure 11. Total Harmonic Distortion (THD) vs Frequency ( $V_+ = 3.3\text{ V}$ )

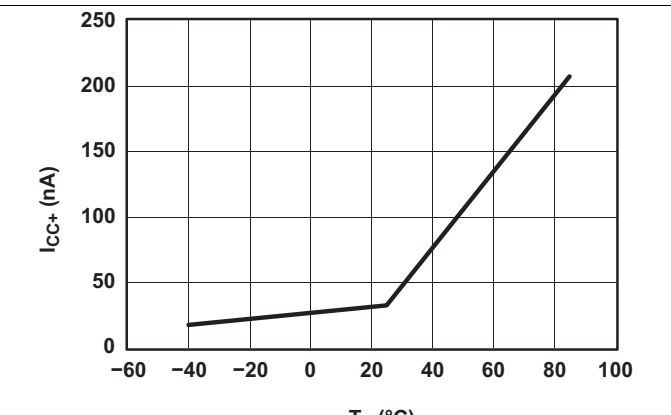


Figure 12. Power-Supply Current vs Temperature ( $V_+ = 5\text{ V}$ )

## 7 Parameter Measurement Information

**Table 1. Parameter Description**

SYMBOL	DESCRIPTION
$V_{COM}$	Voltage at COM
$V_{NC}$	Voltage at NC
$V_{NO}$	Voltage at NO
$r_{on}$	Resistance between COM and NC or COM and NO ports when the channel is ON
$r_{peak}$	Peak on-state resistance over a specified voltage range
$\Delta r_{on}$	Difference of $r_{on}$ between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$V_{IH}$	Minimum input voltage for logic high for the control input (IN)
$V_{IL}$	Maximum input voltage for logic low for the control input (IN)
$V_I$	Voltage at the control input (IN)
$I_{IH}, I_{IL}$	Leakage current measured at the control input (IN)
$t_{ON}$	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
$t_{OFF}$	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
$t_{BBM}$	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
$Q_C$	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$ , $C_L$ is the load capacitance and $\Delta V_{COM}$ is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
$C_I$	Capacitance of control input (IN)
$O_{ISO}$	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
$X_{TALK}$	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion is defined as the ratio of the root mean square (RMS) value of the second, third, and higher harmonics to the magnitude of fundamental harmonic.
$I_+$	Static power-supply current with the control (IN) pin at $V_+$ or GND
$V_{OUTU}$	Output voltage during an undershoot event. This is measured by turning off a specific channel and applying an undershoot voltage at the input of the switch.
$V_{OUTO}$	Output voltage during an overshoot event. This is measured by turning off a specific channel and applying an overshoot voltage at the input of the switch.

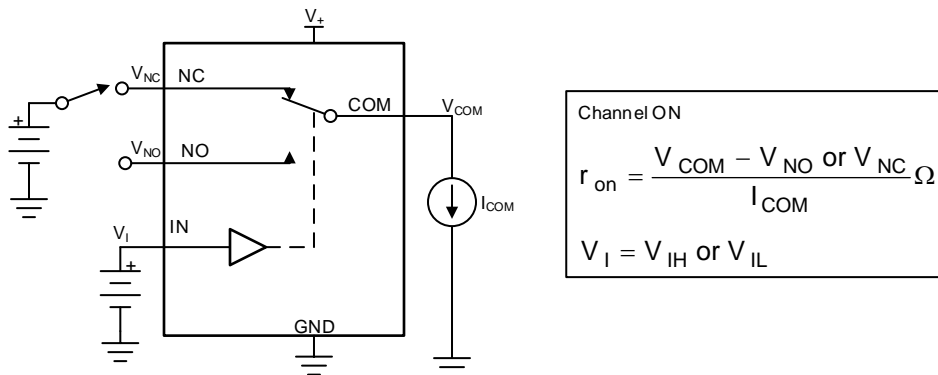


Figure 13. ON-State Resistance ( $r_{on}$ )

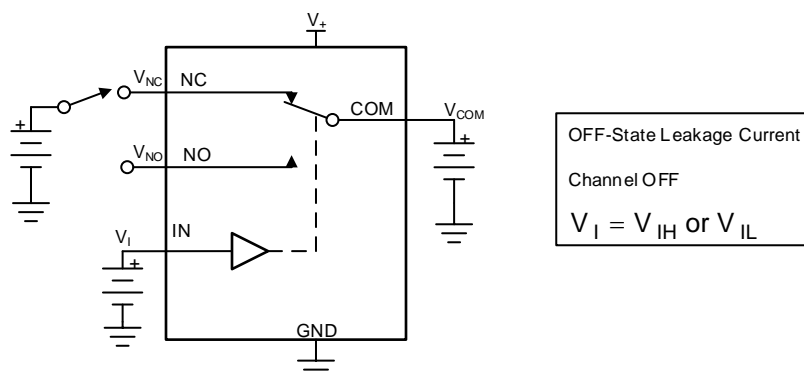


Figure 14. OFF-State Leakage Current ( $I_{NC(OFF)}$ ,  $I_{NC(PWROFF)}$ ,  $I_{NO(OFF)}$ ,  $I_{NO(PWROFF)}$ ,  $I_{COM(OFF)}$ ,  $I_{COM(PWROFF)}$ )

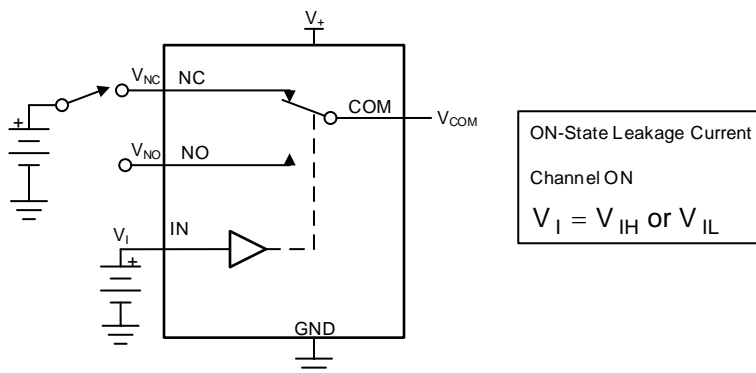


Figure 15. ON-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{NC(ON)}$ ,  $I_{NO(ON)}$ )



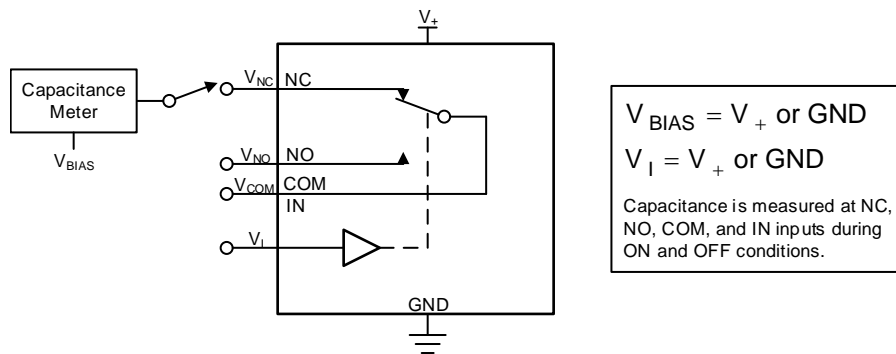
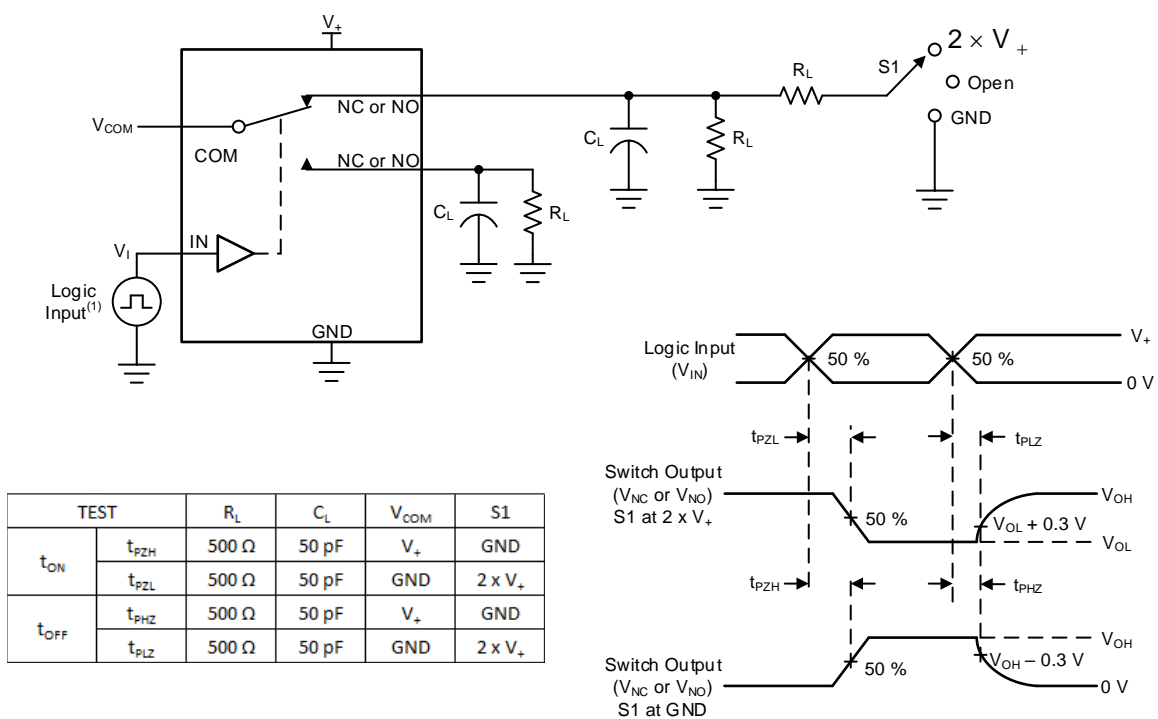


Figure 16. Capacitance ( $C_{IN}$ ,  $C_{COM(ON)}$ ,  $C_{NC(OFF)}$ ,  $C_{NO(OFF)}$ ,  $C_{NC(ON)}$ ,  $C_{NO(ON)}$ )



(1) All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.

Figure 17. Turn-On ( $t_{ON}$ ) and Turn-Off ( $t_{OFF}$ ) Time

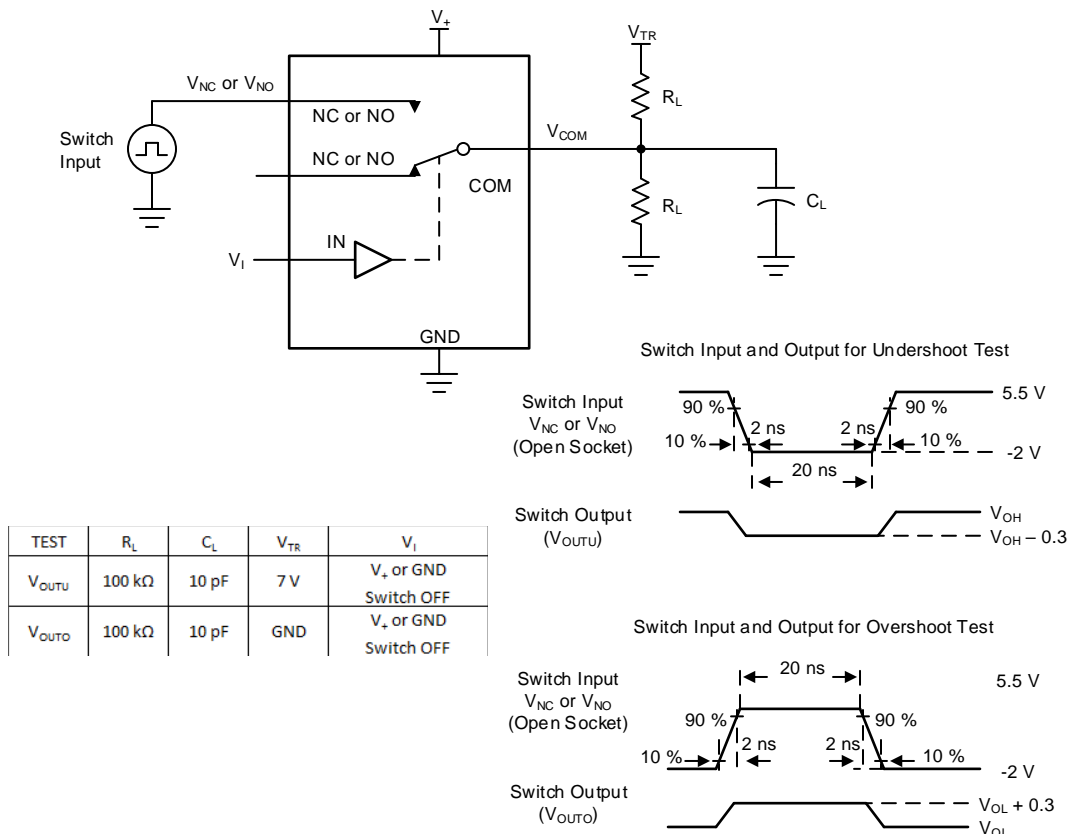
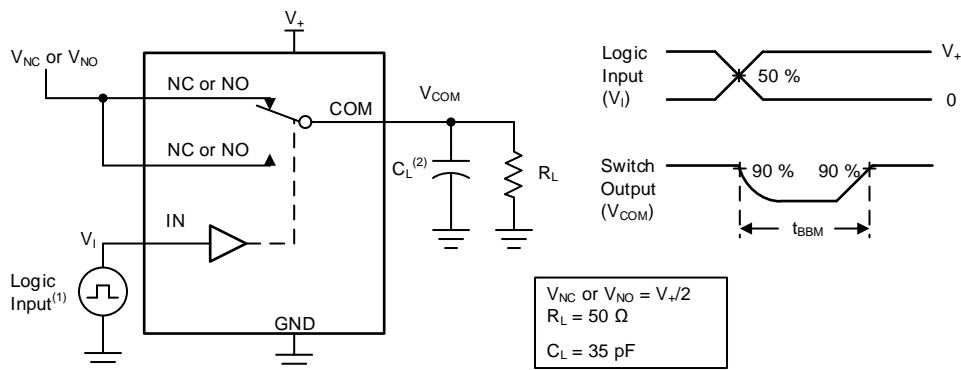


Figure 18. Undershoot and Overshoot Test



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr < 5 ns, tf < 5 ns.
- (2) CL includes probe and jig capacitance.

Figure 19. Break-Before-Make (tBBM) Time

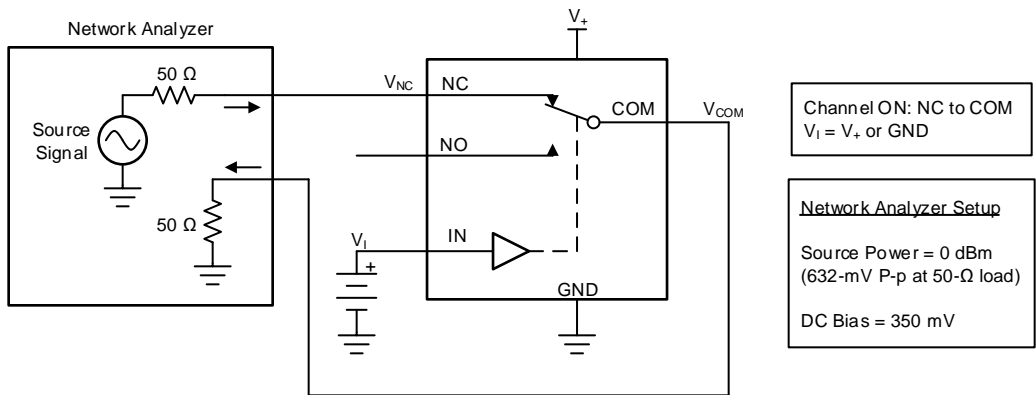


Figure 20. Bandwidth (BW)

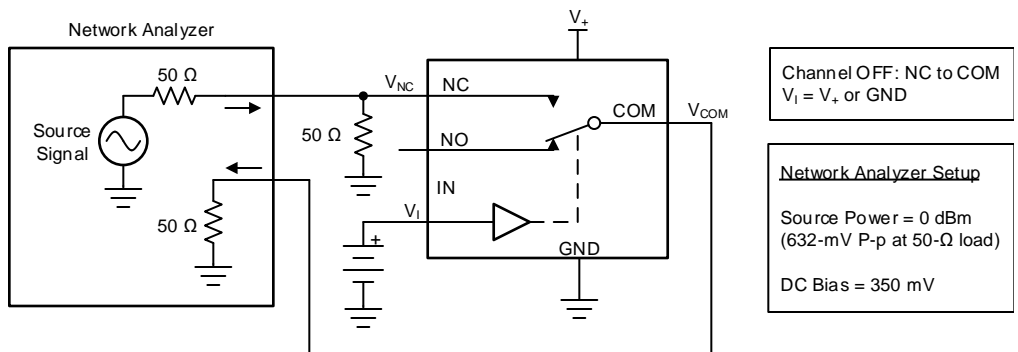


Figure 21. OFF Isolation ( $O_{ISO}$ )

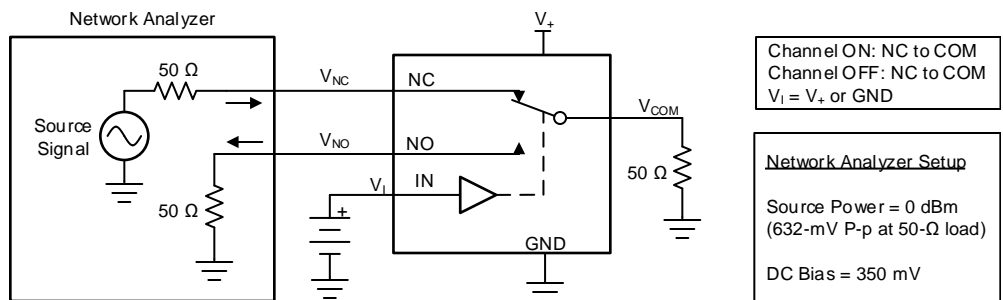
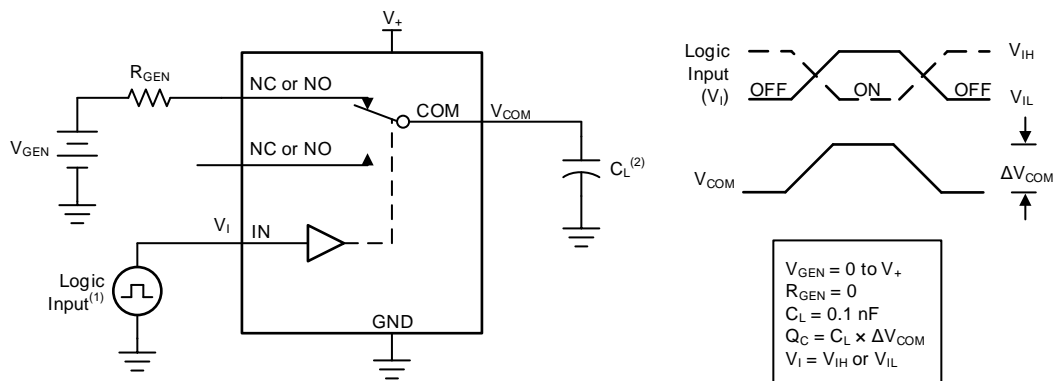
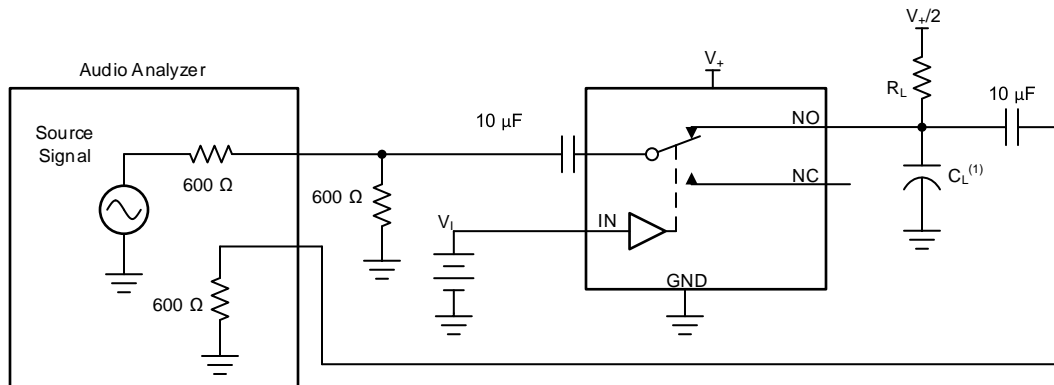


Figure 22. Crosstalk ( $X_{TALK}$ )



- (1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- (2) C<sub>L</sub> includes probe and jig capacitance.

**Figure 23. Charge Injection (Q<sub>c</sub>)**



- (1) C<sub>L</sub> includes probe and jig capacitance.

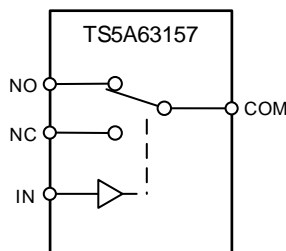
**Figure 24. Total Harmonic Distortion (THD)**

## 8 Detailed Description

### 8.1 Overview

The TS5A63157 is a single-pole, double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. This device can handle both digital and analog signals. Signals up to  $V_+$  (peak) can be transmitted in either direction.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Integrated Overshoot and Undershoot Protection Circuitry

The TS5A63157 senses overshoot and undershoot events at the I/Os and responds by preventing voltage differentials from developing and turning the switch on.

#### 8.3.2 Isolation in Powered-Off Mode, $V_+ = 0$ V

The TS5A63157 provides isolation when the supply voltage is removed ( $V_+ = 0$  V). When the TMUX1511 is powered-off, the I/Os of the device remain in a high-Z state. Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path.

#### 8.3.3 Break-before-make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as break-before-make delay.

### 8.4 Device Functional Modes

Table 2. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TS5A63157 can be used in a variety of customer systems. The TS5A63157 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

### 9.2 Typical Application

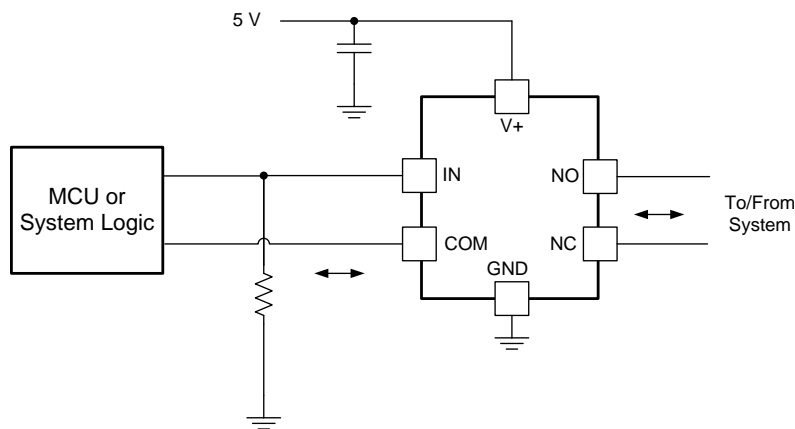


Figure 25. System Schematic for TS5A63157

#### 9.2.1 Design Requirements

In this particular application,  $V_+$  was 1.8 V, although  $V_+$  is allowed to be any voltage specified in . A decoupling capacitor is recommended on the  $V_+$  pin. See for more details.

#### 9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

#### 9.2.3 Application Curve

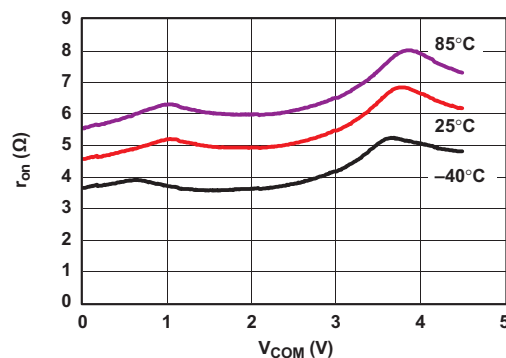


Figure 26.  $r_{on}$  vs  $V_{COM}$ ,  $V_+ = 5$  V

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the .

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  bypass capacitor is recommended. If there are multiple pins labeled  $V_{CC}$ , then a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each  $V_{CC}$  because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu\text{F}$  bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased  $I_{CC}$  or unknown switch selection states.

### 11.2 Layout Example

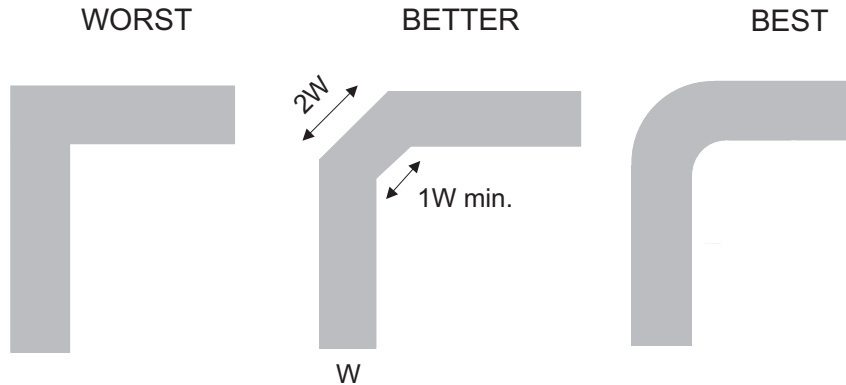


Figure 27. Trace Example

## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A63157DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(JBEF, JBER)	<a href="#">Samples</a>
TS5A63157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JBEF	<a href="#">Samples</a>
TS5A63157DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(J75, J7F, J7R)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A63157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A63157DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A63157DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A63157DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A63157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

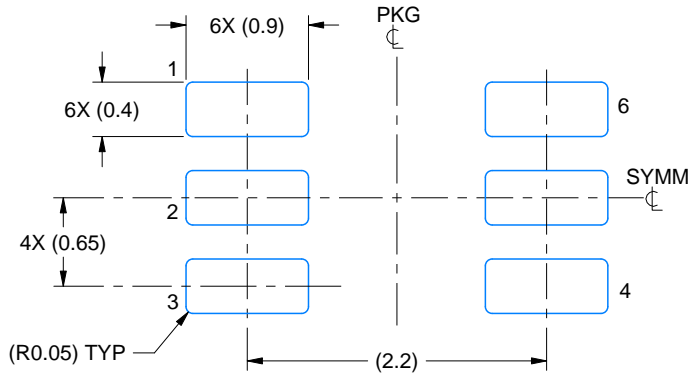
## TAPE AND REEL BOX DIMENSIONS



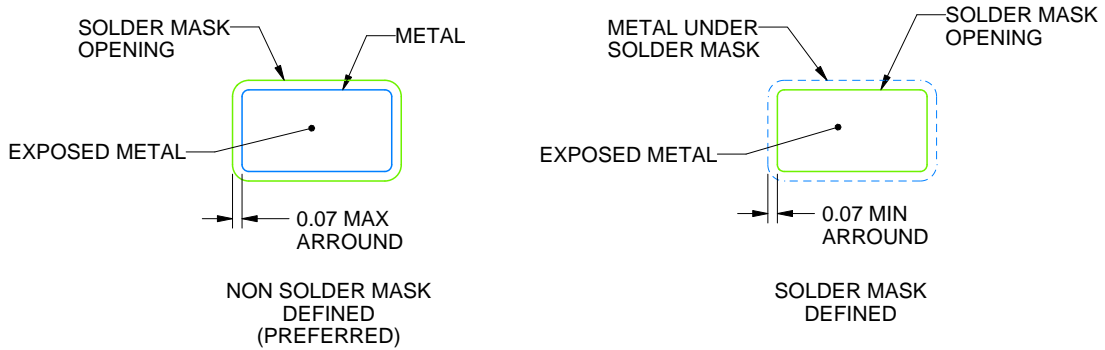
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A63157DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A63157DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TS5A63157DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
TS5A63157DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A63157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

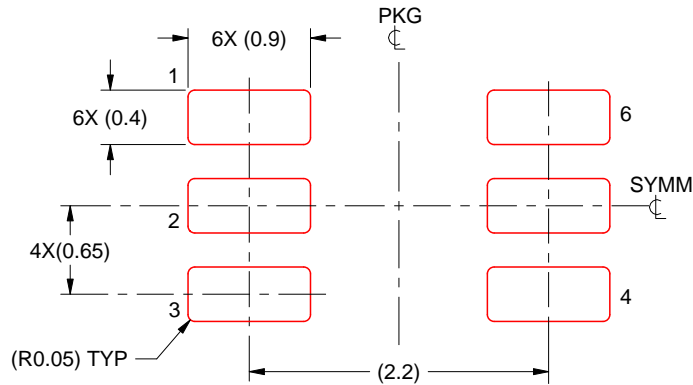


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.





# EXAMPLE BOARD LAYOUT

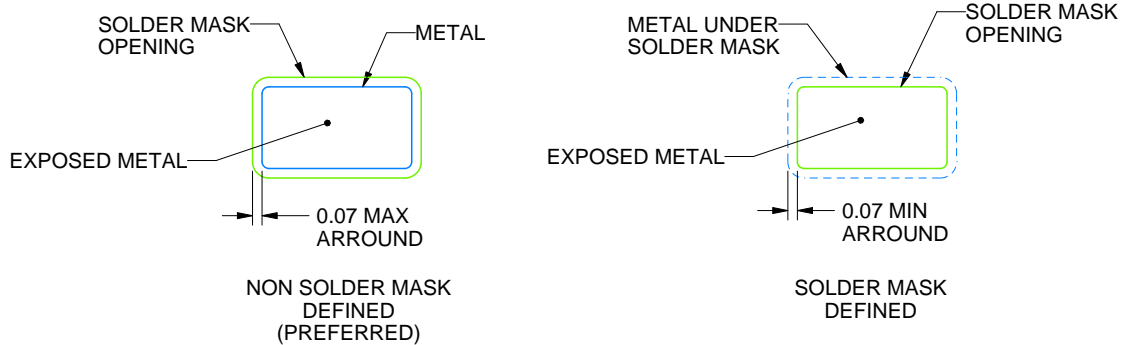
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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