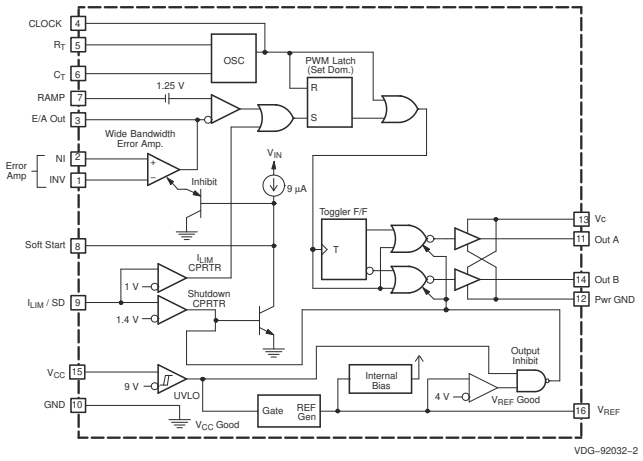
UC1825B-SP V 类耐辐射高速 PWM 控制器

1 特性

- 符合 QML-V 标准，SMD 5962-8768106
- 5962**R**8768106VYC：
  - 耐辐射加固保障 (RHA) 能力高达 100krad(Si) 总电离剂量 (TID) [1]
- 与电压或电流模式拓扑兼容
- 实际工作开关频率高达 1MHz
- 50ns 传播延迟到输出
- 大电流双图腾柱输出（2A 峰值）
- 宽带宽误差放大器
- 带有双脉冲抑制功能的全锁存逻辑
- 逐脉冲电流限制
- 软启动/最大占空比控制
- 带有迟滞功能的欠压锁定
- 低启动电流 (1.1mA)

2 应用

- 耐辐射直流/直流转换器
- 卫星总线和有效载荷
- 通信负载
- 光学成像有效载荷
- 雷达成像有效载荷
- 太空运载火箭
- 支持多种拓扑结构：
  - 反激、正激、降压、升压
  - 推挽、半桥、全桥（采用外部接口电路时）



方框图

3 说明

UC1825B-SP PWM 控制器件针对高频开关模式电源应用进行了优化。对在大大增加误差放大器的带宽和转换率的同时，大大减小通过比较器和逻辑电路的传播延迟给与了特别关注。这个控制器设计用于电流模式或电压模式系统，此系统具有输出电压前馈功能。

保护电路包括一个阈值电压为 1V 的电流限制比较器、一个 TTL 兼容关断端口和一个软启动引脚，此引脚可对折为一个最大占空比钳位。此逻辑被完全锁存以提供无抖动运行，并且抑制了输出上的多脉冲。一个具有 800mV 滞后的欠压闭锁部分可确保低启动电流。欠压闭锁期间，输出为高阻抗。

这个器件特有推挽式输出，此输出被设计用来拉、灌来自电容负载（诸如一个功率金属氧化物半导体场效应晶体管 (MOSFET) 的栅极）的高峰值电流。导通状态设计为高电平。

器件信息

器件型号(1)	等级(2)	封装
5962R8768106VYC	飞行等级 QMLV-RHA 100krad(Si)	CFP (16) 10.16mm x 7.10mm
UC1825BHKT/EM	工程样片(3)	
5962R8768106V9A	飞行等级 QMLV-RHA KGD 100krad(Si)	裸片

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 有关器件等级的其他信息，请查看 SLYB235。
(3) 这些器件仅适用于工程评估。器件按照不合规的流程进行加工处理。这些器件不适用于鉴定、生产、辐射测试或飞行用途。这些零器件无法在 –55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。

[1] 辐射耐受性是基于初始器件认证（剂量率 = 10mrad(Si)/s）获得的典型值。提供辐射批次验收测试 - 详细信息请联系厂家。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (April 2019) to Revision A (December 2020)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Added Bare Die Information table to *Pin Configuration and Functions* section	3
• Added UC1825B-SP Bare Die Pin Number Locations figure to *Pin Configuration and Functions* section	3
• Added Bond Pad Coordinates in Microns table to *Pin Configuration and Functions* section	3
• Updated *Synchronization* section	11

5 Pin Configuration and Functions

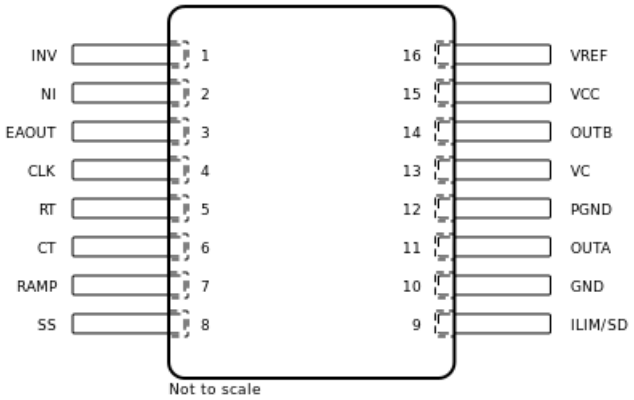


图 5-1. HKT Package
16-Pin CFP
Top View

表 5-1. Pin Functions

NAME	NO.	I/O	DESCRIPTION
CLK	4	O	Output of the internal oscillator.
CT	6	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	O	Output of the error amplifier for compensation.
GND	10	—	Analog ground return pin.
ILIM/SD	9	I	Input to the current limit comparator and the shutdown comparator.
INV	1	I	Inverting input to the error amplifier.
NI	2	I	Non-inverting input to the error amplifier.
OUTA	11	O	High-current totem pole output A of the on-chip drive stage.
OUTB	14	O	High-current totem pole output B of the on-chip drive stage.
PGND	12	—	Ground return pin for the output driver stage.
RAMP	7	I	Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	I	Timing resistor connection pin for oscillator frequency programming.
SS	8	I	Soft-start input pin which also doubles as the maximum duty cycle clamp.
VC	13	—	Power supply pin for the output stage. This pin should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	—	Power supply pin for the device. This pin should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VREF	16	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1- μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

表 5-2. Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Backgrind Si - Finish	GND	AlCu	2000 nm

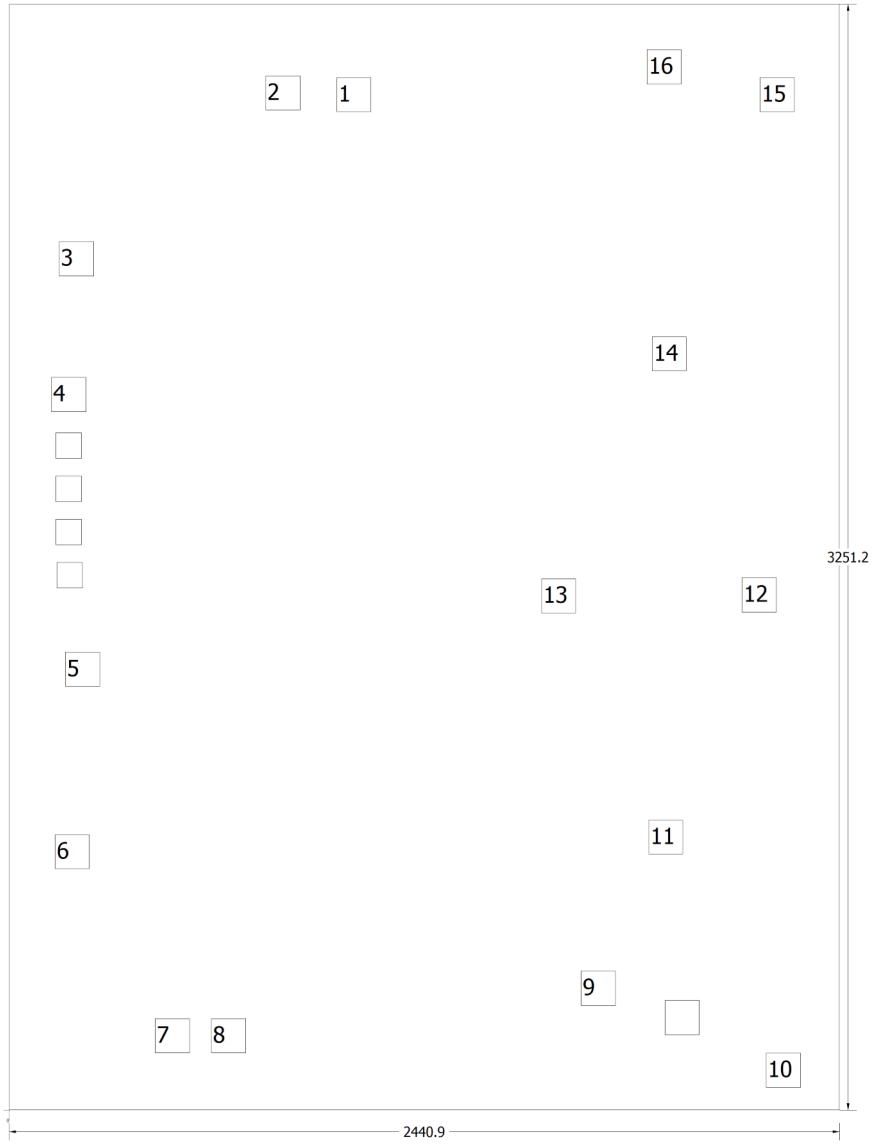


图 5-2. UC1825B-SP Bare Die Pin Number Locations

表 5-3. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
INV	1	962.66	2933.7	1064.26	3035.3
NI	2	754.38	2938.78	855.98	3040.38
EAOUT	3	147.32	2451.1	248.92	2552.7
CLK	4	124.46	2052.32	226.06	2153.92
RT	9	165.1	1244.6	266.7	1346.2
CT	10	134.62	708.66	236.22	810.26
RAMP	11	429.26	167.64	530.86	269.24
SS	12	594.36	167.64	695.96	269.24
ILIM/SD	13	1681.48	307.34	1783.08	408.94
GND	15	2225.04	66.04	2326.64	167.64
OUTA	16	1879.6	751.84	1981.2	853.44
PGND	17	2153.92	1463.04	2255.52	1564.64
VC	18	1564.64	1460.5	1666.24	1562.1
OUTB	19	1889.76	2171.7	1991.36	2273.3
VCC	20	2207.26	2933.7	2308.86	3035.3
RAMP	21	1874.52	3014.98	1976.12	3116.58

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply voltage	VC, VCC		30	V
	Output current, source or sink, OUTA, OUTB	DC		0.5	A
		Pulse (0.5 μs)		2.0	
	Analog inputs	INV, NI, RAMP	–0.3	7	V
		SS, ILIM/SD	–0.3	6	
	Clock output current	CLK		–5	mA
	Error amplifier output current	EAOUT		5	mA
	Soft-start sink current	SS		20	mA
	Oscillator charging current	RT		–5	mA
	Power dissipation			1	W
	Lead temperature (soldering, 10 seconds)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND; all currents are positive into, negative out of part; pin numbers refer to CFP-16 package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range ($T_A = T_J$ = –55°C to 125°C), unless otherwise noted.

		MIN	MAX	UNIT
V_{CC}	Supply voltage	10	30	V
	Sink/source output current (continuous or time average)	0	100	mA
	Reference load current	0	10	mA

6.4 Thermal Information

THERMAL METRIC[1]		UC1825B-SP HKT (CFP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V, –55°C < T_A < 125°C, T_A = T_J

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Output voltage	T_J = 25°C, I_O = 1 mA	5.024	5.1	5.176	V
Line regulation	10 V < V_{CC} < 30 V		2	20	mV
Load regulation	1 mA < I_O < 10 mA		5	20	mV
Total output variation	Line, load, temperature	5		5.2	V
Output noise voltage	10 Hz < f < 10 kHz		50		μV
Short-circuit current	V_{REF} = 0 V	–15	–50	–100	mA
OSCILLATOR SECTION					
Initial accuracy	T_J = 25°C	360	400	440	kHz
Voltage stability	10 V < V_{CC} < 30 V		0.2%	2%	
Temperature stability	T_{MIN} < T_A < T_{MAX}		5%	16%	
Total variation	Line, Temperature	340		460	kHz
Clock out high		3.9	4.5		V
Clock out low			2.3	2.9	V
Ramp peak[1]		2.6	2.8	3	V
Ramp valley[1]		0.7	1	1.25	V
Ramp valley to peak[1]		1.6	1.8	2.1	V
ERROR AMPLIFIER					
Input offset voltage				10	mV
Input bias current			0.6	3	μA
Input offset current			0.1	1	μA
Open-loop gain	1 V < V_O < 4 V	60	95		dB
CMRR	1.5 V < V_{CM} < 5.5 V	75	95		dB
PSRR	10 V < V_{CC} < 30 V	85	110		dB
Output sink current	$V_{E/AOut}$= 1 V	1	2.5		mA
Output source current	$V_{E/AOut}$ = 4 V	–0.5	–1.3		mA
Output high voltage	$I_{E/AOut}$ = –0.5 mA	4	4.7	5.	V
Output low voltage	$I_{E/AOut}$ = 1 mA	0	0.5	1	V
Gain bandwidth product[1]	f = 200 kHz	5	10.5		MHz
Slew rate[1]		4	9		V/μs

6.5 Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for R_T = 3.65 kΩ, C_T = 1 nF, V_{CC} = 15 V, –55°C < T_A < 125°C, T_A = T_J

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR					
Ramp bias current	V_{Ramp} = 0 V		–1	–5	µA
Duty cycle range		0%		80%	
E/A out zero dc threshold	V_{Ramp} = 0 V	1.1	1.25		V
Delay to output(1)			50	80	ns
SOFT-START					
Charge current	$V_{Soft\ Start}$ = 0.5 V	3	9	20	µA
Discharge current	$V_{Soft\ Start}$ = 1 V	1			mA
CURRENT LIMIT/SHUTDOWN					
Current limit/shutdown bias current	0 < $V_{ILIM/SD}$ < 4 V			15	µA
Current limit threshold		0.9	1	1.1	V
Shutdown threshold		1.25	1.4	1.55	V
Delay to output(1)			50	80	ns
OUTPUT					
Low-level output voltage	I_{OUT} = 20 mA		0.25	0.4	V
	I_{OUT} = 200 mA		1.2	2.2	
High-level output voltage	I_{OUT} = –20 mA	13	13.5		V
	I_{OUT} = –200 mA	12	13		
Collector leakage	V_C = 30 V		10	500	µA
Rise/fall time(1)	C_L = 1 nF		30	75	ns
UNDERVOLTAGE LOCKOUT					
Start threshold		8.8	9.2	9.6	V
UVLO hysteresis		0.4	0.8	1.2	V
SUPPLY CURRENT SECTION					
Startup current	V_{CC} = 8 V		1.1	2.5	mA
I_{CC}	V_{INV} = V_{Ramp} = $V_{ILIM/SD}$ = 0 V, V_{NI} = 1 V		22	33	mA

(1) Parameters ensured by design and/or characterization, if not production tested.

6.6 Typical Characteristics

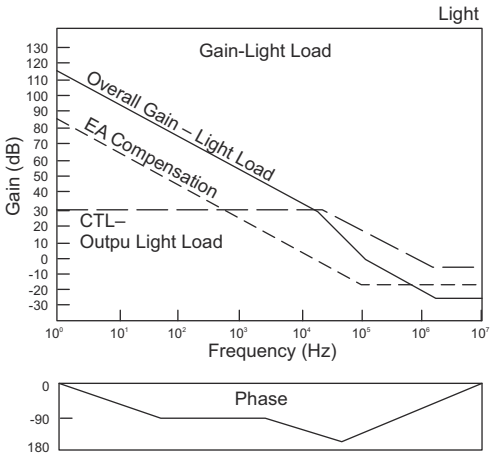


图 6-1. Gain: Light Load

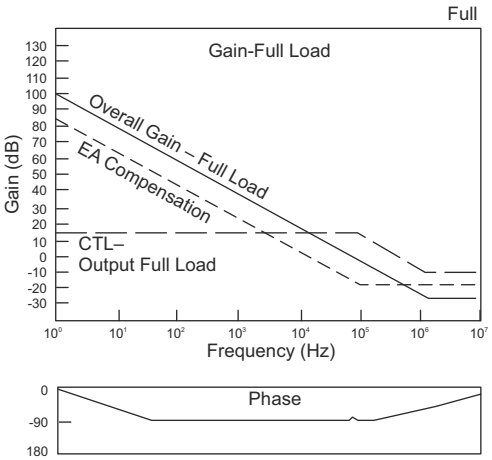


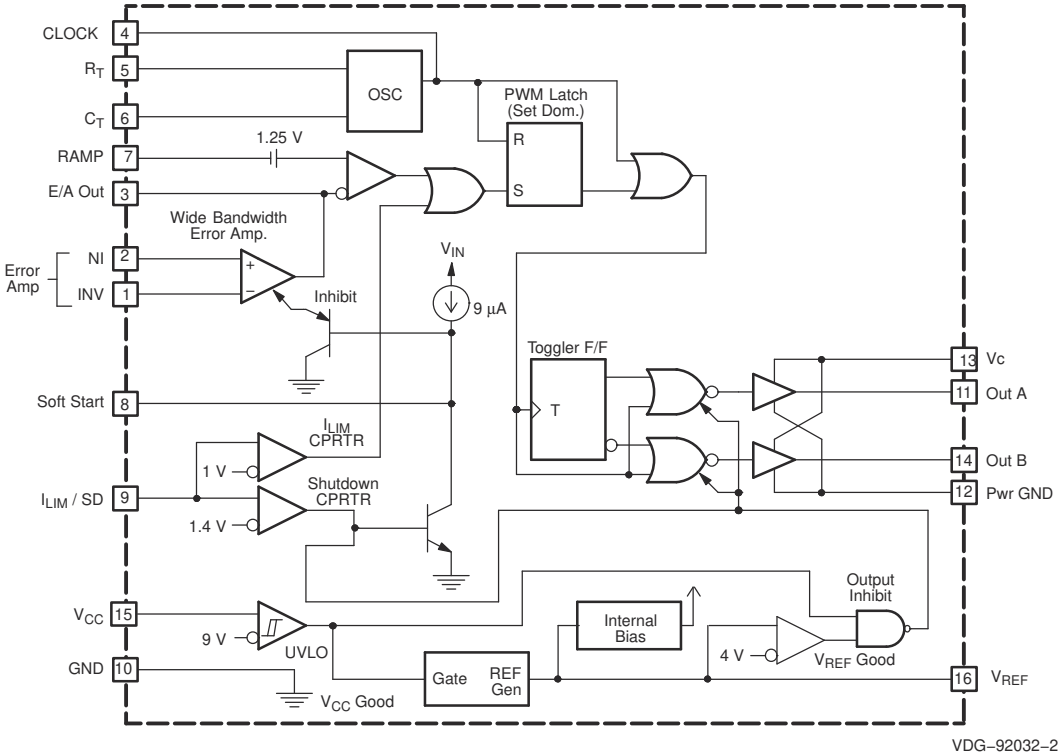
图 6-2. Gain: Full Load

7 Detailed Description

7.1 Overview

UC1825B-SP PWM controller is a radiation hardened version of the standard UC1825 family. Error amplifier gain bandwidth product is 10.5 MHz. Protection circuitry includes a current limit comparator with a 1-V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty-cycle clamp. The logic is fully latched to provide jitter-free operation and prohibit multiple pulses at an output. An undervoltage lockout section with 800 mV of hysteresis assures low start up current. During undervoltage lockout, the outputs are high impedance. This device features totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

7.2 Functional Block Diagram



VDG–92032–2

7.3 Feature Description

UC1825B-SP can be configured as current mode controller, used to support various topologies such as forward, flyback, buck, boost and using an external interface circuit will also support half-bridge, full bridge, and push-pull configurations.

7.3.1 Control Methods

图 7-1 shows the control methods.

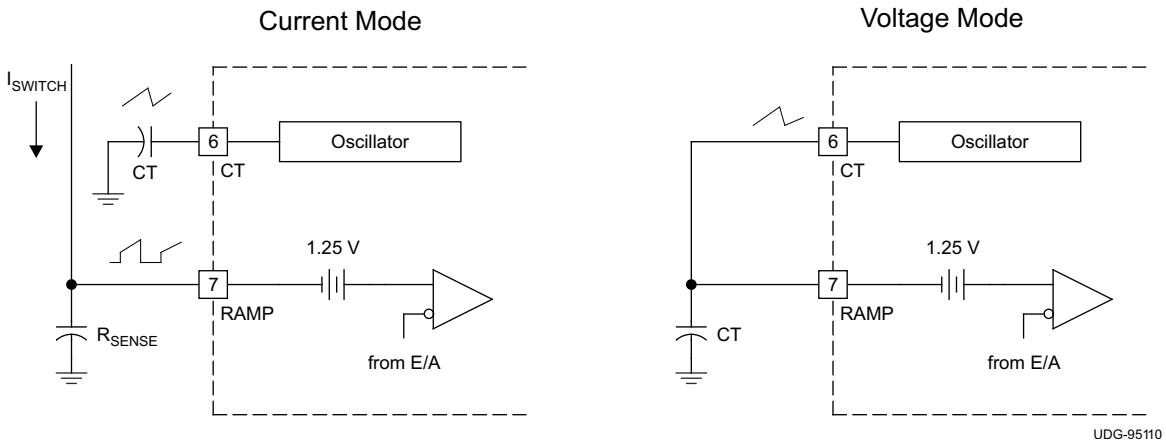


图 7-1. Control Methods

7.3.2 Synchronization

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor (see 图 7-2). Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width must be greater than 10 ns and less than half the discharge time of the oscillator. 图 7-3 shows how to synchronize two ICs, with one as primary and one as secondary. 图 7-4 shows the waveforms in a primary and secondary configuration.

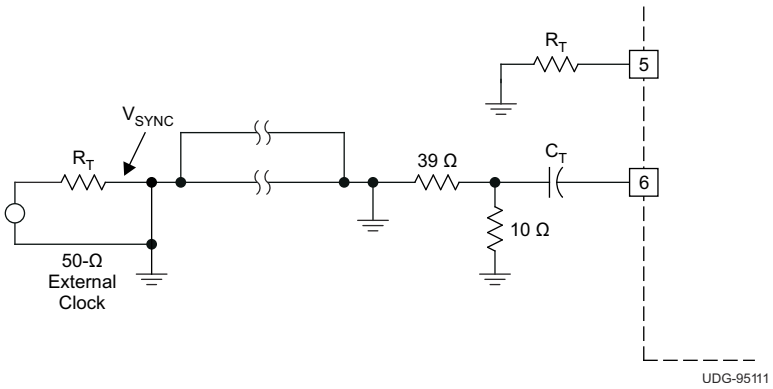


图 7-2. General Oscillator Synchronization

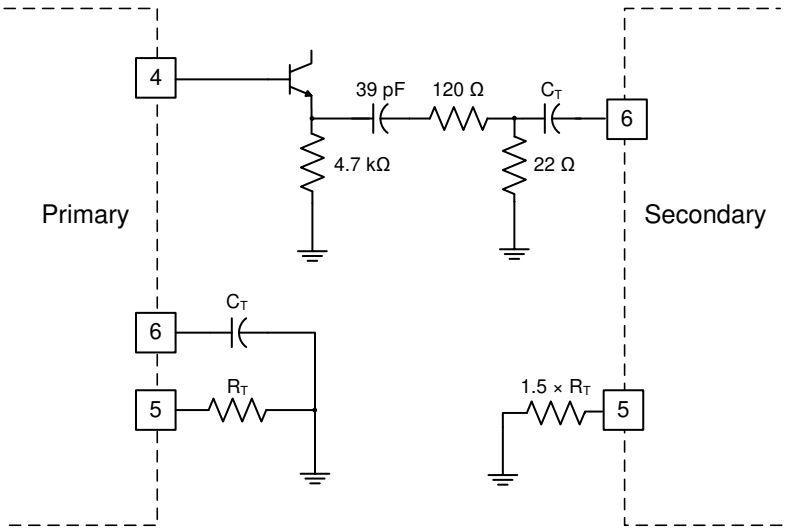


图 7-3. Two Unit Interface

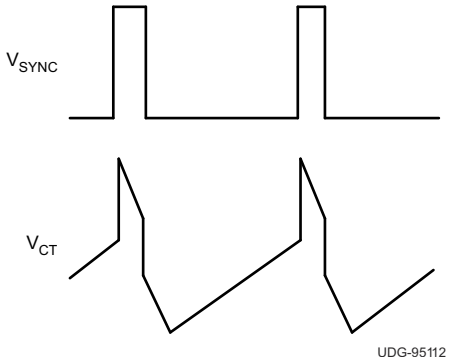


图 7-4. Operational Waveforms

7.3.3 High Current Outputs

Each totem pole output of the UC1825B-SP can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the analog circuitry of the device from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the 图 10-1 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive or capacitive load, typical of a MOSFET gate, as shown in 图 7-5. Schottky diodes must be used because a low forward voltage drop is required.

备注

Do **not** use standard silicon diodes.

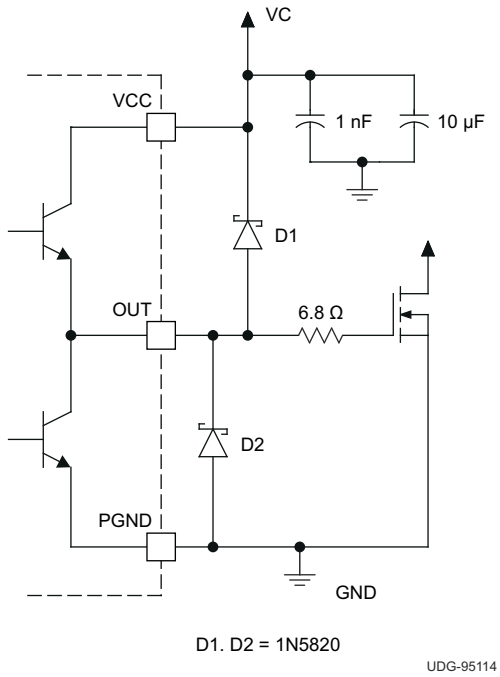


图 7-5. Power MOSFET Drive Circuit

7.3.4 Open Loop Test Circuit

This test fixture is useful for exercising many functions of this device family and measuring their specifications (see 图 7-6). As with any wideband circuit, careful grounding and bypass procedures must be followed. TI highly recommends using a ground plane.

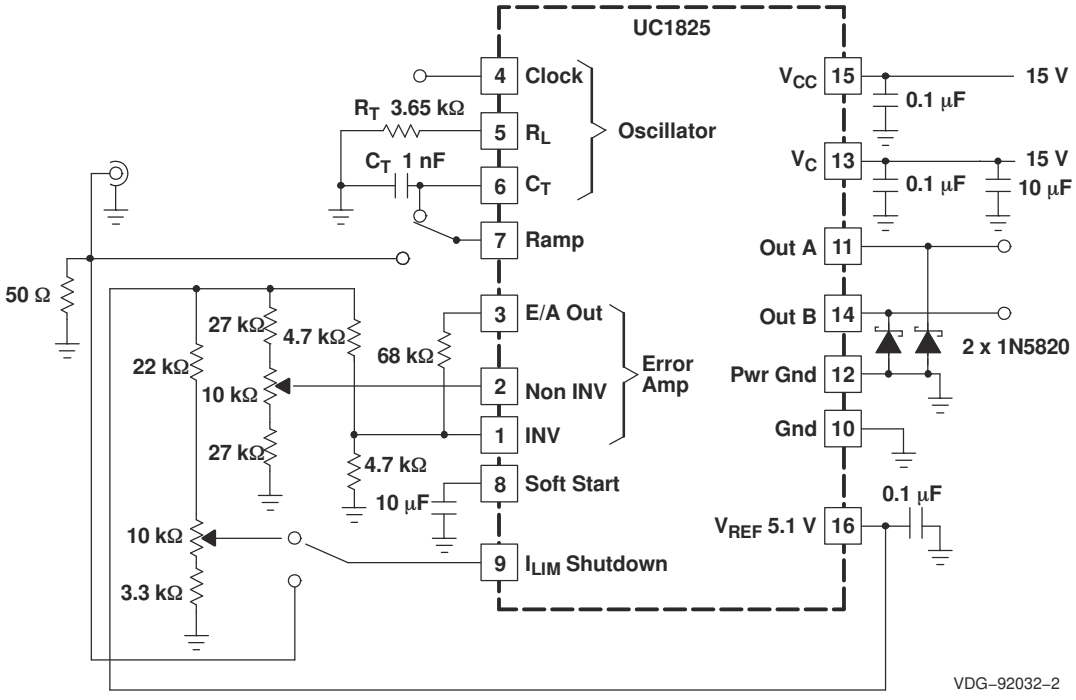


图 7-6. Open Loop Test Circuit Schematic

7.4 Device Functional Modes

The UC1825B-SP is compatible with voltage-mode or current-mode topologies. The UC1825B-SP uses fixed frequency, peak current mode control. An internal oscillator initiates the turn-on of the driver to high-side power switch. The external power switch current is sensed through an external resistor and is compared through internal comparator. The voltage generated at the COMP pin is stepped down through internal resistors. When the sensed current reaches the stepped down COMP voltage, the high-side power switch is turned off.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The oscillator of the UC1825B-SP is a saw tooth (see 图 8-1). The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT must be done first, based on desired maximum duty cycle (see 图 8-3). CT can then be chosen based on the desired frequency (RT) and D_{MAX} (see 图 8-2). 方程式 1 shows the design equations.

$$R_T = \frac{3\ V}{(10\ mA) \times (1 - D_{MAX})} \qquad C_T = \frac{(1.6 \times D_{MAX})}{(R_T \times f)} \tag{1}$$

Recommended values for R_T range from 1 kΩ to 100 kΩ. Control of D_{MAX} less than 70% is not recommended.

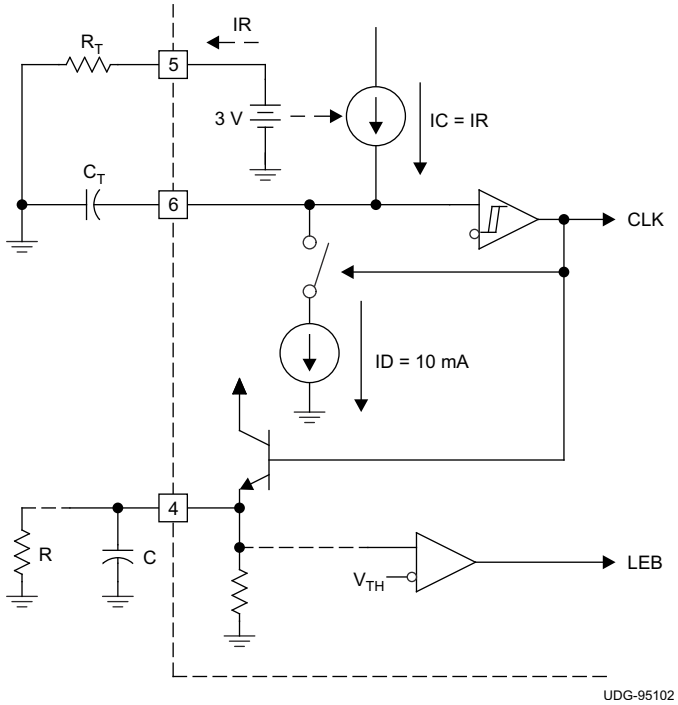


图 8-1. Oscillator

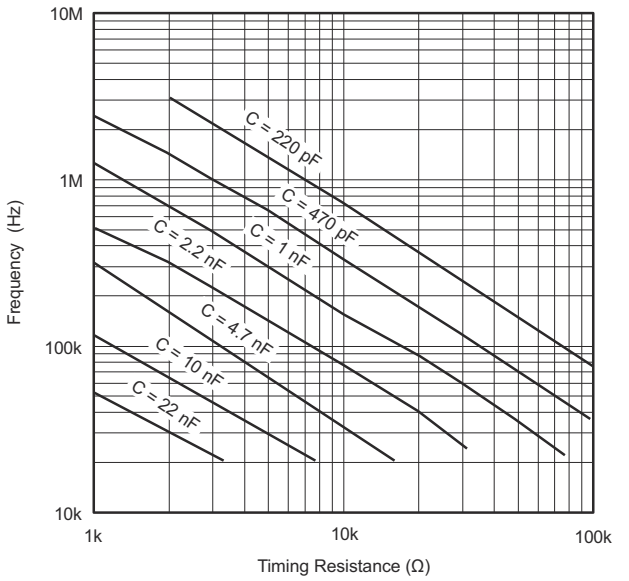


图 8-2. Oscillator Frequency vs Timing Resistance

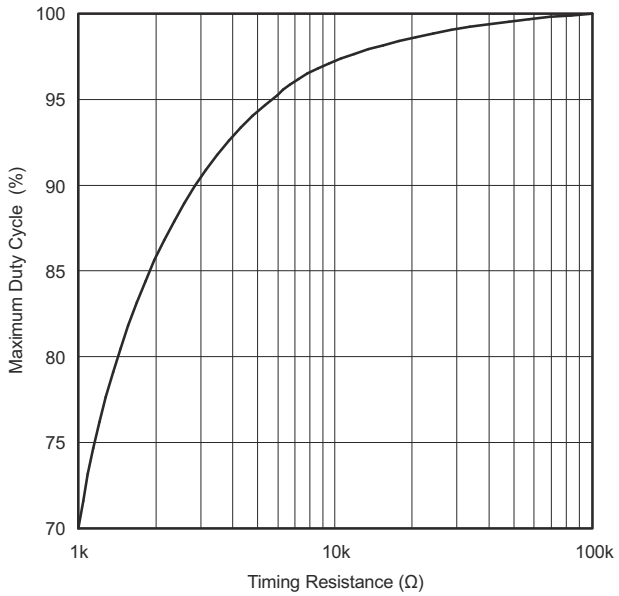


图 8-3. Maximum Duty Cycle vs Timing Resistance

8.2 Typical Application

The UC1825B-SP as a dual output controller that has integrated drivers for a push-pull topology and can be used for half bridge and full bridge applications by using external high side drivers. While the UC1825B-SP originally supported voltage mode topologies, the device with minimal external components can support current mode topologies as well. The RAMP pin is used for the input current sense and the ILIM pin is used as the current limit pin. External components are needed to ensure slope compensation is implemented.

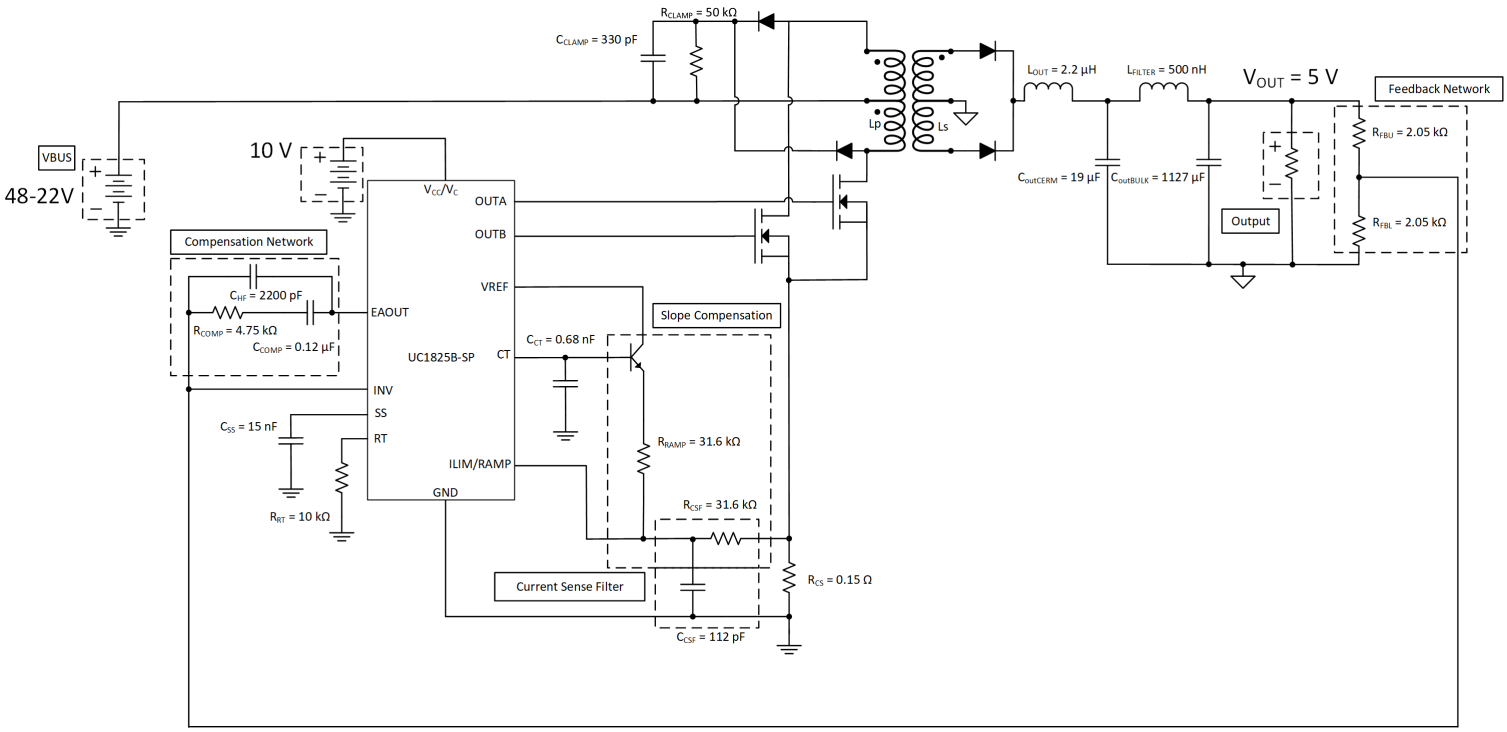


图 8-4. Typical Application

表 8-1. Design Parameters

PARAMETER	SPECIFICATIONS
Input Power Supply	22 to 48 VDC
Output Voltage	5 VDC
Output Current	0 to 10 A
Output Current Pre-load	0.5 mA
Operating Temperature	25°C
Switching Frequency of UC1825B-SP	215 kHz
Peak Input Current Limit	7 A
Bandwidth	~5 kHz
Phase Margin	~80°

8.2.1 System Design Theory

8.2.1.1 Switching Frequency

Choosing a switching frequency has a trade off between efficiency and bandwidth. Higher switching frequencies will have larger bandwidth, but a lower efficiency than lower switching frequencies. A switching frequency of 215 kHz was chosen as a trade off between bandwidth and efficiency. Using 方程式 2 for the UC1825B-SP, R_T and C_T were chosen to be 10 kΩ and 680 pF, respectively.

$$f_{osc} \approx \frac{1.46}{R_t \times C_t} \tag{2}$$

$$f_{osc} \approx \frac{1.46}{7.15\ \ k\Omega\ \ \times\ \ 680\ \ pF} = 215\ \ \ kHz \tag{3}$$

8.2.1.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. There is no minimum limit to the turns ratio of the transformer, just a maximum limit. The equation below will give the turns ratio as a function of duty cycle which if the maximum duty cycle of the converter is used will give you a maximum turns ratio. The UC1825B-SP design targeted a duty cycle of 30%. Since this design is for a dual output device the duty cycle must stay below 50%. If both outputs were running above 50% duty cycle they would have to overlap which is not possible for the topology. The equation of the turns ratio of the transformer is 方程式 4.

$$N_{psMAX} = \frac{2 \times V_{inMIN} \times D_{lim}}{(V_{out} + V_{Diode})} \tag{4}$$

$$N_{psMAX} = \frac{2 \times 22\ \ V \times 0.3}{(5\ \ V + 0.7\ \ V)} = 2.31 \tag{5}$$

Often the turns ratio will slightly change in design due to how the transformer is manufactured. For the UC1825B-SP design a turns ratio of 2.2 was used. Another turns ratio that is important is the turns ratio of the auxiliary winding. The auxiliary winding is found by figuring out what positive voltage is needed from the auxiliary winding. Selecting this voltage lets one pick the turns ratio from the secondary to the auxiliary winding, which in turn allows for the turns ratio from primary to auxiliary to be found. The equation for the turns ratio is 方程式 6.

$$N_{as} = \frac{N_{ps} \times V_{aux}}{V_{inMIN}} \tag{6}$$

$$N_{as} = \frac{2.2 \times 15\ \ V}{22\ \ V} = 1.5 \tag{7}$$

An auxiliary winding of 1.5 was used for the UC1825B-SP design. The primary inductance of the transformer is found from picking an appropriate magnetizing current. The magnetizing current of the transformer is the amount

of current drawn through the windings of the transformer when the output is open circuited. Decreasing the magnetizing current will increase the inductance of the transformer, perhaps to unreasonable values. Increasing the magnetizing current will cause efficiency to decrease. It is desirable to keep the magnetizing current low, thus 6% was picked for the design value. The equation for the auxiliary winding turns ratio is 方程式 8.

$$L_p = \frac{N_{ps} \times V_{inMAX} \times D_{MIN}}{f_{osc} \times \%_{mag} \times I_{out}} \tag{8}$$

$$L_p = \frac{2.2 \times 48 \times 0.13}{215\ \ kHz \times 0.06 \times 10} = 106\ \ \mu H \tag{9}$$

There are quite a few physical limitations when making transformers that will affect the inductance value. For the UC1825B-SP design a primary inductance of 120 µH was used. The output inductor was then picked based on the output inductor ripple current with 方程式 10.

$$L_{inductor} = \frac{\left(\frac{V_{inMAX}}{N_{ps}} - V_f - V_{out}\right) \times D_{MIN}}{f_{osc} \times I_{out} \times \%_{ripple}} \tag{10}$$

$$L_{inductor} = \frac{\left(\frac{48\ \ V}{2.2} - 0.7\ \ V - 5\ \ V\right) \times 0.13}{215\ \ kHz \times 10\ \ A \times 0.45} = 2.14\ \ \mu H \tag{11}$$

In the final design, a 2.2-µH inductor was used. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer, so equations are listed below. Note these equations are only true for continuous conduction mode. Peak currents are higher at the maximum input voltage while the RMS current is highest at the minimum input voltage. These are also idea values and don't take into account efficiency. Final designs needs to be optimized depending on the specific application requirements. Equations that show how to calculate these for this design are below:

$$I_{secMAX} = I_{out} + 0.5 \times \%_{ripple} \times I_{out} \tag{12}$$

$$I_{secMAX} = 10\ \ A\ \ +\ \ 0.5 \times 0.445 \times 10\ \ A\ \ =\ \ 12.23\ \ A \tag{13}$$

$$I_{priMAX} = \frac{I_{secMAX} + 0.5 \times \%_{mag} \times I_{out}}{N_{ps}} \tag{14}$$

$$I_{priMAX} = \frac{12.23\ \ A + 0.5 \times 0.06 \times 10\ \ A}{2.2} = 5.7\ \ A \tag{15}$$

$$I_{secMAX(VinMIN)} = I_{out} + \frac{D_{MAX} \times \left(\frac{V_{inMIN}}{N_{ps}} - \left(V_{out} + V_f\right)\right)}{2 \times f_{osc} \times L_{inductor}} \tag{16}$$

$$I_{secMAX(VinMIN)} = 10\ \ A + \frac{0.285 \times \left(\frac{22\ \ V}{2.2} - \left(5\ \ V\ \ +\ \ 0.7\ \ V\right)\right)}{2 \times 215\ \ kHz \times 2.2\ \ \mu H} = 11.3\ \ A \tag{17}$$

$$I_{priMAX(VinMIN)} = \frac{I_{secMAX(VinMIN)} + 0.5 \times \%_{mag} \times I_{out}}{N_{ps}} \tag{18}$$

$$I_{priMIN(VinMIN)} = \frac{11.3\ \ A\ \ + 0.5 \times 0.06 \times 10}{2.2} = 5.27\ \ A \tag{19}$$

$$I_{secMIN(VinMIN)} = I_{out} - \frac{D_{MAX} \times \left(\frac{V_{inMIN}}{N_{ps}} - \left(V_{out} + V_f\right)\right)}{2 \times f_{osc} \times L_{inductor}} \tag{20}$$

$$I_{secMIN(VinMIN)} = 10\ \ A - \frac{0.285 \times \left(\frac{22\ \ V}{2.2} - \left(5\ \ V\ \ +\ \ 0.7\ \ V\right)\right)}{2 \times 215\ \ kHz \times 2.2\ \ \mu H} = 8.7\ \ A \tag{21}$$

$$I_{priMIN(VinMIN)} = \frac{I_{secMIN(VinMIN)} - 0.5 \times \%_{mag} \times I_{out}}{N_{ps}} \quad (22)$$

$$I_{priMIN(VinMIN)} = \frac{8.7\ \ A\ \ - 0.5 \times 0.06 \times 10}{2.2} = 3.82\ \ A \quad (23)$$

$$t_{onMAX} = \frac{\left(V_{out} + V_f\right) \times N_{ps}}{2 \times f_{osc} \times V_{inMIN}} \quad (24)$$

$$t_{onMAX} = \frac{(5\ \ V\ \ + 0.7\ \ V) \times 2.2}{2 \times 215\ \ kHz \times 22\ \ V} = 1.33\ \ \mu s \quad (25)$$

$$m_{pri} = \frac{I_{priMAX(VinMIN)} - I_{priMIN(VinMIN)}}{t_{onMAX}} \quad (26)$$

$$m_{pri} = \frac{5.27 - 3.82}{1.33\ \ \mu s} = 1090226\ \ A/s \quad (27)$$

$$I_{priRMS} = \sqrt{D_{MIN} \times \left(\frac{\left(m_{pri} \times t_{onMAX}\right)^2}{3} + \frac{m_{pri}}{2} \times I_{priMIN(VinMIN)} \times t_{onMAX} + I_{priMIN(VinMIN)}{}^2 \right)} \quad (28)$$

$$I_{priRMS} = \sqrt{0.285 \times \left(\frac{(1090226\ \ A/s \times 1.33\ \ \mu s)^2}{3} + \frac{1090226\ \ A/s}{2} \times 3.82\ \ A \times 1.33\ \ \mu s + \left(3.82\ \ A\right)^2 \right)} = 2.27\ \ A \quad (29)$$

8.2.1.3 RCD and Diode Clamp

For the UC1825BEVM-CVAL a resistor and capacitor in combination with a diode was used to clamp the voltage of the switch node. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, one must first decide how much the node is allowed to overshoot. The equation for finding the voltage of the clamp is 方程式 30.

$$V_{clamp} = K_{clamp} \times N_{ps} \times \left(V_{out} + V_{Diode}\right) \quad (30)$$

Note that K_{clamp} is recommended to be 1.5 as this will allow for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the RCD clamp voltage is allowed to change over the switching cycle, can allow one to figuring out starting values for the resistor and capacitor using 方程式 31 and 方程式 32.

$$R_{clamp} = \frac{V_{clamp}{}^2}{\frac{1}{2} \times L_{leakage} \times I_{PriPeak}{}^2 \times \frac{V_{clamp}}{V_{clamp} - N_{ps} \times \left(V_{out} + V_{Diode}\right)} \times f_{osc}} \quad (31)$$

$$C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp} \times V_{clamp} \times R_{clamp} \times f_{osc}} \quad (32)$$

A starting value of 10% is generally used for ΔV_{clamp}.

8.2.1.4 Output Diode

The voltage stress by the converter on the diode can be found with 方程式 33.

$$V_{DiodeStress} = V_{out} + \frac{V_{inMAX}}{N_{ps}} \quad (33)$$

$$V_{DiodeStress} = 5\ \ V + \frac{48\ \ V}{2.2} = 26.8\ \ V \quad (34)$$

Note that any diode picked should have a voltage rating of well above this value as it does not include parasitic spikes in the equation. The UC1825-SP diode was picked to have a voltage rating of 60 V.

8.2.1.5 Main Switching MOSFETs

Each switch applies the input voltage across the transformer and the voltage is then divided down by the turns ratio and applied to the secondary side. Since the magnitude of the voltage across the windings is the input voltage, when the switch is off the primary switching MOSFETs will see twice the input voltage as the voltage stress plus some amount of ringing. This means the MOSFETs chosen for a push-pull topology should have a voltage rating of about 2.5 to 3 times higher than the input voltage.

8.2.1.6 Output Filter and Capacitance

For most designs, a ripple voltage is picked and the output capacitance is figured out from that value. The output capacitance value needs to be able to withstand a full output current step as well as keep the voltage ripple of the output low. The UC1825B-SP design started similar to that using the equations for voltage ripple and load step with 方程式 35 and 方程式 37.

$$C_{out} > \frac{I_{out} \times 2 \times D_{MAX}}{V_{Ripple} \times f_{osc}} \tag{35}$$

$$C_{out} > \frac{10 \;\; A \times 2 \times 0.3}{50 \;\; mV \times 200 \;\; kHz} = 600 \;\; \mu F \tag{36}$$

$$C_{out} > \frac{\Delta I_{step}}{2\pi \times \Delta V_{out} \times f_{co}} \tag{37}$$

$$C_{out} > \frac{10 \;\; A}{2\pi \times 0.3 \;\; V \times 5 \;\; kHz} = 1060 \;\; \mu \; F \tag{38}$$

A value of around 1145 µF was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. This was done in order to keep output voltage ripple as low as possible. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics will help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple will be attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. The equations below allow for finding the amount of attenuation that will come from a specific output filter inductance. An inductance of 500 nH was chosen to attenuate the output voltage ripple. The value was chosen to put the resonant frequency pole well before the switching frequency of the design as well as the zero from the ESR of the bulk capacitors to provide more attenuation.

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{L_{Filter} \times C_{oBulk}}} \tag{39}$$

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{0.5 \;\; nH \times 1127 \;\; \mu F}} = 6.7 \;\; kHz \tag{40}$$

$$F_{Zero} = \frac{1}{2\pi \times C_{oBulk} \times ESR_{oBulk}} \tag{41}$$

$$F_{Zero} = \frac{1}{2\pi \times 1127 \;\; \mu F \times 0.009 \;\; \Omega} = 15.69 \;\; kHz \tag{42}$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{f_{osc}}{f_{resonant}}\right) - 20 \times \log_{10}\left(\frac{f_{osc}}{f_{zero}}\right) \tag{43}$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{200 \;\; kHz}{6.7 \;\; kHz}\right) - 20 \times \log_{10}\left(\frac{200 \;\; kHz}{15.69 \;\; kHz}\right) \;\; = 36.88 \;\; dB \tag{44}$$

Sometimes the output filter can cause peaking at high frequencies. This can be damped by adding a resistor in parallel with the inductor which will decrease efficiency. For the UC1825B-SP design 0.5 Ω was used as a very conservative value. The resistance needed to damp the peaking can be calculated using the following equations:

$$\omega_o = \sqrt{\frac{2(C_{oCerm} + C_{oBulk})}{L_{Filter} \times C_{oCerm} \times C_{oBulk}}} \tag{45}$$

$$\omega_o = \sqrt{\frac{2(19\ \ \mu F + 1127\ \ \mu F)}{500\ \ nH \times 19\ \ \mu F \times 1127\ \ \mu F}} = 463\ \ kHz \tag{46}$$

$$R_{Filter} = \frac{R_o \times L_{Filter} \times \left(C_{oCerm} + C_{oBulk}\right) - \frac{L_{Filter}}{\omega_o}}{\frac{R_o \times (C_{oCerm} + C_{oBulk})}{\omega_o} - L_{Filter} \times C_{oCerm}} \tag{47}$$

$$R_{Filter} = \frac{0.5 \times 500\ \ nH \times \left(19\ \ \mu F + 1127\ \ \mu F\right) - \frac{500\ \ nH}{463\ \ kHz}}{\frac{0.5 \times (19\ \ \mu F + 1127\ \ \mu F)}{463\ \ kHz} - 500\ \ nH \times 19\ \ \mu F} = 0.232\ \ \Omega \tag{48}$$

8.2.1.7 Compensation

Type IIB compensation was picked for the topology, adding a pole and a zero to the frequency response. The location of where the pole and zero should be placed will depend on the desired crossover frequency and the ESR zero of the output capacitors. The zero in compensation should be placed at least a decade before the crossover frequency for the maximum phase boost. Note that compensation values were picked with a crossover frequency of 5 kHz in mind for this design. The pole from the compensation should be placed at the zero created by the ESR of the output capacitor.

$$f_{zESR} = \frac{1}{2\pi \times C_{out} \times ESR} = \frac{1}{2\pi \times 1146\ \ \mu F \times 0.009\ \ \Omega} = 15.43\ \ kHz \tag{49}$$

$$f_{pCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} = \frac{1}{2\pi \times 4.75\ \ k\Omega \times 2200\ \ pF} = 15.23\ \ kHz \tag{50}$$

$$f_{zCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{1}{2\pi \times 4.75\ \ k\Omega \times 0.12\ \ \mu F} = 279\ \ Hz \tag{51}$$

The zero from compensation was placed well before the 500-Hz mark which is appropriate. The pole from compensation was optimized while the circuit was tested and thus it was found that placing the pole a little bit earlier smoothed out the frequency response.

8.2.1.8 Sense Resistor

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is over the current limit set. The voltage threshold of the CS pin is around 1 V and the shutdown current should be above the max current you expect. The max current limit will depend on the specific design. The equation used to find the max current limit is 方程式 52.

$$R_{cs} = \frac{V_{CS\ Threshold}}{I_{limit}} \tag{52}$$

$$R_{CS} = \frac{1\ \ V}{6.66\ \ A} = 0.15\ \ \Omega \tag{53}$$

8.3 Application Curves

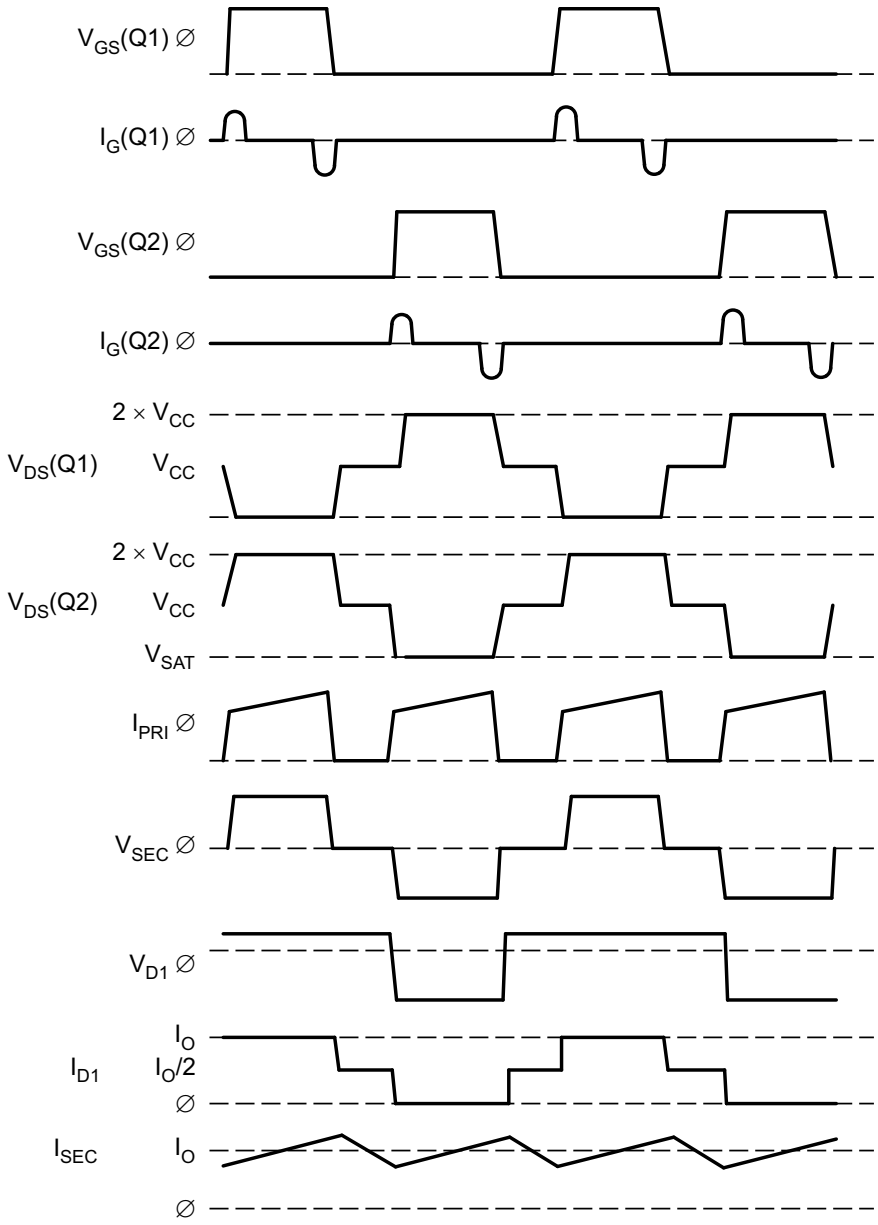


图 8-5. Basic Push-Pull Waveforms

图 8-6. Voltage Stress Across Main Switching MOSFETS Q1 and Q2

The test in 图 8-6 was done with 48-V input and a 10-A output load.

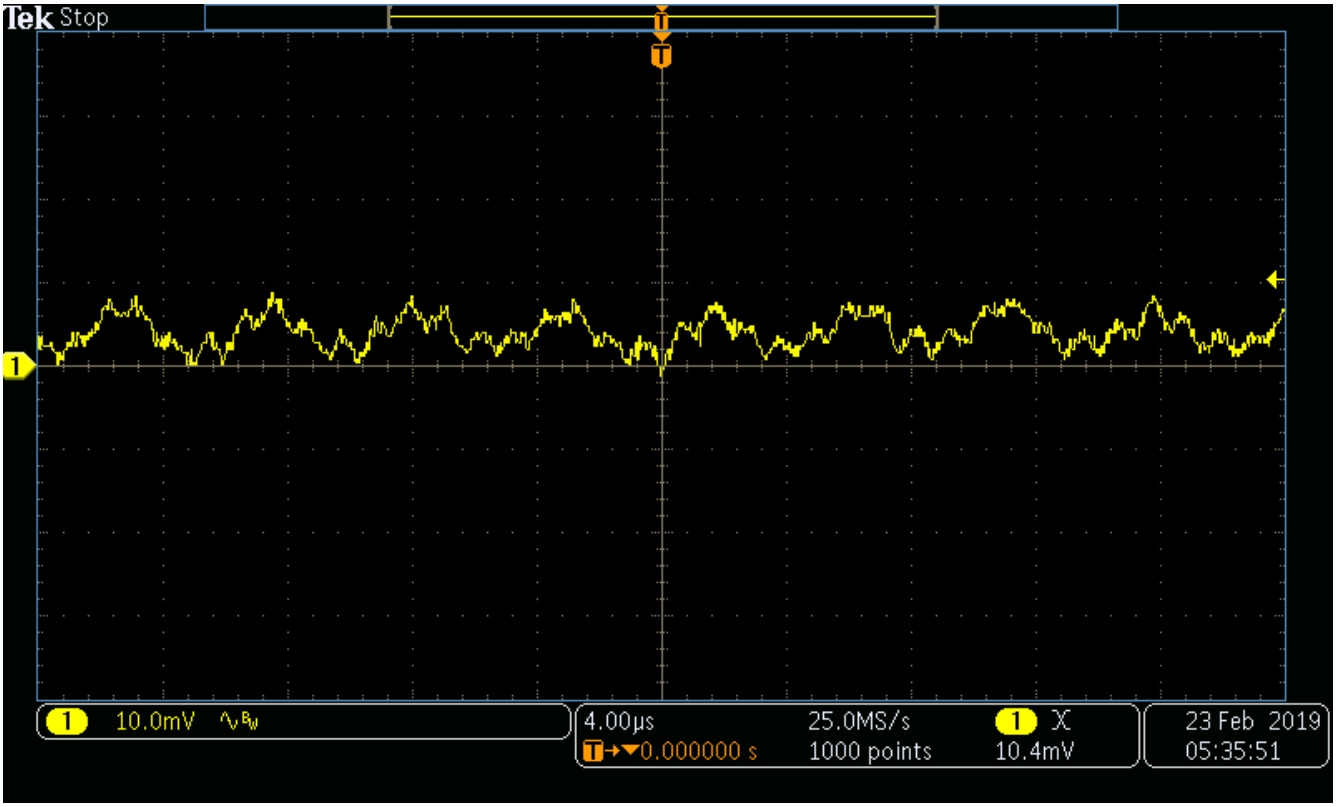


图 8-7. Output Voltage Ripple With 48 V_{IN}

Output voltage ripple test in 图 8-7 was done with 48-V input and 10-A output current.

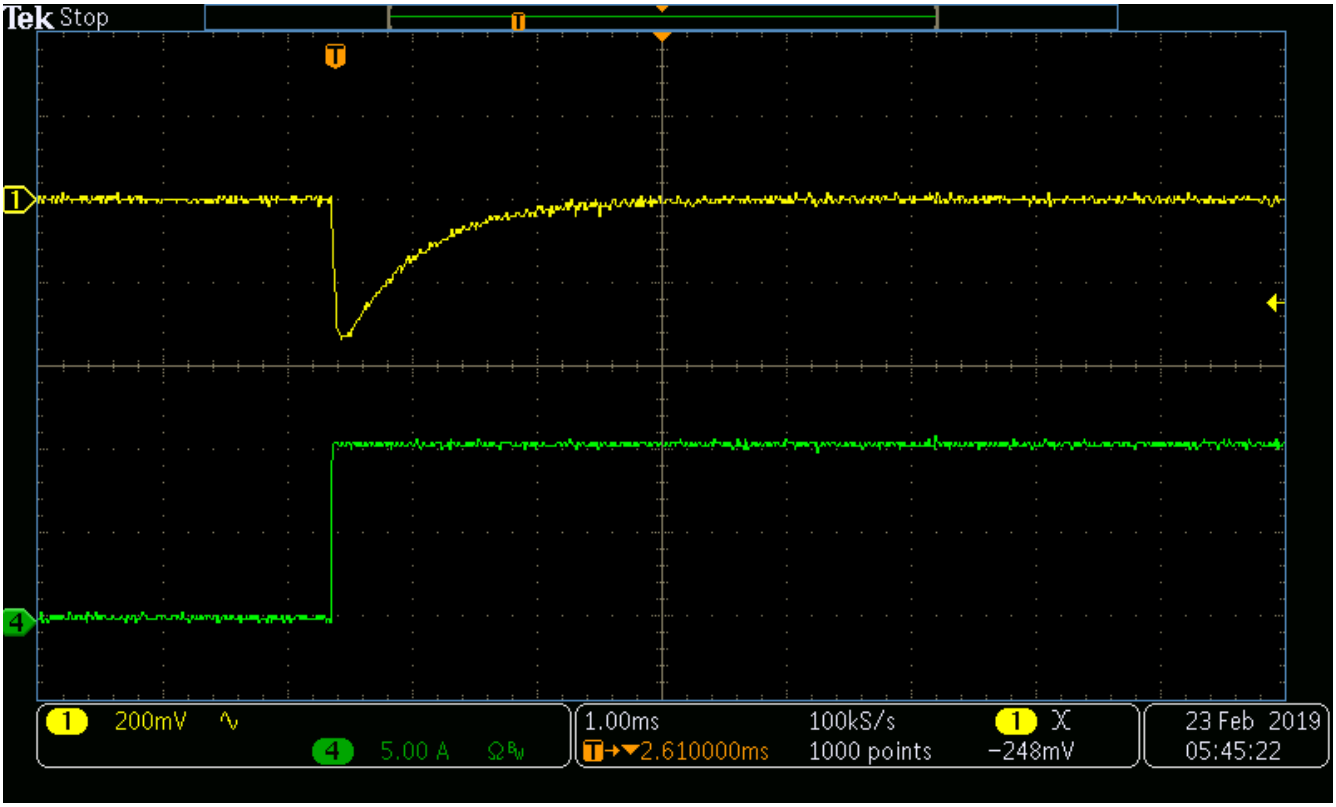


图 8-8. Full Output Voltage Transient With 48 V_{IN}

Full step up transient in 图 8-8 was done with 48-V input and output current was stepped from 0 A to 10 A.

9 Power Supply Recommendations

The UC182B-SP is designed to operate from an input voltage supply range between 10 V and 30 V. This input supply should be well regulated. If the input supply is located more than few inches from the UC1825B-SP converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 100 μF is a typical choice; however, this may vary depending upon the output power being delivered.

The UC1825B-SP controller can be used to convert power efficiently using any of several standard topologies such as push-pull, forward, half-bridge, or full bridge. Design tradeoffs of cost, size, and performance narrow the field to the one that is most appropriate. For a typical application, such as in 节 8.2, push-pull converter topology is highlighted.

10 Layout

10.1 Layout Guidelines

Always use a low EMI inductor with a ferrite-type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

10.1.1 Feedback Traces

Run the feedback trace as far from the inductor and noisy power traces as possible. The feedback trace should be as direct as possible and somewhat thick, which sometimes involves a trade-off, but keeping the feedback trace away from inductor EMI and other noise sources is more critical. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

10.1.2 Input/Output Capacitors

When using a low-value ceramic input filter capacitor, it must be located as close as possible to the VIN pin of the IC. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, it must also be positioned as close as possible to the IC. Using surface-mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

10.1.3 Compensation Components

External compensation components for stability must also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. Locate the surface-mount components away from the inductor.

10.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode must be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) must be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multilayer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback, compensation, and components are) for improved performance. On multilayer boards, the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per
200 mA of current if the trace must conduct a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one state when the switch is

off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

10.1.5 Ground Planes

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC must be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET must connect to power ground as must the return connection for input power to the system and the bulk input capacitor. The output must be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF must be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. TI recommends low ESR/ESL ceramic 1-mF capacitors for both VCC and VREF. All analog circuitry must likewise be bypassed to the signal ground plane. See 图 10-1.

10.2 Layout Example

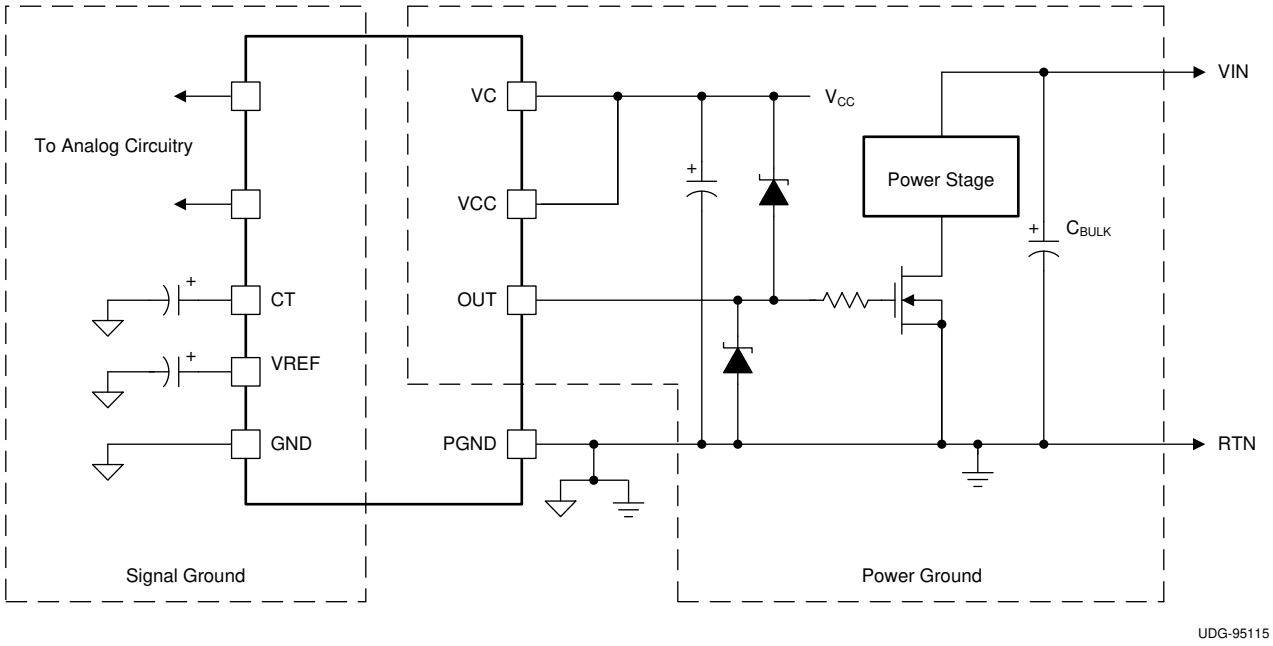


图 10-1. Ground Planes Diagram

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Unitrode Application Note U-93*, SLUA075
- *Unitrode Application Note U-97*, SLUA101
- *Unitrode Application Note U-110*, SLUA053

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R8768106V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R8768106VYC	ACTIVE	CFP	HKT	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R8768106VYC UC1825BHKT-SP	Samples
UC1825BHKT/EM	ACTIVE	CFP	HKT	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	UC1825BHKT/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

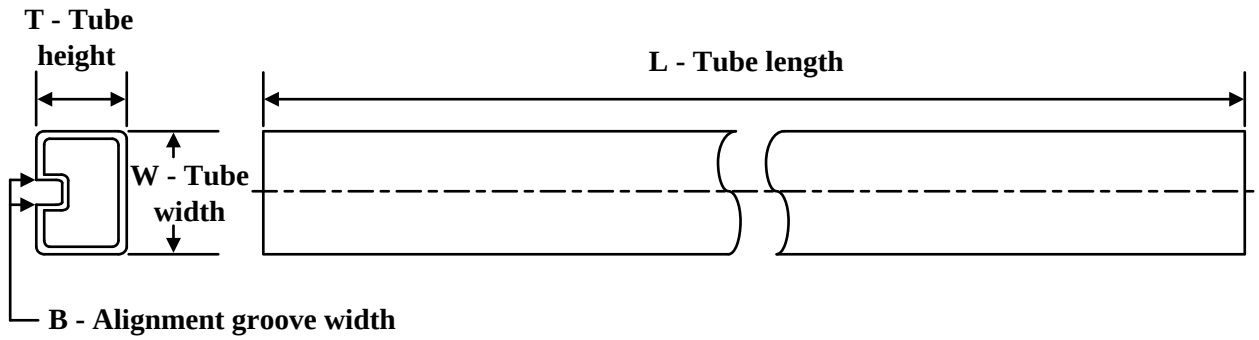
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

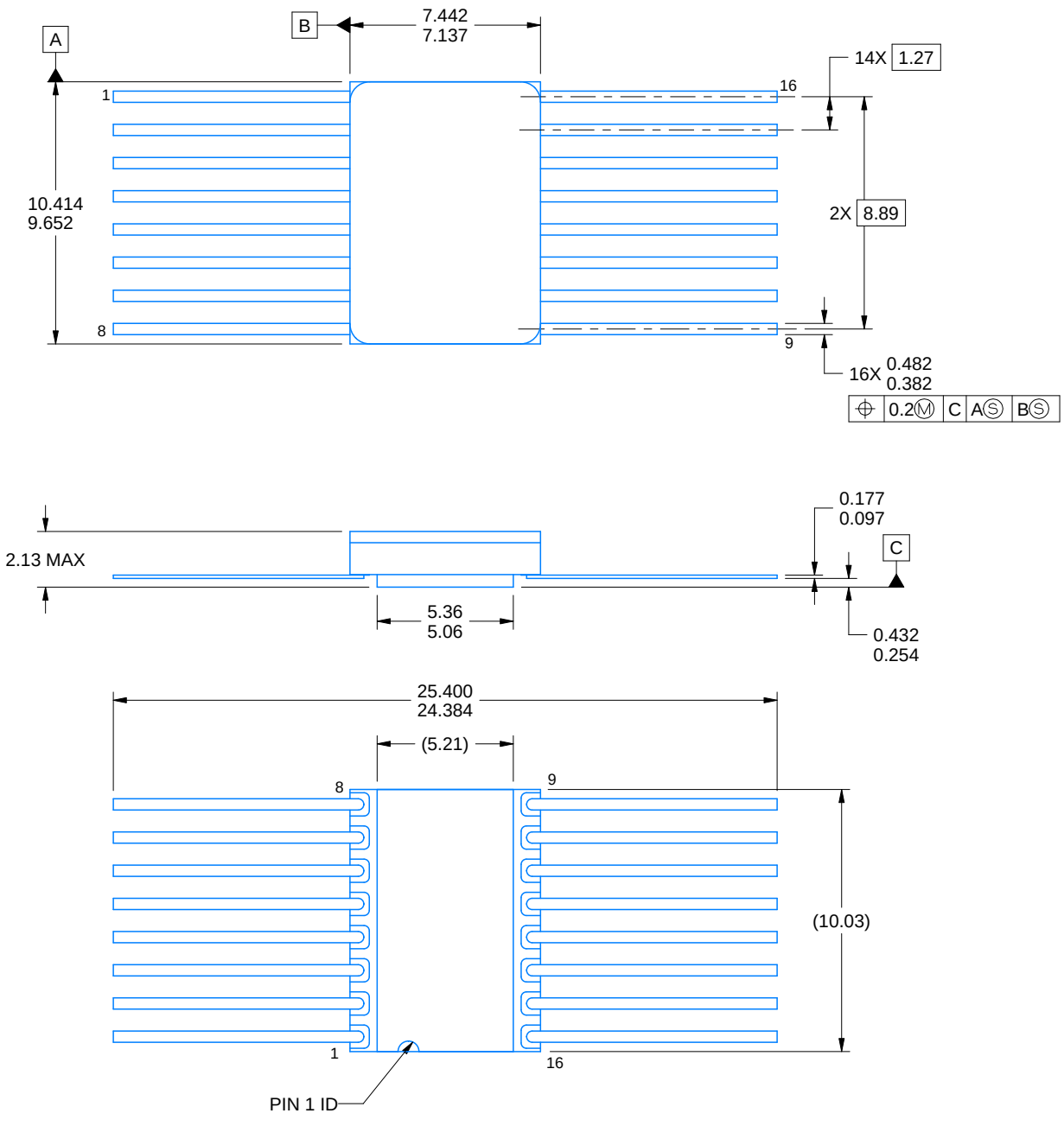
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R8768106VYC	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA
UC1825BHKT/EM	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKT0016A

CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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