UCC5880-Q1 具有高级保护功能、适用于汽车应用的隔离式 20A 可调栅极驱动 IGBT/SiC MOSFET 栅极驱动器

1 特性

- 具有实时可变驱动强度的双路输出驱动器
  - ±15A 和 ±5A 驱动电流输出
  - 用于在没有 SPI 时进行驱动强度调整的数字输入引脚 (GD*)
  - 3 电阻设置 R1、R2 或 R1||R2
  - 用于米勒钳位晶体管的集成式 4A 有源米勒钳位或可选的外部驱动器
- 支持初级侧和次级侧主动短路 (ASC)
- 内部和外部电源欠压和过压保护
- 驱动器内核温度检测和过热保护
- 短路保护：
  - 针对 DESAT 事件具有 110ns 响应时间
  - DESAT 保护 – 可承受高达 14V 的电压
  - 基于分流电阻器的短路 (SC) 和过流 (OC) 保护
  - 可配置保护阈值和消隐时间
  - 可编程软关断 (STO) 和两级软关断 (2STO) 电流
- 集成 10 位 ADC
  - 能够测量电源开关温度、直流链路电压、驱动器内核温度、DESAT 引脚电压、VCC2 电压
  - 可编程数字比较器
- 高级 VCE/VDS 钳位电路
- 符合功能安全标准
  - 专为功能安全应用开发
  - 有助于使 ISO 26262 系统设计符合 ASIL D 要求的文档
- 集成型诊断：
  - 针对保护比较器的内置自检 (BIST)
  - 用于功率器件运行状况监测的栅极阈值电压测量
  - INP 至晶体管栅极路径完整性
  - 内部时钟监测
  - 故障警报和警告输出 (nFLT*)
  - ISO 通信数据完整性检查
- 可通过 SPI 对器件进行重新配置、验证、监控和诊断
- 150V/ns CMTI
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C2b

2 应用

- 电动汽车和混合动力汽车牵引逆变器
- 电动汽车和混合动力汽车电源模块

3 说明

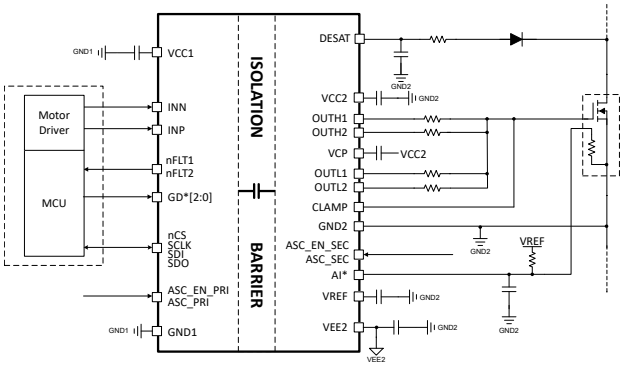
UCC5880-Q1 器件是一款高度可配置的隔离式栅极驱动器，具有可调驱动强度，旨在电动汽车/混合动力汽车应用中用于驱动高功率 SiC MOSFET 和 IGBT。该器件提供功率晶体管保护功能，例如基于分流电阻的过流保护、过热保护（PTC、NTC 或二极管）以及 DESAT 检测，包括在这些故障期间可选择的软关断或两级软关断。集成的 10 位 ADC 可用于监控多达 2 个模拟输入、VCC2、DESAT 以及栅极驱动器温度，从而增强系统管理。集成的诊断和检测功能可简化符合 ASIL 标准的系统的设计。这些功能的参数和阈值可使用 SPI 进行配置，因此该器件几乎可与任何 SiC MOSFET 或 IGBT 一同使用。

器件信息

器件型号	封装(1)	封装尺寸(2)	封装尺寸（标称值）
UCC5880-Q1	DFC（SSOP，32）	10.3mm × 10.3mm	10.5mm x 7.5mm

(1) 有关所有可用封装，请参阅“机械、封装和可订购信息”部分。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图

Table of Contents

4 Pin Configuration and Functions

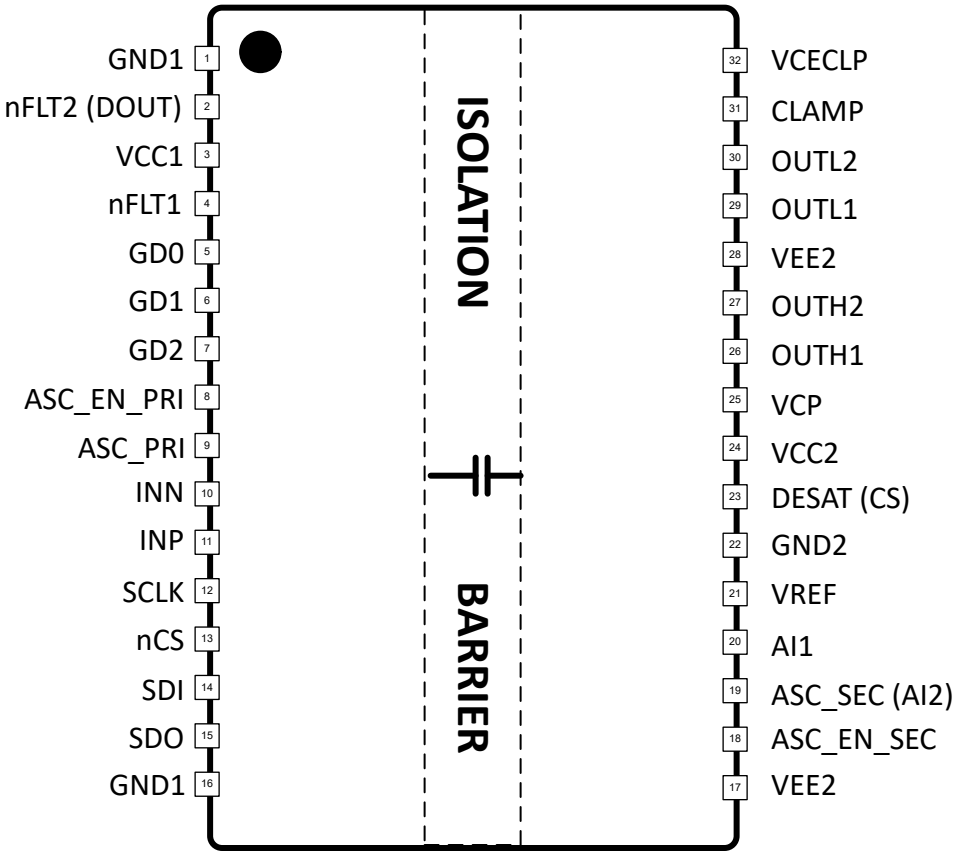


图 4-1. 32-Pin DFC SSOP Package Top View

表 4-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GND1	1, 16	P	Primary Side Ground. Connect all GND1 pins together and to the PCB ground plane on the primary side. Prioritize pin 1 for supply and input filter decoupling.
nFLT2 (DOUT)	2	O	Fault Indicator Output 2. nFLT2 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT2 low when the fault occurs. nFLT2 is high when all faults are either non-existent or masked. It is recommended to add an external pull up resistor to VCC1 if faster rise time is needed. Additionally, nFLT2 may be configured as DOUT (push/pull) to provide the host controller a PWM signal with a duty cycle relative to the ADC input of interest.
VCC1	3	P	Primary Side Power Supply. Connect a 3V to 5.5V power supply to VCC1. Bypass VCC1 to GND1 with ceramic bulk capacitance as close to the VCC1 pin as possible.
nFLT1	4	O	Fault Indicator Output 1. nFLT1 is used to interrupt the host when a fault occurs. Faults that are unmasked pull nFLT1 low when the fault occurs. nFLT1 is high when all faults are either non-existent or masked. It is recommended to add an external pull up resistor to VCC1 if faster rise time is needed.
GD0	5	I	OUTL1/2 and OUTH1/2 Selector Inputs. GD* select combinations of OUT*1 and OUT*2 with user-selectable resistors. Drive all GD* high to force the gate of the power transistor low and reset all faults. See Adjustable Gate Drive Outputs (OUTL* OUTH*) for more details. Tie to GND1 if not used.
GD1	6	I	
GD2	7	I	
ASC_EN_PRI	8	I	Primary-side Active Short Circuit Enable Input. ASC_EN_PRI enables the ASC function and forces the output to follow the ASC_PRI pin input state. When ASC_EN_PRI is low, the OUT* pins follow the INP and INN pin logical truth table. Tie to GND1 if not used.
ASC_PRI	9	I	Primary-side Active Short Circuit Polarity Input. The OUT* pins follow the logic level at ASC_PRI when the ASC_EN_PRI input is driven high. See the ASC section for more details. Tie to GND1 if not used.
INN	10	I	Negative PWM Input. INN is connected to the INP from the opposite arm of the half-bridge. If INP and INN overlap, the Shoot Through Protection (STP) engages and forces output low. Tie to GND1 if not used.
INP	11	I	Positive PWM Input. INP drives the state of the driver output. With the driver enabled, when INP is high, OUTH* is pulled high. When INP is low, OUTL* is pulled low. CMOS input logic level determined by the VCC1 voltage. INP is connected to the INN of the opposite arm of the half-bridge. If INP and INN overlap, STP engages and forces output low.
SCLK	12	I	SPI Clock. SCLK is the clock signal for the main SPI interface. The SPI interface operates with clock rates up to 4MHz.
nCS	13	I	SPI Chip Selection Input. nCS is an active low input used to activate the SPI peripheral device. Drive nCS low during SPI communication. When nCS is high, SDO is set to disabled (high-impedance) and commands on SDI are ignored. Tie to VCC1 if not used.
SDI	14	I	SPI Data Input. SDI is the data input for the main SPI interface. Data is sampled on the falling edge of CLK, SDI must be in a stable condition to ensure proper communication.
SDO	15	O	SPI Data Output. SDO is the data output for the main SPI interface. Data is clocked out on the falling edge of CLK, SDO is changed with a rising edge of CLK.
VEE2	17, 28	P	Secondary Negative Power Supply. Connect all VEE2 supply inputs together. Connect a -12V to 0V power supply to VEE2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VEE2 to GND2 with at least 1uF of low-impedance ceramic capacitors as close to pin 28 as possible, to encourage gate current flow through pin 28.
ASC_EN_SEC	18	I	Secondary-side Active Short Circuit Enable Input. ASC_EN_SEC enables the ASC function, overriding the INP command and forcing the output of the driver to the defined safe state, set by CONTROL2[ASC_LEV_SEL] register. When ASC_EN_SEC is low, the output is controlled by primary side pins. Tie to GND2 if not used.
ASC_SEC	19	I	ASC_SEC (AI2) defaults to Active Short Circuit Polarity Input. When programmed as ASC_SEC, the OUT* pins follow the logic level at ASC_SEC when the ASC_EN_SEC input is driven high.
AI2		I	ASC_SEC (AI2) can be programmed as an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.

表 4-1. Pin Functions（续）

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AI1	20	I	Analog Input 1. AI1 is an ADC input that digitizes analog voltages up to 4.0V. Additionally, a programmable “digital comparator” is available to signal faults when the voltage is above/ below (selectable) the programmed threshold. This is useful for monitoring the DC-LINK voltage or phase voltage during the switching cycle. Tie to GND2 if not used.
VREF	21	P	Internal ADC Voltage Regulator Output. VREF provides an external 5.0V reference voltage, which is internally scaled down to 4.0V for the ADC. Bypass VREF to GND2 with at least 1uF of ceramic capacitance.
GND2	22	P	Gate Drive Supply Reference. Connect GND2 to the power FET source/ IGBT emitter. ASC_EN_SEC, ASC_SEC (AI2), AI1, VREF, and DESAT are referenced to GND2.
DESAT	23	I	Current Sense Input/ Desaturation based Short Circuit Detection Input. DESAT (CS) is configurable to sense over-current conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For DESAT applications, bypass DESAT to GND2 with a ceramic capacitor and, in parallel, connect a Schottky diode with the cathode connected to the DESAT pin, and the anode connected to GND2. See the applications section for details on calculating the component values. Additionally, connect the DESAT pin to a resistor to the anode of a diode to the collector of the power FET. The DESAT pin detects a fault when the VDS/VCE voltage of the power FET exceeds the SPI programmable threshold while the power FET is on. Tie to GND2 if not used.
CS		I	Current Sense Positive Input/ Desaturation based Short Circuit Detection Input. CS (DESAT) is configurable to sense over-current and short-circuit conditions in resistor sense applications, or DESAT over-current in VCE/VDS sensing applications. For sense resistor based applications, connect DESAT (CS) pin to the positive side of the sense element through an RC. The current limit threshold is programmable via SPI. Tie to GND2 if not used.
VCC2	24	P	Secondary Positive Power Supply. Connect a 15V to 30V power supply to VCC2. The total voltage rail from VCC2 to VEE2 must not exceed 30V. Bypass VCC2 to GND2 and VCC2 to VEE2 with bulk ceramic capacitance as close to the VCC2 pin as possible. Additional capacitance may be needed depending on the gate charge of the power device.
VCP	25	P	High-side Drive Supply. VCP supplies power for the OUTH* drive. Bypass VCP to VCC2 with a ceramic capacitor between 10nF and 100nF, as close to the VCP pin as possible.
OUTH1	26	O	Gate driver source pins (OUTH1 = $15A_{PK}$, OUTH2 = $5A_{PK}$). When the driver is active and commanded high, OUTH* pins are used to source current to the gate of the power FET to drive the output high. Connect OUTH* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTH1 and OUTH2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTH1 only, OUTH2 only, and OUTH1 + OUTH2).
OUTH2	27	O	
OUTL1	29	O	Gate driver sink pins (OUTL1 = $15A_{PK}$, OUTL2 = $5A_{PK}$). When the driver is active and commanded low, OUTL* pins are used to sink current from the gate of the power FET to drive the gate low. Connect OUTL* pins to the gate of the power FET through individual gate resistors. The value of the gate resistor is chosen based on the slew rate required for the application. Different slew rates are programmed by using different resistor values for OUTL1 and OUTL2. The two outputs are enabled “on the fly” using the GD* inputs to set 3 different slew rates (OUTL1 only, OUTL2 only, and OUTL1 + OUTL2).
OUTL2	30	O	
CLAMP	31	O	Miller Clamp pin. The CLAMP pin is used to hold the gate of the power FET strongly to VEE2 while the power FET is "off". CLAMP is configurable as an internal Miller clamp, or to drive an external clamping circuit. When using the internal clamping function, connect CLAMP directly the power FET gate. When configured as an external clamp, connect CLAMP to the gate of an external pulldown MOSFET. Disable and tie to VEE2 if not used.
VCECLP	32	I	VCE Clamp Input. VCECLP clamps to a diode above the VCC2 rail and indicates a fault when the voltage at VCECLP is above the VCECLPth voltage. Bypass VCECLP to VEE2 with ceramic capacitor and, in parallel, connect a resistor. See the applications section for details on calculating the component values. Additionally, connect VCECLP to the anode of a zener diode to the collector/drain of the power FET. Tie to VEE2 if not used.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Power Supply Recommendations

5.1 VCC1

VCC1 supports an input range of 3V to 5.5V in order to support both 3.3V and 5V controller signaling. VCC1 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC1 are recorded in FAULT2[UVLO1_FAULT] and FAULT2[OVLO_FAULT1], respectively.

5.2 VCC2

VCC2 operates within an input range of 12V and 30V, allowing for use in IGBT and SiC applications. VCC2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VCC2 are recorded in FAULT2[UVLO2_FAULT] and FAULT2[OVLO2_FAULT], respectively.

5.3 VEE2

VEE2 operates with an input range of -12V to 0V, allowing a negative gate bias on the power FET during turn-off in both IGBT and SiC applications. This prevents the power FET from unintentionally turning on due to current inducted from the Miller effect. For operation with a unipolar supply, connect VEE2 to GND2. VEE2 is monitored with both an undervoltage and overvoltage comparator circuit to ensure valid operation. UV and OV conditions of VEE2 are recorded in FAULT2[UVLO3_FAULT] andFAULT2[OVLO3_FAULT], respectively.

6 Layout

6.1 Layout Guidelines

Layout best practices must be followed to achieve robust performance from UCC5880-Q1. Failure to follow best practices may lead to low noise immunity. Reach out to TI engineers for feedback during schematic phase, component placement phase, and trace/plane layout phase of board design.

6.1.1 Component Placement

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCC1 and GND1 pins and between the VCC2, VEE2 and GND2 pins to support high peak currents when turning the external power transistor on and off.
- Place the VCP and VREF caps as close to the device as possible.

6.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This decreases the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Ensure a small loop area/inductance between VCP and VCC2.
- Analog signals measured with the integrated ADC on AI1 and AI2 pins must be effectively isolated from high gate switching currents in GND2 net. It is recommended to create Kelvin connections for these measurements to reduce impact of ground bounce caused by high di/dt in the gate drive loop.

6.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC5880-Q1’ s isolation performance.
- For half-bridge, or high-side/low-side configurations, where the high-side and low-side drivers could operate with a DC-link voltage up to 1000 VDC, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.
- Conformal coating is commonly used in systems to limit pollution degree and enable shorter creepage/ clearance distances.

6.1.4 Thermal Considerations

- The power dissipated in UCC5880-Q1 is directly proportional to the VCC1, VCC2, and VEE2 voltages, capacitive loading, and switching frequency. Proper PCB layout helps dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VCC2 and VEE2 planes is recommended, with priority on maximizing the connection to VEE2.
- If there are multiple layers in the system, it is also recommended to connect the VCC2 and VEE2 to their respective internal planes using multiple vias of adequate size. However, it is still critical to ensure that there are not any traces/planes from different high voltage planes overlapping.

6.2 Layout Example

Please refer to UCC5880EVM-057 Evaluation Module (EVM) design for layout example.

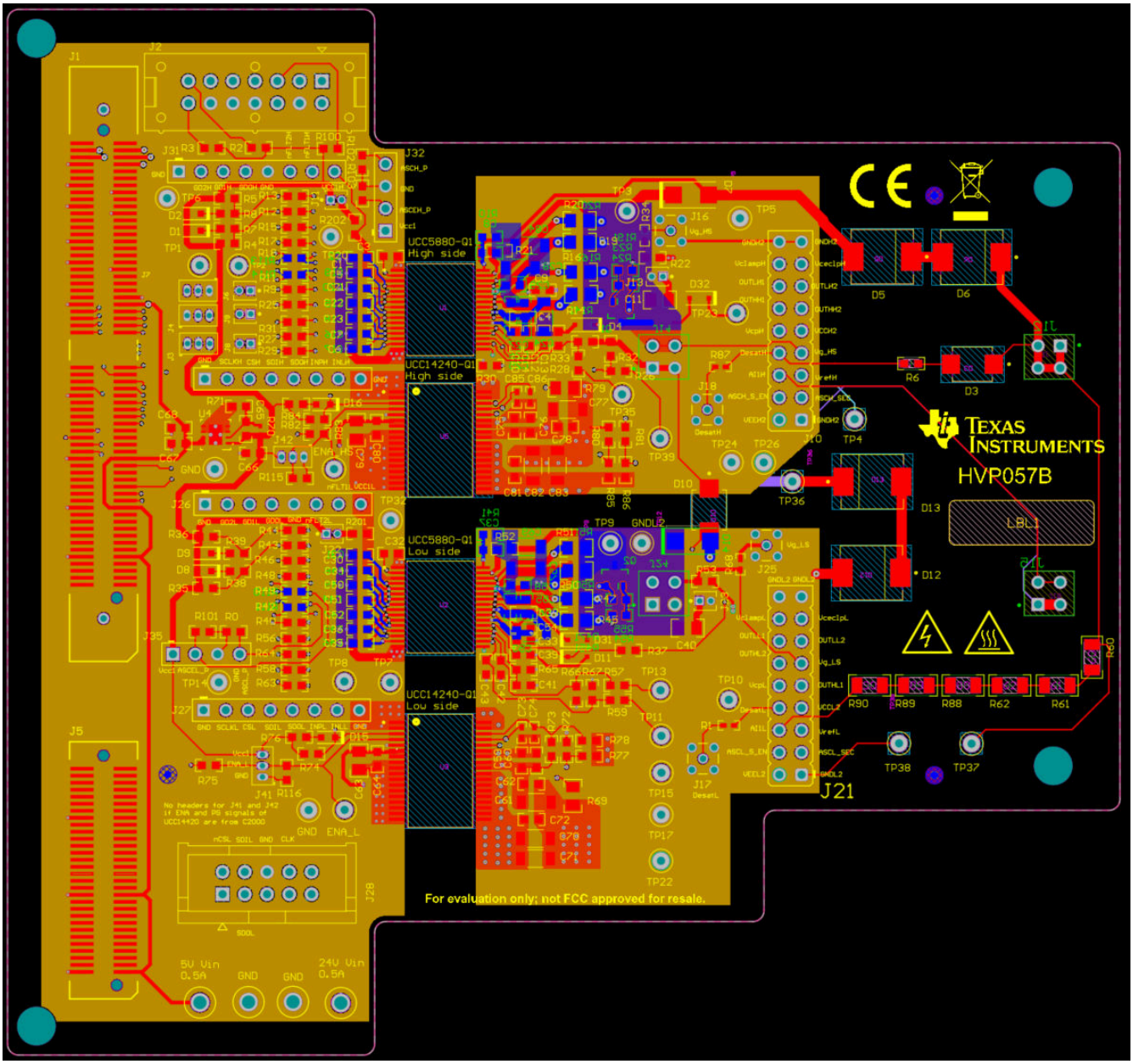


图 6-1. 2D Layout Example

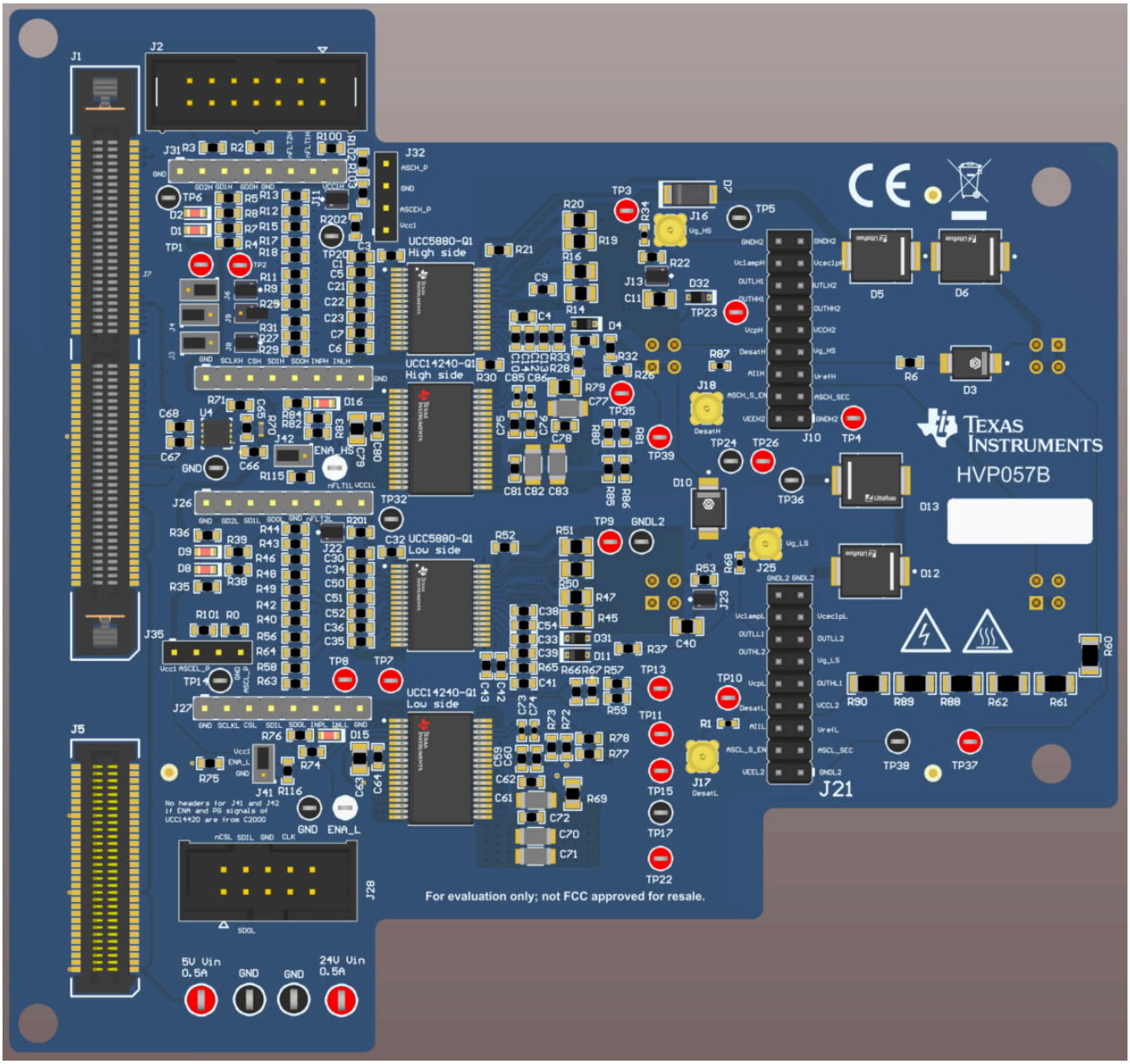


图 6-2. 3D Layout Example

7 Device and Documentation Support

7.1 Device Support

7.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

7.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2022) to Revision A (February 2024)	Page
• 将“预告信息”更改为“量产数据”	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5880QDFCRQ1	ACTIVE	SSOP	DFC	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5880Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

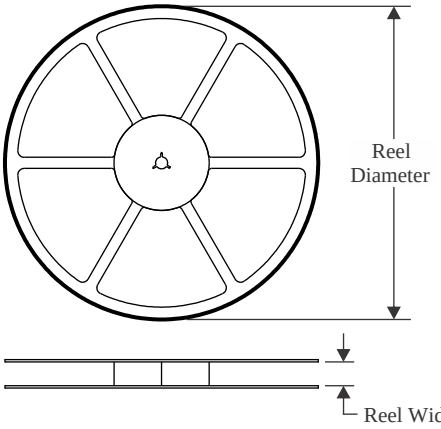
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

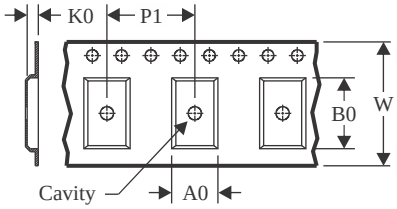
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

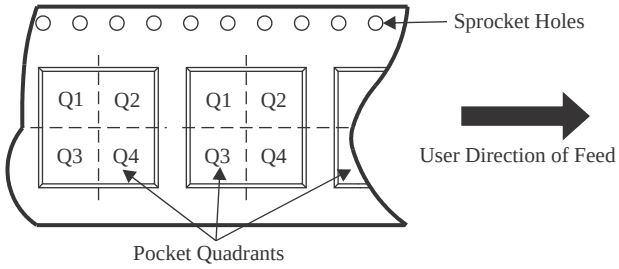


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

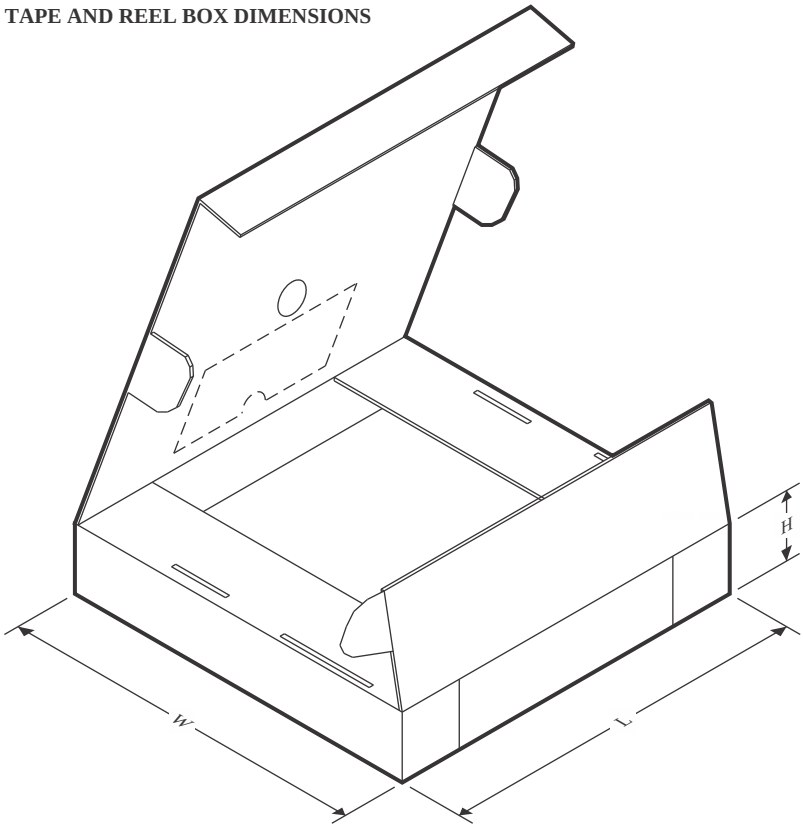
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5880QDFCRQ1	SSOP	DFC	32	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

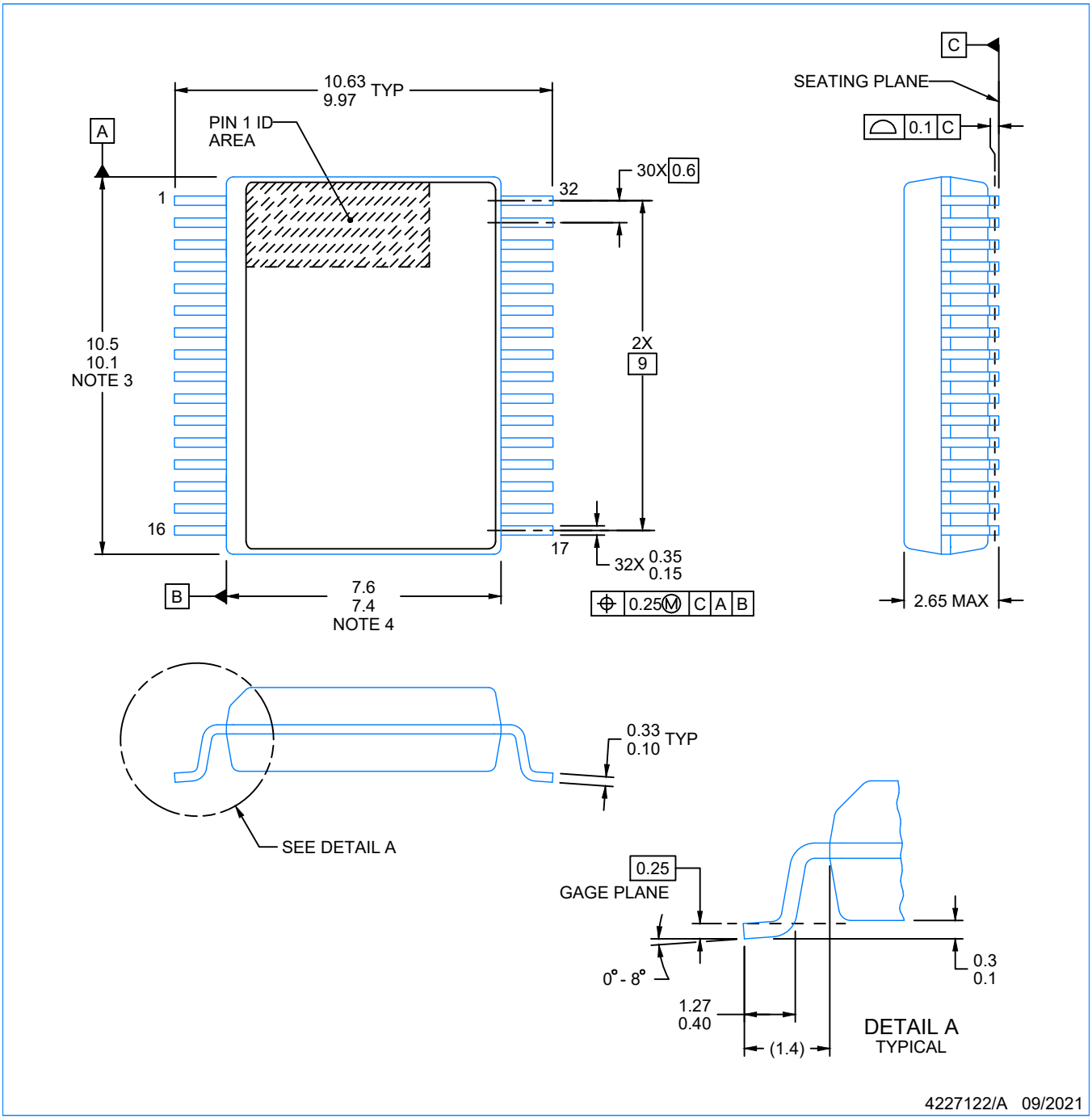
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5880QDFCRQ1	SSOP	DFC	32	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DFC0032A

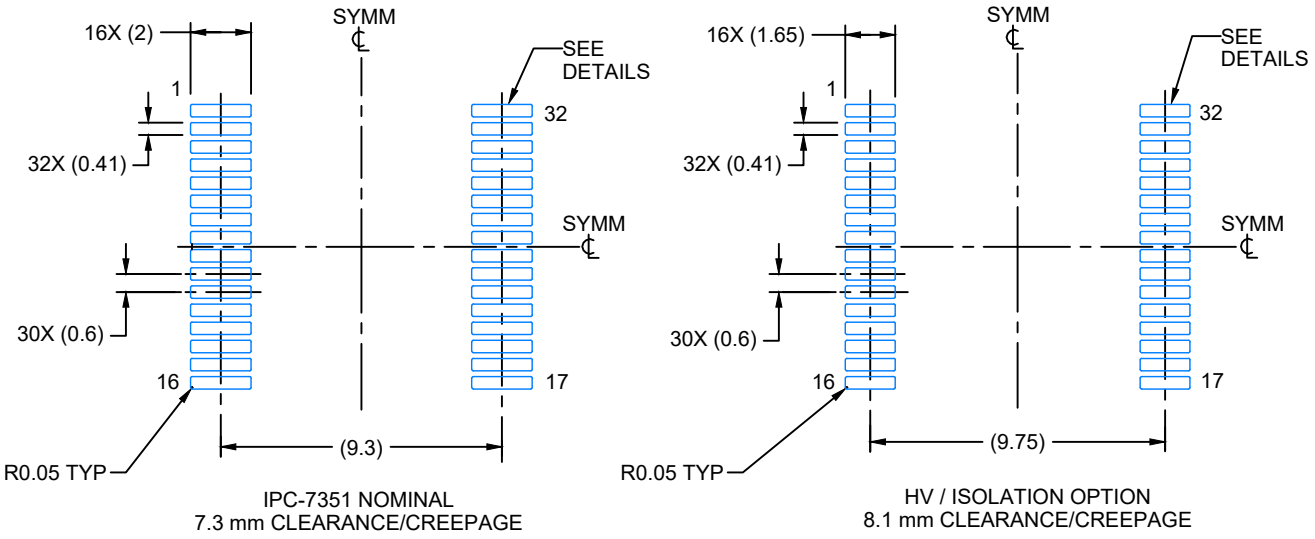
SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE

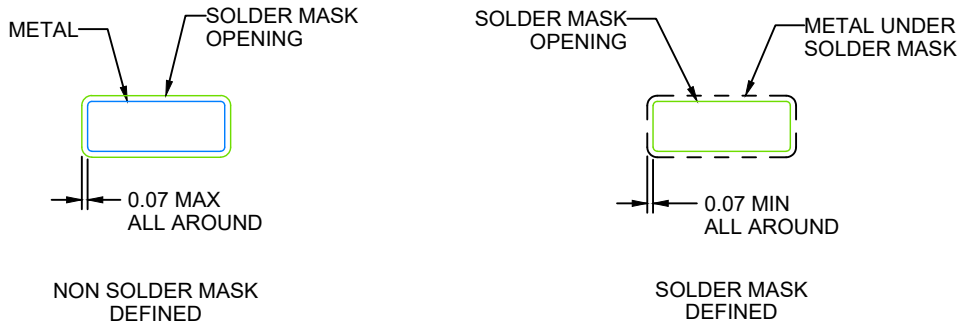


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X

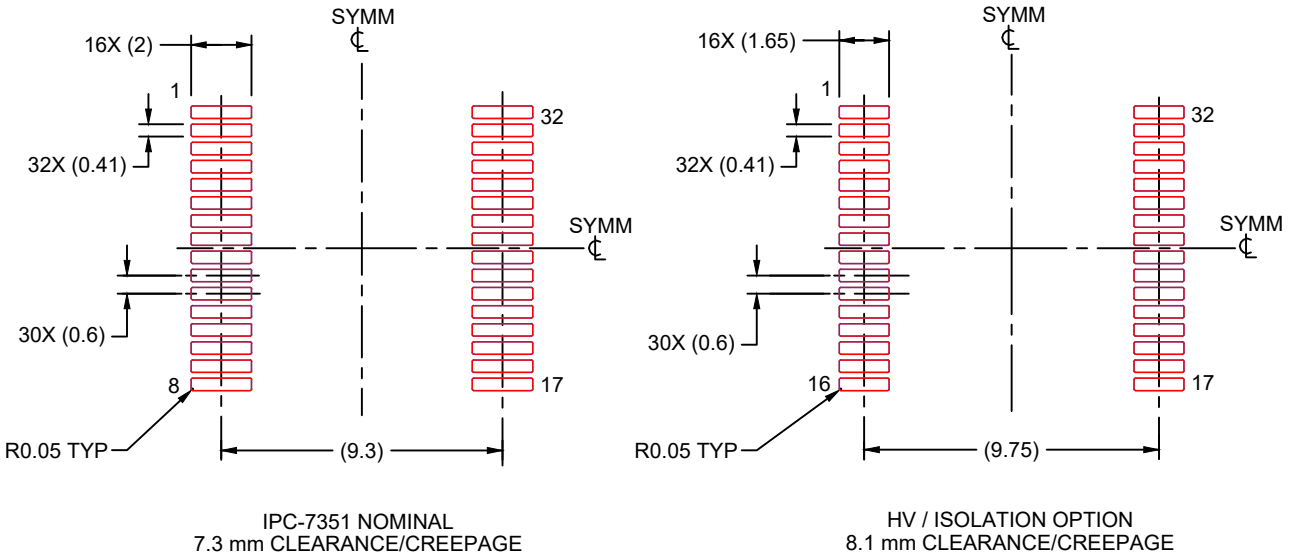


SOLDER MASK DETAILS

4227122/A 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4227122/A 09/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265