LM5180-Q1 Single-Output EVM User's Guide

With input voltage range and current capability as specified in Table 1, the family of PSR flyback DC/DC converters from TI provides flexibility, scalability, and optimized solution size for a range of applications. Using an 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch, these converters enable isolated DC/DC solutions with high density and low component count.

Table 1. PSR Flyback DC/DC Converter Family

PSR FLYBACK CONVERTER	INPUT VOLTAGE RANGE	PEAK SWITCH CURRENT (TYP)	MAXIMUM LOAD CURRENT, V_{OUT} = 12 V, N_{PS} = 1		
			V_{IN} = 4.5 V	V_{IN} = 13.5 V	V_{IN} = 24 V
LM5181-Q1	4.5 V to 65 V	0.75 A	90 mA	180 mA	225 mA
LM5180-Q1	4.5 V to 65 V	1.5 A	180 mA	360 mA	450 mA
LM25180-Q1	4.5 V to 42 V	1.5 A	180 mA	360 mA	450 mA
LM25183-Q1	4.5 V to 42 V	2.5 A	300 mA	600 mA	750 mA
LM25184-Q1	4.5 V to 42 V	4.1 A	500 mA	1 A	1.25 A

The LM5180EVM-S05 evaluation module (EVM) is a flyback DC/DC converter that employs primary-side regulation (PSR) based on sampling of the primary winding voltage of the transformer to achieve high efficiency in a small footprint. It operates over a wide input voltage range of 10 V to 65 V, providing a regulated 5-V output using a transformer with 3 : 1 turns ratio. Operating without an optocoupler or transformer auxiliary winding, the converter delivers an output voltage with ±1.5% regulation.

The EVM design uses the LM5180-Q1 65-V PSR flyback converter. An integrated 100-V, 1.5-A power MOSFET provides ample margin for line transients and switch (SW) node voltage spikes related to transformer parasitic leakage inductance. Load regulation errors related to transformer secondary winding resistance are avoided by virtue of the quasi-resonant boundary conduction mode (BCM) control scheme. Additional features includes current-mode control with internal compensation, hiccup-mode fault protection, programmable soft-start, and optional output voltage temperature compensation. Input UVLO protects the converter at low input voltage conditions, and the EN/UVLO pin supports adjustable UVLO with user-defined hysteresis for application specific power-up and power-down requirements.

The LM(2)5180 and LM(2)5180-Q1 converters are available in a 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch to enable isolated DC/DC solutions with high density and low component count. Wettable flank pins provide a visual indicator of solderability, which reduces inspection time and manufacturing costs in high-reliability industrial and automotive applications. See the LM5180 and LM5180-Q1 data sheets for more information. Use the LM5180-Q1 with WEBENCH® Power Designer to create a custom regulator design. Furthermore, you can download the *LM5180 Quickstart Calculator* to optimize component values and examine predicted efficiency performance across line and load ranges.

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1 High Density EVM Description

The LM5180-Q1 single-output EVM is designed to use a regulated or non-regulated high-voltage input rail ranging from 10 V to 65 V to produce a tightly-regulated, isolated output voltage of 5 V at load currents of 1 A (or higher depending on V_{IN}). This wide V_{IN} range isolated DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The power-train passive components selected for this EVM, including flyback transformer, flyback rectifying diode, and ceramic input and output capacitors, are available from multiple component vendors. Transformers with functional or basic grade isolation are available with isolation voltages of 1.5 kV and greater.

1.1 Typical Applications

- Automotive HEV/EV powertrain systems
- Sub-AM band automotive body electronics
- Traction inverters: IGBT and SiC gate drivers
- Isolated field transmitters and field actuators
- Building automation HVAC systems
- Isolated bias power rails

1.2 Features and Electrical Performance

- Tightly-regulated, isolated output voltage of 5 V with ±1.5% load regulation from 1% to 100% load
- Wide V_{IN} operating range of 10 V to 65 V
- Rated full load current of 1 A at V_{IN} = 24 V
- Maximum switching frequency of 350 kHz remains below the AM band
- High efficiency across wide load current range
  - Full load efficiency of 86% and 85.5% at V_{IN} = 24 V and 48 V, respectively
  - 86% efficiency at half-rated load, V_{IN} = 24 V
- 1.3-mA and 1-mA no-load supply current at V_{IN} = 24 V and 48 V, respectively
- Ultra-low conducted and radiated EMI signatures
  - Optimized for CISPR 25 Class 5 requirements
  - Soft switching avoids diode reverse recovery
  - Input π-stage EMI filter with damping from electrolytic capacitor ESR
- BCM control architecture provides fast line and load transient response
  - Peak current-mode control
  - Quasi-resonant switching for reduced power loss
  - Internal loop compensation
- Integrated 100-V flyback power MOSFET
  - Provides large margin for input voltage transients
- Cycle-by-cycle overcurrent protection (OCP)
- Monotonic prebias output voltage start-up
- User-adjustable soft-start time using capacitor connected between SS/BIAS and GND
  - Option for external bias using auxiliary winding connected to SS/BIAS
- Resistor-programmable input voltage UVLO with customizable hysteresis for applications with wide turnon and turnoff voltage difference
  - Input UVLO set to turn on and off at V_{IN} of 9.5 V and 6.5 V, respectively
- Fully assembled, tested, and proven PCB layout with 50-mm × 35-mm total footprint

2 EVM Performance Characteristics

Table 2. Electrical Performance Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		10	24	65	V
Input voltage turnon, V_{IN-ON}	Adjusted using EN/UVLO divider resistors			9.5		V
Input voltage turnoff, V_{IN-OFF}				6.5		
Input voltage hysteresis, V_{IN-HYS}				3		
Input current, no load, I_{IN-NL}	I_{OUT} = 0 A	V_{IN} = 24 V		1.3		mA
		V_{IN} = 48 V		1		
		V_{IN} = 65 V		1		
Input current, disabled, I_{IN-OFF}	V_{EN} = 0 V	V_{IN} = 24 V		10		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} (1)			4.95	5.025	5.1	V
Output current, I_{OUT} (2)	V_{IN} = 12 V				0.8	A
	V_{IN} = 24 V				1.2	
	V_{IN} = 48 V				1.4	
Output voltage regulation, ΔV_{OUT}	Load regulation, V_{IN} = 24 V	I_{OUT} = 10 mA to 1 A		1%		
	Line regulation, I_{OUT} = 500 mA	V_{IN} = 10 V to 65 V		1%		
Output voltage ripple, V_{OUT-AC}	V_{IN} = 24 V, I_{OUT} = 1 A			50		mVrms
Output overcurrent protection, I_{OCP}	V_{IN} = 24 V			1.55		A
	V_{IN} = 48 V			1.55		
Soft-start time, t_{SS}				8		ms
SYSTEM CHARACTERISTICS						
Switching frequency, F_{SW-NOM}	V_{IN} = 24 V, I_{OUT} = 0.5 A			350		kHz
Half-load efficiency, η_{HALF} (1)	I_{OUT} = 0.5 A	V_{IN} = 12 V		86%		
		V_{IN} = 24 V		86%		
		V_{IN} = 48 V		84%		
		V_{IN} = 65 V		82%		
Full load efficiency, η_{FULL}	I_{OUT} = 1 A	V_{IN} = 24 V		86%		
		V_{IN} = 36 V		86%		
		V_{IN} = 48 V		85.5%		
		V_{IN} = 65 V		84.5%		
Isolation rating (3)					1500	V
LM5180 junction temperature, T_J			–40		150	°C

(1) The default output voltage of this single-output EVM is 5 V. Efficiency and other performance metrics can change based on operating input voltage, load current, externally-connected output capacitance, and other parameters.
(2) The maximum output power delivered by the LM5180-Q1 PSR flyback converter increases with input voltage.
(3) The selected flyback transformer provides functional isolation to 1500 V DC.

3 Application Circuit Diagram

Figure 1 shows the schematic of an LM5180 PSR flyback converter (EMI filter stage not shown). Soft start (SS), temperature compensation (TC), and UVLO (EN/UVLO) components are shown that are configurable as required for the specific application.

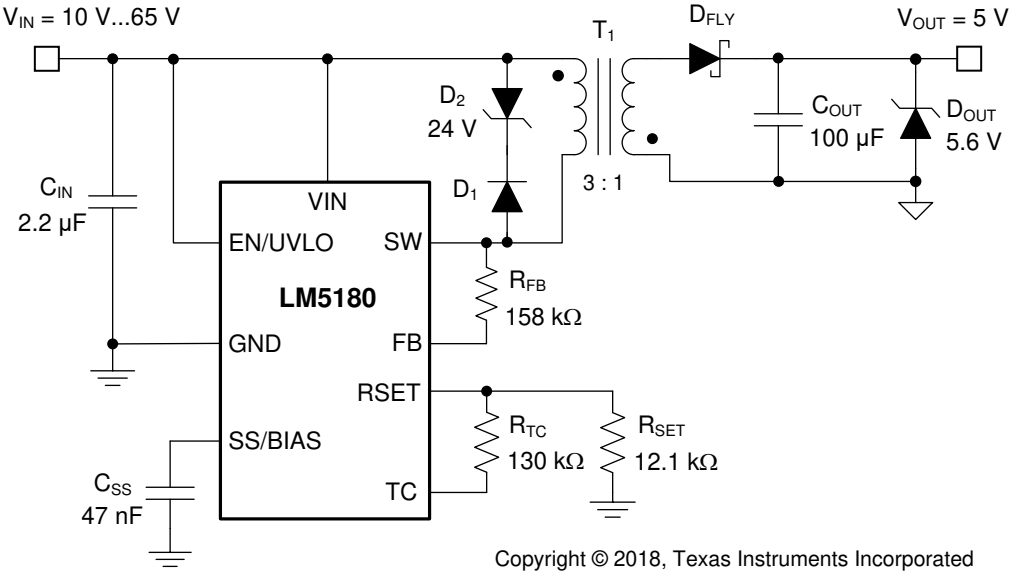

Figure 1. LM5180 PSR Flyback Converter Simplified Schematic

4 EVM Photo

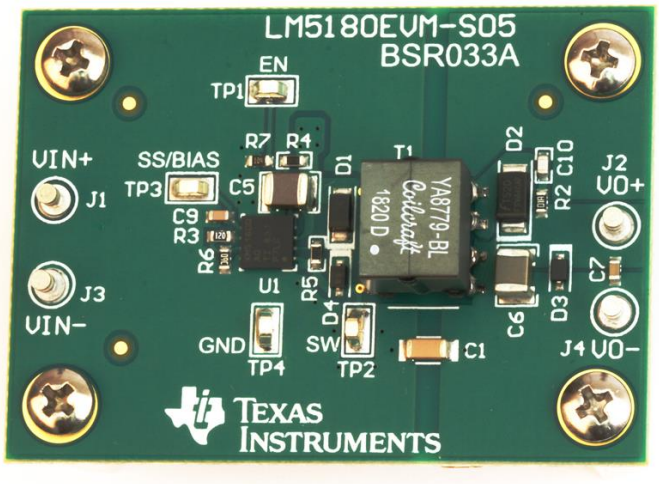

Figure 2. EVM Photo (Top Side), 50 mm × 35 mm

CAUTION

Caution Hot surface.
Contact may cause burns.
Do not touch.

5 Test Setup and Procedure

5.1 Test Setup

Table 3. EVM Connections

LABEL	DESCRIPTION
VIN+	Positive input voltage power and sense connection
VIN–	Negative input voltage power and sense connection
VOUT+	Positive output voltage power and sense connection
VOUT–	Negative output voltage power and sense connection
EN	ENABLE input. Tie to GND to disable converter
SW	SW node connection

Referencing the EVM connections described in Table 3, the recommended test setup to evaluate the LM5180EVM-S05 is shown in Figure 3. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before power is applied to the EVM.

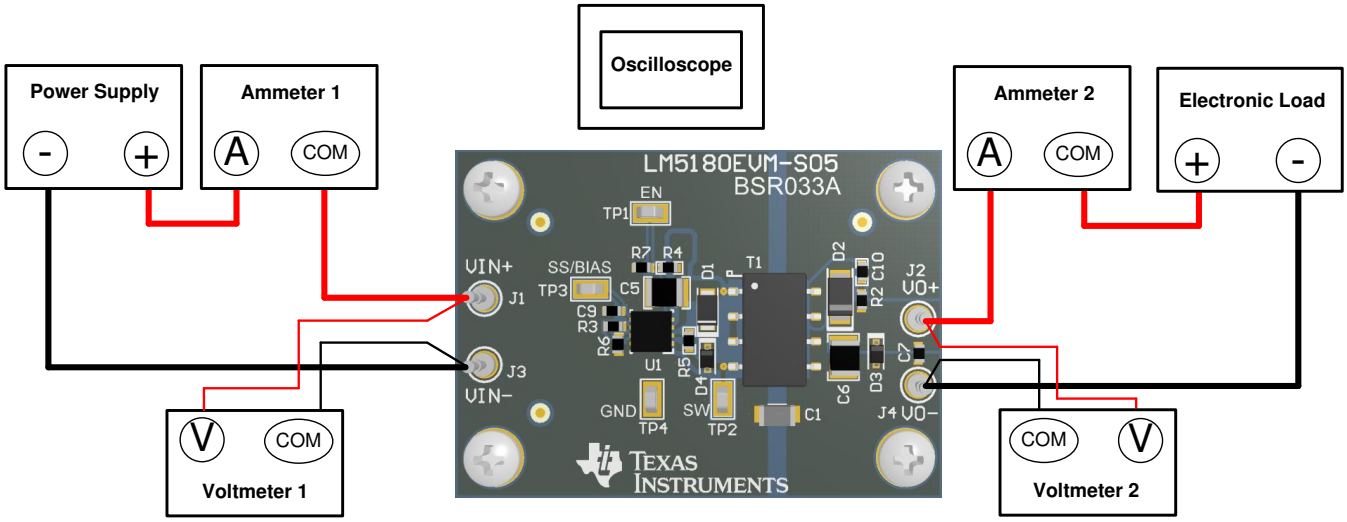

Figure 3. EVM Test Setup

CAUTION

Refer to the LM5180 data sheet, LM5180 Quickstart Calculator, and WEBENCH® Power Designer for additional guidance pertaining to component selection and converter operation.

5.2 Test Equipment

Voltage Source: The input voltage source V_{IN} must be a 0–65-V variable DC source capable of supplying 0.5 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set the voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT+ to VOUT–. Set the voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set the ammeter to 1-second aperture time.
- **Ammeter 2:** Output current. Set the ammeter to 1-second aperture time.

Electronic Load: The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 Adc to 1 Adc at 5 V. For a no-load input current measurement, disconnect the electronic load as it can draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that may be live or energized.

5.3 Recommended Test Setup

5.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1 A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 3. An additional input bulk capacitor is recommended to provide damping if long input lines are used.
- Connect voltmeter 1 at VIN+ and VIN– connection points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

5.3.2 Output Connections

- Connect an electronic load to VOUT+ and VOUT– connections. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeter 2 at VOUT+ and VOUT– connection points to measure the output voltage.
- Connect ammeter 2 to measure the output current.

5.4 Test Procedure

5.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 10 mA.
- Increase input source from 0 V to 24 V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 0.5 A.
- Using voltmeter 2 to measure the output voltage, V_{OUT}, vary the load current from 10 mA to 1 A DC; V_{OUT} should remain within the load regulation specification.
- Set the load current to 0.5 A (50% rated load) and vary the input source voltage from 10 V to 65 V; V_{OUT} must remain within the line regulation specification.
- Decrease load to 0 A. Decrease input source voltage to 0 V.

6 Test Data and Performance Curves

Figure 4 through Figure 11 present typical performance curves for the LM5180EVM-S05. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Conversion Efficiency

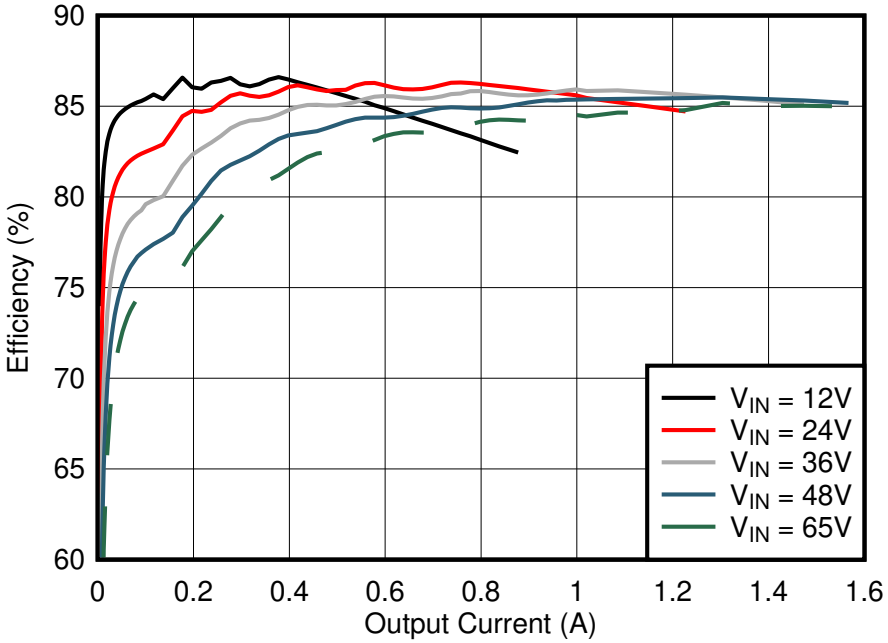

Figure 4. Conversion Efficiency (Linear Scale)

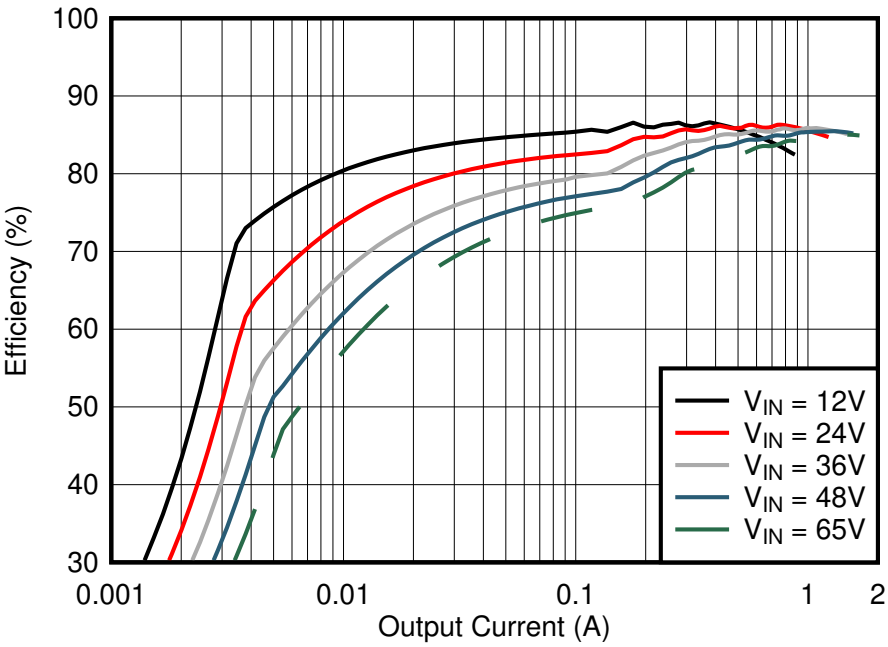

Figure 5. Conversion Efficiency (Log Scale)

6.2 Load Regulation

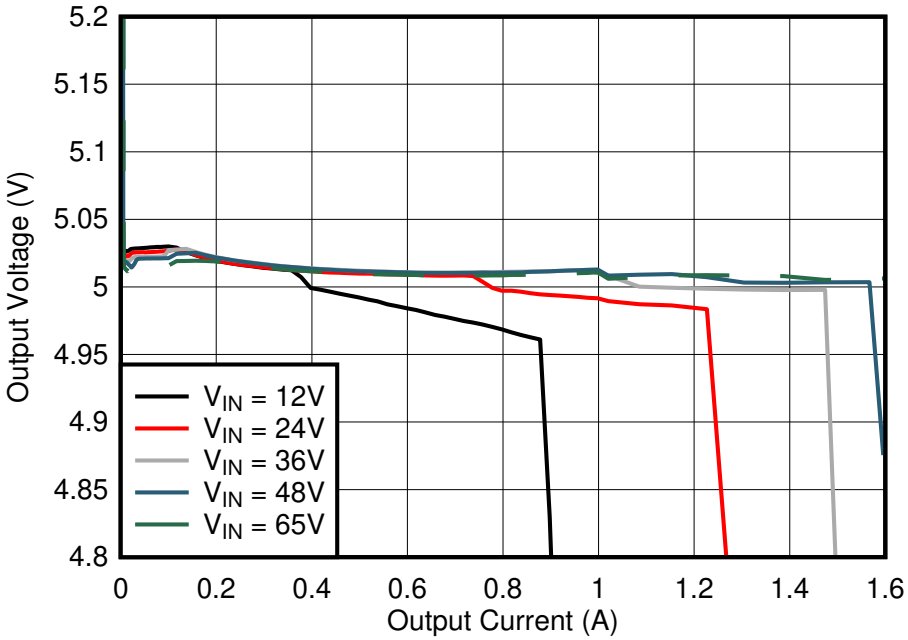

Figure 6. Load Regulation (Linear Scale)

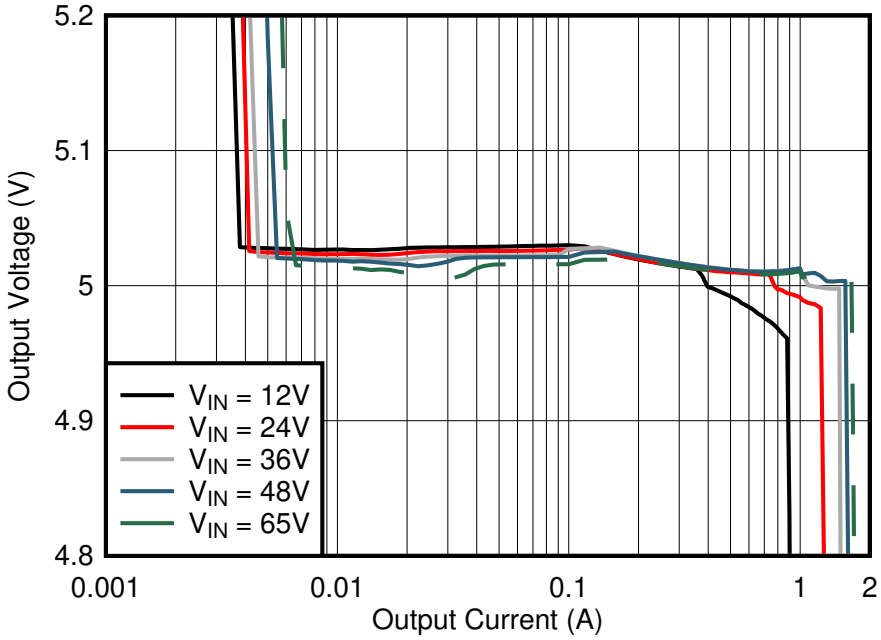

Figure 7. Load Regulation (Log Scale)

6.3 Operating Waveforms

6.3.1 Switching

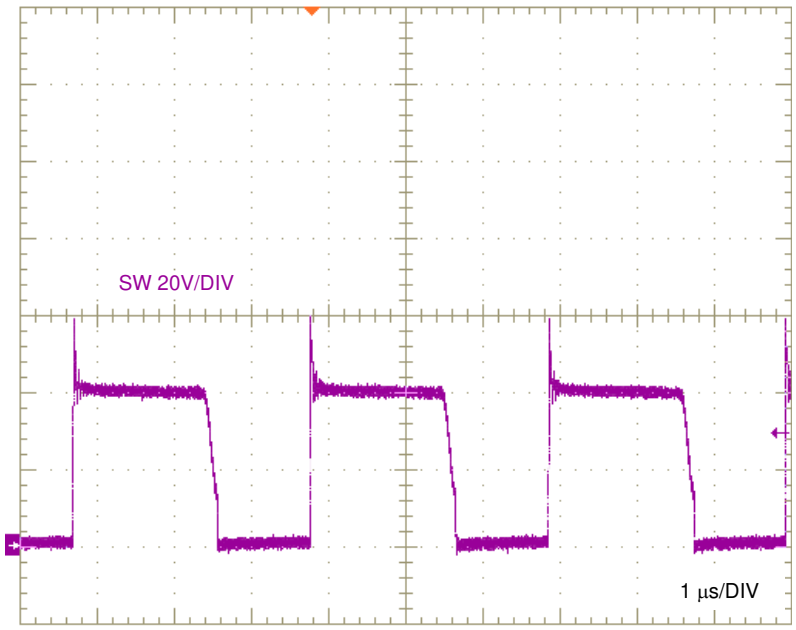

Figure 8. SW Node Voltage, V_{IN} = 24 V, I_{OUT} = 1 A

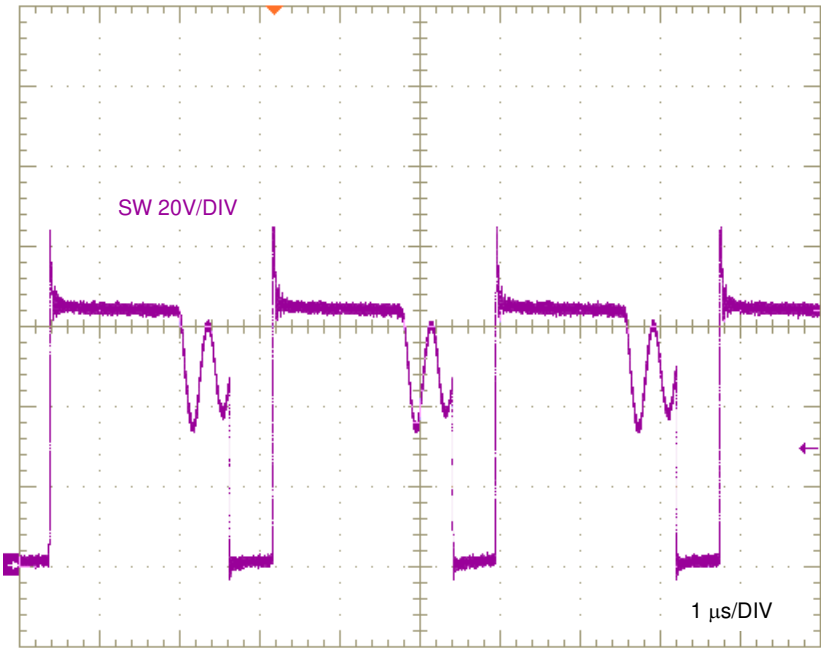

Figure 9. SW Node Voltage, V_{IN} = 48 V, I_{OUT} = 1 A

6.3.2 Load Transient Response

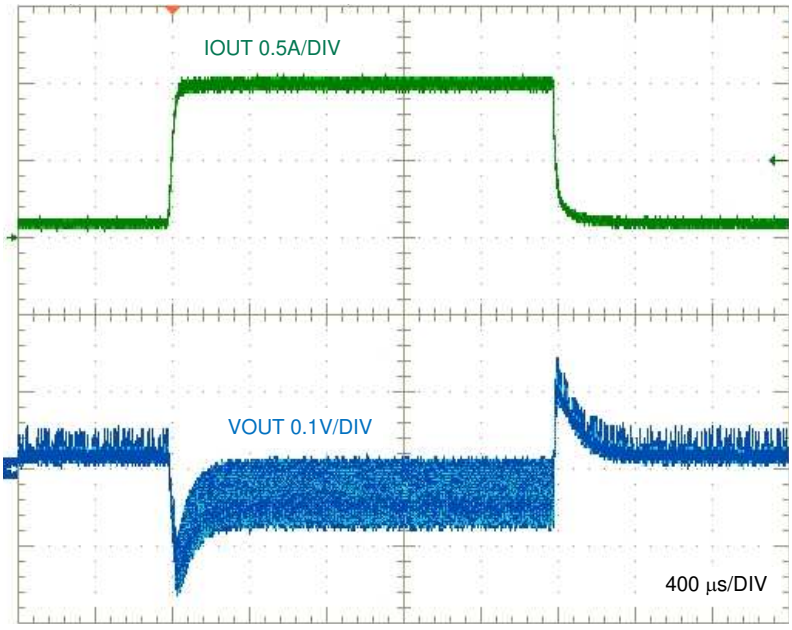

Figure 10. Load Transient Response, V_{IN} = 24 V, 0.1 A to 1 A at 1 A/µs

6.3.3 Start-Up (1)

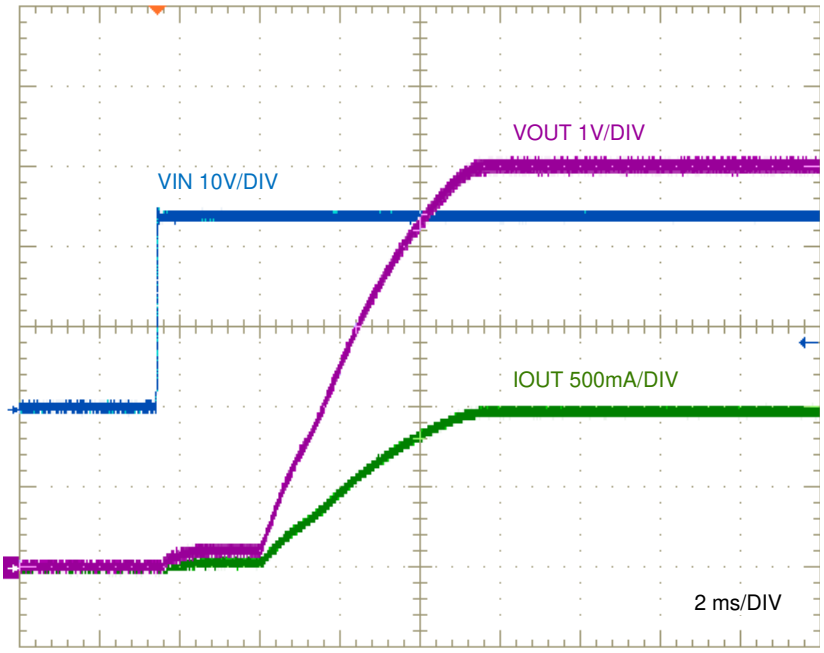

Figure 11. Start-Up, V_{IN} = 24 V, I_{OUT} = 1 A Resistive

(1) The internal soft-start timer is applicable here as the SS capacitor was not installed during these start-up tests.

6.4 Enable On

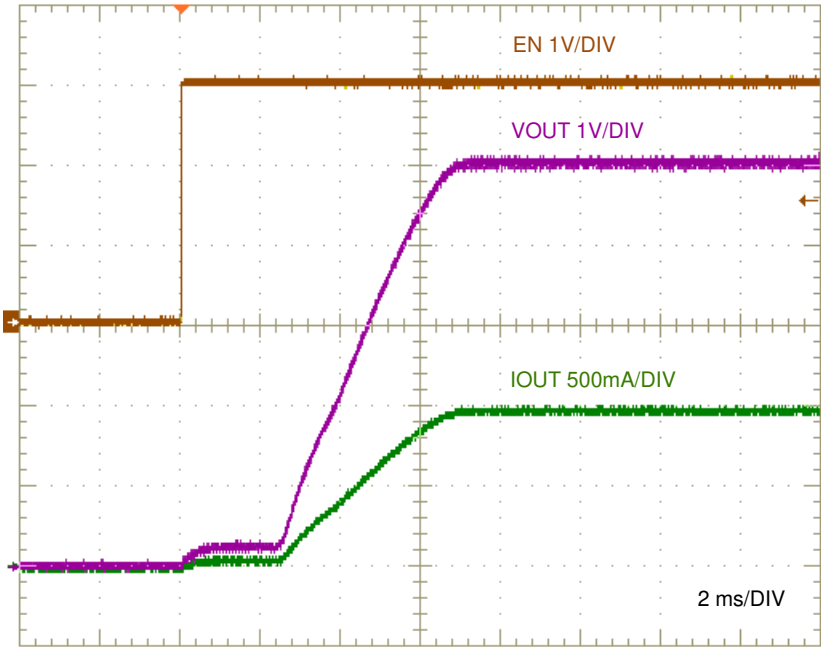

Figure 12. Enable On, V_{IN} = 24 V, I_{OUT} = 1 A

6.5 CISPR 25 EMI

Figure 13 and Figure 14 present the EMI performance of the LM5180-Q1 EVM at 12-V and 24-V inputs, respectively. Conducted emissions are measured over a frequency range of 150 kHz to 108 MHz using a 5-µH LISN according to the CISPR 25 specification. CISPR 25 class 5 peak and average limit lines are denoted in red. The yellow and blue spectra are measured using peak and average detection, respectively.

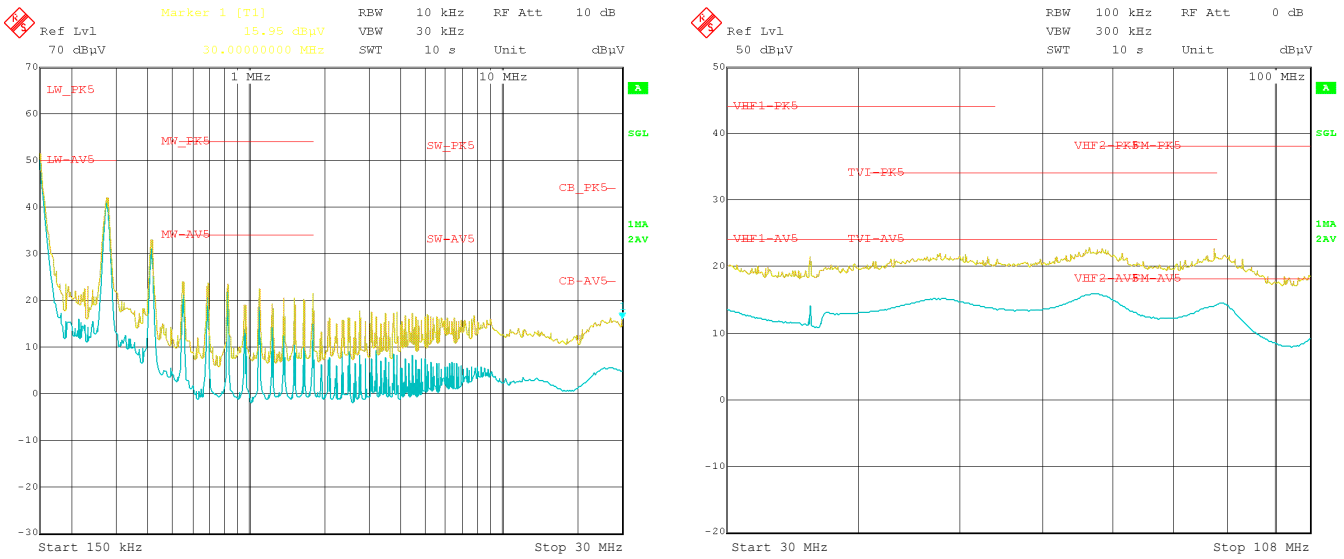

Figure 13. CISPR 25 Class 5 Conducted Emissions Plot, V_{IN} = 12 V, I_{OUT} = 0.85 A, (a) 150 kHz to 30 MHz, (b) 30 MHz to 108 MHz

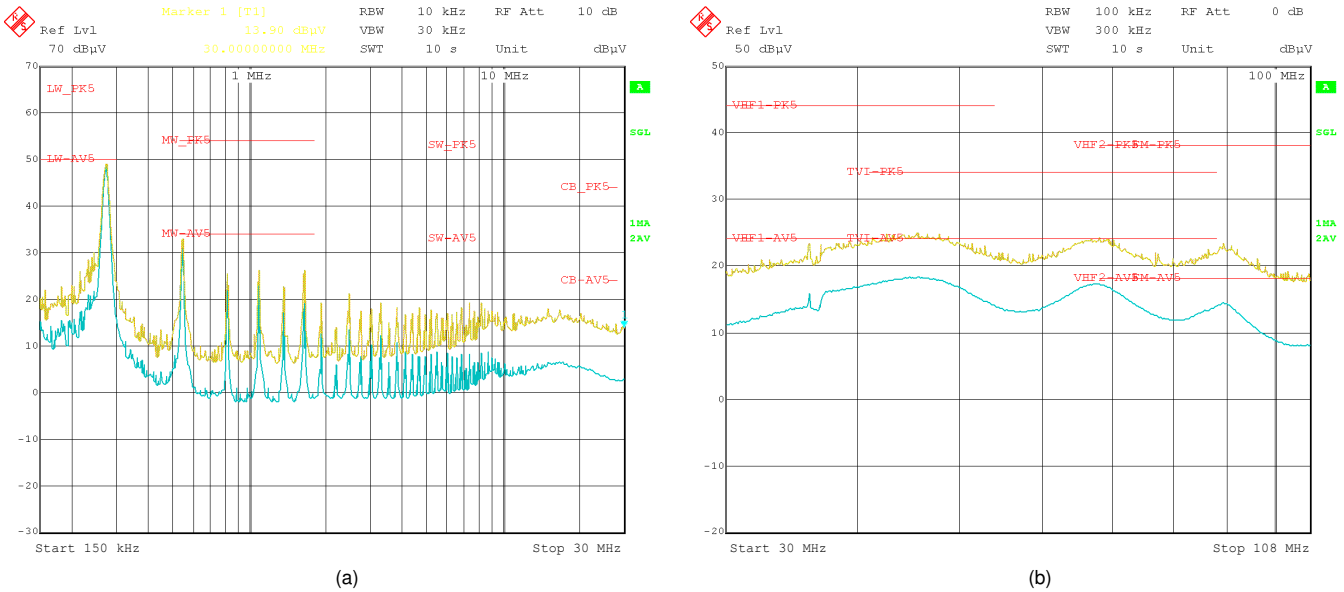

Figure 14. CISPR 25 Class 5 Conducted Emissions Plot, V_{IN} = 24 V, I_{OUT} = 0.85 A, (a) 150 kHz to 30 MHz, (b) 30 MHz to 108 MHz

Figure 15 presents the radiated emissions from 30 MHz to 1 GHz using a biconical/log antenna with horizontal polarization. CISPR 25 class 5 peak and average limit lines are denoted in purple and red, respectively. The blue and green spectra are measured using peak and average detectors, respectively.

For both conducted and radiated emissions measurements, the transformer core is shielded using a copper strap tied to primary GND.

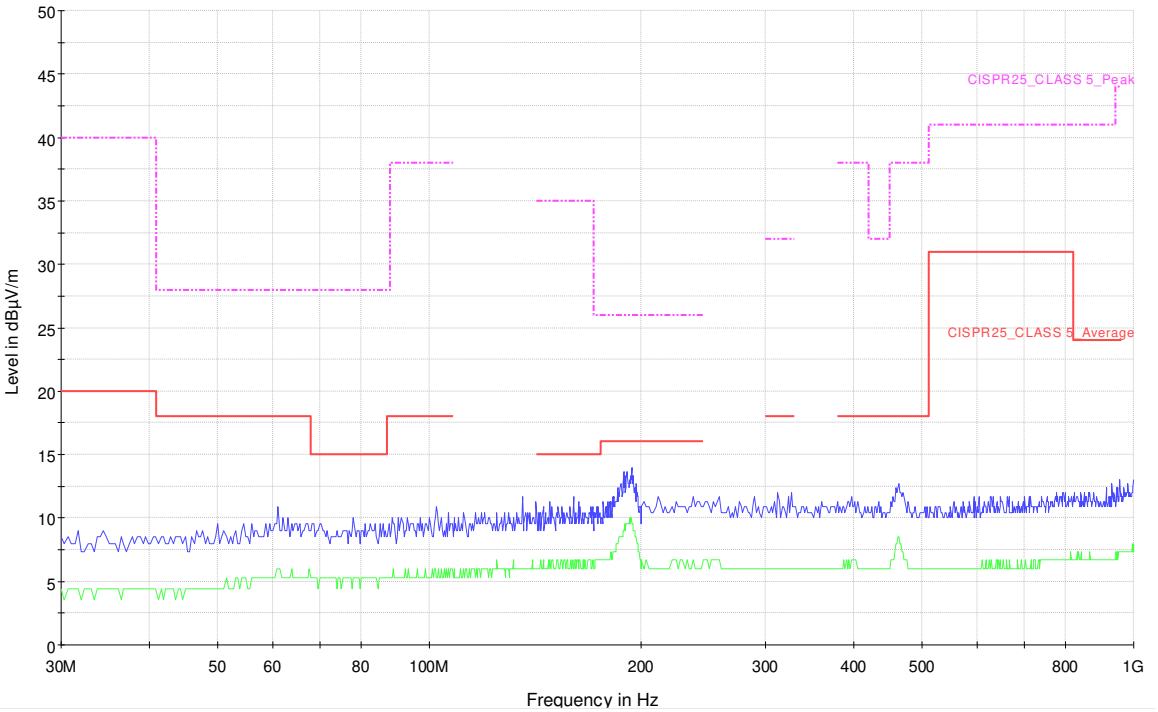

Figure 15. CISPR 25 Class 5 Radiated Emissions Plot, V_{IN} = 13.5 V, I_{OUT} = 0.5 A

7 EVM Documentation

7.1 Schematic

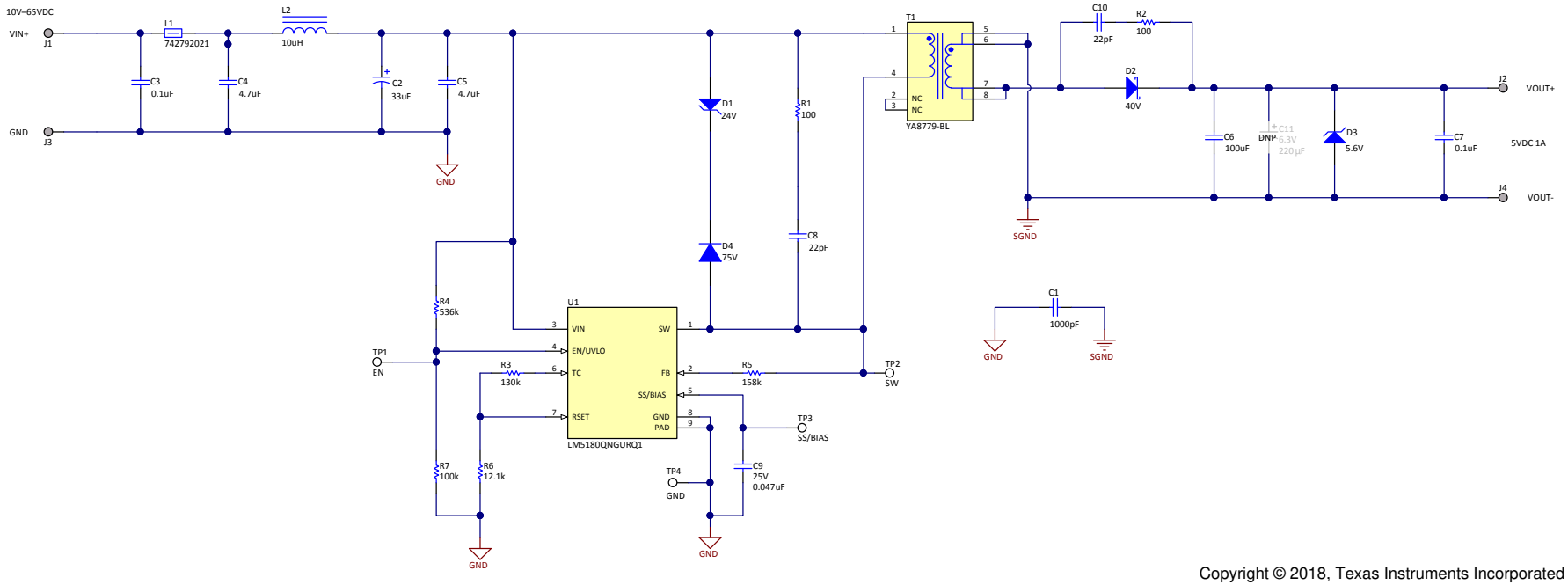

Figure 16. PSR Flyback EVM Schematic

7.2 Bill of Materials

Table 4. Bill of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, Ceramic, 1 nF, 2 kV, X7R, 1206	202R18W102KV4E	Johanson Dielectrics Inc.
1	C2	Aluminum Electrolytic, 33 µF, 100 V, ±20%, AEC-Q200 grade 2	EEE-FK2A330P	Panasonic
1	C3	Capacitor, Ceramic, 0.1 µF, 100 V, X7R, 0603	C1608X7R1A105K080AC	TDK
2	C4, C5	Capacitor, Ceramic, 4.7 µF, 100 V, X7S, 1210	C3225X7S2A475M200AB	TDK
			GRJ32DC72A475KE11	Murata
1	C6	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 1210	C3225X5R0J107M250AC	TDK
			885012109004	Würth Electronik
			GRM32ER60J107ME20	Murata
		Capacitor, Ceramic, 100 µF, 6.3 V, X7S, 1210	GRM32EC70J107ME15	Murata
			JMK325AC7107MM-P	Taiyo Yuden
1	C7	Capacitor, Ceramic, 0.1 µF, 25 V, X7R, 0603	Std	Std
2	C8, C10	Capacitor, Ceramic, 22 pF, 100 V, X7R, 0603	Std	Std
1	C9	Capacitor, Ceramic, 47 nF, 16 V, X7R, 0603	Std	Std
1	D1	Zener, 24 V, 1 W, PowerDI-123, AEC-Q101	DFLZ24-7	Diodes Inc.
		Zener, 24 V, 1 W, SOD-123	DFLZ24-TP	Micro Commercial
1	D2	Schottky diode, 40 V, 3 A, SMA, AEC-Q101	FSV340AF	Onsemi
1	D3	Zener diode, 5.6 V, SOD-523	BZT52C5V6T-7	Diodes Inc.
1	D4	Switching diode, 75 V, 0.25 A,, SOD-123	CMDD4448	Central Semi
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips Panhead	NY PMS 440 0025 PH	B & F Fastener Supply
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone Electronics
1	L1	Ferrite bead, 22 Ω at 100 MHz, 8 mΩ max, 0805	742792021	Würth Electronik
1	L2	Inductor, 10 µH ±30%, 120 mΩ, 1 A	744042100	Würth Electronik
1	T1	Transformer, 30 µH, 2A Isat, 3 : 1 turns ratio, 10.2 mm × 9.3 mm × 10.6 mm	YA8779-BLD	Coilcraft
			750317605	Würth Electronik
2	R1, R2	Resistor, Chip, 100 Ω, 1/8W, 5%, 0805	Std	Std
1	R3	Resistor, Chip, 130 kΩ, 1/16W, 1%, 0603	Std	Std
1	R4	Resistor, Chip, 536 kΩ, 1/16W, 1%, 0603	Std	Std
1	R5	Resistor, Chip, 158 kΩ, 1/16W, 1%, 0603	Std	Std
1	R6	Resistor, Chip, 12.1 kΩ, 1/16W, 1%, 0603	Std	Std
1	R7	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0603	Std	Std
1	U1	IC, LM5180-Q1, wide V_{IN} PSR flyback converter, WSON-8	LM5180QNGURQ1	TI
1	PCB1	PCB, FR4, 2 layer, 1 oz, 50 mm x 35 mm	PCB	–
4	J1, J2, J3, J4	Turret, PTH, 4.72 mm, VIN+, VIN–, VOUT+, VOUT–	1573-2	Keystone Electronics
4	TP1, TP2, TP3, TP4	Test point for EN, SW, SS/BIAS, GND	5015	Keystone Electronics

7.3 PCB Layout

Figure 17 through Figure 20 show the design of a 2-layer PCB with 1-oz copper thickness. The EVM is a two-sided design with post connections for VIN+, VIN–, VOUT+ and VOUT–.

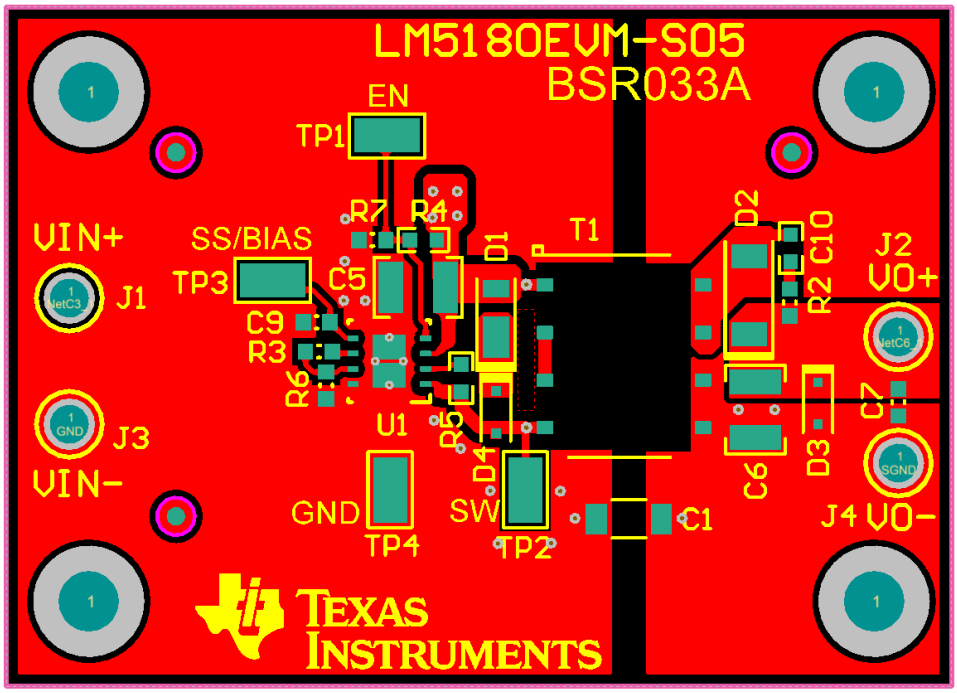

Figure 17. Top Copper (Top View)

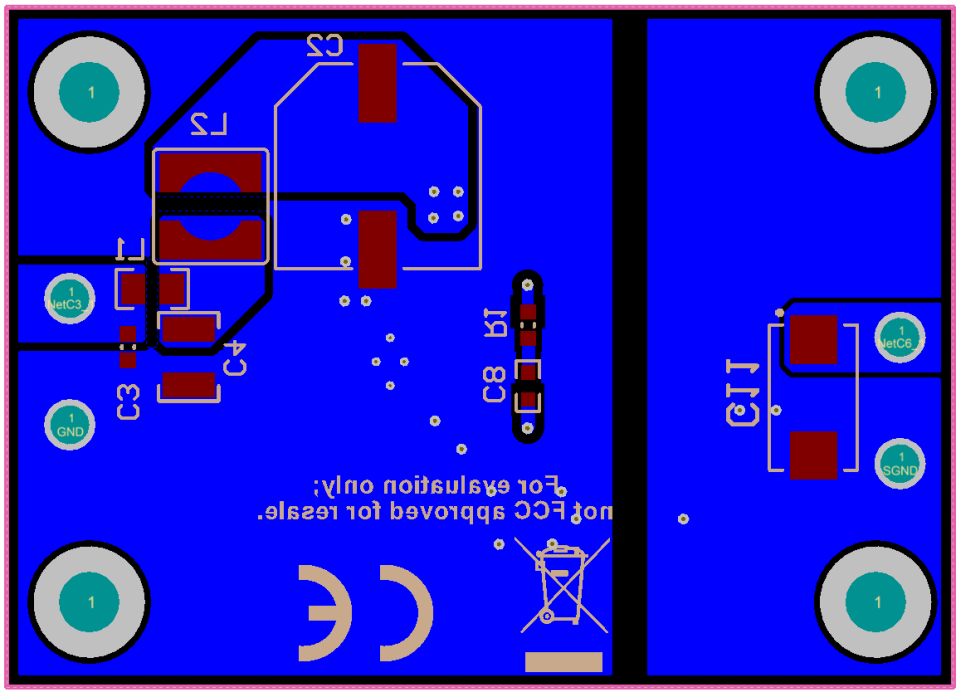

Figure 18. Bottom Copper (Top View)

7.4 Assembly Drawings

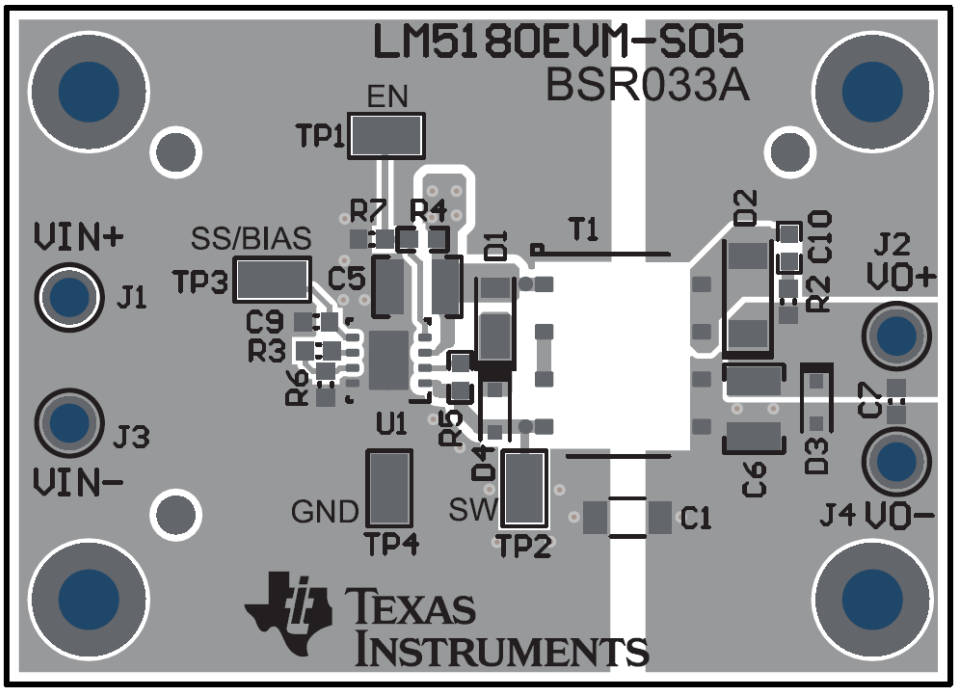

Figure 19. Top Component Drawing

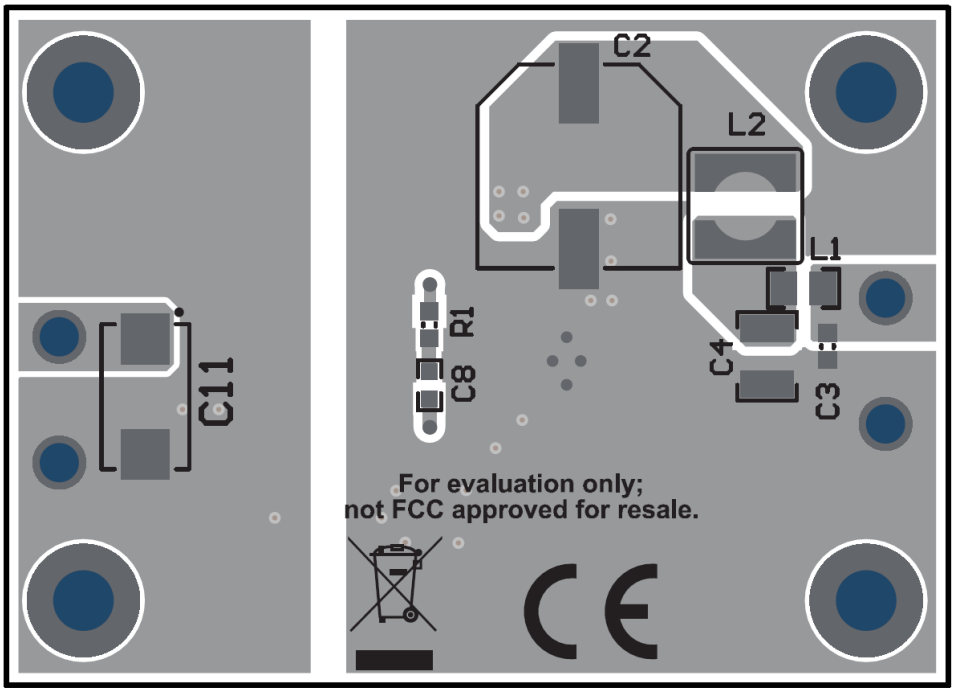

Figure 20. Bottom Component Drawing

7.4.1 PCB Layout Tips

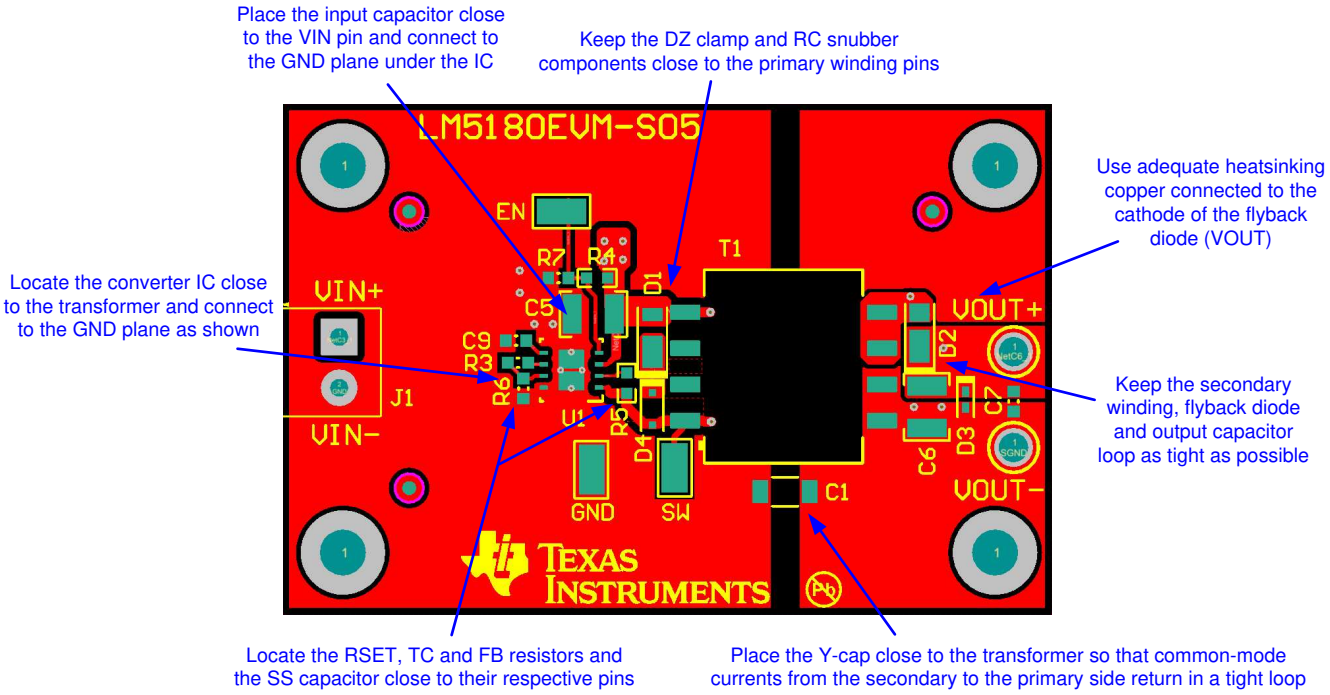

Figure 21. Layout Design Tips for a Single-output PSR Flyback Converter

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

For development support see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
- LM5180 PSR Flyback Converter Quickstart Calculator and PSPICE simulation model

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *LM5180EVM-DUAL Dual-Output EVM User's Guide* (SNVU609)
- *LM25184EVM-S12 EVM User's Guide* (SNVU680)
- *IC Package Features Lead to Higher Reliability in Demanding Automotive and Communications Equipment Systems* (SNVA804)
- *PSR Flyback Transformer Design for mHEV Applications* (SNVA805)
- *How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density* (SLYT779)
- *Why Use PSR-Flyback Isolated Converters in Dual-Battery mHEV Systems* (SLYT791)
- TI Designs:
  - *Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller*
  - *Compact, Efficient, 24-V Input Auxiliary Power Supply Reference Design for Servo Drives*
  - *Reference Design for Power-Isolated Ultra-Compact Analog Output Module*
  - *HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design*
  - *4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers*
  - *Channel-to-Channel Isolated Analog Input Module Reference Design*
  - *SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET*
  - *>95% Efficiency, 1-kW Analog Control AC/DC Reference Design for 5G Telecom Rectifier*
  - *3.5-W Automotive Dual-output PSR Flyback Regulator Reference Design*
- TI Technical Articles:
  - *Flyback Converters: Two Outputs are Better Than One*
  - *Common Challenges When Choosing the Auxiliary Power Supply for Your Server PSU*
  - *Maximizing PoE PD Efficiency on a Budget*
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications* (SLYY104)
  - *An Overview of Conducted EMI Specifications for Power Supplies* (SLYY136)

  - *An Overview of Radiated EMI Specifications for Power Supplies* (SLYY142)
- *Under the Hood of Flyback SMPS Designs* (SLUP261)
- *Flyback Transformer Design Considerations for Efficiency and EMI* (SLUP338)

8.2.1.1 PCB Layout Resources

- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply – Layout Considerations* (SLUP230)
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x* (SNVA721)
- TI Technical Articles:
  - *High-Density PCB Layout of DC-DC Converters*

8.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design by Insight, Not Hindsight* (SNVA419)
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* (SNVA183)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Thermal Design Made Simple with LM43603 and LM43602* (SNVA719)
- *PowerPAD Thermally Enhanced Package* (SLMA002)
- *PowerPAD Made Easy* (SLMA004)
- *Using New Thermal Metrics* (SBVA025)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from C Revision (April 2019) to D Revision **Page**

- Added PSR flyback converter family in *Table 1* 1
- Updated *Section 1.1* 3
- Added PCB layout tips in *Section 7.4.1* 19
- Updated list of collateral in *Section 8* 20

Changes from B Revision (February 2019) to C Revision **Page**

- Changed "...delivers an output voltage with ±1% regulation" to "...delivers an output voltage with ±1.5% regulation" 1
- Changed "±1% load regulation" to "±1.5% load regulation" 3
- Changed Soft-start time, t_{SS} from "5 ms" to "8 ms" 4
- Changed "V_{IN} = 24 V, I_{OUT} = 0.85 A, (a) 150 kHz to 30 MHz, (b) 30 MHz to 108 MHz" to "V_{IN} = 13.5 V, I_{OUT} = 0.5 A" in caption of Figure 15 14

Changes from A Revision (October 2018) to B Revision **Page**

- Changed Vin-max to 65 V 1
- Added CISPR 25 EMI results 13

Changes from Original (July 2018) to A Revision **Page**

- Changed photo in Figure 2 5
- Added new waveforms 8

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