

UNDERSTANDING THE DDC112's CONTINUOUS AND NON-CONTINUOUS MODES

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This application bulletin provides additional information on how the DDC112's continuous and non-continuous modes work and how to effectively operate the part in either mode. It is intended to supplement the information in the DDC112's data sheet and therefore skips some of the basic explanations of operation. For a good introduction to the DDC112, please refer to the data sheet.

A brief overview of the continuous and non-continuous modes is given first. Then, the state diagram of the state machine controlling the modes is shown and discussed. Timing diagrams follow that illustrate operation in both modes. Finally, some special considerations are explained.

OVERVIEW

The DDC112 is a dual-channel, dual-integrator analog-to-digital converter (ADC). Designed for use with current output sensors such as photodiodes, it integrates the applied current for a user-controlled integration period, T_{INT} . Using a dual-integrator for each channel allows the input signal to be continuously integrated, as will be explained below. When the integration is complete, the outputs of the appropriate integrators are multiplexed to a single, 20-bit voltage ADC which generates the final digital readings. Figure 1 shows a simplified block diagram of the DDC112.

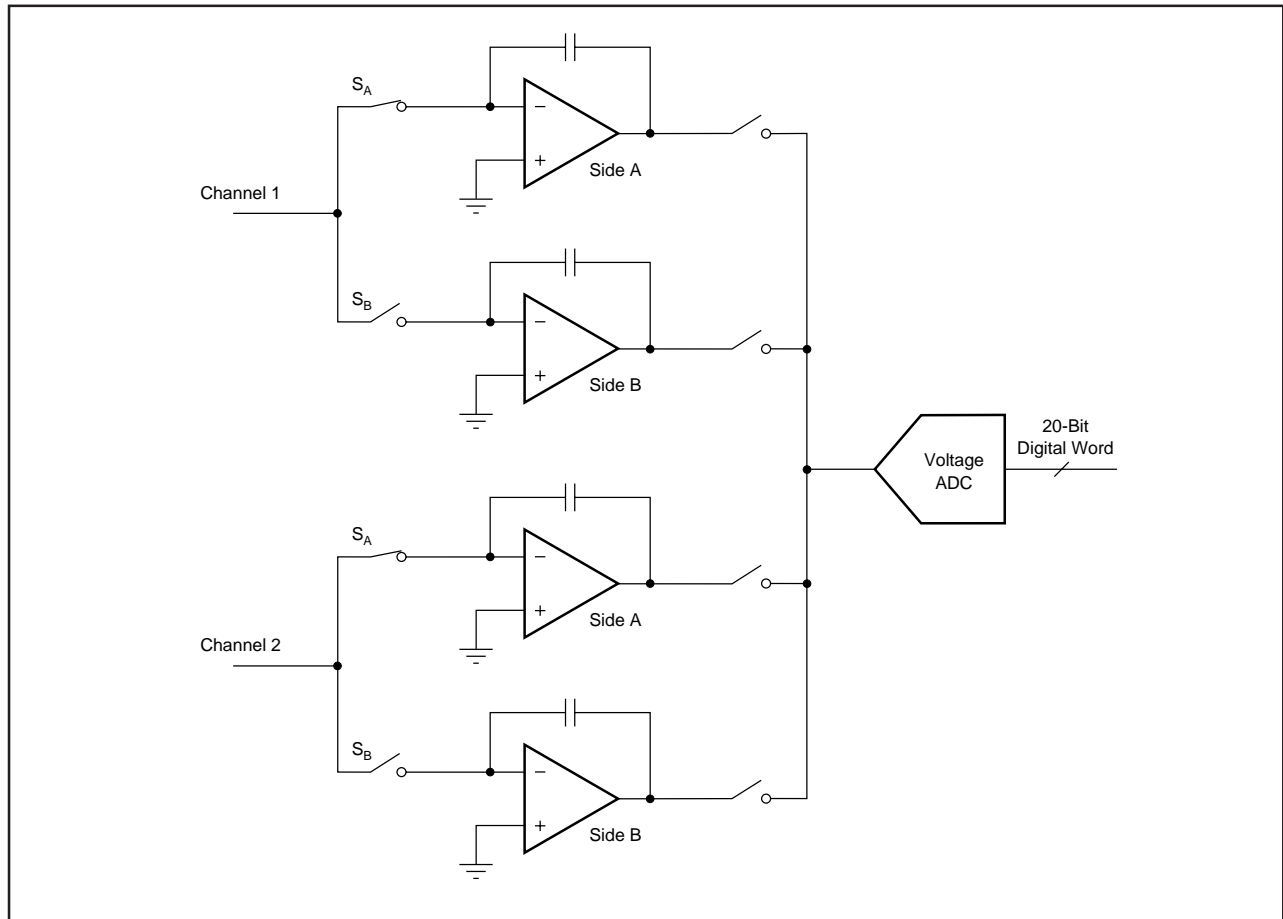


FIGURE 1. DDC112 Block Diagram.

To understand how the dual-integrator allows continuous integration of the input signal, it helps to consider a simple analogy. Imagine a sink with a faucet. You want to measure the water (current from the photosensor) coming out of the faucet. To measure the water you use two cups (integrators), cup “A” and cup “B” (the size of the cups corresponds to the size of the integration capacitors). You put cup A under the faucet and allow it to fill with water for some amount of time (T_{INT}). When the time is up, you pull it out and quickly put cup B in its place. Now, while cup B is collecting the water, you measure the level of water in cup A, then empty it. When it’s time to remove cup B, you switch it with cup A and then measure the level of water in cup B and empty it. This cycle continues on and on as you continuously collect and measure the water.

The above descriptions and analogy are for the DDC112’s continuous mode (“cont” mode). The only requirement to operate in this mode is that the integration time, set by the CONV signal, be long enough to allow the non-integrating side time enough to complete its tasks. These include performing the measurement with the voltage ADC, then resetting and auto-zeroing the integrator. When these are finished, the non-integrating side is ready to begin another integration cycle. (The two integrators in the dual-integrator topology of each channel are referred to as “side A” and “side B”. Side A integrates when CONV is a logic level HIGH while side B integrates when CONV is a logic level LOW.) The data sheet specifies T_{INT} must be $\geq 500\mu s$ for $CLK = 10MHz$. This limit includes a slight margin to allow for jitter in CONV. The actual time needed to measure, reset and auto-zero the integrator is $479.4\mu s$ for $CLK = 10MHz$.

Revisiting the faucet analogy, say cup B is collecting the water while you are measuring cup A. Now if you remove cup B too soon, cup A will not be ready to be placed back under the faucet since it is still being measured. Instead, you will have to set cup B aside, finish measuring cup A, then begin measuring cup B. Once you’re done, you can then put cup A under the faucet and begin collecting the water again. Part of the time neither cup is under the faucet; the water collection is no longer continuous.

For $T_{INT} < 479.4\mu s$ with $CLK = 10MHz$, there is not enough time for the non-integrating side to finish the measurement, reset and auto-zero cycle. Since that side’s integrator is not ready to begin integrating, the input signal should not be switched over to that side when CONV toggles. Instead, the DDC112 enters the non-continuous mode (“ncont” mode) where the input signal is no longer continuously integrated. The DDC112 waits for the measurement, reset and auto-zero

to finish. Once they are done, it again begins integrating the input signal on the appropriate signal from CONV. During the time when neither side of the dual-integrator is integrating the signal, the input of the DDC112 is shorted to ground. This prevents the sensor’s current from charging up the input node. Shorting the sensor to ground isn’t a problem. While the DDC112 is integrating, the sensor is connected to a virtual ground produced by the integrator’s operational amplifier.

Keeping track of the status of the DDC112 during the ncont mode is a little trickier than in the cont mode. The current status of CONV is not sufficient to determine the DDC112’s state. The history of CONV is also needed since the status of the internal operations of measurement, reset and auto-zero isn’t visible to the user. However, just as in the cont mode, the action of the DDC112 is ultimately controlled by CONV. The state diagram described below, as well as the subsequent timing diagrams, will hopefully help in understanding how to generate the proper CONV pattern and thereby operate in the ncont mode

STATE DIAGRAM

The state diagram for the DDC112 is shown in Figure 2. In all, there are 8 states. Table I provides a brief explanation of each of the states.

| STATE | MODE | DESCRIPTION |
|-------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 1 | Ncont | Complete m/r/az of side A, then side B (if previous state is state 4). Initial power-up state when CONV is initially held HIGH. |
| 2 | Ncont | Prepare side A for integration. |
| 3 | Cont | Integrate on side A. |
| 4 | Cont | Integrate on side B; m/r/az on side A. |
| 5 | Cont | Integrate on side A; m/r/az on side B. |
| 6 | Cont | Integrate on side B. |
| 7 | Ncont | Prepare side B for integration. |
| 8 | Ncont | Complete m/r/az of side B, then side A (if previous state is state 5). Initial power-up state when CONV is initially held LOW. |

TABLE I. State Descriptions.

Four signals are used to control progression around the state diagram: CONV and mbsy and their complements. The state machine uses the level as opposed to the edges of CONV to control the progression. mbsy is an internally generated signal not available to the user. It is active whenever a measurement/reset/auto-zero (m/r/az) cycle is in progress.

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During the cont mode, mbsy is not active when CONV toggles. The non-integrating side is always ready to begin integrating when the other side finishes its integration. Consequently, keeping track of the current status of CONV is all that is needed to know the current state. Cont mode operation corresponds to states 3-6. Two of the states, 3 and 6, only perform an integration (no m/r/az cycle).

mbsy becomes important when operating in the ncont mode; states 1, 2, 7, and 8. Whenever CONV is toggled while mbsy is active, the DDC112 will enter or remain in either ncont state 1 (or 8). After mbsy goes inactive, state 2 (or 7) is entered. This state prepares the appropriate side for integration. As mentioned above, in the ncont states, the inputs to the DDC112 are grounded.

One interesting observation from the state diagram is that the integrations always alternate between sides A and B. This relationship holds for any CONV pattern and is independent of the mode. States 2 and 7 insure this relationship during the ncont mode.

When power is first applied to the DDC112, the beginning state is either 1 or 8, depending on the initial level of CONV. For CONV held HIGH at power-up, the beginning state is 1. Conversely, for CONV held LOW at power-up, the beginning state is 8. In general, there is a symmetry in the state

diagram between states 1-8, 2-7, 3-6 and 4-5. Inverting CONV results in the states progressing through their symmetrical match.

TIMING EXAMPLES

Cont Mode

A few timing diagrams will now be discussed to help illustrate the operation of the state machine. These are shown in Figures 3 through 9. Table II gives generalized timing specifications in units of CLK periods. Values in μs for Table II can be easily found for a given CLK. For example, if $\text{CLK} = 10\text{MHz}$, then a CLK period = $0.1\mu\text{s}$. t_1 in Table II would then be $479.4\mu\text{s}$.

| SYMBOL | VALUE (CLK periods) | DESCRIPTION |
|--------|------------------------------------------|------------------------------|
| t_1 | 4794 | Cont mode m/r/az cycle |
| t_2 | 4212 ($t_{\text{INT}} > 4794$) | Cont mode data ready |
| | 4212 ± 3 ($t_{\text{INT}} = 4794$) | |
| t_3 | 4212 ± 3 | 1st ncont mode data ready |
| t_4 | 4548 | 2nd ncont mode data ready |
| t_5 | 9108 | Ncont mode m/r/az cycle |
| t_6 | ≥ 240 | Prepare side for integration |

TABLE II. Timing Specifications Generalized in CLK Periods.

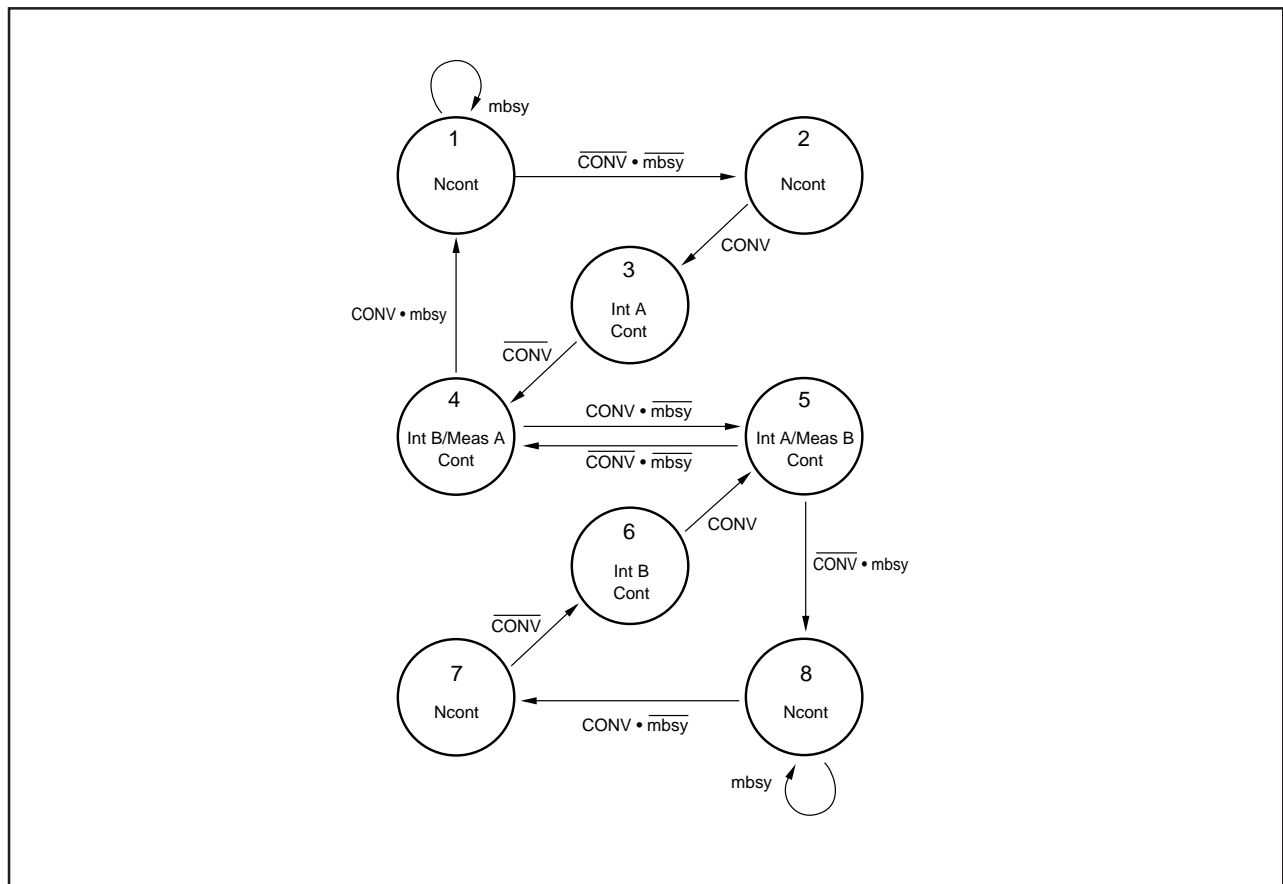


FIGURE 2. State Diagram.

Figure 3 shows a few integration cycles beginning with initial power-up for a cont mode example. The top signal is CONV and is supplied by the user. The next line indicates the current state in the state diagram. The following two traces show when integrations and measurement cycles are underway. The internal signal mbsy is shown next. Finally, DVALID is given. As described in the data sheet, DVALID goes active LOW when data is ready to be retrieved from the DDC112. It stays LOW until DXMIT is taken LOW by the user. In Figure 3 and the following timing diagrams, it is assumed that DXMIT is taken LOW soon after DVALID goes LOW. The text below the DVALID pulse indicates the side of the data and arrows help match the data to the corresponding integration. The signals shown in Figures 3 through 9 are drawn at approximately the same scale.

In Figure 3, the first state is ncont state 1. The DDC112 always powers up in the ncont mode. In this case, the first

state is 1 because CONV is initially HIGH. After the first two states, cont mode operation is reached and the states begin toggling between 4 and 5. From now on, the input is being continuously integrated, either by side A or side B. The time needed for the m/r/az cycle, t_1 , is the same time that determines the boundary between the cont and ncont modes described earlier in the Overview section. DVALID goes LOW after CONV toggles in time t_2 , indicating that data is ready to be retrieved. As shown in Table II, there are two values for t_2 , depending on T_{INT} . The reason for this will be discussed in the last section on special considerations.

Figure 4 shows the result of inverting the logic level of CONV. The only difference is in the first three states. Afterwards, the states toggle between 4 and 5 just as in the previous example.

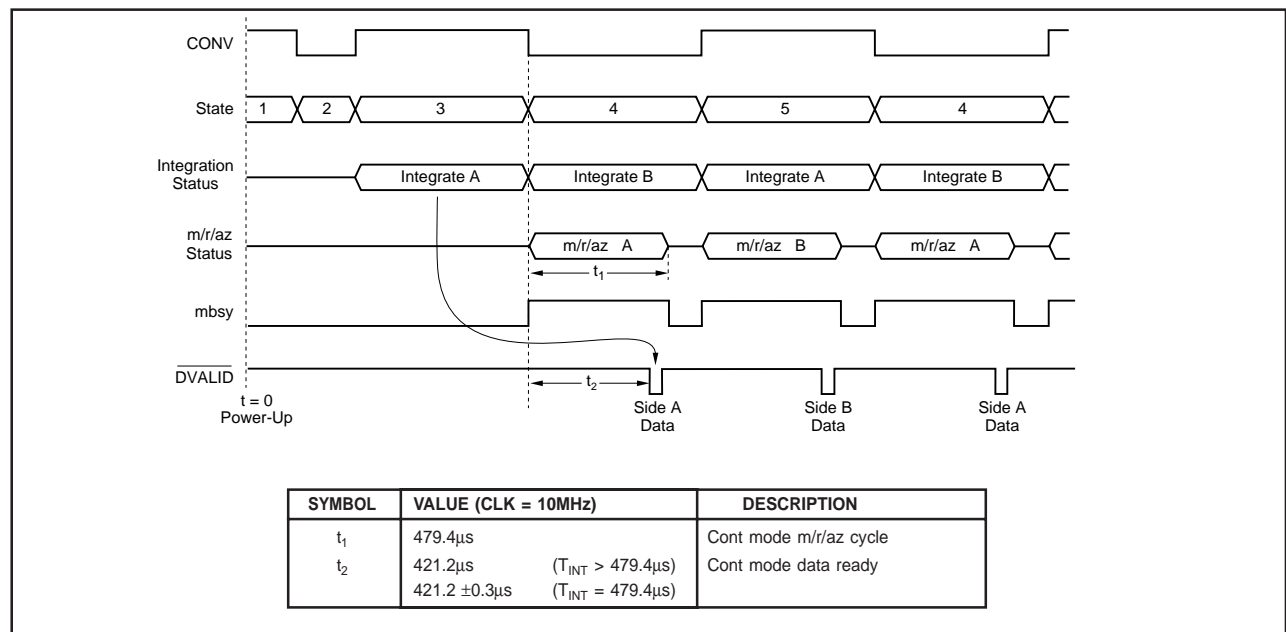


FIGURE 3. Continuous Mode Timing (CONV HIGH at power-up).

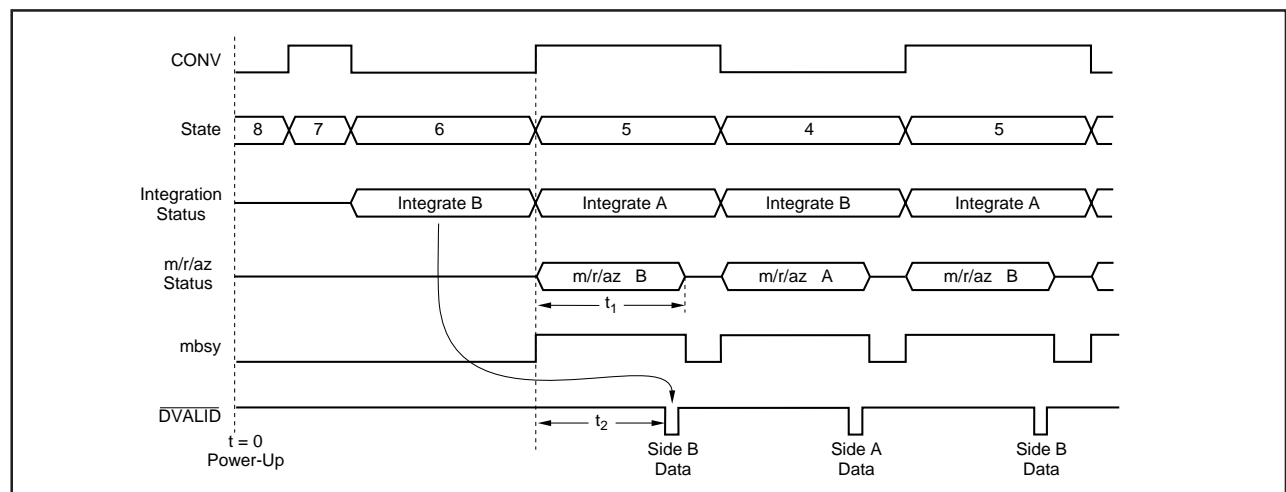


FIGURE 4. Continuous Mode Timing (CONV LOW at power-up).

Ncont Mode

Figure 5 illustrates operation in the ncont mode. The integrations come in pairs (i.e., sides A/B or sides B/A) followed by a time during which no integrations occur. During that time, the previous integrations are being measured, reset and auto-zeroed. Before the DDC112 can advance to states 3 or 6, both sides A and B must be finished with the m/r/az cycle which takes time t_5 . When the m/r/az cycles are completed, time t_6 is needed to prepare the next side for integration. This time is required for the ncont mode because the m/r/az cycle of the ncont mode is slightly different from that of the cont mode. After the first integration ends, \overline{DVALID} goes LOW in time t_3 . This is the same time as in the cont mode. The second data will be ready in time t_4 after the first data is ready.

One result of the naming convention used in this application bulletin is that when the DDC112 is operating in the “ncont mode”, it passes through both “ncont mode states” and “cont mode states”. For example, in Figure 5, the state pattern is 3, 4, 1, 2, 3, 4, 1, 2, 3, 4... where 3 and 4 are cont mode states. “Ncont mode” by definition means that for some portion of the time, neither side A nor B is integrating. States that perform an integration are labeled “cont mode states” while those that do not are called “ncont mode states”. Since integrations are performed in the ncont mode, just not continuously, some cont mode states must be used in a ncont mode state pattern.

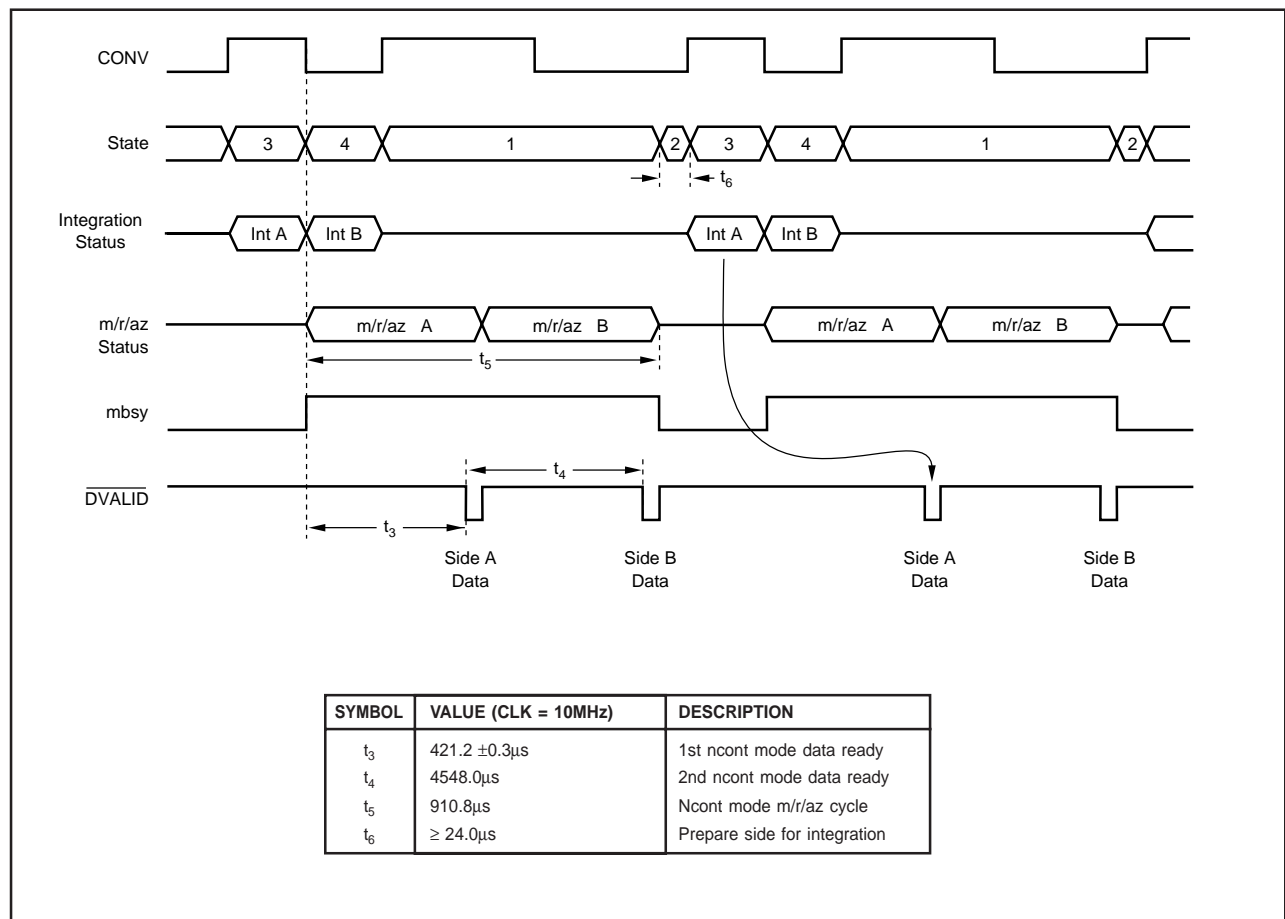


FIGURE 5. Non-Continuous Mode Timing.

Looking at the state diagram, one can see that the CONV pattern needed to generate a given state progression is not unique. Upon entering states 1 or 8, the DDC112 remains in those states until mbsy goes LOW, independent of CONV. As long as the m/r/az cycle is underway, the state machine ignores CONV. Figure 6 illustrates this. The top two signals are different CONV patterns that produce the same state. This feature can be a little confusing at first, but it does allow flexibility in generating ncont mode CONV patterns. For example, the DDC112 Evaluation Fixture operates in the ncont mode by generating a square wave with pulse width $< t_1$. Figure 7 illustrates operation in the ncont mode using a 50 % duty cycle CONV signal with $T_{INT} = 1620$

CLK periods. Care must be exercised when using a square wave to generate CONV. There are certain integration times that must be avoided since they produce very short intervals for state 2 (or state 7 if CONV is inverted). As seen in the state diagram, the state progresses from 2 to 3 as soon as CONV is HIGH. The state machine does not insure that the duration of state 2 is long enough to properly prepare the next side for integration (t_6 in Table II). This must be done by the user with proper timing of CONV. For example, if CONV is a square wave with $T_{INT} = 3042$ CLK periods, state 2 will only be 18 CLK periods long, therefore, t_6 will not be met.

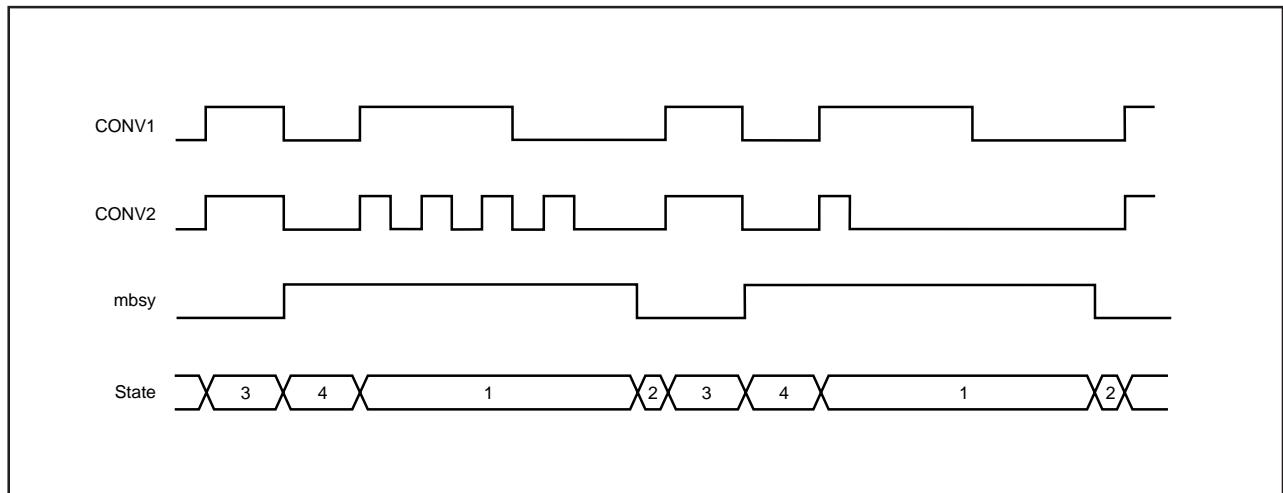


FIGURE 6. Equivalent CONV Signals in Non-Continuous Mode.

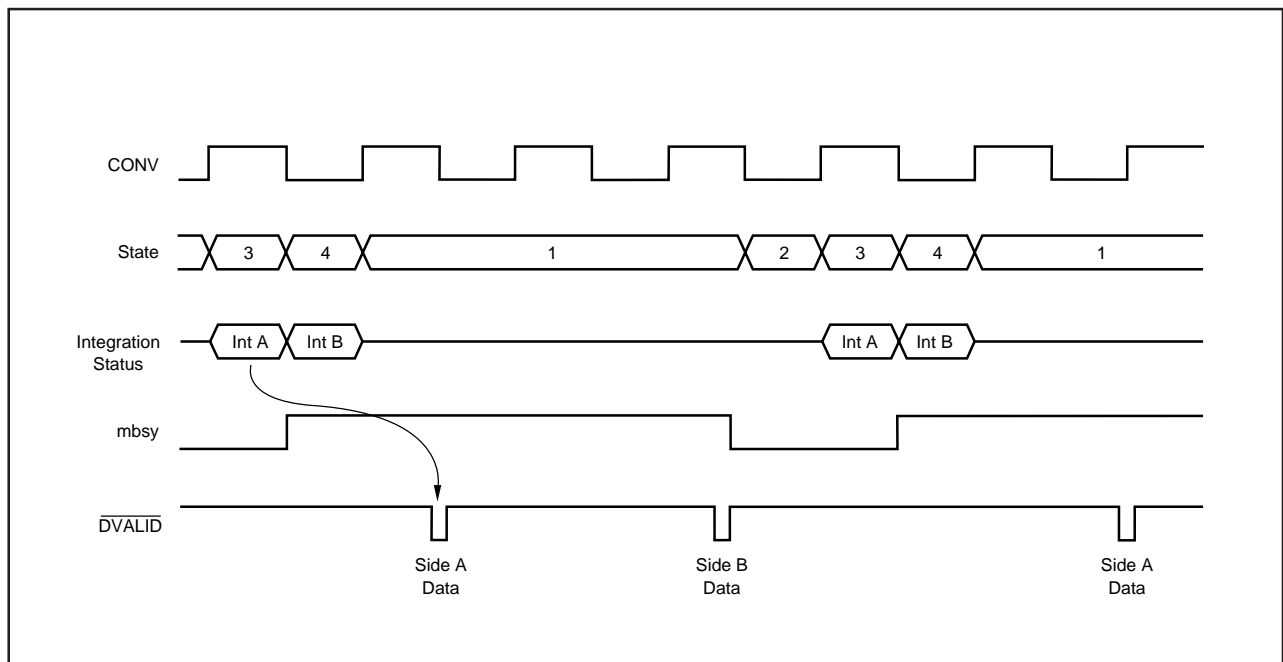


FIGURE 7. Non-Continuous Mode Timing with a 50% Duty Cycle CONV Signal.

Changing Between Modes

Changing from the cont to ncont mode occurs whenever $T_{INT} < t_1$. Figure 8 shows an example of this transition. In this figure, the cont mode is entered when the integration on side A is completed before the m/r/az cycle on side B is complete. The DDC112 completes the measurement on sides B and A during states 8 and 7 with the input signal shorted to ground. Ncont integration begins with state 6.

Changing from the ncont to cont mode occurs when T_{INT} is increased so that T_{INT} is always $\geq t_1$. Figure 9 illustrates this transition. With a longer T_{INT} , the m/r/az cycle has enough time to finish before the next integration begins and continuous integration of the input signal is possible. For the special case of the very first integration when changing to the cont mode, T_{INT} can be $< t_1$. This is allowed because there is no simultaneous m/r/az cycle on the side B during state 3—there is no need to wait for it to finish before ending the integration on side A.

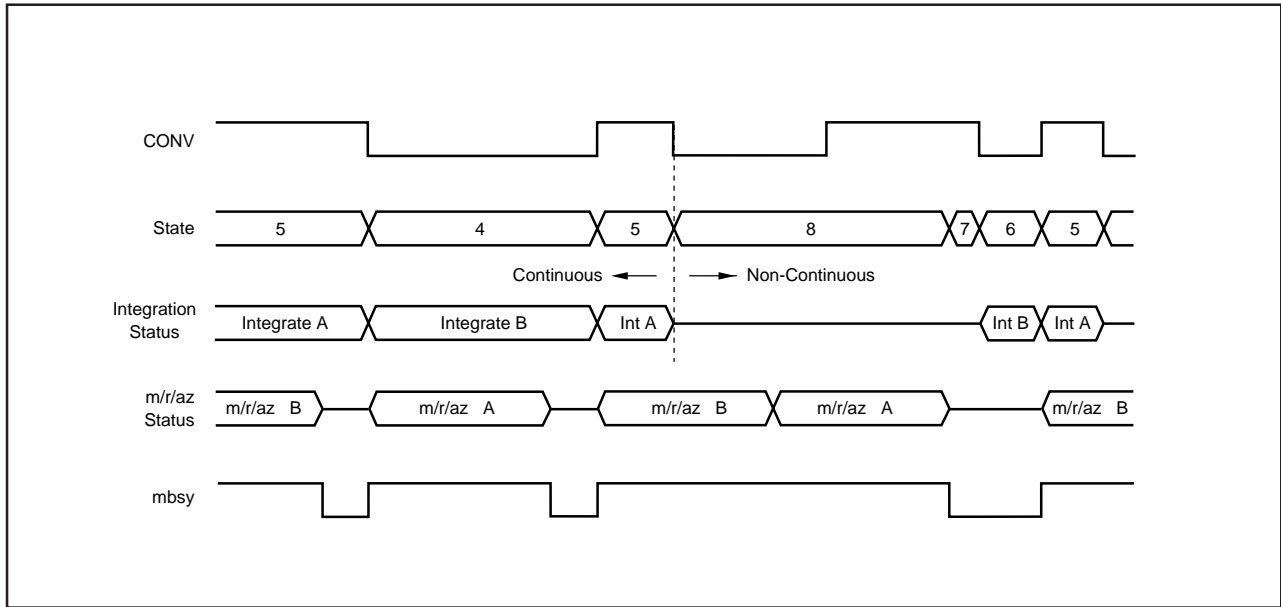


FIGURE 8. Changing from Continuous Mode to Non-Continuous Mode.

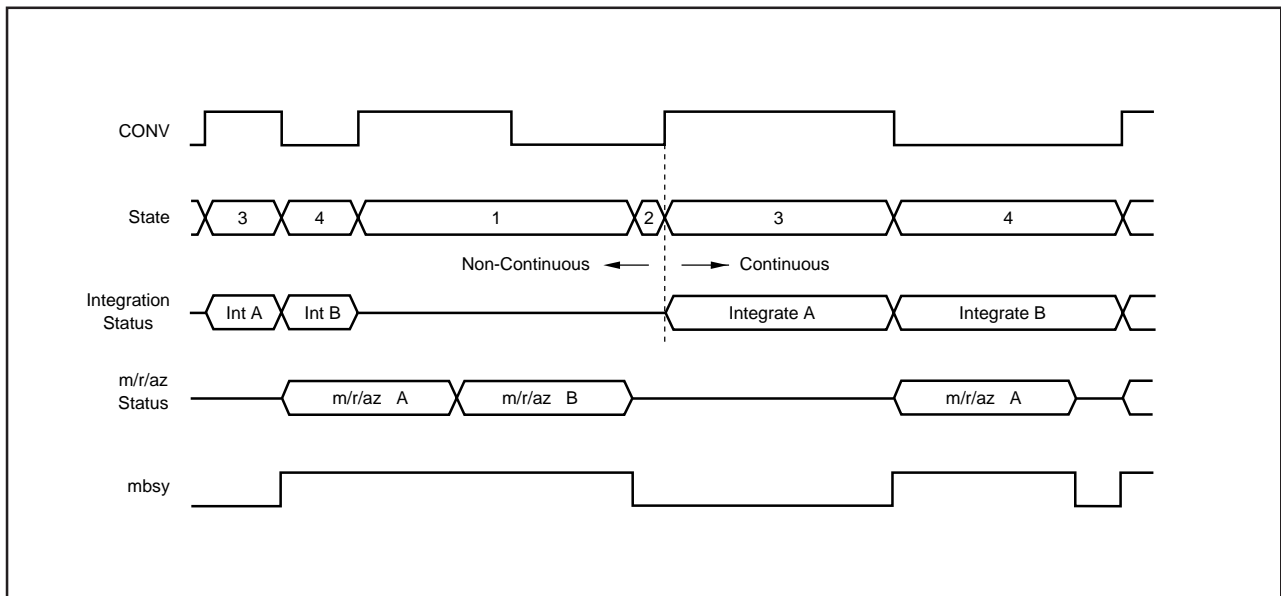


FIGURE 9. Changing from Non-Continuous Mode to Continuous Mode.

SPECIAL CONSIDERATIONS

NCONT MODE INTEGRATION TIME

The DDC112 uses a relatively fast clock. For $CLK = 10\text{MHz}$, this allows T_{INT} to be adjusted in steps of 100ns since CONV should be synchronized to CLK. However, for the internal measurement, reset and auto-zero operations, a slower clock is more efficient. The DDC112 divides CLK by six and uses this slower clock with a period of 600ns to run the m/r/az cycle and data ready logic.

Because of the divider, it is possible for the integration time to be a non-integer number of slow clock periods. For example, if $T_{INT} = 5000\text{ CLK periods}$ ($500\mu\text{s}$ for $CLK = 10\text{MHz}$), there will be $833\frac{1}{3}$ slow clocks in an integration period. This non-integer relationship between T_{INT} and the slow clock period causes the number of rising and falling slow clock edges within an integration period to change from integration to integration. The digital coupling of these edges to the integrators will in turn change from integration to integration which produces noise. The change in the clock edges is not random, but will repeat every 3 integrations. The coupling noise on the integrators appears as a tone with a frequency equal to the rate at which the coupling repeats.

To avoid this problem in cont mode, the internal slow clock is shut down after the m/r/az cycle is complete when it is no longer needed. It starts up again just after the next integration begins. Since the slow clock is always off when CONV toggles, the same number of slow clock edges fall within an integration period regardless of its length. Therefore, $T_{INT} \geq 4794\text{ CLK periods}$ will not produce the coupling problem described above.

For the ncont mode however, the slow clock must always be left running. The m/r/az cycle is not completed before an integration ends. It is then possible to have digital coupling to the integrators. The digital coupling noise depends heavily

on the layout of the printed circuit board used for the DDC112. For solid grounds and power supplies with good bypassing, it is possible to greatly reduce the coupling. However, for guaranteeing the best performance in the ncont mode, the integration time should be chosen to be an integer multiple of $1/(2f_{\text{SLOWCLOCK}})$. For $CLK = 10\text{MHz}$, the integration time should be an integer multiple of 300ns. $T_{INT} = 100\mu\text{s}$ is not—a better choice would be $T_{INT} = 99\mu\text{s}$.

DATA READY

The \overline{DVALID} signal which indicates that data is ready is generated using the internal slow clock. The phase relationship between this clock and CLK is set when power is first applied and is random. Since CONV is synchronized with CLK, it will have a random phase relationship with respect to the slow clock. When $T_{INT} > t_1$, the slow clock will temporarily shut down as described above. This shutdown process synchronizes the internal clock with CONV so that the time between when CONV toggles to when \overline{DVALID} goes LOW (t_2 and t_3 in Table II) is fixed.

For $T_{INT} \leq t_1$, the internal slow clock, is not allowed to shut down and the synchronization never occurs. Therefore, the time between CONV toggling and \overline{DVALID} indicating data is ready has uncertainty due to the random phase relationship between CONV and the slow clock. This variation is $\pm 1/(2f_{\text{SLOWCLOCK}})$ or $\pm 3/f_{\text{CLK}}$. The timing to the second \overline{DVALID} in the ncont mode will not have a variation since it is triggered off the first data ready (t_4 in Table II) and both are derived from the slow clock.

Polling \overline{DVALID} to determine when data is ready eliminates any concern about the variation in timing since the readback is automatically adjusted as needed. If the data readback is triggered off the toggling of CONV directly (instead of polling), then waiting the maximum value of t_2 or t_3 insures that data will always be ready before readback occurs.

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