Application Report
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RF Sampling ADC With 800 MHz of IBW LTE

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ABSTRACT

This document describes a candidate device, ADC32RFx5, for the next generation (5G) cellular system that shows a total of 800 MHz of Instantaneous Bandwidth (IBW) using Long Term Evolution (LTE) patterns (40 of LTE 20 MHz) processed from Matlab after being captured from TSW14J56 evaluation module out of ADC32RFx5.

There are many of key technologies to help the air interface of 5G deployed in the near future such as enhanced data rate, reduced latency, increased frequency bands with a ultra-wide bandwidth. Massive MIMO (Multi-Input Multi-Output) will give us improved spectral efficiency for multi mobile users within cell, and hybrid beamforming will increase cell coverage for multi users. But, those architectures will increase hardware complexity and power consumption of the system while requiring large number of power-hungry converters. At the same time, massive connectivity for uplink (UL) also should be supported with scalable data rates for 5G system. To show much better spectral efficiency, 800 MHz of IBW is fed into ADC32RFx5 which is a direct RF sampling analog to digital converter (ADC).

Another aspect of 5G is the specification of future waveform which is still under discussion. Orthogonal frequency division multiplexing (OFDM) has been a waveform for 4G system so far but the potential waveform of physical layer for 5G is not defined yet. There are some candidates to be deployed in 5G system in the future, which are filter bank multi carrier (FBMC), universal filtered multi carrier (UFMC), generalized frequency division multiplexing (GFDM) and filtered OFDM (f-OFDM). These kinds of future waveform will handle higher data rate with wider bandwidth than LTE pattern, and also have different filtering and windowing from 4G standards.

The ADC32RFx5 is a family of high performance dual channel 14-bit, 3-Gsps RF ADCs, capable of having input frequencies up to 2.5 GHz and beyond. Designed for high signal-to-noise ratio (SNR), the ADC32RFx5 delivers a noise floor of –155 dBFS/Hz. Together with its exceptional spurious free dynamic range (SFDR) performance, this device can cover even the toughest receiver requirements such as multi-carrier GSM and 5G receiver in the future.

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1 Theory of Operation

The family of ADC32RFx5 is a dual-channel 14-bit analog to digital converter (ADC) and provides 3 Gsps of ADC sample rate. This device has a total of 8 lane JESD204B interfaces, 4-lane per ADC, with a maximum input bit rate of 12.3 Gbps. ADC32RFx5 supports JESD204B subclass 1 for multi-chip synchronization by using SYSREF. Up to 32 of decimation function enables system designers to receive minimum 93.75 Msps of baseband rate to FPGA, and four independent Numerically Controlled Oscillator (NCO) supports 4 different frequency bands from one ADC32RFx5 device.

Each of ADC channels is internally connected two dual band digital down converters (DDC) and independent 16-bit numerically controlled oscillator (NCO). The DDC block in ADC32RFx5 can also be bypassed to achieve the maximum Nyquist bandwidth, which supports more than 1GHz of IBW for the next generation (5G) cellular system.

The ADC32RFx5 provides on-chip DDC block that can be controlled with serial-to-parallel interface (SPI) register settings and the GPIO pins. The DDC block supports 2 basic operating modes – receiver (RX) with single or dual band DDC or wide bandwidth observation receiver. Each of ADC channels is followed by two DDC chains consisting of the decimation filter along with 16-bit NCO, and the output to FPGA can be real or complex format.

In this document, 800MHz (40xLTE20MHz) of IBW from DAC38RF8xEVM is fed into the input of ADC32RFx5EVM. The application report *RF Sampling DAC with 800 MHz of LTE IBW* (SLAA709) describes the profile of test pattern, operation of DAC38RF8x and evaluated performance from the board.

1.1 The Profile of Test Pattern for the Input of ADC32RFx5EVM

The 200MHz of IBW LTE pattern was created by combining 10 of LTE TM3.1 20MHz carriers and each of LTE 20MHz carriers was generated with different Cell ID to avoid peak regrowth. Figure 1 shows 9.75dB of peak-to-average ratio (PAR) of 200MHz IBW at 0.01% from complementary cumulative distribution function (CCDF) curve. In general, LTE single carrier shows around 9.7dB of PAR at 0.01% of CCDF without crest factor reduction (CFR) processing. Considering the average PAR of LTE single carrier, 200MHz of LTE pattern mentioned in this document does not have peak regrowth from multi-carrier generation.

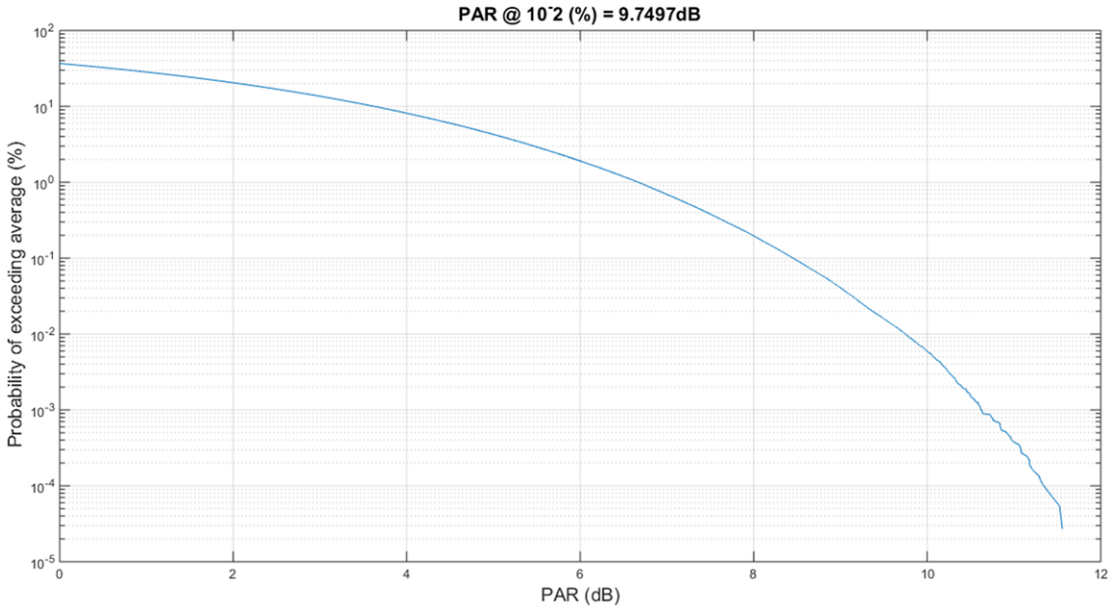

Figure 1. 9.75dB of PAR at 0.01% from CCDF Curve

DAC38RF8x has four Serializer/Deserializer (SerDes) I/Q lane pairs per DAC channel, which is 8 configurable JESD204B serial lanes shown as below in Figure 5. The highest speed of each SerDes lane is 12.5Gbps. The generated 200MHz of LTE pattern is fed into four SerDes interface shown as Figure 2, and then combined into 800MHz of LTE IBW.

Theoretically, we can expect peak regrowth by 6dB as the phase of four LTE 200MHz is overlapped. Therefore, the PAR of 800MHz pattern into ADC32RFx5EVM would be around 15.75dB (= 9.75dB + 6dB) at 0.01%.

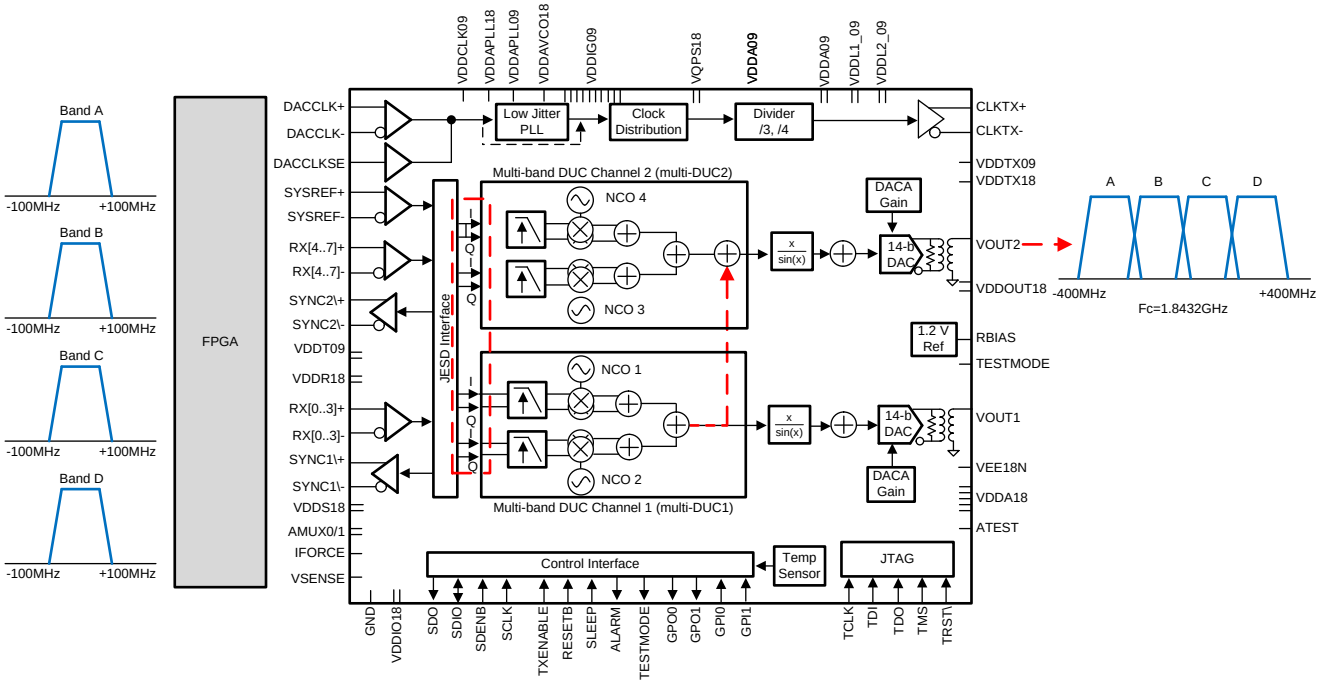

Figure 2. Block Diagram of DAC38RF8xEVM Operation

By using crest factor reduction (CFR), peak-to-average power ratio (PAR) can be reduced and this technique contributes the increased RMS output power by the amount of peak reduction. With the same scenario, the output power from DAC38RF8xEVM can be increased and this will also give us an increased input power to the input of ADC32RFx5EVM. As mentioned earlier in this document, the waveform specification for 5G is still under discussion and the 800MHz of LTE pattern is just a reference waveform to show the capability of RF sampling devices such as ADC32RFx5 and DAC38RF8x to handle such a wide signal bandwidth.

Figure 3 shows 800MHz of LTE patterns captured from spectrum analyzer. The center frequency out of DAC38RF8xEVM is 1843.2MHz and this will give us 614.4MHz located image of 800MHz IBW after ADC sampling process from ADC32RFx5EVM. As the sampling frequency (Fs) of ADC32RFx5 is 2457.6MHz, the choice of 1843.2MHz (= 3 x Fs/4) of input frequency makes it easier for real-to-complex baseband processing compared to other input frequencies. This digital quadrature demodulation (DQDM) process does not require any multiplier logic implementation from the demodulation process in FPGA or ASIC.

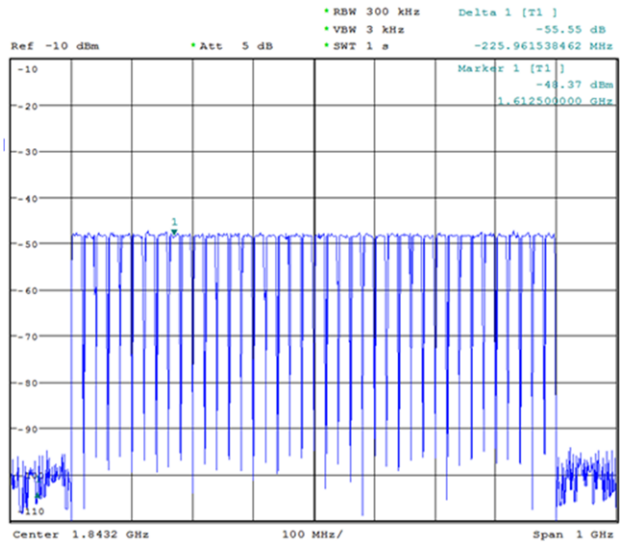

Figure 3. 800MHz of IBW at 1.8432GHz captured from Spectrum Analyzer

1.2 Operation of ADC32RFx5

ADC32RFx5 has 4 SerDes I/Q lanes per ADC channel, which is 8 configurable JESD204B serial lanes shown as below in Figure 6. The highest speed of each SerDes lane is 12.3Gbps and JESD204B Subclass 1 is supported to achieve multi-chip synchronization by using external SYSREF clock. Each of ADC channel is followed by two dual band digital-down-converters (DDC) chains consisting of the digital filter along with 16-bit of numerically controlled oscillator (NCO).

ADC32RFx5EVM has onboard LMK04828 (Ultra low noise JESD204B compliant clock jitter cleaner with dual loop PLL) for JESD204B clock and SYSREF generation and also onboard LMX2582 (High performance wide band PLL synthesizer) for the sampling clock of ADC32RFx5.

1.2.1 Configuration of ADC32RFx5 for DDC Bypass

Table 1 describes configuration parameters of ADC32RFx5 for this application. As digital down-converter (DDC) is bypassed, 4 NCO blocks along with decimators in ADC32RFx5 are disabled so current consumption of this device will be minimized and at the same time maximum of Nyquist bandwidth can be achieved.

The suggested setting for DDC bypass mode is 82820 of LMFS JESD204B parameters and 12-bit of output resolution. With this configuration, the maximum sampling clock speed is guaranteed to support more than 1GHz of IBW pattern.

Table 1. Example of ADC32RFx5 Configuration Parameters

PARAMETERS	VALUE	UNIT
ADC Clock Frequency	2457.6	MHz
Baseband Output Rate	2457.6	MHz
# of ADC	Dual	ADC
# of I/Q Pairs per ADC	2	I/Q Pair
# of SerDes Lanes per ADC	4	Lane
Decimation Factor	1	/
Target Input Frequency	1843.2	MHz
NCO Frequency Path AB for ADCA	0	MHz
NCO Frequency Path CD for ADCA	0	MHz
NCO Frequency Path AB for ADCA	0	MHz
NCO Frequency Path CD for ADCB	0	MHz
JESD204B Frame Format for "LMFS"	82820	

- L: Number of lanes per converter device
- M: Number of converters per device
- F: Number of octets per frame
- S: Number of samples per converter per frame cycle

1.2.2 Hardware Setup for the evaluation of ADC32RFx5EVM

Figure 4 describes the block diagram to evaluate ADC32RFx5. The output pattern of DAC38RF8xEVM is directly fed into the input port of ADC32RFx5EVM through the external RF cable. The application report (SLAA709) describes the architecture to transmit 800MHz of IBW. The RF output frequency of DAC38RF8xEVM is 1843.2MHz and 800MHz of In-phase and Quadrature-phase (I/Q) patterns can be captured from TSW14J56 through HSDC Pro which is software tool to transmit & capture test patterns.

In this application, ADC32RFx5 is configured as real architecture for the DDC bypass mode and therefore 2457.6MHz of sampling clock gives us DC-to-1228.8MHz of 1st Nyquist bandwidth. The RF input frequency of ADC32RFx5 is 1843.2MHz and the 800MHz of IBW is located in the 2nd Nyquist zone. From the nature of ADC sampling process, the target pattern is mirrored into 1st Nyquist area, which is located 614.4MHz.

The sampled I/Q data out of ADC32RFx5EVM is transferred to TSW14J56 through FPGA Mezzanine Card (FMC) connecter, which follows the ANSI/VITA standard. The received I/Q samples can be stored into the external onboard 1GB of SDRAM on TSW14J56 for the signal analysis and HSDC Pro display the received pattern in frequency domain shown as Figure 5. The high speed data converter pro (HSDC Pro) GUI is a PC program designed to aid in evaluation of most TI high speed data converter and AFE platforms, which is designed to support the entire TSW14xx series of data capture and pattern generation cards.

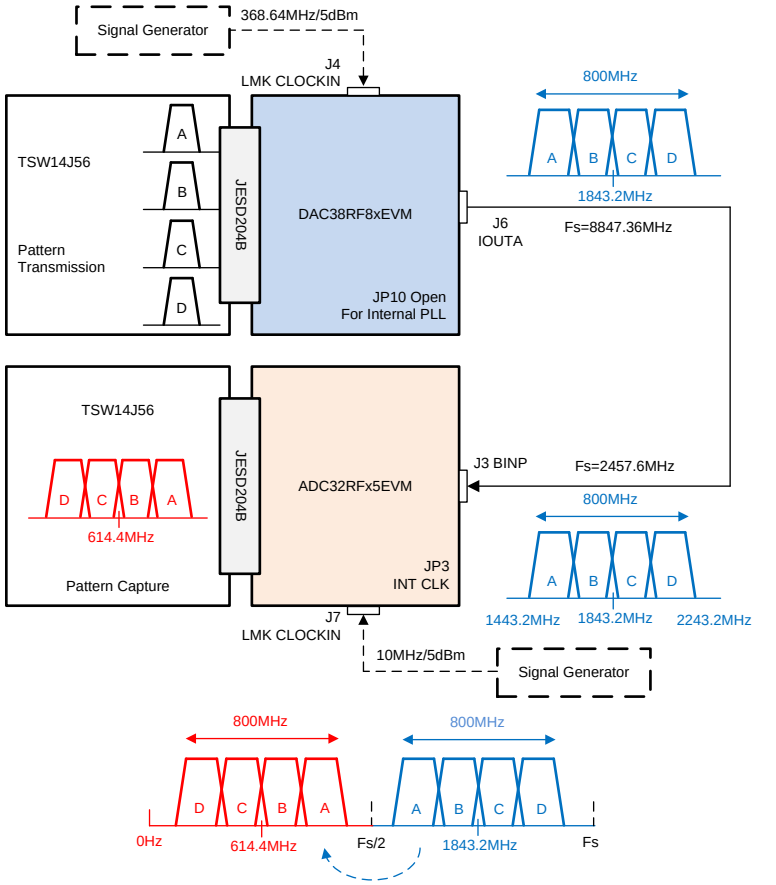

Figure 4. Hardware Setup for ADC32RFx5EVM

1.2.3 Captured 800MHz LTE pattern from HSDC Pro

Figure 5 shows the captured 800MHz of IBW from HSDC Pro. The channel power shows -21dBFS over 800MHz shown as below. From the RF DAC application note (SLAA709), each of 200MHz pattern has 9.74dB of PAR and the same four 200MHz patterns are combined to create 800MHz of IBW. During this combining process, each phase of four carriers are overlapped and this cause 15.74dB of increased PAR by 6dB (= 10 x log10(4)). Therefore the headroom of input pattern is 5.26dB (= 15.74-(-21dBFS)), which means the RMS input power to ADC32RFx5 can be boosted by 5.26dB.

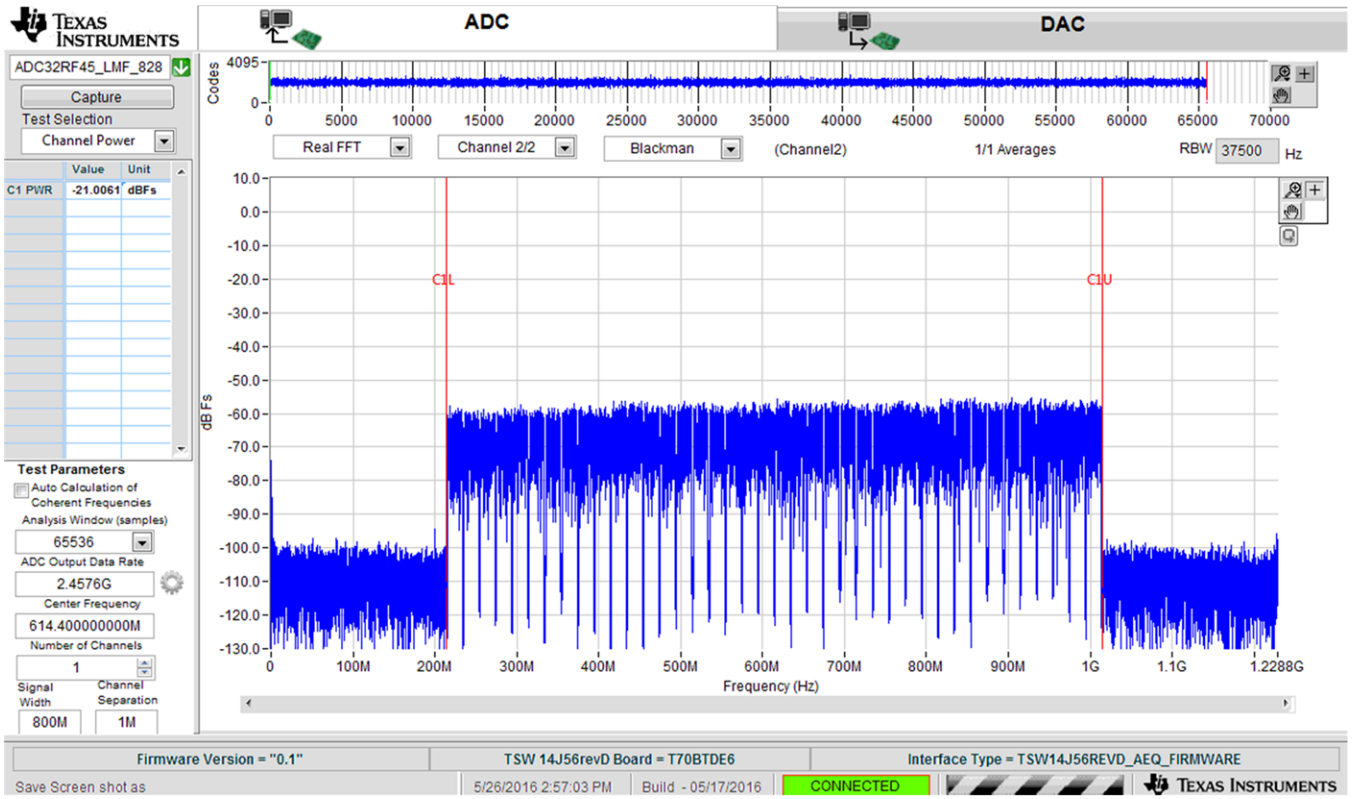

Figure 5. 800MHz of IBW captured from HSDC Pro

The captured 800MHz LTE pattern is located at 614.4MHz shown as Figure 5 and this is mirrored one from the RF input located at 1843.2MHz in 2nd Nyquist zone.

Figure 6 describes an example of direct sampling processing from ADC32RFx4 from the view point of customer FPGA. As the output of ADC32RFx5 is still 614.4MHz located intermediate frequency (IF) in analog domain, customer will require some digital processes to down-convert the intermediate frequency (IF) to baseband and convert real-to-complex I/Q patterns. As section 2.1 in this document mentions the benefit from using digital quadrature demodulation (DQDM), the processing in FPGA for signal demodulation requires just adder and subtract logic blocks which is quite simple.

After demodulating 800MHz pattern located at 614.4MHz, the original 800MHz RF input at 1843.2MHz shall be relocated to 1228.8MHz and this can be filtered out in FPGA.

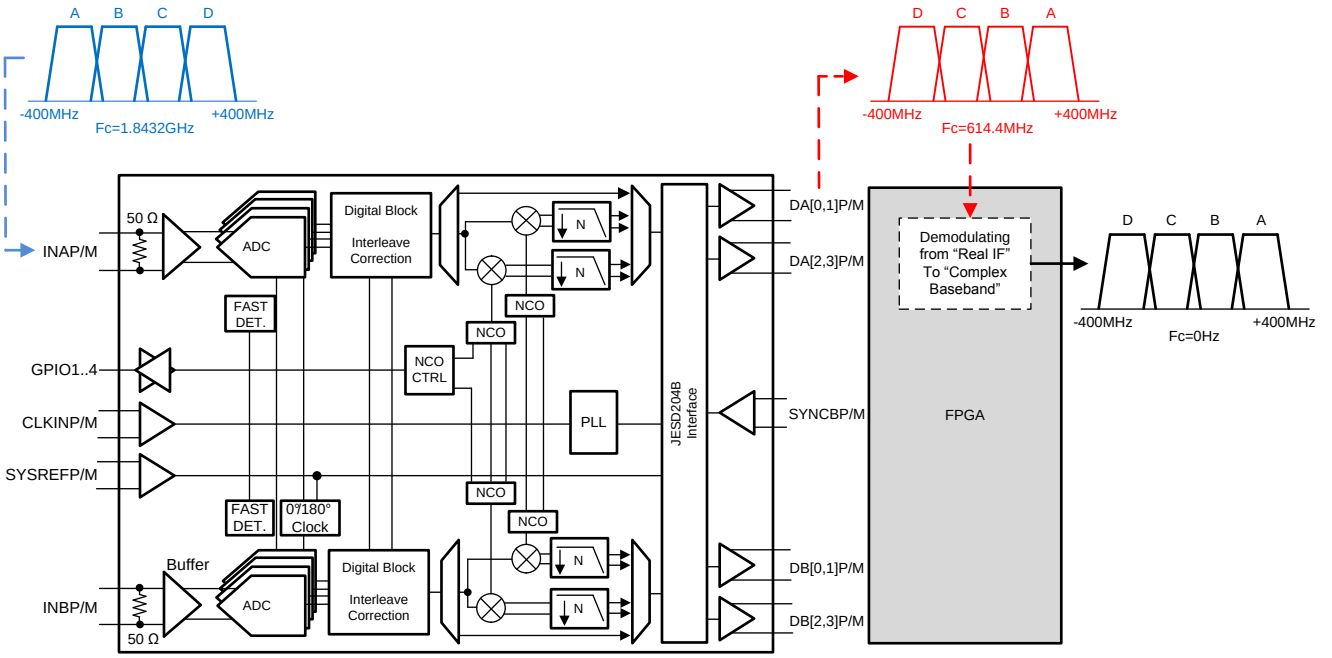

Figure 6. Example of Commercial Application Diagram

2 Performance Evaluated from ADC32RFx5EVM

With the captured 800MHz of IBW pattern from TSW14J56 evaluation module, digital quadrature demodulation (DQDM) and real-to-complex processes were applied to this pattern through MATLAB. The same behavioral function processed from Matlab shall be implemented in FPGA of commercial system before delivering this baseband pattern to modem block. Figure 7 shows 800MHz of complex baseband pattern which has -614.4MHz to +614.4MHz of complex Nyquist bandwidth after MATLAB process. The captured 800MHz pattern out of ADC32RFx5 shows the same level of spectral flatness to the output pattern of DAC38RF8xEVM.

Not only digital down-converter (DDC) bypass mode but ADC32RFx5 digitizes analog signals to digital samples with down-conversion of RF input signal using DDC so there is no need of quadrature demodulation correction to restore signal quality. Quadrature mismatch is caused by analog path because analog domain always includes imperfection of phase, offset and gain component between In-phase and Quadrature-phase (I/Q) path. TI's RF sampling DAC and ADC do not require quadrature mismatch correction because modulation process is achieved by using digital up/down conversion within device. This is another benefit from using RF sampling devices along with GHz-Nyquist-bandwidth to support the next generation (5G) cellular system.

In this document, digital down-converter (DDC) bypass mode was used for this application and this is equivalent to /1 of decimation factor of DDC. Other than DDC bypass mode, ADC32RFx5 has up to 32 of decimation factors along with 4 independent 16-bit of numerically controlled oscillator (NCO) and these features enable system designers to deploy multi-band receiver architecture using one ADC32RF4x device.

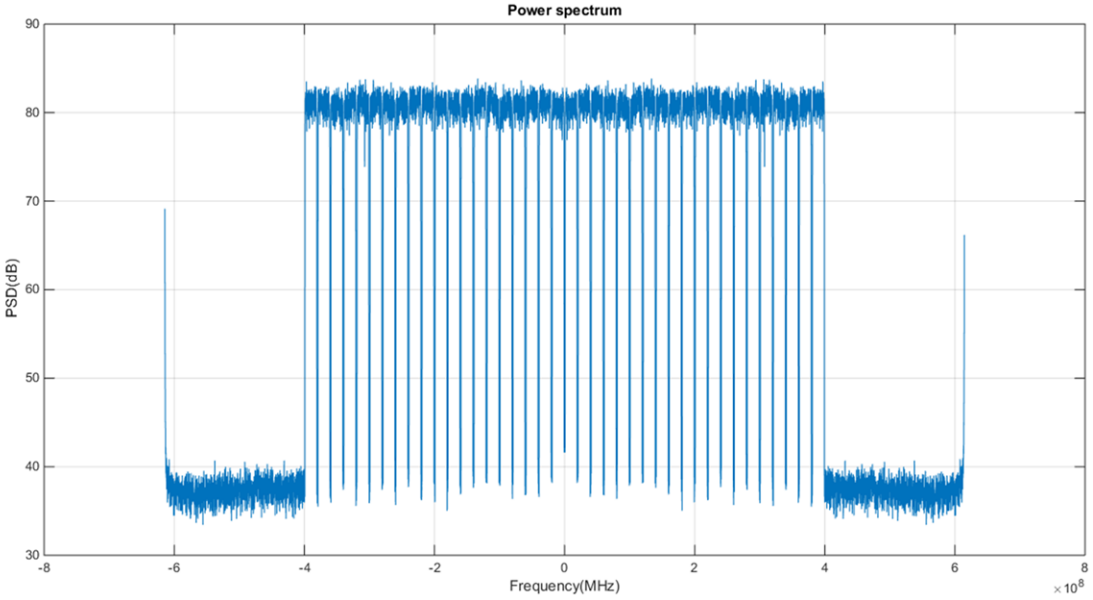

Figure 7. Demodulated 800MHz Pattern with Real-to-Complex from MATLAB

The benefit from using DDC bypass mode of ADC32RFx5 gives system designers to implement the next generation (5G) cellular system to handle more than 1GHz of IBW pattern. 800MHz of LTE pattern was demonstrated from ADC32RFx5EVM together with the capability of 800MHz pattern generation from DAC38RF8xEVM.

References

Solutions for Design and Evaluation of 5G Candidate Waveforms from Keysight Technologies

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