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ABSTRACT

This document describes and discusses the topic of CMOS Latch-Up ranging from theory to testing of products. The recently proposed modifications to JEDEC standard JESD78 are discussed along with progress for making it more analog friendly with respect to special pin functions and/or high voltage requirements.

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1 ⁽¹⁾ Introduction

Latch-Up today is still a potentially potent source of failure in the qualification flow at manufacturers and in the customer application. As IC's get smaller, so do the dimensions between transistors within an IC. Transistor spacing can create conditions for Latch-Up. Texas Instruments is influencing the industry to consider more complete methods to stress Latch-Up in all products but in particular, analog products. The goal at Texas Instruments is to continuously improve the quality and reliability of the products.

1.1 What is Latch-Up?

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path. CMOS and BiCMOS circuits use NMOS and PMOS transistors to create the circuit functions. In the design of the CMOS integrated circuit, the proximity of the PN junctions that form the NMOS and PMOS transistors create inherent parasitic transistors and diodes. These parasitic structures create PNP Thyristors, also called silicon-controlled rectifiers (SCRs). Excursions (overshoots and undershoots) outside the normal operating voltage and current levels can trigger PNP Thyristors and may cause Latch-Up. Latch-Up is not a risk if the voltage and current levels applied to the device adhere to the absolute maximum ratings.

1.2 Latch-Up Model

Early in CMOS development, Latch-Up was recognized as a problem to be solved. Research and development into the causes led to several papers in the 1980's discussing causes and methods to lessen the influence of Latch-Up. The NMOS and PMOS circuits form parasitic PNP structures that can be triggered when a current or voltage impulse is directed into an input, output or power supply.

[Figure 1](#) shows a typical, simple, cross-section of a CMOS inverter in an N-Well, P- substrate, CMOS process. The PMOS forms a parasitic vertical PNP from the P+ source/drain of the transistor (emitter), the N-Well (base) and the substrate (collector). A lateral NPN is formed from the N+ source/drain (emitter), P-substrate (base) and the N-Well (collector). The resultant circuit describes a PNP (as shown in [Figure 2](#)).

As an example, if a current impulse strikes the PMOS drain, the P+ / N-Well junction (Q1) becomes forward biased. If the impulse is high enough (sustainable for a sufficient length of time), the carriers injected into the substrate cause a voltage drop across the substrate resistance. The bias across the P- / N+ (substrate to NMOS drain) in Q2 is then high enough to turn-on Q2. The Q2 collector current will then flow into the base of Q1. At that time, the Latch-Up becomes self-sustaining, a positive feedback loop has been formed. Only cessation of the power supply can stop the Latch-Up condition.

Temperature effects (external and internal to the product) can also influence the Latch-Up immunity of products. As temperature increases, the substrate and well resistances rise allowing the bias to reach a critical value sooner. Also, the effective distance between the N+, P+ and N-Well diffusions narrows allowing easier capture of excited carriers.

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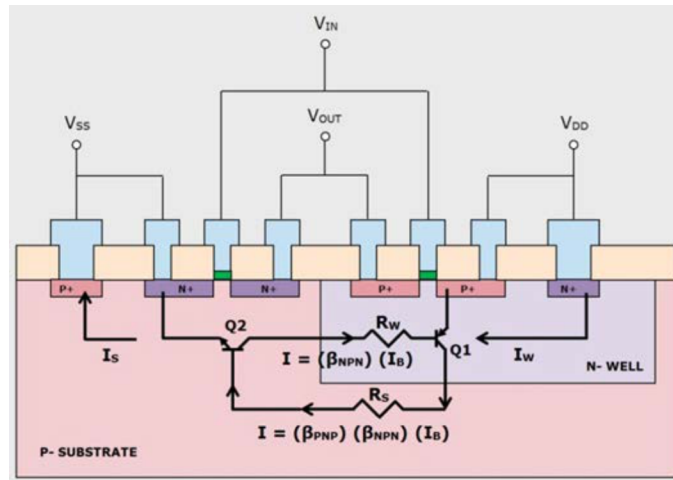


Figure 1. Cross-Section of a CMOS Inverter

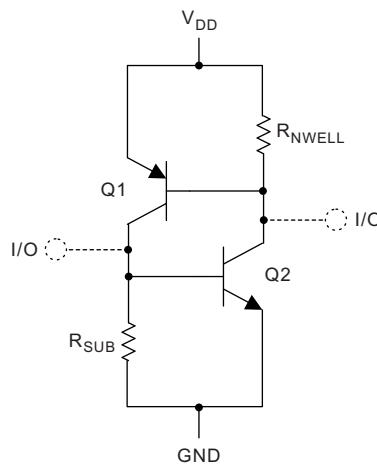


Figure 2. Lateral NPN

1.3 Mitigating Latch-Up

There are methods employed to reduce the possible onset of Latch-Up. Spacing of the elements of each transistor, diode, resistor and capacitor are now being controlled through process characterization and design rules to help minimize the effect of current or voltage pulses on the products. Additionally, guard rings have been added around known radiators in the circuits or if spacing concerns are critical around individual PMOS and NMOS transistors, diodes or substrate resistors. Guard rings act as injected carrier syphons allowing these carriers to flow to the supply or ground. Also, the use of substrate ties and well taps act as excited carrier syphons and are guided by design rules for placement. These ties and taps are necessary for Latch-Up immunity. Another very effective method of quenching Latch-Up is to use an EPI (epitaxial silicon) layer. The EPI layer is doped appropriately for the best transistor performance (more lightly doped than the remaining lower portion of the substrate that is highly doped). The highly doped substrate directs majority carriers to ground and reflects minority carriers making the guard rings more effective (see Figure 3). Even with these safeguards, there is a possibility of parasitic transistors in circuits that are not identified. These unidentified Latch-Up sources need to be identified; one way is a Latch-Up stress test.

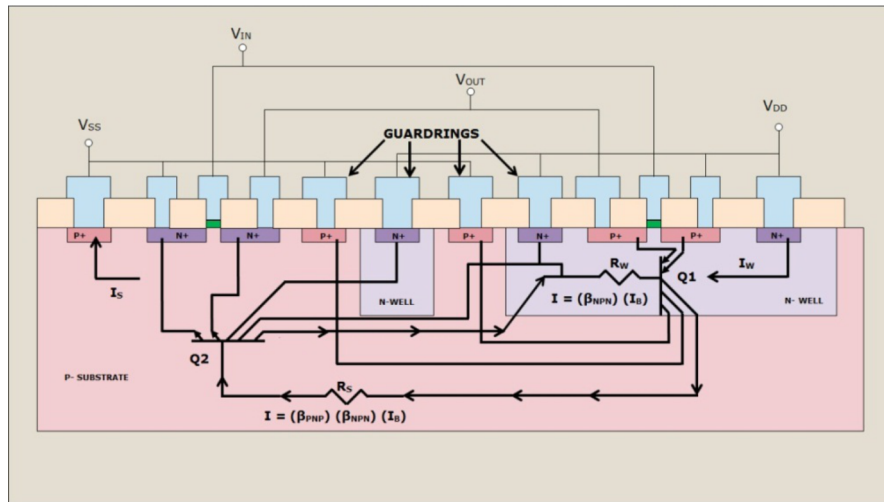


Figure 3. Cross-Section With Guard Rings Included

2 Latch-Up Testing Methods

Latch-Up stress methods prior to the late 1980's were accomplished on bench set-ups with the use of curve tracers or other bench set-ups. In 1988, an industry team released the first Latch-Up standard, JESD17. This standard proposed a method of characterization based mostly on digital CMOS circuit concepts. In 1997, the JEDEC team proposed another Latch-Up standard (JESD78) that built on JESD17 adding more detail to the stress and giving a robustness criteria for the first time. JESD78 remains a standard mostly based on digital CMOS technology and test methods. The current revision, Revision D, does not have a robustness criterion; it has reverted to being a characterization standard. Analog products do not necessarily fit well into the methodology since there are generally specific bias values that work outside a zero or one condition. There are efforts underway on the JEDEC Latch-Up team to add analog methodology, which will likely be completed late in 2015.

2.1 Latch-Up Standard

The current Latch-Up standard, JESD78, stresses pins categorized by type. These types are input, output, bi-directional (I/O), power supply and ground. Input, output and bi-directional pins, in most cases, receive a current stress pulse. The power supply receives an over-voltage stress, a voltage pulse. The pulse widths can be chosen from a range of values but most often in the industry, 2 ms to 10 ms is preferred. The current pulse height typical values are 100 mA while the over-voltage is 1.5 x V_{MAX} (operating). Products requiring clocking or other timing signals can use test vectors in either a Latch-Up tester or an ATE. Timing or pins receiving vectors generally are not stressed since the stress pulse may interfere with the part set-up creating a false failure. [Figure 4](#), [Figure 5](#) and [Figure 6](#) show the stress waveforms from JESD78.

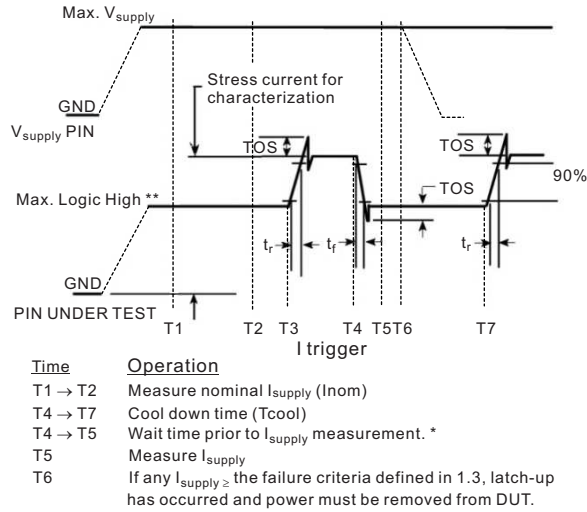


Figure 4. Positive Current Pulse Waveform

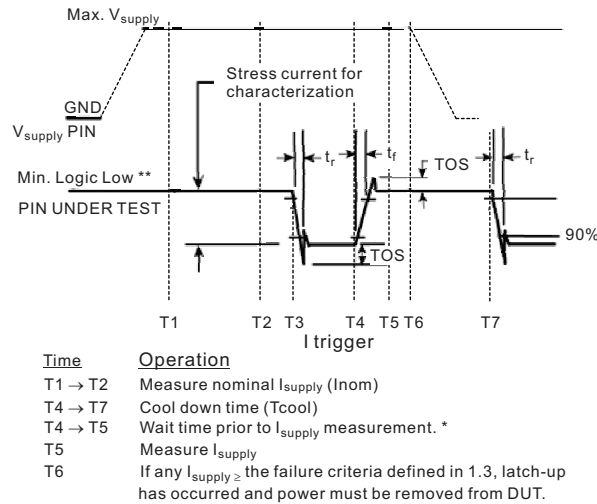


Figure 5. Negative Current Pulse Waveform

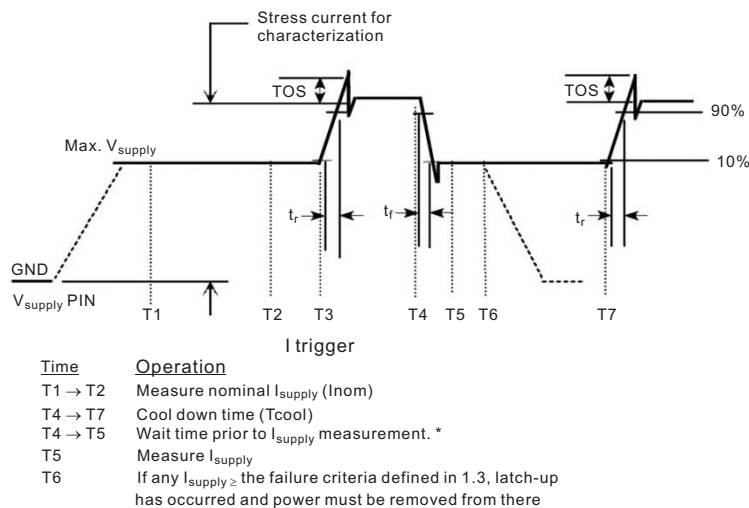


Figure 6. Over-Voltage Stress Waveform

2.2 Current Injection Stress

When stressing products the goal is to stress in every combination of input bias conditions and subsequent output conditions that can be achieved without disrupting the stability of the product. To start, one needs to place the product into a known, stable state that has a reproducible INOM. With inputs high, all of the pins held high are exposed to a positive polarity current pulse. Any pins required to be low for product stability are not stressed. The inputs that can switch to low are then pulsed with a negative pulse and any pin held high for stability is not stressed. There may be pins held high or low for stability that cannot tolerate a current pulse. Outputs depending on the output condition will have a pulsed current of the same polarity. The high-Z condition is preferred, if possible, since it gives the opportunity to stress it with both positive and negative pulses. Bi-directional pins will need to be configured in a specific state and then stressed appropriately.

2.3 Over-Voltage Stress

The over-voltage stress test is set-up to determine the ability of the power supplies to withstand transient voltages. For digital products, each input condition (high and low) must be checked by the over-voltage test. The power supplies are then stressed with over-voltage values either at $1.5 \times V_{MAX}$ or MSV (see Figure 6).

2.4 Signal Latch-Up

Similar to the Latch-Up description in Section 1.1, that defines a malfunction of the IC, generally, a shorting of the power supply to ground, Signal Latch-Up (sLU) is also a malfunction of the IC; however, a shorting of the signal to ground as opposed to the traditional shorting of the power supply to ground. Latch-Up is detected by a sustained increase in I_{SUPPLY} after the applicable stress is removed. Signal Latch-Up does not manifest itself in a sustained increase in I_{SUPPLY} , but rather detected in a sustained increase in I_{SIGNAL} after the applicable stress is removed. While Latch-Up is generally not a problem associated with normal operation, Signal Latch-Up can be a problem associated with normal operation depending on the signal application. During the design of signal ESD protection structures, there can be intentional SCRs employed that encourage selected parasitic PNP diodes to trigger under an ESD event. While ESD is an unpowered event, this is not a concern and actually desirable. However, during normal operation since an intentional SCR could exist between a signal pin to ground and the signal pin could be tied or driven to a “hi” state, care must be taken by using design rules on the product to limit effects of Signal Latch-Up, thereby, mitigating the effect of excursion that could trigger the signal ESD SCR and effectively short the signal to ground. If a signal pin is tied or driven to a “lo” state, then the signal voltage is below the ESD SCR holding voltage and signal Latch-Up will not occur.

2.5 Analog Product Testing

As is noted in the Scope of JESD78,

“As these technologies have evolved, it has been necessary to adjust this document to the realities of characterization with limits not imagined when the first Latch-Up document was generated some 25 years ago. Though it would be simpler to make the original limits of 1.5 times the maximum pin operating voltage an absolute level of goodness, the possibilities of success at this level are limited by the very low voltage technologies, and the medium and high voltage CMOS, BiCMOS and Bipolar technologies (>40 V). The concept of maximum stress voltage (MSV) allows the supplier to characterize Latch-Up in a way that differentiates between Latch-Up and EOS. This revision will make it more transparent to the end user that given the limits of certain technologies the subsequent Latch-Up characterizations are valid.”

2.5.1 Maximum Stress Voltage for Latch-Up (MSV)

Since the advent of the JEDEC standard, the testing methodology has been digital CMOS centric. Over the years as power supply voltages increased, stressing at $1.5 \times V_{MAX}$ became increasingly difficult if not impossible to do. Companies that produced high voltage products tested Latch-Up with levels less than $1.5 \times V_{MAX}$. Stressing at less than $1.5 \times V_{MAX}$ was necessitated by the fact that transistor catastrophic breakdowns would be breached. So, in 2010, the JEDEC Latch-Up team decided to bring JESD78 up to common practice and created a new term called Maximum Stress Voltage for Latch-Up (MSV). MSV is generally a number less than a catastrophic transistor breakdown voltage and generally greater than the absolute maximum voltage (V_{ABSMAX}) listed in the device-specific data sheets.

Since the introduction of MSV, there have been numerous questions about how to determine the MSV value. MSV can be determined for each manufacturing process by either starting with one diode drop above the V_{MAX} and stepping the voltage up to catastrophic breakdown or choose a value near the catastrophic breakdown based on process characterization. There are no fixed rules for determining MSV, each user can determine and document the MSV as the standard is currently written. In an upcoming revision of JESD78, there will be additional informative guidance for determining MSV.

2.5.2 Stressing Special Pins

Analog and mixed signal products may have a combination of pin functions that require some pins to be treated as digital pins and others as analog pins. Generally, the analog pins will have only one bias setting to function properly, so, there is one stress to perform on those types of pins. The digital pins can have vectors and clocks and must be treated as described in JESD78. Analog and mixed signal products can also have special function pins that can be difficult to know how to stress. Examples of special pins may be LDO, PWM, BOOT, PHASE, HB, VCC and others. In general, these pins provide a bias to other pins on the same product or help regulate the product's operation or provide bias to other devices. There is considerable debate on how to stress these pins. Some would like to test these pins as they are configured in a normal application. Others want to stress them as either outputs as power supplies or inputs as power supplies. A JESD78 Latch-Up Sub-Team is working on the resolving this issue; the results of this team's activity will be in a future revision of the standard.

In this example, using a voltage regulator, [Figure 7](#) shows a set-up that treats these pins as if they were in a common application setting.

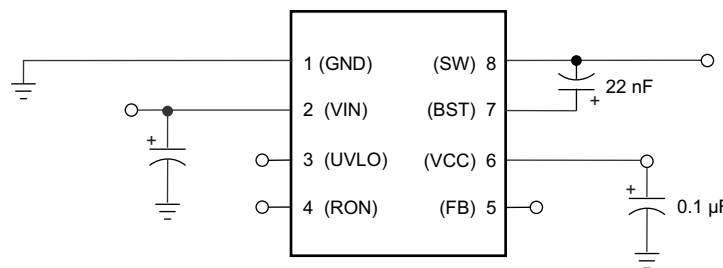


Figure 7. Typical Voltage Regulator Application Set-Up for Latch-Up Stress

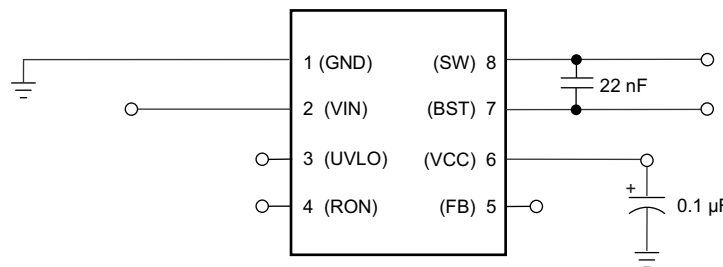


Figure 8. Typical Voltage Regulator Set-Up for Latch-Up Stress

There are two pins that may have more than one way to be stressed: pins 6 and 7. Each, in the application, provides a bias or control charge flow to another pin or provide internal regulation support. One could stress both pins without the capacitors but categorizing them into a group may be difficult. Pin 6 provides a bias, is it a power supply or output? Pin 7 provides charge control to pin 8, is it an output or power supply? Additionally, Pin 7 must always be within a small voltage above Pin 8. Each category could be applied (see [Figure 8](#)). If each is an output then the pins would receive both a positive and negative current pulse since output can fluctuate between positive and negative values. Both pins can be labeled as power supplies and biased to a correct value. If this is the case then an over-voltage pulse will be applied. In many scenarios, neither of these configurations will work. Knowledge of the circuitry supporting the pin of interest will be important in assigning the proper stress type. Generally, avoidance of an unstable condition is paramount. If stability is not achieved, the results are not trustworthy. Engineering judgment may be necessary to properly exercise the pins.

Another option, described in Annex A of JESD78D, is to not directly stress these pins and have the capacitors in place particularly if the device is unstable during any other set-up. The over-voltage test on pin 2 would internally stress each of the externally unstressed pin(s). The part's stability is generally very good with this type of set-up since Pin 7 and Pin 8 will maintain the required voltage separation. The remaining pins would be stressed as their descriptions require.

2.5.3 High Voltage Testing

High voltage CMOS and BiCMOS devices can have some unique problems when Latch-Up stress is applied. In many cases MSV will have to be applied. Also in many of today's high voltage products, there is little headroom above the data sheet $V_{ABS\text{MAX}}$ to set the current stress voltage clamps without potentially causing a catastrophic failure. There may be cases under these conditions that $V_{ABS\text{MAX}}$ may need to be used. There is also the consideration that most Latch-Up test equipment has a 100 V/1 A ceiling on their sourcing voltage and current. When confronted with this problem one can define the V_{MAX} at a lower value and do the over-voltage and current pulse voltage clamps at the machine maximum voltage. Another possibility is to add external power supplies that reach the desired value and stress appropriately.

In the example shown in Figure 9, a mixed signal multi-port regulator is stressed using a combination of digital and analog methods. The product required vectors on the serial peripheral interface (SPI) to set the conditions of the drivers and the other outputs. This device also used charge pump drivers that, in the application, were controlled by a network of diodes, a resistor and capacitors to provide a bias to the charge pump pin. Any stress on these charge pump driver pins would cause the device to malfunction (become unstable). This is a closed network and susceptible only through other power supply variation. This network was not stressed during Latch-Up testing. All of the outputs and drivers were stressed both with positive and negative current pulses. The SPI clocked pins were not stressed for stability reasons. The overvoltage stress on the three power supplies was set for the 5 V supply at $1.5 \times V_{\text{MAX}}$, the 12 V supply used an MSV of $1.2 \times V_{\text{MAX}}$ and the 60 V supply used an MSV of $1.1 \times V_{\text{MAX}}$. Initial testing of this product found Latch-Up problems in the driver and sense pins which was understood and corrected. Upon retest the product passed all Latch-Up criteria.

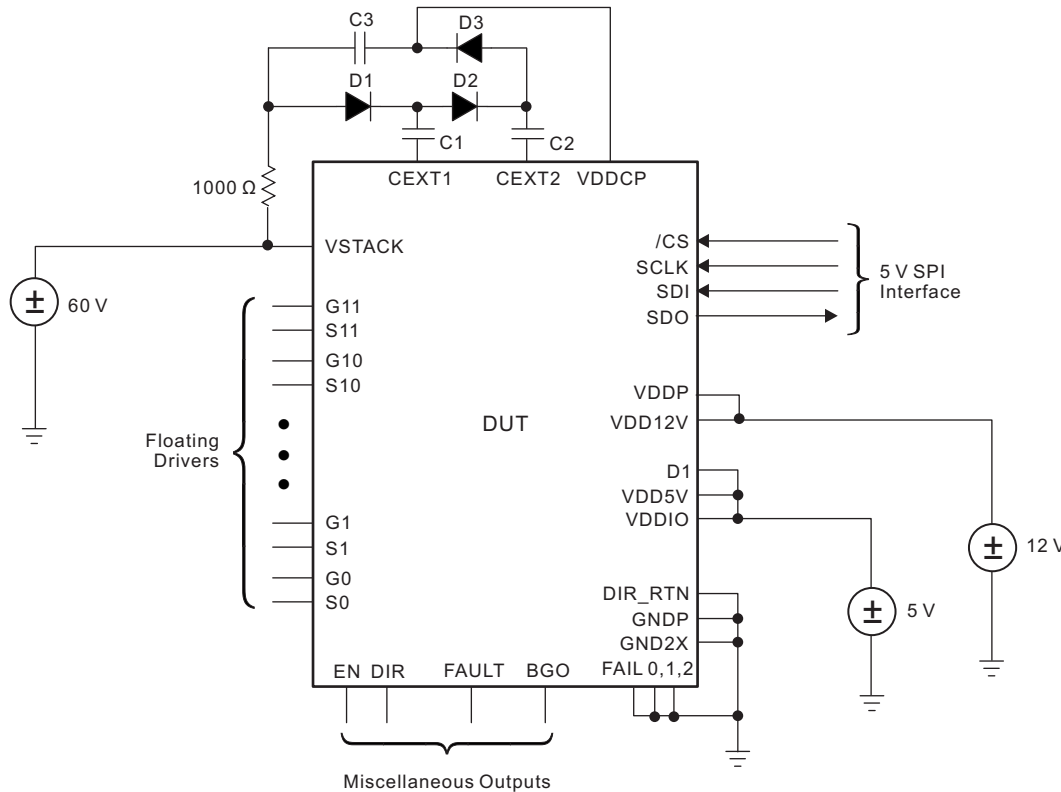


Figure 9. Product With Multiple Regulators Controlled by SPI

3 References

- *Latchup in CMOS Technology*, Ronald Troutman, 1986, Kluwer Academic Publishers
- *Latch-Up, ESD, and Other Phenomena (SLYA014)*
- JESD78D: IC Latch-Up Test at: www.Jedec.org

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