GTLP in BTL Applications

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ABSTRACT

This application report addresses the issues a designer might face when using a GTLP device in a BTL/FB+ application when a legacy BTL/FB+ bus implementation is still in use. Key BTL/FB+ and GTLP device characteristics are compared, and additional GTLP value-added features are discussed.

To demonstrate that GTLP devices can be used in BTL/FB+ applications, the reference voltage (V_{REF}) and termination voltage (V_{TT}) were modified to BTL/FB+ specifications in TI's 20-slot GTLP EVM and waveforms showing system performance are presented. The experiment has shown GTLP technology is suitable for BTL/FB+ applications if maximum output-current ratings are observed.

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Introduction

In the past, the standard solutions for driving bus lines of backplane systems were transistor-transistor logic (TTL) or 5-V CMOS logic circuits. However, some issues resulted from the large 3.3-V or 5-V voltage swing, such as low system frequency performance and noise generated when the outputs switch simultaneously.

An open-collector backplane transceiver logic (BTL) bus with a reduced output voltage swing (<1V) that mitigates these concerns was introduced in the FutureBus Plus (FB+) family of devices. The falling edge is generated actively by the open-collector driver, and the rising edge is generated by a passive pullup network. A pullup network, with the termination resistance matching the loaded bus line impedance, provides optimum signal integrity and incident-wave switching.

Many BTL/FB+ backplanes are in operation. Engineers looking to the future see open-drain Gunning transceiver logic plus (GTLP) devices as a lower-power, higher-frequency migration path. However, their investment in the existing BTL backplanes and cards must be maintained for at least several more years.

This application report discusses how GTLP devices can be substituted for FB+ devices and operated at BTL signal levels until all the cards have been converted to GTLP, or until the higher system frequencies available from GTLP are needed for increased data throughput. Then, the entire BTL system can be converted easily to GTLP signal levels simply by changing the reference voltage and reducing the backplane termination voltage.

Background

FB+ devices are 5-V V_{CC} BiCMOS translators that operate between TTL logic levels on the card and BTL signal levels on the backplane. The backplane signals are generated by an open collector and a termination network (see Figure 1). The saturation voltage of the pulldown transistor and the forward voltage of the serially connected diode generate the output low-level voltage of 1.1 V. The high level of 2.1 V comes from the termination resistor (R_{TT}) connected to the termination voltage of 2.1 V. R_{TT} should equal the loaded-bus line impedance (Z), but the effective dc resistance, as seen by the driver in a typical double-terminated backplane, is R_{TT} in parallel with R_{TT} or one-half R_{TT}. Matching R_{TT} with Z ensures incident-wave switching and improves signal integrity. FB+ devices can handle a current (I_{OL}) up to 100 mA, which equals a R_{TT} of 20 Ω or an effective line impedance of 10 Ω ($R = (V_{OH} – V_{OL})/I_{OL}$). For safe detection of logic levels, the inputs are designed with differential amplifiers and a fixed threshold at 1.55 V ± 75 mV, exactly in the middle of the voltage swing. FB+ logical-layer specification is, according to IEEE Std 1194.1-1991 (BTL) and IEEE Std 896-1991 (FB+), describing node management, live insertion, and profiles. However, the physical layer can be used stand-alone, without the logical layer.

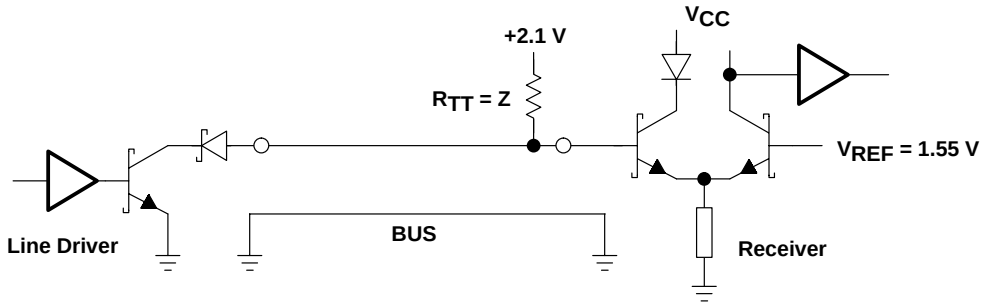


Figure 1. Open-Collector Bus System Using BTL/FB+ Devices

The basic concept of the Gunning transceiver logic (GTL) bus (see Figure 2) is identical to the BTL system, but in a CMOS technology and at a lower voltage level. Because of the missing diode in the open-drain outputs, the low level is 0.4 V. With a high level of 1.2 V, the voltage swing is reduced to only 0.8 V. The threshold is set in the middle of the voltage swing at 0.8 V by the variable V_{REF} input. With a drive capability of 40 mA, GTL devices can drive an effective resistance of around 0.8 V/40 mA = 20 Ω, or a termination resistor R_{TT} of 40 Ω in a double-terminated backplane. As a result of the 0.4-V V_{OL} level and the 40-mA I_{OL} current drive, the maximum output dc power dissipation of one output is 16 mW. These low-power drivers are typically integrated into ASICs for point-to-point applications, and normally are not used in heavily loaded multipoint applications.

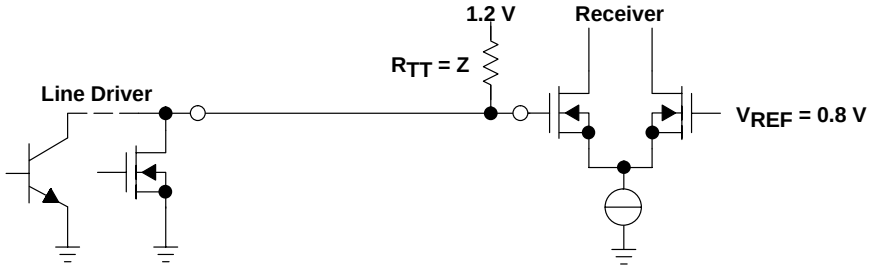


Figure 2. Open-Drain Bus System Using GTL Devices

The GTLP family combines the high-drive benefits of the BTL family, with the reduced power consumption of the GTL family. GTLP specifically is designed and optimized for heavily loaded multipoint backplane applications with a slow, controlled, backplane edge rate, and includes features needed for live insertion and withdrawal.

GTL and GTLP devices support two different signal-level specifications: GTL (JEDEC Standard JESD 8-3) and GTL+ signal levels first used by Intel™ in their Pentium™ processors. GTL voltage swing is from 0.4 V to 1.2 V, with the threshold in the middle of the voltage swing at 0.8 V. GTL+ voltage swing is from 0.55 V to 1.5 V, with the threshold at 1.0 V. GTLP devices, which are optimized for backplane applications and are designated with the SN74GTLP prefix, are optimized for the higher noise-margin GTL+ signal levels to indicate they have a slower slew rate with improved output-edge control, and to differentiate them from point-to-point GTL+-optimized devices.

Both FB+ and GTLP devices are commonly used in multiple-bit, multipoint double-terminated parallel backplanes (see Figure 3). The device turns on to pull the signal low and turns off to allow the termination resistors to pull the signal high, up to the termination voltage. The benefit of this open-collector/open-drain technology is that the output either is sinking current or is in the high-impedance state (3-state), but never sources current. This reduces the power consumption over typical Thevenin or ac terminations. Other benefits include the ability to pick a termination-resistor value that matches the loaded backplane impedance (Z), ensuring incident-wave switching/optimum signal integrity, and no destructive bus-contention issues if multiple devices are on at the same time, which also facilitates a wired-OR arrangement. The loaded backplane impedance, Z, always is lower than the natural bus line impedance (Z_O) and varies from system to system, depending on stub length, slot pitch, device C_{iO}, and type of connectors. Surface-mount ceramic-bypass capacitors (0.82 nF) should be connected between V_{TT} and GND on every fourth data bit, to minimize current fluctuations.

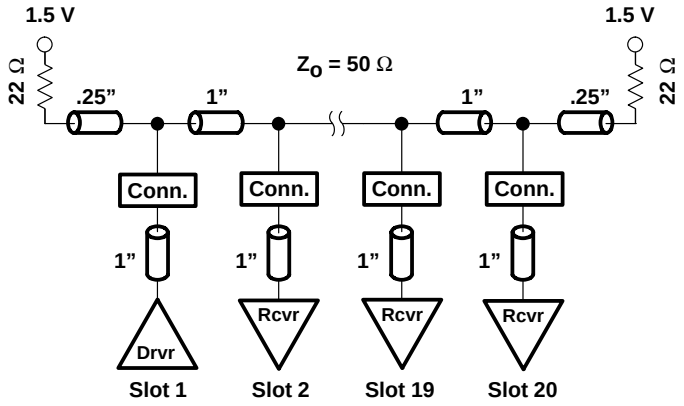


Figure 3. Typical Backplane Physical Representation

FB+ and GTLP Characteristics Comparison

Table 1 compares the FB2033A with the high-drive GTLP2033 device, which is soon to be released. Each characteristic is discussed in general and then in detail if the difference is material to the use of GTLP devices in BTL/FB+ applications. Values of C_{io}, I_{CC}, and t_{pd} are design goals and are subject to change.

Table 1. FB+ and GTLP 8-Bit Registered Transceiver Characteristics Comparison

	CHARACTERISTIC	FB+	GTLP
A-port/daughter card	Logic levels	TTL	LVTTL
	Transistors type – input/output	CMOS/bipolar	CMOS/CMOS
	Drive levels	–32/55 mA	±24 ma
	Bus hold	None	None
	I_{off} and PU3S to support hot insertion	Yes	Yes
B-port/backplane	Signal levels	BTL	GTLP
	Input – differential	±75 mV around fixed threshold of 1.55 V	±50 mV around variable threshold of 1.0 V
	Transistor type – output	Bipolar open collector	CMOS open drain
	Drive levels	100 mA @ 1.1 V	100 mA @ 0.55 V
	Input/output capacitance (C_{io} – max)	6 pF	10.5 pF
	Slew rate – typical rise/fall	0.39/0.33 V/ns	0.5/0.43 V/ns
	I_{off}/PU3S and BIAS V_{CC} to support live insertion	Yes, 1.62 V to 2.1 V	Yes, 0.95 V to 1.05 V
Device	V_{CC}	5 V	3.3 V
	Technology	0.8-μ BiCMOS	0.65-μ CMOS
	I_{CC}	120 mA	40 mA
	Power consumption	100 mW	50 mW
	Transparent mode – maximum propagation delay (GTLP ERC slow or fast for higher/lower values)	A to B 4.6 ns B to A 5.6 ns	A to B 7.7 or 6.3 ns B to A 5.5 ns
	Logic functions	Many – both are exactly the same.	
	ESD	HBM – 2000 V MM – 200 V CDM – 1000 V	HBM – 2000 V MM – 200 V CDM – 1000 V
	Temperature range	0°C to 70°C	–40°C to 85°C
	Package offerings	52-pin TQFP	48-pin TSSOP, TVSOP, or VFBGA
	IEEE Std 1149.1 JTAG	No pins assigned	No pins assigned

A-Port/Daughter-Card Side of the Device

- Logic levels – The logic levels are compatible because the threshold, V_{IH}, V_{OH}, and V_{IL} logic levels are the same. GTLP is 5-V tolerant.
- Transistor types and drive levels – They are not significantly different. Most applications do not require the higher drive and work well with the balanced drive of ±24 mA. Also, GTLP is offered with a series-damping-resistor (SDR) option that reduces the drive to ±12 mA, and provides better signal integrity into smaller lumped loads.
- Bus hold – Neither device has the bus-hold feature. The A port of most GTLP devices that do not feature the split 3-wire A port is featured with bus hold.
- Hot insertion – Both families support hot insertion with the I_{off} and power-up 3-state (PU3S) features.

B-Port/Backplane Side of the Device

- Signal levels – Signal levels are not compatible (see Figure 4). The level of noise margin is about the same; only the input thresholds of operation are different. As discussed in the following paragraphs, GTLP devices can operate at BTL signal levels by changing V_{REF} to 1.55 V and raising V_{TT} to 2.1 V.

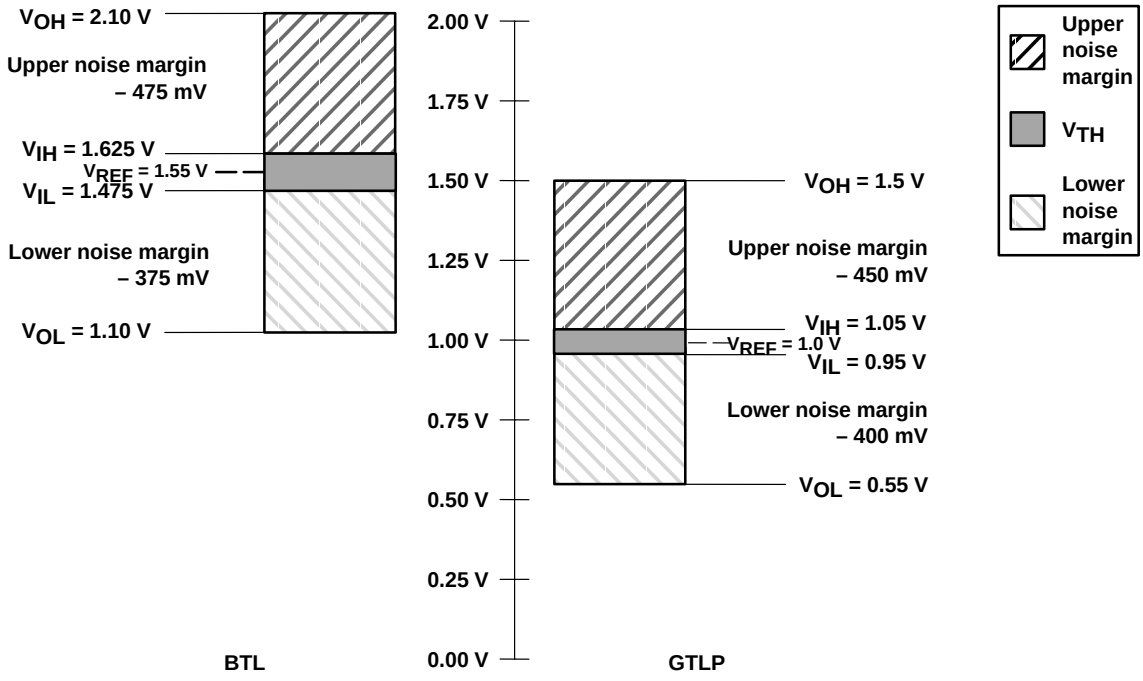


Figure 4. BTL and GTLP Signal-Level Comparison

- Differential input – FB+ devices have a fixed differential input set at 1.55 V, whereas GTLP devices have a variable differential input that is set via the external V_{REF} control pin. Normally, V_{REF} is two-thirds of V_{TT} so that, when V_{TT} is 1.5 V, V_{REF} is 1.0 V. As shown in Figure 5, the GTLP reference level is set by this simple R/2R resistor network, with R typically being a one-fourth-watt resistor in the range of 1 k$\Omega \pm 1\%$. The advantage of this external V_{REF} and R/2R network is that it maintains the upper and lower noise margin if V_{TT} fluctuates. The maximum input V_{REF} current to a GTLP device is 10 μA. A 0.1-μF to 0.01-μF bypass capacitor should be located as close to the V_{REF} pin as possible to stabilize the voltage.

  When GTLP is used in BTL applications, the resistor network simply is changed to R/3R so that V_{REF} is set at 1.575 V when V_{TT} is changed to 2.1 V. When the card is converted from BTL to GTLP signal levels, simply change the 3R resistor to 2R, and the proper reference voltage is set when V_{TT} is reduced from 2.1 V to 1.5 V.

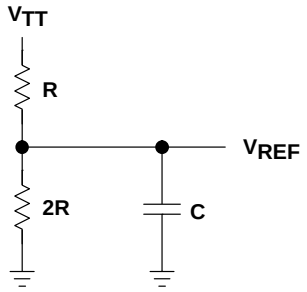


Figure 5. GTLP V_{REF} Resistor Network

- Transistor type – FB+ and GTLP operate the same using only a pulldown transistor on the output, with FB+ bipolar transistors being called open collector and GTLP CMOS transistors being called open drain.
- Drive levels – The drive or current-sinking capability is the same and is 100 mA, to allow termination-resistor R_{TT} values down to 22 Ω (effective termination resistance of 11 Ω) if the voltage swing is limited to 1 V. In actual applications, the GTLP V_{OL} is lower, and higher R_{TT} values are required to avoid exceeding the recommended I_{OL}.
- Input/output capacitance (C_{io} maximum) – The FB+ decoupling diode reduces the maximum output capacitance to about 6 pF. Increased output capacitance of 10.5 pF (8.5 pF typical) is seen in GTLP devices, compared to FB+ devices. This is directly attributable to the GTLP CMOS process, which requires larger-area output structures compared to bipolar output structures used on FB+ devices. This increase in capacitance reduces the loaded-bus line impedance that can be compensated for by lowering R_{TT}. The higher loading reduces t_{pd} and increases the time of flight.
- Live insertion – Both support live insertion through the use of I_{off}, PU3S, and BIAS V_{CC} circuitry. BIAS V_{CC} circuitry precharges the outputs to mid-swing levels to prevent glitching active data on the backplane when cards are inserted or removed, and is disabled when V_{CC} is connected. FB+ BIAS V_{CC} output is fixed at 1.62 V to 2.1 V, whereas the GTLP device BIAS V_{CC} output is fixed at 0.95 V to 1.05 V. If GTLP devices are used at BTL signal levels, the precharge is below the threshold level and may not be as effective in preventing data glitches. However, in the GTLP EVM (a specially designed backplane for customer use), no glitching was noted when GTLP devices were operated at BTL levels.

Device Characteristics

- V_{CC} – FB+ uses 5-V V_{CC}, whereas GTLP uses 3.3-V V_{CC}. The lower V_{CC} is more compatible with newer, higher-performance devices being used in current and future board designs.
- Technology – FB+ uses an older 0.8-μ bipolar process, whereas GTLP uses a newer 0.65-μ CMOS process that has the main advantage of lower power consumption.
- I_{CC} – I_{CC} is the amount of current used by the device and is a factor in computing power consumption. CMOS construction reduces GTLP device I_{CC} to about one-third of FB+ levels.
- Power consumption – Several factors influence power consumption: V_{CC}, I_{CC}, frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance. GTLP power consumption and overall heat dissipated is about one-half of FB+ levels.
- Propagation delay – The A-to-B and B-to-A propagation delays are larger in the GTLP devices due to the slower edge slew rate and the slower CMOS process. High-drive GTLP devices have the option of a smaller t_{pd} by increasing the slew rate through the use of the edge-rate-control (ERC) circuitry. The ERC pin controls slew rate.
- Logic functions – GTLP devices are available in several different functions and package options (see Table 2). FB+ is available in several different functions (see Table 3).
  - Most FB+ devices have split input (AI) and output (AO) buses on the A port, something only the GTLP1394, GTLP1395, and GTLP2033/34 in the GTLP family have. Please contact the GTLP team at gtlp@list.ti.com if you would like a GTLP replacement for your existing FB+ application.
  - The FB1650 emulates the FB2031 and the FB2040.
  - The FB2033A is slightly faster than the FB2033K (custom device released to the general market).

Table 2. High-Drive GTLP Functions

DEVICE	AVAILABILITY	FUNCTION	PINS	PACKAGE
SN74GTLP1394	Now	2-bit bus transceiver with split LVTTL port and feedback path	16	SOIC, TSSOP, and TVSOP
SN74GTLPH1612	Soon	18-bit universal bus transceiver	64	TSSOP
SN74GTLPH1616	Soon	17-bit universal bus transceiver with buffered clock	64	TSSOP
SN74GTLPH1645	Soon	16-bit bus transceiver	56	TSSOP, TVSOP, and VFBGA
SN74GTLPH1655	Soon	16-bit bus transceiver	64	TSSOP
SN74GTLP1395	Soon	2-bit bus transceiver with split LVTTL port and feedback path	20	SOIC, TSSOP, TVSOP, and VFBGA
SN74GTLP21395	Soon	2-bit bus transceiver with split LVTTL port and feedback path	20	SOIC, TSSOP, TVSOP, and VFBGA
SN74GTLP2033	Soon	8-bit inverted registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP22033	Soon	8-bit inverted registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP2034	Soon	8-bit registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP22034	Soon	8-bit registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLPH1627	Soon	18-bit bus transceiver with synchronous clock outputs	64	TSSOP

Table 3. FB+ Functions

DEVICE	FUNCTION	PINS	PACKAGE
SN74FB1650	18-bit universal storage transceiver with split TTL I/O	100	PCA
SN74FB1651	17-bit universal storage transceiver with delayed buffered clock with split TTL I/O	100	PCA
SN74FB1653	17-bit universal storage transceiver with delayed buffered clock with split LVTTL I/O (3.3-V and 5-V V_{CC})	100	PCA
SN74FB2031	9-bit address/data transceiver with clock and latch	52	RC
SN74FB2032	9-bit arbitration contest competition transceiver	52	RC
SN74FB2033A	8-bit registered transceiver with split TTL I/O	52	RC
SN74FB2033K	8-bit registered transceiver with split TTL I/O	52	RC
SN74FB2040	8-bit status/sync transceiver with split TTL I/O	52	RC
SN74FB2041A	7-bit transceiver with split TTL I/O	52	RC

- ESD – Both FB+ and GTLP meet the minimum electrostatic discharge (ESD) standards in human-body model (HBM), 2000 V; machine model (MM), 200 V; and charged-device model (CDM), 1000 V. During testing, the GTLP devices pass 4000-V HBM and 3000-V CDM.
- Temperature ranges – FB+ is offered in commercial (0°C to 70°C) and military (–55°C to 125°C) temperature ranges, with some of the newer devices also ac specified for the industrial (–40°C to 85°C) temperature range. GTLP is offered in industrial (–40°C to 85°C) and select devices will be offered in the military (–55°C to 125°C) temperature ranges. Please contact the GTLP team at gtlp@list.ti.com for additional information on the devices in the military temperature range.
- Package offerings – FB+ devices are packaged in older technology, larger, more expensive thin quad flatpack packages that include a thermal heat sink in the 100-pin packages to help dissipate the heat generated by the bipolar outputs. GTLP devices are packaged in modern packages, including the often-requested TSSOP package and, where possible, in the smaller TVSOP packages. Select GTLP devices also are offered in the new very fine-pitch ball grid array (VFBGA) and the dual-die, low-profile, fine-pitch ball grid array (LFBGA) package.
- IEEE Std 1149.1 JTAG – Most FB+ devices have JTAG TAP pins assigned, but no devices with JTAG features have been released. The GTLP team is evaluating JTAG functionality in GTLP devices in VFBGA/LFBGA packages, and solicits your input on the desirability of this feature.
- Price – Comparing suggested resale pricing, the FB2033 is about 85% higher than the GTLP2033. There are similar price differentials for other devices in both families.

Advanced Features of GTLP Devices Not Incorporated in FB+ Devices

- OEC™ circuitry – The low-to-high transition output edge-control circuitry has been improved significantly. The slew rate has been held to about 0.5 V/ns on the rising edge and helps prevent ringing on heavily loaded backplanes, allowing a much higher maximum frequency.
- TI-OPC™ circuitry – GTLP devices feature overshoot-protection circuitry that actively ports backplane energy to GND when the signal level is greater than 0.7 V to 0.8 V above V_{REF}. This prevents large overshoots on improperly terminated or unevenly loaded backplanes during low-to-high signal transition, which limits the subsequent undershoot that would reduce the upper noise margin.
- Edge-rate control (ERC) – This feature allows designers to select either a slow-rising-edge slew rate (about 0.4 V/ns) or a slightly faster slew rate (about 0.45 V/ns). The faster slew rate reduces the maximum propagation delay, allowing a higher system frequency. The maximum frequency with a slow ERC is about 87 MHz, while a fast ERC is about 125 MHz. In BTL applications, the slow ERC should be selected by applying the correct logic level to the external ERC control pin as shown in Table 4. $\overline{\text{ERC}}$ is the inverse of ERC and is implemented on some GTLP devices where the control pin replaced a GND pin in the comparable medium-drive GTLP device.

Table 4. B-Port Edge-Rate Control

LOGIC LEVEL		B-PORT OUTPUT EDGE RATE
ERC	$\overline{\text{ERC}}$	
H	L	Slow
L	H	Fast

GTLP Data-Sheet Changes Required for BTL/FB+ Applications

Analysis of high-drive GTLP TI-SPICE model data of GTLP and BTL signal levels shows little change in dc specifications, timing requirements, and switching characteristics. This is because the GTLP device always is operated from 3.3-V V_{CC}, even if the B-port output voltage is pulled to 2.1 V. Overall voltage swing is about 0.6 V larger than normal GTLP voltage swings when operated at BTL signal levels.

GTLP Waveforms in BTL Backplane

The GTLP evaluation module (EVM) backplane (see Figure 6) was designed and manufactured to allow factory-trained GTLP Product Marketing Engineers worldwide to have a tool to showcase the GTLP family of products, and to demonstrate how loading and termination affect signal integrity. Currently, there are units in China, Germany, Japan, Korea, and the United States. Demonstrations can be scheduled by contacting your local Texas Instruments Technical Sales Representative or the GTLP team at gtlp@list.ti.com.

– Used to investigate how length/board spacing/driver position affects signal integrity
– 48 bits broken into 8-bit widths at increments of 2, 4, 8, 12, 16, and 20 slots
– One bit for source-synchronous clock option
– Clock-frequency options of 23, 50, 66, 75, 87, and 100 MHz
– Termination-resistor options of 25, 33, 38, and 50 Ω in 20-slot length (Group 1)

Figure 6. GTLP EVM Backplane

As shown in Figure 7, the high-drive SN74GTLPH1655DGGR is used on the driver and receiver cards. There is a removable termination card at either end of the backplane to allow performance with different values of R_{TT} to be examined. Two cards (driver and receiver) were modified to operate at BTL signal levels by changing the R/2R V_{REF} resistor network to R/3R. V_{TT} for the entire backplane was changed from 1.5 V to 2.1 V by changing the resistor in the 1.5-V V_{TT} regulator that sets the output voltage.

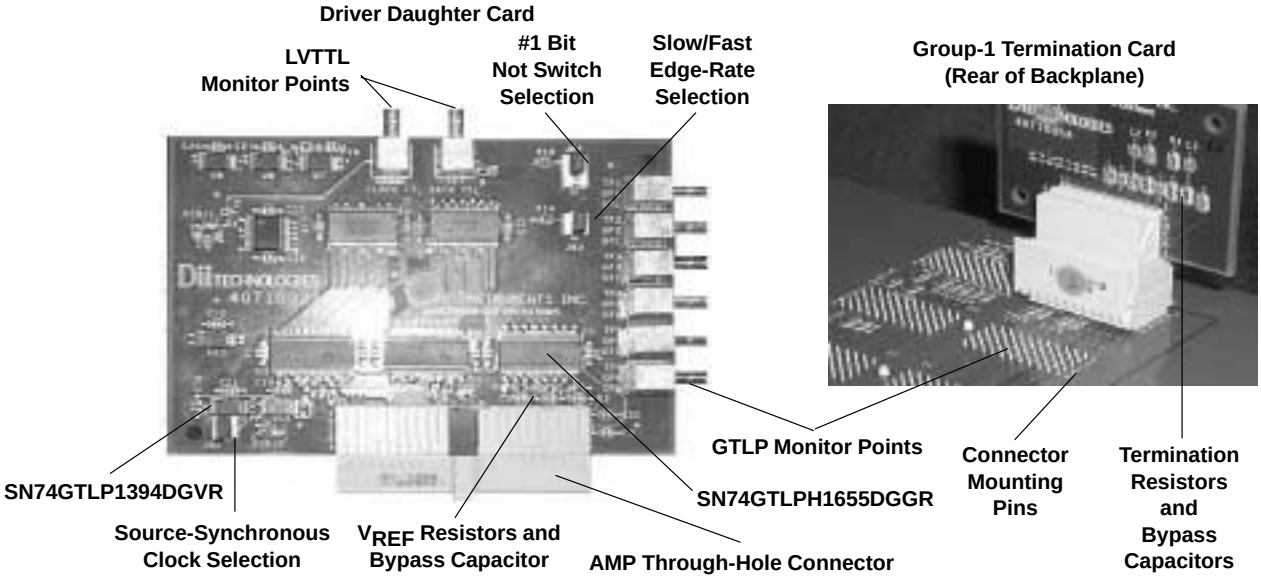
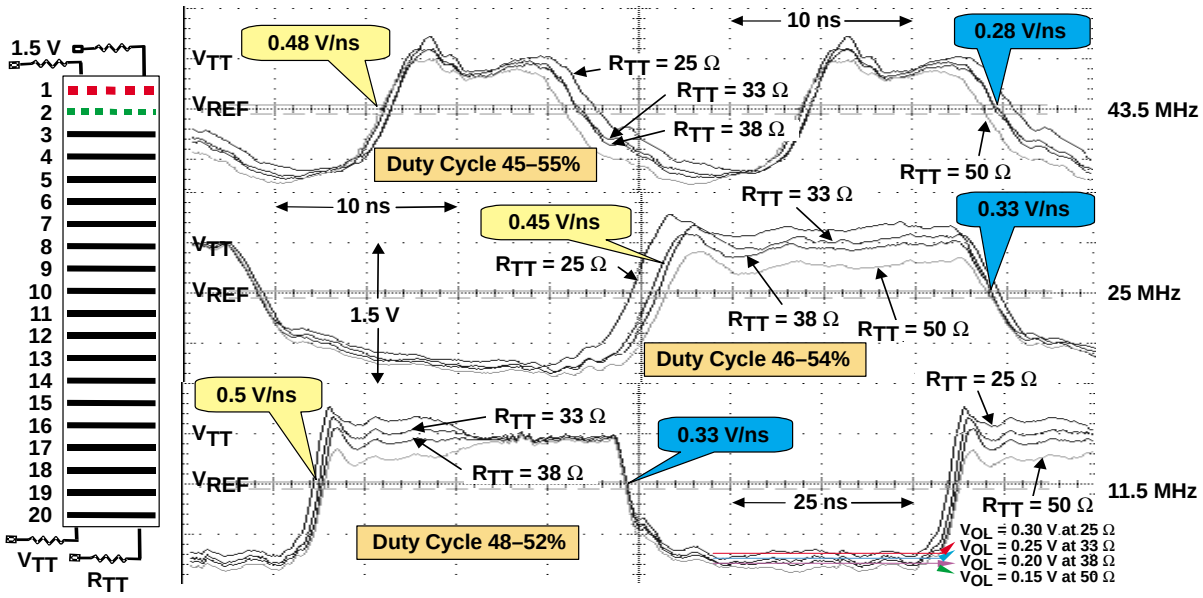


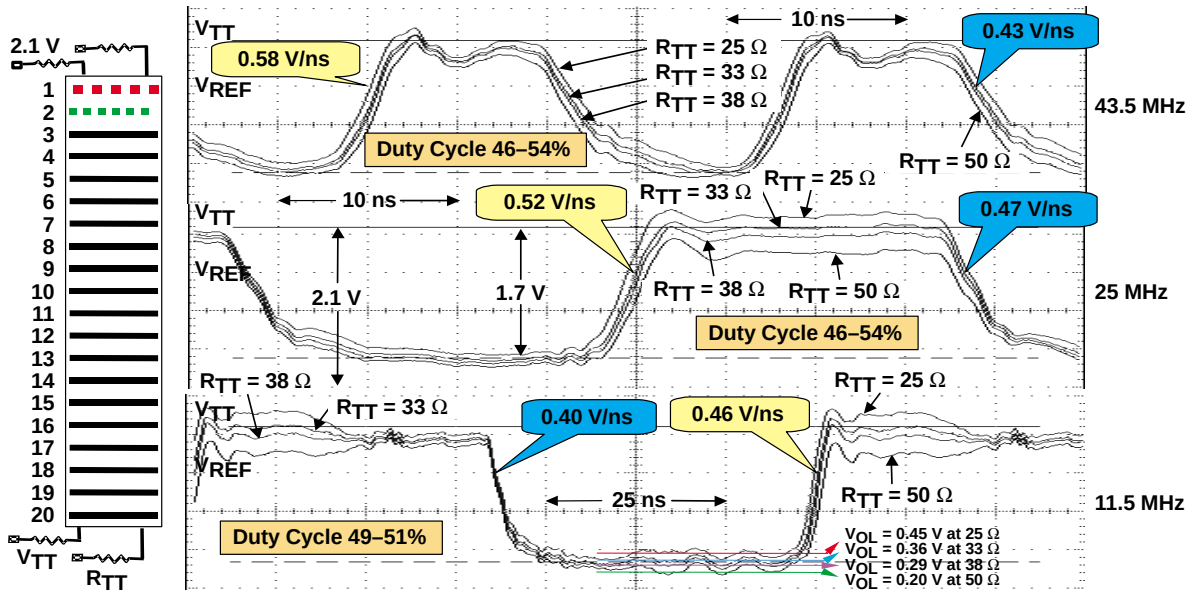
Figure 7. GTLP EVM Driver and Termination Cards

Waveforms using the GTLPH1655 device at both normal GTLP signal levels and BTL signal levels in the fully loaded 17.9-in.-long, 20-slot backplane at various terminations and frequencies are shown in Figures 8 and 9. The GTLP2033 has the same B-port outputs as the GTLPH1655 and other high-drive GTLP devices, so performance is similar. The actual data frequency of the waveform is shown, and is one-half the actual clock frequency. Waveforms were taken at the backplane connector pin. The performance of the GTLP device is excellent at both signal levels. An R_{TT} of 33 Ω most closely matches the loaded-bus line impedance as seen by the well-behaved incident wave. Other high-drive GTLP devices are expected to operate in a similar manner at BTL signal levels.



Fully Loaded Backplane (Driver in Slot 1, Receiver in Slot 2)
SN74GTLPH1655DGGR With Edge-Rate Control in Slow

Figure 8. GTLPH1655 Waveforms at GTLP Signal Levels (Group 1, Bit 1)



Fully Loaded Backplane (Driver in Slot 1, Receiver in Slot 2)
SN74GTLPH1655DGGR With Edge-Rate Control in Slow

Figure 9. GTLPH1655 Waveforms at BTL Signal Levels (Group 1, Bit 1)

Table 5 compares slew rates and duty cycles for Figures 8 and 9. The slew rates and duty cycles were measured at the optimum termination, which is 33 Ω.

Table 5. Waveform Slew Rate and Duty Cycle

LEVEL	MONITOR POINT	DATA FREQUENCY (MHz)	L-H SLEW RATE (V/ns)	H-L SLEW RATE (V/ns)	DUTY CYCLE (%)
GTLP	G1 B1	11.5	0.5	0.33	48–52
GTLP	G1 B1	25	0.45	0.33	46–54
GTLP	G1 B1	43.5	0.48	0.28	45–55
BTL	G1 B1	11.5	0.46	0.40	46–54
BTL	G1 B1	25	0.52	0.47	46–54
BTL	G1 B1	43.5	0.58	0.43	46–54

In Figures 8 and 9, V_{OL} is lower than the specification levels of 0.55 V at GTLP levels and 1.1 V at BTL levels. This larger voltage swing can reduce the maximum possible frequency, increases EMI, and changes the lower end of possible R_{TT} values. Table 6 is a comparison of V_{OH} and V_{OL} at 11.5 MHz with the termination resistance. The I_{OL} was calculated based on $I_{OL} = 2 \times \Delta V/R_{TT}$. The GTLP data sheet lists a recommended maximum device I_{OL} at V_{OL} of 0.4 V and 0.55 V. The lowest termination-resistor value that is possible without exceeding these limits also is calculated, based on $R_{TT} = 2 \times \Delta V/I_{OL}$.

Table 6. V_{OH} and V_{OL} vs I_{OL}

LEVEL	MONITOR POINT	R_{TT} (Ω)	V_{OH} (V)	V_{OL} (V)	ΔV (V)	I_{OL} (mA)	MAXIMUM RECOMMENDED R_{TT} (Ω)	
							I_{OL} 66 mA AT 0.4 V	I_{OL} 100 mA AT 0.55 V
GTLP	G1 B1	25	1.46	0.30	1.16	93	35.2	23.2
GTLP	G1 B1	33	1.45	0.25	1.20	73	36.4	24.0
GTLP	G1 B1	38	1.43	0.20	1.23	65	37.3	24.6
GTLP	G1 B1	50	1.42	0.15	1.27	51	38.5	25.4
BTL	G1 B1	25	2.00	0.45	1.55	124	50.0	31.0
BTL	G1 B1	33	1.93	0.35	1.58	96	47.9	31.6
BTL	G1 B1	38	1.90	0.29	1.61	85	48.8	32.2
BTL	G1 B1	50	1.86	0.20	1.66	66	50.3	33.2

As R_{TT} is reduced, V_{OL} increases because the device has a finite capacity for pulling down the bus voltage. V_{OH} on the monitored bit is reduced at higher levels of R_{TT} because a larger share of V_{TT} is consumed in the fixed 255-Ω test-monitor-point bit resistor. Without this leakage path, which is not found on commercial backplanes, V_{OH} goes to V_{TT}, as shown on the unmonitored bit waveforms.

There are different levels of recommended I_{OL} for the GTLP device at 0.4 V and 0.55 V, because these are points on the voltage vs current (VI) curve that approximate best where the device will be operated. The absolute I_{OL} limit is twice the recommended limit. The device may catastrophically fail at the absolute limit, and the design life of 24,000 hours is degraded on an increasing curve as I_{OL} is operated at the recommended limit, except for brief (<2 ns) time periods where it can be operated at higher levels during ac switching. It is clear that, when using GTLP devices at BTL levels, proper termination must be traded off against natural line impedance without exceeding the maximum recommended I_{OL}.

Frequently Asked Questions

Q: Where can I get more information on GTLP devices?

A: Visit the GTLP internet home page at www.ti.com/sc/gtlp, or e-mail the GTLP team at gtlp@list.ti.com for additional information, data sheets, simulation models, and samples.

Conclusion

GTLP can be used on new BTL/FB+ cards with only a simple modification to the V_{REF} resistor network (R/2R to R/3R) and the shift of V_{TT} (1.5 V to 2.1 V) with limited performance degradation. GTLP allows maximum system frequencies at least comparable to FB+ devices (about 40-MHz clock), while providing advantages that include 3.3-V V_{CC} with 5-V tolerance, smaller TSSOP or BGA surface-mount packages, smaller 2-bit through larger 32-bit functions, lower power consumption, lower cost, and an easy migration path to higher system frequencies (up to 125 MHz) in the future, with a simple reversal of the V_{REF} network to R/2R and reduction of V_{TT} to 1.5 V.

The major disadvantages are that GTLP currently is not offered in exactly the same functionality/control or split A-port inputs and outputs as existing FB+ devices, the output capacitance (C_{io}) is larger, and R_{TT} and the natural bus line impedance must be selected so that the recommend I_{OL} is not exceeded.

The GTLP Team at Texas Instruments should be contacted if there is BTL/FB+ functionality that currently is not offered in the GTLP high-drive family.

Glossary

BiCMOS	Device technology that combines high drive of bipolar outputs with lower power consumption of CMOS inputs
Bipolar	Device technology that has high drive outputs, but has high power consumption
BTL	Backplane transistor logic, which operates at signal levels of V_{TT} = 2.1 V, V_{REF} = 1.55 V, and V_{OL} = 1.1 V
CMOS	Device technology that has balanced drive outputs and low power consumption
FB+	FutureBus Plus devices are designed to operate at BTL signal levels.
GTL	Gunning transceiver logic, which operates at signal levels of V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{OL} = 0.4 V
GTL+	A derivative of GTL that operates at higher-noise-margin signal levels of V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{OL} = 0.55 V and moves V_{REF} from the normal ground-bounce area
GTLP	Gunning transceiver logic plus, which normally is associated with optimized edge-rate devices that allow higher-frequency operation in heavily loaded backplane applications at GTL+ signal levels
R_{TT}	Bus line-termination resistance that should be equal to Z for incident-wave switching and optimum signal integrity
Z	Bus line loaded impedance, taking into account the natural impedance and capacitive loads
Z_o	Bus line natural impedance that is set by type of line construction and dimensions

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